Introduction

QDRII+ and the QDRII SRAM devices are ideally suited for bandwidth-intensive and low-latency applications such as controller buffer memory, look-up tables (LUTs), and linked lists. QDRII+ and QDRII SRAM memory architecture features separate read and write ports operating twice per clock cycle to deliver a total of four data transfers per cycle.

Stratix® III and Stratix IV I/Os are specifically designed to support double-data rate (DDR) external memory standards such as the QDRII+ and QDRII SRAM. Combined with the new self-calibrating physical interface, the ALTMEMPHY megafunction, Stratix III and Stratix IV devices deliver performance of up to 400 MHz or 1.6 Gbps on top and bottom I/O banks. Table 1 lists the maximum clock rate support for Stratix III devices interfacing with QDRII+ and QDRII SRAM devices.

Table 1. Stratix III Maximum Clock Rate Support for External Memory Interfaces with Half-Rate PHY (Note 1), (2)

<table>
<thead>
<tr>
<th>Memory Standards</th>
<th>-2 Speed Grade</th>
<th>-3 Speed Grade</th>
<th>-4 Speed Grade</th>
<th>-4L Speed Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VCCL = 1.1 V</td>
<td>VCCL = 1.1 V</td>
<td>VCCL = 1.1 V</td>
<td>VCCL = 0.9 V</td>
</tr>
<tr>
<td>QDRII+ SRAM (2.5 clock cycle latency only) (3)</td>
<td>400</td>
<td>300</td>
<td>350</td>
<td>250</td>
</tr>
<tr>
<td>QDRII SRAM (1.5V or 1.8V)</td>
<td>350</td>
<td>300</td>
<td>300</td>
<td>250</td>
</tr>
</tbody>
</table>

Notes to Table 1:
1. Numbers are preliminary until characterization is final. The supported operating frequencies listed here are memory interface maximums for the FPGA device family. Your design’s actual achievable performance is based on design and system-specific factors, as well as static timing analysis of the completed design.
2. The maximum clock rate support for the external memory interfaces with the half-rate PHY stated in the table applies to both commercial and industrial grade.
3. Stratix III devices in the 780- and 1152-pin packages support x36 QDRII+/QDRII SRAM at a lower maximum frequency as detailed in Table 3.
4. The Column I/Os refer to Top and Bottom I/Os. The Row I/Os refer to Left and Right I/Os. Hybrid mode refers to DQ/DQS groups wrapping over Column I/Os and Row I/Os of the device.
Table 2 lists the maximum clock rate support for the Stratix IV devices interfacing with QDRII+ and QDRII SRAM devices.

**Table 2.** Stratix IV Maximum Clock Rate Support for External Memory Interfaces with Half-Rate PHY  
*(Note 1)*

<table>
<thead>
<tr>
<th>Memory Standards</th>
<th>All Stratix IV E Devices and Stratix IV GX devices with 1152-pin (with 24 transceivers), 1517-pin, and 1932-pin packages</th>
<th>Stratix IV GX devices with 780-pin and 1152-pin (with 16 transceivers) packages</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Top/Bottom I/O Banks</td>
<td>Left/Right I/O Bank <em>(Note 2)</em></td>
</tr>
<tr>
<td>QDRII+ SRAM (2.5 clock cycle latency only) <em>(Note 3)</em></td>
<td>400</td>
<td>350</td>
</tr>
<tr>
<td>QDRII SRAM (1.5-V &amp; 1.8-V HSTL) <em>(Note 3)</em></td>
<td>350</td>
<td>300</td>
</tr>
</tbody>
</table>

**Notes to Table 2:**

(1) Numbers are preliminary until characterization is final. The supported operating frequencies listed here are the memory interface maximum for the FPGA device family. Your design’s actual achievable performance is based on the design and system-specific factors, as well as static-timing analysis of the completed design.

(2) The left and the right I/O banks do not support 1.5 V HSTL and SSTL Class II I/O standards.

(3) Stratix IV devices in the 780- and 1152-pin packages support ×36 QDRII+/QDRII SRAM at a lower maximum frequency as detailed in Table 4.
Figure 1 and Figure 2 show the Stratix III and the Stratix IV input, output, and output-enable register paths for the QDRII+ and QDRII SRAM interface.

**Figure 1.** Stratix III and Stratix IV IOE Input Registers for QDRII+/QDRII SRAM Interface

**Notes to Figure 1:**

1. This shifted clock can be from the DQS logic block or from a global clock line.
2. This shifted clock comes from the CQn logic block.
3. The half-rate data (dio_rdata0_1× to dio_rdata3_1×) and clock (resync_clk_1×) signals feed into a dual-port RAM in the FPGA core.
This application note describes Altera’s recommended design flow to implement a QDRII+ or a QDRII SRAM memory interface on a Stratix III device. You can implement the same design flow on a Stratix IV device as well. An example of a design walk-through that details the critical aspects of this flow is provided, including:

- Instantiating the physical interface (PHY) to a QDRII or QDRII+ or a QDRII SRAM device.
- Setting the appropriate constraints on the PHY.
- Verifying the design functionality using simulation.
- Timing closure using the TimeQuest Timing Analyzer in the Quartus® II software.

Notes to Figure 2:

1. Data coming from the FPGA core are at half the frequency of the memory interface.
2. This half-rate clock comes from the PLL.
3. The write clock can come from the PLL. The DQ (mem_d) write clock (write_clk_2x) and the QDRII+/QDRII SRAM input clock (mem_clk) have a 90° offset between them.
Use this application note along with the following literature:

- External Memory Interfaces in the Stratix III Devices chapter of the Stratix III Device Handbook.
- External Memory Interfaces in the Stratix IV Devices chapter of the Stratix IV Device Handbook.
- ALTMEMPHY Megafuction User Guide.
- AN 438: Constraining and Analyzing Timing for External Memory Interfaces in Stratix III and Cyclone III Devices.

Memory Interface Design Flow

Altera recommends the design flow described in this section as the best practices for successful memory interface implementation in Stratix III and the Stratix IV devices. A detailed discussion of each step shown in Figure 3 appears in this section. The next section includes a design example that discusses the shaded design flow steps (Figure 3) in detail.
Figure 3. Stratix III and Stratix IV IOE Output and Output-Enable Path Registers for QDRII+/QDRII SRAM Interface

Note to Figure 3:
(1) This step is optional, but it is recommended.
Step 1: Select a Device

The first step in memory interface design is to determine the bandwidth required by your system. Bandwidth can be expressed as:

\[
\text{Bandwidth} = \text{Data width (bits)} \times \text{data transfer rate (1 per second)} \times \text{efficiency}
\]

In quadruple data rate memories like the QDRII+ or the QDRII SRAM, the data transfer rate is four times the clock rate. Hence, the data transfer rate for a 400 MHz interface is 1600 Mbps. The efficiency is the percentage of time the data bus is transferring data. It is dependent on the type of memory. For example, in a QDRII+ or a QDRII SRAM memory interface with separate write and read ports, the efficiency would be 100% when there is an equal number of read and write operations on these memory interfaces.

After calculating the bandwidth of the memory interface, determine which memory and FPGA device to use. Altera has a memory selection white paper that highlights the differences between the various memory types.

For information about your memory device, refer to the Selecting the Right High-Speed Memory Technology for Your System White Paper.

Altera’s FPGA devices support the various data widths for different memory interfaces. Stratix III and Stratix IV devices offer dedicated DQS circuitry for DQ group widths ranging from \(\times4\) to \(\times36\). In the \(\times36\) mode, there is one DQS/CQn pin pair that can clock 36 DQ pins using a dedicated peripheral clock network. When interfacing with QDRII+ or the QDRII SRAM devices with a 36-bit read and write busses, connect the memory’s CQ/CQn pins to the Stratix III or the Stratix IV device’s DQS/CQn pins and connect the Q pins to the DQ pins. The number and width of DQ groups supported on each density and package combination differs, so you must determine the FPGA device density and package combination best suits your needs.

Support for 36-bit wide DQ groups is only available in Stratix III and Stratix IV devices in 1517-pin and 1760-pin packages. Stratix III and Stratix IV devices in 780-pin and 1152-pin packages also support \(\times36\) mode emulation by using \(\times16/\times18\) DQS/DQ groups.
Table 3 and Table 4 summarize the maximum clock rate supported with the ×36 mode emulation for Stratix III and Stratix IV devices.

**Table 3. Stratix III Maximum Clock Rate Support with ×36 Mode Emulation (Note 1), (2), (3)**

<table>
<thead>
<tr>
<th>Memory Standards</th>
<th>-2 Speed Grade</th>
<th>-3 Speed Grade</th>
<th>-4 Speed Grade</th>
<th>-4L Speed Grade</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>QDRII+ SRAM (2.5 clock cycle latency only)</td>
<td>300 MHz</td>
<td>250 MHz</td>
<td>250 MHz</td>
<td>250 MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>QDRII SRAM (1.5 or 1.8V)</td>
<td>300 MHz</td>
<td>250 MHz</td>
<td>250 MHz</td>
<td>250 MHz</td>
<td>MHz</td>
</tr>
</tbody>
</table>

**Notes to Table 3:**

1. Numbers are based on using half-rate PHY and are preliminary until characterization is final. The supported operating frequencies listed here are memory interfaces maximums for the FPGA device family. Your design’s actual achievable performance is based on the design and system-specific factors, as well as static-timing analysis of the completed design.

2. The performance listed in Table 3 is lower than the performance listed in Table 1 due to the double-loading of the CQ/CQn pins. Double-loading causes degradation in the signal slew rate that affects the FPGA delay. Furthermore, due to the difference in slew rate, there is a shift in the setup and hold time window. You can perform an IBIS simulation to illustrate the shift in the clock signals.

3. The maximum clock rate support for external memory interfaces with the x36 Mode Emulation stated in the table applies to both commercial and industrial grade.

**Table 4. Stratix IV Maximum Clock Rate Support with the ×36 Mode Emulation (Note 1), (2)**

<table>
<thead>
<tr>
<th>Memory Standards</th>
<th>-2 Speed Grade (MHz)</th>
<th>-3 Speed Grade (MHz)</th>
<th>-4 Speed Grade (MHz)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>QDRII + SRAM (2.5 clock cycle latency only)</td>
<td>300 250 167 MHz</td>
<td>250 167 MHz</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>QDRII SRAM (1.5 or 1.8V)</td>
<td>300 250 167 MHz</td>
<td>250 167 MHz</td>
<td>MHz</td>
<td></td>
</tr>
</tbody>
</table>

**Notes to Table 4:**

1. The numbers are based on using half-rate PHY and are preliminary until characterization is final. The supported operating frequencies listed here are memory interface maximums for the FPGA device family. Your design’s actual achievable performance is based on the design and system-specific factors, as well as static-timing analysis of the completed design.

2. The performance listed in Table 4 is lower than the performance listed in Table 2 due to the double-loading of the CQ/CQn pins. Double-loading causes degradation in the signal slew rate that affects the FPGA delay. Furthermore, due to the difference in slew rate, there is a shift in the setup and hold time window. You can perform an IBIS simulation to illustrate the shift in the clock signals.

For more information on the ×36 QDRII + QDRII/SRAM interface support in the F780 and F1152-pin packages, refer to the Supporting ×36 QDRII+/ QDRII SRAM Interfaces in the F780 and F1152-Pin Packages section of the Stratix III Device Handbook and Stratix IV Device Handbook respectively.

For information on the Stratix III and the Stratix IV FPGA density and package support for the different memory types, refer to the External Memory Interfaces in Stratix III Devices chapter of the Stratix III Device Handbook and the External Memory Interfaces in Stratix IV Devices chapter of the Stratix IV Device Handbook.
The maximum number of interfaces that you can implement on any given device is limited by the resource availability (number of DQ groups of desired width, number of phase-locked loops (PLLs), number of delay-locked loops (DLLs), and clock resources). For example, the EP3SL150F1152 device supports four ×18 groups on each side of the device. This allows you to interface with a total of 16 QDRII+ or QDRII SRAM devices. Also, each instance of the ALTMEMPHY megafuction for the QDRII+ and the QDRII SRAM requires one PLL, one DLL, and four clock resources. The EP3SL150F1152 supports a total of eight PLLs, four DLLs, and 80 clock networks (16 global and 64 regional clocks). The four DLLs enable support for four unique memory interface clock frequencies and each DLL is able to drive two adjacent sides of the device. The final consideration is to check the availability of the core resources (the adaptive logic modules (ALMs) and TriMatrix memory blocks), and user I/O pins for other memory interface signals including the write data, the address, the command, and memory clock signals.

Step 2: Create a Project in the Quartus II Software

After selecting the appropriate Stratix III or Stratix IV FPGA device, create a project in the Quartus II software that targets the chosen device.

For step-by-step instructions on creating a Quartus II software project, refer to the Tutorial in the Quartus II Online Help.

Step 3: Instantiate PHY

For all the Stratix III and the Stratix IV memory interface designs, use the ALTMEMPHY megafuction when instantiating the physical interface to the memory device. This megafuction features a license-free physical interface that should be used with your memory interface driver logic. Since SRAM devices do not need a memory controller, Altera does not offer such a product. You should connect the local signals of the memory interface to logic in your top-level design that will access the memory.

For detailed information about the architecture, ports, parameters, and the resource usage information of the PHY, refer to the ALTMEMPHY Megafunction User Guide.

When implementing wider interfaces using multiple memory chips, you can configure a single ALTMEMPHY megafuction instance to support independent read and write signals for each memory device, the shared address, and the command signals to all memory devices. When implementing multiple independent interfaces (interfaces operating at different clock rates or interfaces with independent address and command buses), you should create unique ALTMEMPHY megafuction instances for each of the interface.

For details on sharing device resources (PLLs, DLLs, and clock networks) across multiple instances of the PHY, refer to AN 462: Implementing Multiple Memory Interfaces Using the ALTMEMPHY Megafuction.

For the QDRII+ SRAM interface, the ALTMEMPHY supports devices with 2.5 clock cycle latency directly. QDRII+ SRAM devices with 2.0 clock cycle latency are not supported by the ALTMEMPHY.
Step 4: Perform RTL/Functional Simulation (Optional)

Simulating the design to verify functionality is optional but is recommended to ensure the interface performs as intended in your system. When you instantiate the ALTMEMPHY megafunfunction using the MegaWizard® Plug-In Manager, the software provides you with an option to generate a simulation model of the PHY in either the Verilog HDL or the VHDL. This PHY functional simulation model is a cycle-accurate HDL model file produced by the Quartus II software. These models work with the Altera-supported VHDL and Verilog HDL simulators. You also need to get the memory’s simulation model file from the memory vendor in order to perform the simulation.

Step 5: Add Constraints

The next step in the design process is to add the appropriate device constraints related to the external memory interface. These constraints include the timing, the I/O standards, the output-enable group and DQ/DQS group assignments. The Quartus II software MegaWizard Plug-In Manger generates the .sdc/.tcl files containing these constraints for each ALTMEMPHY megafunction instance.

The ALTMEMPHY megafunction requires the use of the TimeQuest Timing Analyzer and is fully timing-constrained using synopsys design constraints (SDC) assignments. The SDC timing constraints are derived from the parameters you entered for the ALTMEMPHY megafunction, based on the QDRII+ or QDRII SRAM data sheet and tolerances from the board layout. The ALTMEMPHY megafunction uses the TimeQuest Timing constraints along with the Quartus II timing–driven fitter to achieve timing closure.

After instantiating the ALTMEMPHY megafunction, the ALTMEMPHY MegaWizard Plug-In Manger generates the following files that you need to apply in order to properly constrain your design (Table 5).

Table 5. Constraint Files Created by the ALTMEMPHY MegaWizard Plug-In Manager

<table>
<thead>
<tr>
<th>File Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;variation_name&gt;_ddr_timing.sdc</td>
<td>Sets timing constraints for the ALTMEMPHY megafunction instance.</td>
</tr>
<tr>
<td>&lt;variation_name&gt;_pin_assignments.tcl</td>
<td>Adds I/O standard settings for all memory interface pins, and adds output enable group assignments to ensure VREF rules are met when design contains input/bi-directional pins.</td>
</tr>
<tr>
<td>&lt;variation_name&gt;_assign_dq_groups.tcl</td>
<td>Adds DQ group to place the CO/CQn pins and Q input pins on appropriate the DQ/DQS locations. Adds memory interface pin group assignments to relate the D/BWSn output pins together and K/Kn output clock pins together for the Quartus II fitter to place them correctly.</td>
</tr>
</tbody>
</table>

For detailed information on creating, generating, and setting the constraints for the PHY, refer to the ALTMEMPHY Megafunction User Guide.

You must add the appropriate pin location and pin loading assignments to the memory interface signals in your design, in addition to timing and device constraints for the rest of your design. Table 6 lists the memory interface pin connections between a QDRII+ or a QDRII SRAM device and a Stratix III or a Stratix IV device.
Stratix III devices provide an independent DQS logic block for each DQS and CQn pin for complementary read data-strobe/clock operations. In the Stratix III pin tables, the differential DQS pin-pairs are denoted as DQS pins and DQSn pins, while the complementary DQS signals are denoted as DQS pins and CQn pins. DQSn pins and CQn pins are marked in the pin table separately. Each CQn pin connects to a DQS logic block and the shifted CQn signals go to the negative-edged input registers in the IOE registers.

The Quartus II software has the Advanced I/O Timing feature that allows the timing analysis to take the board setup into consideration, specifically for bi-directional or output pins, for more accurate timing analysis results. This feature is turned on for Stratix III and Stratix IV devices by default. When using the Advanced I/O Timing feature, you should specify the board setup information such as the capacitance and inductance of the board traces, the pull-up or pull-down resistor values, at both far-end, and near-end of the transmission line, as well as the termination voltage.

You can either specify the information in the Board Trace Model setup through the Device and Pin Options dialog box in the Quartus II software for all the output or bi-directional pins (Figure 4), or separately for the each pin or net group, such as the address bus, through the Quartus II Pin Planner (Figure 5). The board traces information from the Quartus II Pin Planner takes precedence over the information from the Device and Pin Options settings.

Table 6. Memory Interface Pin Connections between QDRII+ or QDRII SRAM and Stratix III or Stratix IV Devices

<table>
<thead>
<tr>
<th>Interface Pin Description</th>
<th>Pin on Memory Device</th>
<th>Pin on FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read clock</td>
<td>CQ, CQn</td>
<td>DQS and CQn</td>
</tr>
<tr>
<td>Read data</td>
<td>Q</td>
<td>DQ</td>
</tr>
<tr>
<td>Data valid (1)</td>
<td>QVLD</td>
<td>DQ</td>
</tr>
<tr>
<td>Write data</td>
<td>D</td>
<td>DQ (2)</td>
</tr>
<tr>
<td>Byte write</td>
<td>BWSn</td>
<td>DQ (2)</td>
</tr>
<tr>
<td>Memory &amp; Write clocks</td>
<td>K, Kn</td>
<td>DQ and DQSn (2)</td>
</tr>
<tr>
<td>Address</td>
<td>A</td>
<td>Any User I/O</td>
</tr>
<tr>
<td>Control signals</td>
<td>WPSn, RPSn</td>
<td>Any User I/O</td>
</tr>
</tbody>
</table>

Notes to Table 6:
(1) The data valid (QVLD) signal from QDRII+ SRAM devices is not used by the ALTMEMPHY megafunction.
(2) These signals should be assigned to the same write DQ/DQS group.
Include only the board information. You do not need to include the FPGA device’s pin or package capacitance, on-chip termination or drive strength setting. Typically, the far-end capacitance equals the input capacitance of the far-end device being interfaced to.

**Figure 4.** Stratix III and Stratix IV IOE Output and Output-Enable Path Registers for QDRII+/QDRII SRAM Interface.

**Figure 5.** Board Trace Model Setup for Individual Pin or Net Group
Step 6: Compile the Design and Verify the Timing Closure

After constraining the design, compile the design in the Quartus II software. During the generation of the ALTMEMPHY megafunction, the MegaWizard Plug-In Manager generates a script called `<variation_name>_report_timing.tcl` that generates a custom timing margin report for that PHY instance. After compiling the design in the Quartus II software, run the timing script to produce the timing report for different timing paths in the design, such as write data, read data, address, and command timing paths.

For information about timing constraints and timing analysis methodology used by the ALTMEMPHY megafunction, refer to AN 438: Constraining and Analyzing Timing for External Memory Interfaces in the Stratix III and Cyclone III Devices.

Step 7: Adjust the Constraints

In the timing report for your ALTMEMPHY instance, you can see the worst case setup and hold margins for the different timing paths in the design. If the setup and hold margins are unbalanced, achieve a balanced setup and hold margins by adjusting the phase setting of the clocks that are used in these paths.

For example, in the case of the address and the command timing margin, the address and command outputs are clocked by an address and command clock that is 90° offset with respect to the system clock. The system clock is used to clock the K/K# clock outputs going to the memory. If the report timing script indicates that using the default phase-shift-setting for the address and command clock results in more setup margin than hold margin, adjust the address and command clock to have higher phase shift than the default setting so that there will be more hold margin. Similarly, adjust the address and command clock to have fewer phase offset with respect to the system clock if there is more hold margin than setup margin with the default settings. These clock-phase-shift adjustments can be made by editing the ALTMEMPHY megafunction instance in the MegaWizard Plug-In Manager.

For detailed information about the clocks used in the PHY megafunction, refer to the ALTMEMPHY Megafunction User Guide.

Step 8: Determine Board Design Constraints

After closing the timing for the design, evaluate the trade-offs posed by various board design choices. Different factors contribute to the signal integrity that can affect the overall timing margin for the memory and the FPGA. Some factors to consider that can affect the signal integrity include the termination scheme used, the slew rate, drive strength settings on the FPGA, and the loading seen by the driver. You should evaluate the trade-offs between the different types of termination schemes, effects of output drive strengths, and the loading, so that you can navigate through the multiple combinations and choose the best possible settings for your design.
Altera offers the following application notes regarding high-speed board design information:

- AN 315: Guidelines for Designing High-Speed FPGA PCBs
- AN 224: High-Speed Board Layout Guidelines
- AN 75: High-Speed Board Designs

Stratix III and Stratix IV devices support both series and parallel on-chip termination (OCT) resistors to improve signal integrity. Another benefit of the Stratix III and the Stratix IV OCT feature is eliminating the need for external termination resistors on the FPGA side. This feature simplifies the board design and reduces the overall board cost. The OCT features offer user-mode calibration to compensate for any variation in voltage and temperature during normal operation to ensure that the OCT values remain constant. The parallel and series OCT features on Stratix III and Stratix IV devices are available in either 25-Ω or 50-Ω setting.

For the uni-directional signals found in the QDRII+ and the QDRII SRAM interfaces, Altera’s recommended default setting is calibrated parallel OCT 50-Ω for input signals and calibrated series OCT 50-Ω for output signals. For the write clock signals Altera recommends series OCT 50-Ω without calibration. You should perform board simulations to validate if these recommendations are optimal for your system.

**Step 9: Perform Board Level Simulations**

To determine the correct board constraints, run board-level simulations to see if the settings provide the optimal signal quality. With many variables that can affect the signal integrity of the memory interface, simulating the memory interface provides an initial indicator of the memory interface’s performance. There are various electronic design automation (EDA) simulation tools available to perform board level simulations. The simulations should be performed on the data, clock, control, command and address signals. If the memory interface does not have good signal integrity, adjust the settings, such as the drive strength setting, termination scheme or termination values, to improve the signal integrity.

Note that changing these settings affects the timing. It may be necessary to go back to the timing closure step if these change.

**Step 10: Verify FPGA Functionality**

Perform system-level verification to correlate the system against your design targets. Use Altera’s SignalTap® II Logic Analyzer to help in this effort.

For detailed information about using the SignalTap II, refer to the Design Debugging Using the SignalTap II Embedded Logic Analyzer chapter in volume 3 of the Quartus II Handbook.
Design Example for QDRII+ SRAM Interface at 400 MHz

This section describes the memory interface design flow outlined above and implements a QDRII+ SRAM memory interface with a Stratix III FPGA using Altera’s Stratix III development board. This design example implements an 18-bit wide, 400 MHz or 1600 Mbps memory interface on the Stratix III EP3SL150F1152C2 device.

Although the design example is specifically for the QDRII+ SRAM memory interface with a Stratix III device, the design flow when using a QDRII SRAM or with a Stratix IV FPGA for the memory interface is the same.

Step 1: Select a Device

For this design, choose the Stratix III EP3SL150F1152C2 device. This device supports four ×18 QDRII interfaces on the I/O banks at each side of the device, at speeds up to 400 MHz. The memory device on the Stratix III development board is an 18-bit wide, 36Mbit, 4-word burst, Cypress CY7C1263V18 QDRII+SRAM device.

Step 2: Create a Project in the Quartus II Software

Create a project in the Quartus II design software to implement your QDRII+ SRAM memory interface. If you have already created a project that you would like to implement the memory interface, open that project. Set the target device as the Stratix III EP3SL150F1152C2 device as shown in Figure 6.

Figure 6. Targeting the EP3SL150F1152C2 Device in Your Quartus II Software Project

For step-by-step instructions for creating a Quartus II software project, refer to the Tutorial in the Quartus II Online Help.
Step 3: Instantiate PHY

Instantiate the ALTMEMPHY megafunction variation using the following steps:

1. Invoke the MegaWizard Plug-In Manager under the Tools menu in the Quartus II software, and select Create a new custom megafunction variation (Figure 7).

   **Figure 7.** Launching the MegaWizard Plug-In Manager

2. Select the ALTMEMPHY megafunction from the list of I/O megafunctions. Choose Stratix III as the target device family, Verilog HDL as the output file type, enter an instance name of your choice (for example, fred) and click Next (Figure 8).

   **Figure 8.** Creating Megafunction Variation
3. In the ALTMEMPHY parameterization page that appears, select **Stratix III** as the target device family, select the 2 speed grade, and enter the **clock rates** for the PLL reference input and the memory interface. For this example, set the PLL reference input frequency to **125 MHz** and memory clock rate to **400 MHz** (Figure 9).

Select **Half** under the selection for **Local interface clock frequency**. Full-rate PHY for the QDRII+/QDRII interface is currently not supported.

From the Memory Preset List, set the **Memory type** to QDRII+ SRAM and select memory preset titled **QDRII+ 1M ×18 BL4 CL2.5 400 MHz**.

**Figure 9.** Parameterizing the ALTMEMPHY for Your Target Memory Type and Frequency

4. The QDRII+SRAM device is a **2M × 18** device, so you need to select the option to **Modify Parameters**. This launches a memory preset editor window that you can modify all the memory parameters. Set the **Address width** to **19**. Verify that the other memory timing parameters match the QDRII+ SRAM datasheet as well. After making all necessary updates, select **OK**. This will create a custom memory preset with your selections (Figure 10).
5. Enter the dedicated clock phase for the address/command clock and the board skew specification for your design. These parameters account for skew across all the memory interface pins including K/K#/CQ/CQ# clock pins, D/Q data pins, and address and command pins. You can also fix the read latency. Use the default setting that is 0 cycle, where the read latency is referred as non-deterministic latency. This minimum read latency equals the worst-case latency measured out of all of the DQS groups. Otherwise, you can specify a latency between 15 and 22 cycles, where the latency is deterministic (Figure 11). For more information on the read latency setting, refer to the ALTMEMPHY User Guide.

6. In the Controller Interface Settings page, click Next to proceed.
7. For performing functional simulation, select **Generate simulation model** (Figure 12).
8. Select **Finish**. The MegaWizard Plug-In Manager generates all the necessary files for your ALTMEMPHY instance.

Upon the completion of the ALTMEMPHY megafuction instance generation, the Megawizard Plug-In Manager provides detailed instructions to apply the generated constraints as shown in **Figure 13**. This will be discussed in Step 5. With the ALTMEMPHY instance generated, you must now connect the PHY instance to the driver logic in your design.

Since SRAM devices do not need a memory controller, Altera does not offer such a product. You should connect the local signals of the memory interface from the PHY to the logic that will access the memory in your top-level design.
Figure 13. Instructions for Applying Constraints for the PHY

Step 4: Perform RTL/Functional Simulation (Optional)

For performing the functional simulation of your memory interface, use the functional models of the ALTMEMPHY megafunction generated by the MegaWizard Plug-In Manager in “Step 3: Instantiate PHY”. You should use this model along with your own driver or test bench that issues read and write operations, and a memory model.

The Verilog HDL or VHDL simulation model of the PHY can be found in your project directory and is named <variation_name>_all_mem_phy_qdrii_sequencer_wrapper.vo/.vho.

The design example includes the driver, test bench, as well as the memory model that allows you to perform functional simulation on the design. Use the ModelSim- Altera simulator to perform the functional simulation. The design example also comes with a script file that will direct the simulator to perform the necessary compilation and simulation.

Open the ModelSim- Altera simulator and change the path to your project folder. From the File menu, select Change Directory and specify your project directory. To run the simulation, from the Tools menu, go to TCL and select Execute Macro. From your project directory, go to the modelsim directory and run the run_all.do file. This file directs the ModelSim simulator to compile the necessary files and execute the wave.do file for the simulator to display the waveforms. Figure 14 shows the ModelSim simulation waveform of the design example.
Step 5: Add Constraints

As mentioned in Step 3, Figure 13 lists the steps you should follow to add the relevant timing and device constraints for your memory interface.

To add constraints, follow these steps:

1. Enable the TimeQuest Timing Analyzer tool under Settings, Timing Analyzer Settings. All designs using the ALTMEMPHY megafunction are required to use the TimeQuest Timing Analyzer for proper and accurate timing analysis.

2. Add the `<variation_name>_ddr_timing.sdc` file to your project. This file contains all the necessary timing constraints for the memory interface portion of your design (Figure 15).
Figure 15. Adding Timing Constraints for the PHY

3. Add the I/O standard and output enable group assignments for your memory interface pins by executing the `<variation_name>_pin_assignments.tcl` file (Figure 16). Output enable group assignments are required so as not to violate the requirements for the maximum number of pins driving out of a VREF group when a voltage-referenced input pin or bi-directional pin is present.

Note that the pin names listed in this script are generic names. You should modify them to match the top-level pin names in your design.
4. Enable the **Optimize Hold Timing** option for **All Paths** for the Quartus II fitter, under **Settings, Fitter Settings**. Specifying the All Paths setting directs the Fitter to optimize the hold time of all paths by adding delay to the appropriate paths.

5. Add the DQ group and memory interface pin group assignments for your memory interface pins by executing the `<variation_name>_assign_dq_groups.tcl` file. Executing this file groups the pins into the DQ/DQS read and write groups. It also directs the fitter to appropriately place all DDR related hardware blocks (like the DLL and DQS delay chain) relevant to those pins.

   ![Tcl Scripts](image)

   ```tcl
   #Please Run This Script Before Compiling
   if (!([info exists ::ppl_instance_name]) (set ::ppl_instance_name CURRENT_STRENGTH_NEU "NL")
   set_instance_assignment -name CURRENT_STRENGTH_NEU "NL"
   set_instance_assignment -name CURRENT_STRENGTH_NEU "NL"
   set_instance_assignment -name CURRENT_STRENGTH_NEU "NL"
   set_instance_assignment -name CURRENT_STRENGTH_NEU "NL"
   set_instance_assignment -name CURRENT_STRENGTH_NEU "NL"
   set_instance_assignment -name CURRENT_STRENGTH_NEU "NL"

   #End of Script
   ```

   Note that the pin names listed in this script are generic names and you should modify them to match the top-level pins names in your design.

   Executing the `<variation_name>_assign_dq_groups.tcl` file does not make the pin location assignments to the pins. You still need to make the pin location assignments based on your board layout. For the Stratix III Host Board, you can use the `SIII_host_qdrii_pin_location.tcl` file from the design example to create the pin location assignment.

In addition to adding constraints for all of your memory interface blocks, you should ensure that the rest of your design is also appropriately constrained. For example, you may need to add timing constraints into other clocks in your design, including the reference clock input to the ALTMEMPHY megafunction’s PLL instance.

When using the Quartus II Advanced I/O Timing option, provide the board trace information for the output and bi-directional pins of your design through the Board Trace Model in the Quartus II software. Through the Quartus II Pin Planner, you can enter the board trace information for every output or bi-directional pin, or for a net group separately.
From the Quartus II Pin Planner, right-click on the pin or net group, and select Board Trace Model, as in Figure 17.

**Figure 17.** Defining Board Trace Model in the Quartus II Pin Planner

The board trace Model window appears as in Figure 18.

**Figure 18.** Board Trace Model

Depending on your board, enter the values such as the trace length, capacitance/length, inductance/length, pull-up, pull-down and others.
Step 6: Compile the Design and Verify the Timing Closure

After your design is constrained, you are ready to compile your design.

After successfully compiling your design in the Quartus II software, run the timing reporting script generated by the ALTMEMPHY megafuntion during the megafuntion instantiation. This script is called `<variation_name>_report_timing.tcl` and it produces the timing report for the memory interface portion of your design. You can either run the .tcl file from the TimeQuest Timing Analyzer or from the Quartus II Tcl Console.

To run the report timing script in the TimeQuest Timing Analyzer window, open the tool in the Quartus II software. Then complete the following tasks:

- Update timing netlist
- Create timing netlist
- Read SDC file

Perform these tasks by double-clicking Update Timing Netlist in the left Tasks pane that will automatically perform the three tasks. After a task is executed, the task in the Tasks pane turns green.

Run the report timing script next by going to the Script menu and clicking Run Tcl Script. Select the `<variation_name>_report_timing_tcl`. You can also double click Report DDR on the Tasks pane to get the timing numbers.
Figure 19 shows the timing margin reported in the TimeQuest Timing Analyzer window after running the report timing script.

The report timing script provides information about the following margins and paths:

- Address and command setup and hold margin.
- Core setup and hold margin.
- Core reset and removal setup and hold margin.
- Read capture setup and hold margin.
- Write setup and hold margin.

The timing should be verified on every corner of the timing model. You must run the timing report script with all available timing models: slow 0°C, slow 85°C, and fast 0°C model to ensure positive margins across the process, the voltage and the temperature. To analyze timing on a different corner, first double-click Set Operating Conditions in the left pane. Select a new timing corner, then go to the Script menu and re-run the <variation>_report_timing.tcl script.

For more information about the TimeQuest Timing Analyzer window, refer to the TimeQuest Timing Analyzer chapter in volume 3 of the Quartus II Handbook.
For detailed information about timing analysis, refer to AN 438: Constraining and Analyzing Timing for External Memory Interfaces.

**Step 7: Adjust the Constraints**

If the timing report indicates that the setup or hold margins for one of the timing paths is negative, you must adjust the constraints on the design to improve margins for the failing path.

For instance, suppose that the address command timing path fails the hold time, you need to adjust the PLL clock-phase-shift setting for the clock generating the address and command signals to improve the hold margins (by increasing the phase-shift on the clock). This clock setting could be adjusted by editing the ALTMEMPHY megafonction instance in the MegaWizard Plug-In Manager, as shown in Figure 11.

**Step 8: Verify FPGA Functionality**

In order to use SignalTap II Embedded Logic Analyzer to help you verify your design on the board, create a .stp file and add in the necessary signals. You need to specify a clock source as well as the triggering conditions.

The SignalTap II Embedded Logic Analyzer does not allow you to monitor the D, DQ, DQS, and DQSn signals at the pins.

The design example includes the .stp file for you to verify the design on the Stratix III Host Board. Open the system_test.stp file to perform the verification using the SignalTap II Embedded Logic Analyzer. This file has the relevent internal signals added so that you can monitor the signal activities when the Stratix III device performs the read and write operations on the QDRII+SRAM device. Upon successfully configuring the device on the board, you can start monitoring the signal activities. The high pnf signal indicates the design works correctly.
Table 7 contains a design checklist that you can use when implementing QDRII+ and QDRII SRAM memory interfaces in Stratix III and Stratix IV devices.

### Table 7. Checklist for Implementing QDRII+ and QDRII SRAM Memory Interfaces in Stratix III Devices (Part 1 of 2)

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Yes/No</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Select Device</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Have you selected the memory interface frequency of operation and bus width? And, have you selected the FPGA device density and package combination that you will be targeting? Ensure that the target FPGA device supports the desired clock rate and memory bus width, as well as the FPGA must have sufficient I/O pins for the DQ/DQS read and write groups. For detailed device resource information, refer to the device handbook chapter on external memory interface support.</td>
<td></td>
</tr>
<tr>
<td><strong>Instantiate PHY and Controller</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Have you parameterized and instantiated the ALTMEMPHY megafunction for your target memory interface? When instantiating multiple instances of the ALTMEMPHY megafunction, ensure effective sharing of device resources and appropriate constraints by referring to AN 462: Implementing Multiple Memory Interfaces Using the ALTMEMPHY Megafunction.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Have you connected the PHY’s local signals to your driver logic and the PHY’s memory interface signals to top level pins? Ensure that the local interface signals of the PHY are appropriately connected to your own logic. If the ALTMEMPHY megafunction is compiled without these local interface connections, you may encounter compilation problems when the number of signals exceeds the pins available on your target device.</td>
<td></td>
</tr>
<tr>
<td><strong>Functional Simulation</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Have you simulated your design using the RTL functional model? Use the ALTMEMPHY megafunction functional simulation model in conjunction with your own driver logic/testbench, and a memory model to ensure proper read/write transactions to the memory.</td>
<td></td>
</tr>
<tr>
<td><strong>Timing Closure</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Have you added constraints to the PHY and the rest of your design? The ALTMEMPHY megafunction is constrained when you use the generated .sdc file and .tcl files. However, you may need to adjust these settings to best fit your memory interface configuration. Add pin assignment constraints and pin loading constraints to your design. Ensure that generic pin names used in the constraint scripts are modified to match your top level pin names. Note that the loading on memory interface pins is dependent on your board topology (memory components). Provide the board trace information for the output and bi-directional pins through the Board Trace Model in the Quartus II software.</td>
<td></td>
</tr>
</tbody>
</table>
Conclusion

Stratix III and Stratix IV FPGAs complement high-performance QDRII+ and QDRII SRAM devices by providing high memory bandwidth, improved timing margin, and great flexibility in system design. QDRII+ and QDRII SRAM with Stratix III and Stratix IV devices support the high-throughput requirements of today’s communication, networking, and digital signal processing systems.
References

- External Memory Interfaces in Stratix III Devices chapter of the Stratix III Device Handbook
- External Memory Interfaces in the Stratix IV Devices chapter of the Stratix IV Device Handbook
- CY7C1163V18 18-Mbit QDRII+ SRAM Device Data Sheet

Document Revision History

Table 8 shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date &amp; Document Version</th>
<th>Changes Made</th>
<th>Summary of Changes</th>
</tr>
</thead>
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<tr>
<td>July 2008 v1.1</td>
<td>■ Changed application notes title to “AN 461: Design Guidelines for Implementing QDRII+ and QDRII SRAM Interfaces in Stratix III and Stratix IV Devices”.&lt;br&gt;■ Updated Table 1.&lt;br&gt;■ Added Table 2, Table 3, and Table 4.&lt;br&gt;■ Added Figure 1 and Figure 2.&lt;br&gt;■ Replace Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, and Figure 19.&lt;br&gt;■ Added Figure 13, Figure 14, Figure 17, and Figure 18.&lt;br&gt;■ Updated and added additional notes to Table 6.&lt;br&gt;■ Added new paragraph under “Step 3: Instantiate PHY”, “Step 4: Perform RTL/Functional Simulation (Optional)”, “Step 5: Add Constraints”, and “Step 7: Adjust the Constraints” sections.</td>
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<tr>
<td>June 2007 v1.0</td>
<td>■ Initial release</td>
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