DesignPerspective

Transceivers With Integrity.

What is the Stratix® II GX device family?

The 90-nm Stratix II GX family is Altera's third generation of FPGAs with embedded transceivers. Integrating up to 20 serializer/deserializer (SERDES)-based transceivers, Stratix II GX devices operate from 622 Mbps to 6.375 Gbps, delivering low jitter generation, excellent jitter tolerance, and low power consumption.

The devices are part of a complete programmable solution from Altera aimed at the growing number of applications and protocols requiring high-speed serial interconnect. Stratix II GX devices share the same ground-breaking architecture as Altera's high-density Stratix II FPGAs.

When will Stratix II GX devices be available?

Stratix II GX devices are available NOW.

What are the benefits of using the Stratix II GX family?

The Stratix II GX family offers a complete protocol solution of intellectual property (IP) cores, system models, reference designs, signal integrity tools, and supporting collateral so you can complete your high-speed designs quickly and efficiently, improving your time to market.

Additionally, since Altera developed the Stratix II GX family based on customer input and protocol roadmaps, the family provides the industry's best signal integrity and lowest power compared to competing solutions, reducing board layout risks and improving system performance margins.

What standards does the Stratix II GX family support?

The Stratix II GX family supports many protocol standards, including PCI Express, Serial Digital Interface (SDI), XAUI, SONET, Gigabit Ethernet, SerialLite II, Serial RapidIO™ (SRIO), and Common Electrical Interface 6 Gbps Long Reach and Short Reach (CEI-6G-LR/SR) standards.

How do I start a Stratix II GX design?

You can begin designing *now* with the Stratix II GX family using Quartus® II software version 5.1. Quartus II design software is easy to use, with feature-rich synthesis and simulation tools that take full advantage of Stratix II GX performance and design benefits. Quartus II software also integrates seamlessly with all of the leading third-party synthesis and simulation tools. HSPICE and IBIS models for standard and transceiver I/O models are available today, and a Stratix II GX signal integrity development kit is planned to ship in May.

How much power do Stratix II GX transceivers consume?

Significantly lower in power consumption than competitive offerings, Stratix II GX device transceivers consume only 140 mW per channel at 3.125 Gbps and 240 mW per channel at 6.375 Gbps.

Which external memory interfaces are supported by Stratix II GX devices?

The Stratix II GX device family meets the performance requirements of the latest SRAM and DRAM devices, as shown below. You can easily connect external memory devices to Stratix II GX devices to provide additional storage capacity outside of the abundant on-chip memory resources without causing performance bottlenecks. You can purchase Altera- or third-party-developed IP memory controller cores, download royalty-free reference designs from the Altera web site, or develop your own customized cores for your specific application.

High-Performance External Memory Interface Support in Stratix II GX Devices

Memory Technology	I/O Standard	Bus Width	Maximum Clock Speed
SDR SDRAM	LVTTL	72 bits	200 MHz
DDR SDRAM	SSTL-2 Class I, II	72 bits	200 MHz
DDR2 SDRAM	SSTL-18 Class I, II	72 bits	333 MHz
RLDRAM II	SSTL-2 Class I, II	36 bits	300 MHz
QDR SRAM	HSTL-1.8 Class I, II	36 bits	167 MHz
QDRII SRAM	HSTL-1.8 Class I, II	36 bits	300 MHz