System Optimization Through Code Profiling with Streamline

Introduction

When bringing up an embedded system, the debug process can take a long time. Once a system is functionally working, it is often necessary to optimize performance and power. This Architecture Brief describes how the ARM® Streamline tool, contained in the ARM Development Studio 5™ Altera Edition Toolkit, can be used to quickly profile an entire system and optimize for performance and power.

The ARM Development Studio (DS-5) Altera Edition Toolkit provides unique features to help reduce overall debug time on Altera SoC FPGA:

- FPGA Adaptive Debug and Multi-Core Debugging (see Altera SoC FPGA-Adaptive Debug Architecture Brief).
- System Trace on SoC FPGAs containing System Trace Macrocells (STMs) (see System Trace Macrocell (STM) Packs Major Benefits for High-Performance SoC System Debug Technical White Paper).
- Application Code Profiling with Streamline (the focus of this architecture brief).

Key aspects of this Architecture Brief are highlighted in the video “Software Development Tools: Whole Chip Debug” which can be found at www.altera.com/socarchitecture in the “Tools” section.

Profiling CPU Cores and FPGA

System profiling helps developers find answers to the questions:

- Where are the hot spots in the system?
- Which parts of the application to accelerate in the FPGA fabric?
- What are the performance bottlenecks for communicating between processor and FPGA?
- How efficiently is cache being used?

To be helpful in a processor-based system, FPGA events must be part of the profile. With FPGA-adaptive debugging, the ARM DS-5 Streamline profiling tool can ‘see’ the entire chip, not just the dual-core Cortex-A9 processor subsystem. Even as a designer adds hardware processing logic into the FPGA, registers automatically update so that the DS-5 Altera Edition user can ‘see’ these new hardware acceleration engines or specialized processing cores. With the ARM DS-5 Streamline profiling tool, the engineer can understand how the new logic affects bottlenecks and loops in processor threads, as well as whether the power profile improves.
Performance and power analysis tools have become a major area of focus for tools vendors. One important reason to choose mixed SoC and FPGA devices is the ability to use FPGA hardware blocks to accelerate software tasks. For example, FFT decoders or DES decryption algorithms in the FPGA fabric can be used to free up the processor, which can either perform another task in parallel or just go to sleep and save power consumption. For these devices it is essential that tools provide visibility of the relative levels of utilization of the processor and FPGA IP blocks over time. This information can then be used by the designer to optimize the whole system, implementing the right number and type of IP blocks on the FPGA, partitioning the software to make efficient use of them, and balancing the load between hardware resources.

Although instruction trace is often used for optimizing software codecs and other performance critical software, it is not the right kind of analysis tool for understanding system-level performance bottlenecks. For ARM applications processors running complex operating systems such as Linux, analysis tools that rely on OS instrumentation and statistical sampling are normally preferred. The ARM DS-5 Streamline performance analyzer is an example of such type of tool.

The Streamline performance analyzer makes use of a Linux driver running on the target to sample information from the target at regular time intervals and every time that there is a task switch. The information captured is provided as counters for the following types of events:

- Operating system events such as processor load, memory usage and network load.
- Processor events such as branch mis-predictions, level1 cache hits and misses, or number of instruction interlocks.
- System events such as level2 cache misses. These counters are made available by the relevant system IP blocks as memory mapped registers, and enable the user to spot system-level bottlenecks.
- Software annotations, used by applications to report events of interest that the user would like to correlate with performance counters.
When this information is visualized together on a timeline, the interactions between software and hardware are made apparent to the developer, who has better information to optimize the target as a complete system.

On fixed hardware targets, the information provided by Streamline can only be used to change the software. However, on mixed SoC and FPGA devices it can be used to simultaneously optimize hardware and software, by choosing the right FPGA acceleration blocks and adapting the software to use those blocks efficiently. The only infrastructure required in the hardware is memory-mapped registers that count the level of utilization of each different IP block. Streamline can then be configured to access those new counters and display their value over time, correlated with CPU activity and other system-level counters.

Conclusion

This Architecture Brief described how the Altera solution based on the ARM DS-5 Altera Edition Toolkit empowers developers to understand and optimize SoC FPGA applications at the system level, enabling project teams to implement advanced features in these new devices while keeping schedules on track.

Want to Dig Deeper?

For more details on the ARM DS-5™ Altera Edition Toolkit, consult the web site:

For more details on the ARM DS-5 Streamline Performance Analyzer, visit the ARM website at:
http://ds.arm.com/ds-5/optimise/