Architecture Brief

CoreSight Compliant Debug for SoC FPGAs

Introduction

Not all SoC FPGA debug architectures are created equal: some use System Trace Macrocells (STMs) while others use Instruction Trace Macrocells (ITMs). The type of CoreSight macrocell used has a dramatic impact on debug quality, performance and bandwidth. ITMs were designed to process low performance microcontroller debug trace streams; STMs were developed specifically to process high performance debug trace streams found in applications processors like the ARM Cortex-A9 processor debug trace streams. ITMs drop data in high performance systems, while STMs capture and make accessible 100% of the system trace data.

This Architecture Brief explores the implications and advantages of the CoreSight STM to deliver an effective, superior debug framework for Altera SoC FPGAs when coupled with the ARM® Development Studio 5 (DS-5™) Altera Edition Toolkit.

These concepts are related to a larger discussion on the SoC FPGA debugging process which can be found in the Development Tools section of the A Look Inside: SoC FPGAs video series at:

http://www.altera.com/socarchitecture

System Trace Macrocell

One of the key features of Altera SoC FPGAs is the use of the ARM® CoreSight™ System Trace Macrocell (***Figure 1***) to aid in debugging. This was such a key factor that Altera made certain to include this critical functionality in all SoC FPGA devices. Altera SoC FPGAs are the only SoC FPGA devices currently on the market with the CoreSight STM trace element integrated. Furthermore, Altera strategically aligned with ARM to develop the ARM DS-5 Altera Edition Toolkit which was designed hand-in-glove with the STM to deliver a complete debug solution.

So, just what is a System Trace Macrocell?

In essence, the STM processes instrumentation instructions with system-level awareness. It processes trace coming from multiple points in the system, tags the debug trace data with interesting and useful meta-data, and makes all of that information available to a debug tool (such as the ARM DS-5 Altera Edition Toolkit) running on a host.

The ARM STM documentation states:

- "The STM is a trace source that is integrated into a CoreSight system, designed primarily for high-bandwidth trace of instrumentation embedded into software. This instrumentation is made up of memory-mapped writes to the STM Advanced eXtensible Interface (AXI) slave, which carry information about the behavior of the software."[1]
- "… system trace units provide the ability for running software to be instrumented with messaging (either by the programmer, or through a tool flow)."[2]

In other words, the STM provides trace data that can be analyzed retrospectively based on event triggers in software or hardware.

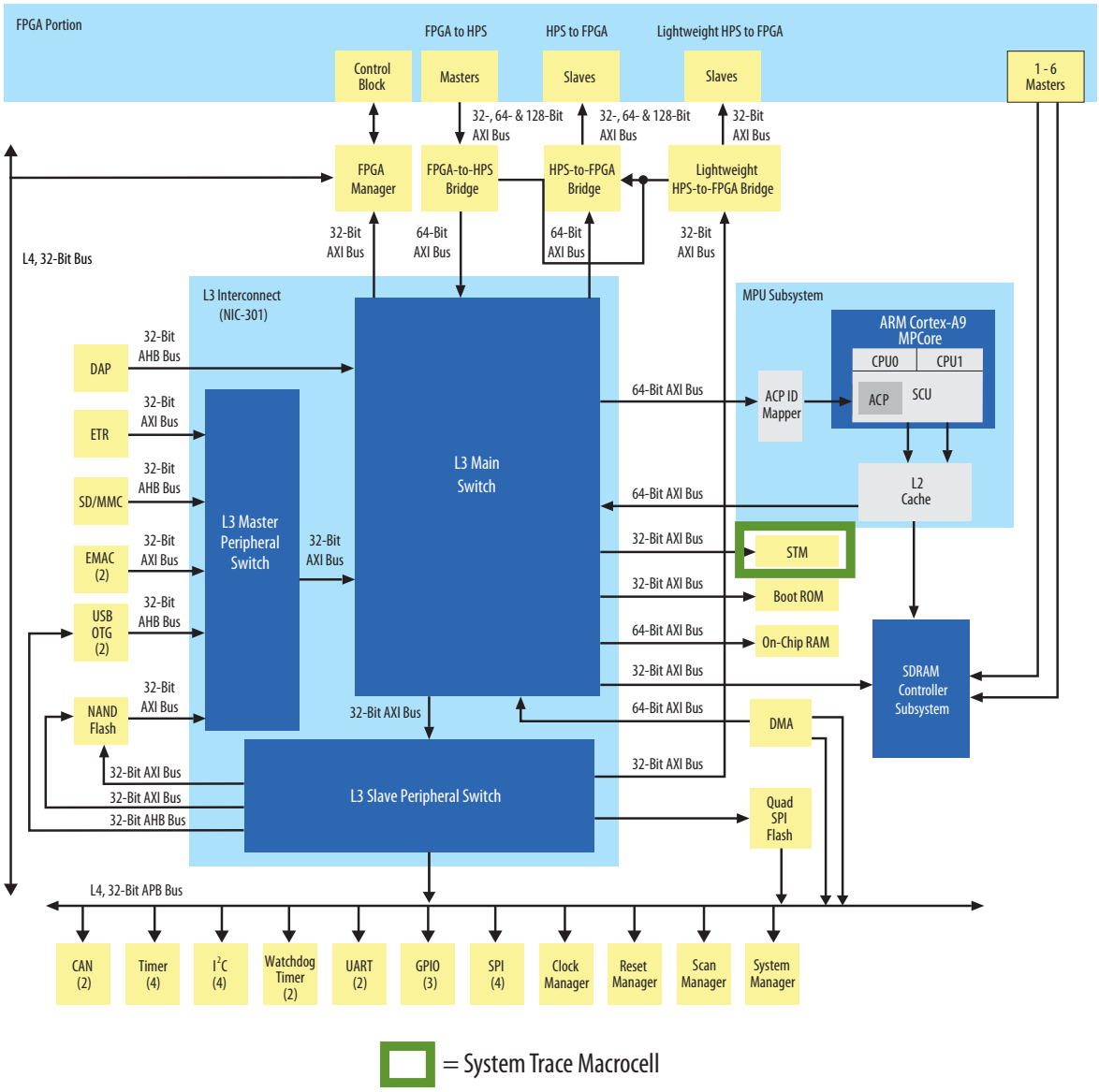
[1] ARM CoreSight System Trace Macrocell Technical Reference Manual, section 1.1

[2] ARM CoreSight Technical Introduction White Paper, p. 6

An STM puts low level source trace data into a system level view. The STM can receive trace data from any of up to 65,000 trace sources. Many of these sources can be CoreSight trace macrocells implemented in the FPGA region of the SoC FPGA device.

STMs either retain source timestamps, or can timestamp data as it is processed. The timestamp precision is high, and facilitates fine-grained cross-correlation of events. What's more, an STM has the ability to 'tag' trace streams with the current user-defined system states. Trace flowing from an STM, through the Debug Access Port (DAP) and into the host system running the ARM DS-5 Altera Edition Toolkit, is chock full of useful debug meta-data. An engineer using the ARM DS-5 Altera Edition Toolkit to debug SoC FPGAs with STMs is well-provisioned to quickly cut through system level complexity, identify root-cause bugs and fix them.

Figure 1: Altera Cyclone® V SoC Block Diagram With The System Trace Macrocell Highlighted



Bus Structure

STMs receive data on a wide, high speed dedicated AXI bus. It has a 32KB FIFO to buffer incoming data. When that FIFO fills up, the STM can signal back-pressure to upstream CoreSight Elements, many of which also contain 32KB FIFOs, to process all of the trace data. These provisions are adequate to support full-performance trace and debug in a high speed, dual-core ARM Cortex-A9 processor system. But performance isn't the whole story.

Altera STMs allow multiple processors and processes to share and directly access the STM without being aware of each other. They are allocated different pages in the STM stimulus space. 128 masters, each supporting 65,536 stimulus ports, enable significant scalability, with 16 stimulus ports (or channels) per 4KB page.

STMs can therefore handle lots of burst data from lots of sources.

Performance

STMs have a dedicated AXI slave to receive trace data and a separate APB interface to deliver macrocell programming information. The STM's AXI bus can burst 4KB of data at a time, or step through one word at a time. The STM output is 32-bit and runs at the host processor speed. This provides plenty of performance for getting trace to the host debug tool.

STMs are aware of all other trace macrocells in the hardened processor subsystem; Embedded Trace Macrocells (ETMs) and Program Trace Macrocells (PTMs) addresses are included in the DAP ROM table.[3] In the event an FPGA designer decides to implement additional CoreSight compliant structures in the SoC FPGA fabric, he or she can. Specifically to support the extensibility of CoreSight compliant debug structures into the FPGA region, Altera has included an entry in the DAP ROM table. It serves as a linked list header in what could be a chain of many debug structures. Designers can therefore link as many debug structures as desired in FPGA regions, confident that corresponding trace data will show up in the debugger. The ARM DS-5 Altera Edition Toolkit makes visible all of the trace data these 'soft logic' CoreSight components produce.

Timestamps

All CoreSight compliant data structures built into Altera SoC FPGA devices can send data with accurate, 48-bit timestamps. Outgoing packets retain the original precision for accurate cross-correlation of data across multiple processing units.

Altera SoC FPGAs' timestamping is flexible. For example, it can be requested for each write independently, based on the address written to. Bandwidth can be optimized by requesting a timestamp for only one write in a message made up of several writes.

Timestamps are automatically correlated with other timestamping trace sources in the CoreSight system. For example, STM trace can automatically be correlated with PTM and ETM trace.

STMs allow users to create up to 32 custom systems states, such as low power or memory transaction ECC error flag; these states are user-defined. So a debug engineer can set up his system states to help understand the conditions – at a system level – that are really going on at the time of unexpected behavior. This can be enormously useful in that it eliminates much guess-work about wider system activities.

CoreSight Debug Circuitry

The ARM DS-5 Altera Edition Toolkit, can access trace data generated by all CoreSight circuitry included in Altera SoC FPGAs, for it to be viewed and analyzed with one design kit.

[3] ARM CoreSight DAP-Lite Technical Reference Manual, section 2.9

Table 1: In-System Debugging Features for SoC FPGA Devices

Function/Feature	Altera SoC EDS (with ARM DS-5 Altera Edition)	Vendor B's Debug Tools
System Level Debug Macrocell	System Trace Macrocell (STM)	Instrumentation Trace Macrocell (ITM)
Accessible via vendor supplied development tools	Yes	No. 3rd party tools are required.
Trace Data Input Bus	Dedicated AXI bus (high speed 32 bit)	Shared APB bus (slow 32 bit every other cycle)
Trace Data Input Bus Details	48MB address space, can burst 4KB data per input processor/peripheral	1KB address space, must write sequential 32b words from each processor / peripheral
Configuration Bus	Dedicated APB	Shared APB
Output to Debug Funnel	32 bit	8 bit
# Events	32 state level events	0 (not supported)
Can trigger external DMA	Yes	No
Timestamp correlation across multiple events	Yes	No
Extensible to CoreSight compliant macrocells implemented in FPGA fabric	Yes	No
Local buffer	1kb in STM	8 bytes in ITM
Debug System Buffer	ETF 32KBytes	ETB 4KBytes
Timestamp accuracy	48b	21b
CPU↔FPGA CoreSight Compliant Cross-Triggering	Yes	No Vendor proprietary
Route Trace Packets to Various Destinations (e.g. DRAM or high-speed transceiver)	Yes CoreSight Embedded Trace Router	No

Conclusion

Coresight STMs contained in Altera SoC FPGAs and accessed by the SoC EDS with ARM DS-5 Altera Edition Toolkit deliver detailed trace data to debug complex systems quickly, confidently and efficiently.

Want to Learn More?

For a high level comparison between STMs vs. ITMs and their implications on debug capability, refer to the technical white paper "System Trace Macrocell (STM) Packs Major Benefits for High-Performance SoC System Debug".

For more details on the ARM DS-5 Altera Edition Toolkit, consult the web site:

http://www.altera.com/devices/processor/arm/cortex-a9/software/proc-arm-development-suite-5.html

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