Scalable, Differentiated, Future Proof

Designing Basestation Channel Cards with FPGAs

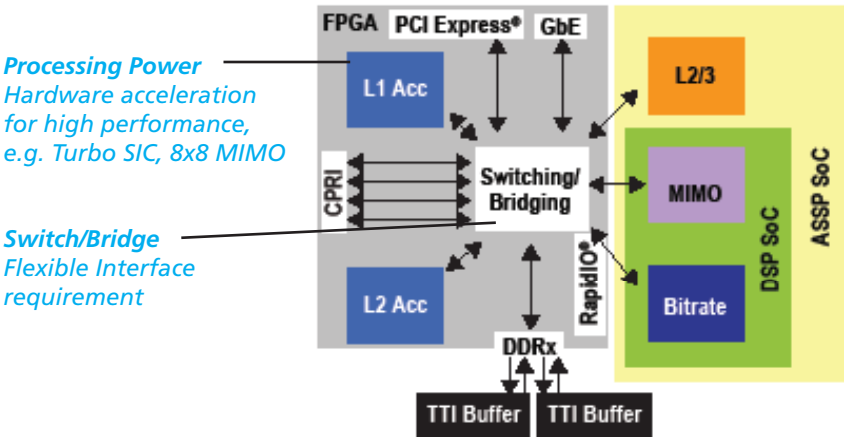
Basestation channel card technology is evolving at a rapid pace to address emerging 4G wireless standards, such as LTE-Advanced, as well as disruptive network architectures, such as baseband pooling for centralized radio access network (C-RAN) and small cells. Altera's broad portfolio of 28-nm FPGAs and ASICs combined with productivity-enhancing software tools, development boards, intellectual property (IP), and reference designs enable you to future proof and differentiate your channel card designs.

Faster and Differentiated Designs, Lower Total Cost

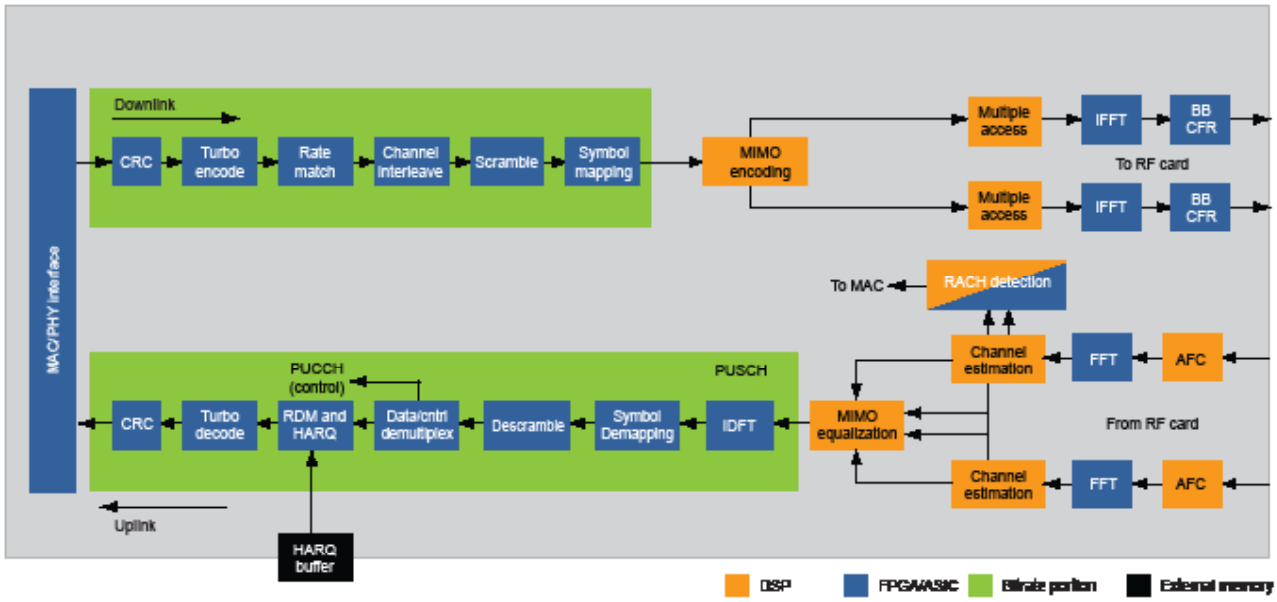
Our technologies enable future-proof, multistandard channel card development, while also providing tools to help accelerate your design cycle and lower total cost of ownership (TCO).

- Comprehensive portfolio of FPGA, SoC FPGA, and ASIC platforms
  - -Stratix® V GS and GX FPGAs for switching/bridging in macro basestation
  - -Arria® V SoC FPGAs for integrated designs such as pico and micro basestation
  - -Cyclone® V FPGAs and SoC FPGAs for co-processing with ASSPs for pico and femto basestation
  - -HardCopy® V ASICs for lowest-cost and lowest-power designs with the smallest board size
- Productivity-enhancing tools, IP, and development boards
  - -Protocol agnostic switching/bridging reference design that demonstrates a framework for building chip-to-chip and board-level switching solutions
  - -L1 and L2 hardware acceleration blocks such as fast Fourier transform (FFT), discrete Fourier transform (DFT), Turbo, and multiple-input/multiple-output (MIMO)
  - -Off-the-shelf IP cores for Common Public Radio Interface (CPRI), Open Base Station Architecture Initiative (OBSAI), and Serial RapidIO® (SRIO) interfaces
  - -Advanced mezzanine card (AMC) form factor development boards from partners such as BittWare

Switching/Bridging and Hardware Acceleration



Example of Hardware/Software Partitioning for LTE PHY Layer Processing



LTE and LTE-A Baseband

The complex PHY layer signal processing in LTE and LTE-A can be broadly divided into bitrate and symbol-rate functionality as show in the figure above.

Altera IP and reference design blocks:

- Complete LTE PUSCH uplink bitrate reference design including blocks such as inverse DFT, symbol demapper, channel deinterleaver, rate dematcher and Turbo decoder
- LTE symbol rate blocks such as channel estimation, MIMO equalization, and FFT/ inverse FFT
- Floating-point matrix arithmetic blocks such as matrix decomposition and matrix inversion
  -DSP Builder Advanced Blockset-based designs
  -Used for advanced receiver processing such as coordinated multipoint (CoMP)
- Layer 2 hardware acceleration blocks such as Snow 3G, robust header compression (ROHC), and advanced encryption standard (AES)
- Timing and synchronization cores including IEEE 1588 v2 and SyncE

Our ecosystem of design service partners offer system-level solutions such as L2, transport stacks, and integrated small cell solutions to help you shorten your development time.

Altera's Connectivity Cores

You can also select from our suite of connectivity cores for commodity interfaces such as CPRI, OBSAI, SRIO, PCIe®, and GigE. Leveraging our expertise in optical transport networks (OTN) technology, we offer transport and basestation connectivity solutions for emerging network architectures such as C-RAN.

Want to dig deeper?

For more information about how Altera's 40-nm transceiver-based device portfolio can support your RRH applications, contact your Altera representative, or visit **www.altera.com/wireless**.

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