Switch to Intelligence

Intel® Tofino™ Intelligent Fabric Processors
Disruption can be exciting, but not with your network

As data centers accelerate into the cloud-native era, it is more important than ever to build your network infrastructure with a software-defined approach.

Intel® Tofino™ Intelligent Fabric Processors (IFPs) are programmable with the Programming Protocol-independent Packet Processors (P4) open source programming language. They deliver intelligence, performance, visibility and control with program-optimized power consumption, real-time in-band network telemetry (INT) and enhanced congestion control for workloads spanning the entire edge-to-cloud spectrum. To support the industry proliferation of artificial intelligence (AI), Intel IFPs offer intelligent packet processing to accelerate machine learning (ML) workloads.

The Intel Tofino IFPs’ comprehensive suite of development and workload-monitoring tools, including Intel® P4 Studio Software Development Environment (Intel® P4 Studio SDE) and Intel® Deep Insight Network Analytic Software, simplifies integration of container-based microservices, provides long-term investment protection, and paves the way to a more secure and self-healing cloud infrastructure.

The Intel Tofino IFPs’ robust set of hardware and software capabilities allows your network engineers to spend more time advancing, rather than maintaining, your network.

Switch to intelligence with Intel Tofino Intelligent Fabric Processors.
Today’s data centers face the challenges of stranded resources, congested data flows, and incompatible platform security. To meet these needs going forward, a new architecture is required. Intel has a vision for this new architecture of the data center of the future. This architecture will have three categories of compute—CPUs for general-purpose compute, “XPU” architectures for application-specific or workload-specific acceleration, and infrastructure processing units (IPUs) for infrastructure acceleration—that will be connected through an intelligent fabric to efficiently utilize data center resources.

Connecting the data center of the future

The intelligent fabric must be able to accommodate numerous complex needs:

- A cloud-native architecture with optimized container-based processing, orchestration, and automation
- AI and distributed, changing workloads that spawn the need for growing network optimizations
- End-to-end security

Service providers must meet all of these needs while maintaining or decreasing investments in network capital expenditures (CapEx) and operating expenses (OpEx).
AI acceleration

AI is becoming ubiquitous. To reach an increasingly higher level of accuracy in real-world applications, ML models are becoming larger and larger, and they are being trained on huge datasets. Therefore, distributed training has become the norm. As the scale and size of DL models increases, distributed DL is becoming communication-bound.

Intel, KAUST, and Microsoft have developed a range of techniques that are effective at mitigating the network-communications bottleneck and accelerating the performance of distributed training using P4-programmable Intel Tofino Intelligent Fabric Processors. These techniques can help improve performance while also reducing the cost of the network in terms of infrastructure and power. The SwitchML open source project was launched in April 2021 by Intel within P4.org.

For more information, visit the following resources:

- [usenix.org/conference/nsdi21/presentation/sapia](usenix.org/conference/nsdi21/presentation/sapia)
- [https://github.com/p4lang/p4app-switchML](https://github.com/p4lang/p4app-switchML)
With P4, networking is now becoming software-defined, and it is catching up with other areas of how IT infrastructure is built. The P4 language gives a common syntax and semantics to define a networking pipeline, and a variety of programmable networking equipment is evolving that can run those workloads.
In general, traditional switch devices have evolved little since their inception in the 1980s, having been optimized for density and simplicity. At the lowest level, these devices perform several simple operations to switch packets or frames, including:

1. Identifying data both from the system and within the frame (parsing packet headers)
2. Performing a set of field lookups and header transformations
3. Selecting an output port on the switch to transmit the modified frame

In legacy switches, these operations are generally implemented as distinct and rigid functions, interconnected with each other in strongly defined ways. A key drawback to this approach is that, in cases where not all these functions are enabled, large parts of the built-in logic can go underutilized or, in many cases, not utilized at all.

The Intel Tofino IFP is the first Ethernet packet switch architecture to utilize the Match-Action Pipeline, which provides highly programmable packet processing capabilities at extremely high data rates. Intel Tofino IFPs enable bandwidth usability to exceed what was previously available on high-bandwidth, purpose-built, fixed-function Ethernet switch ASICs. The programmable nature of Intel Tofino IFP pipelines, combined with the Match-Action Pipeline forwarding model, allows end users to easily define and deploy new forwarding functionality, features, and even novel networking protocols. With Intel Tofino IFPs, end users are empowered to innovate at the speed of software development.

**Optimize workloads, drive high utilization with programmability**

**Fixed-function ASIC:**
Features and table-sizes are hard-coded, not optimized, and often wasted.

**Intel IFP:**
Software defines the headers, table sizes, and packet-processing functions.
The pipeline is fully workload-optimized.
The Intel Tofino IFP family is a portfolio of highly integrated, flexible packet processing devices. Built upon the Protocol Independent Switch Architecture (PISA), Intel Tofino IFPs can be used in many applications and many places in the network, such as ultra-high-density top-of-rack (ToR) systems, multi-chip chassis-based systems, or fabric-interconnection equipment.

The devices’ underlying architecture consists of multiple parallel forwarding pipelines with a large, unified packet buffer and traffic manager, along with Match-Action Pipeline stages and memory resources per pipeline where P4 code for packet processing is implemented through an embedded real-time P4 compiler.

The Intel Tofino Series of P4-programmable Ethernet switch ASICs comprises devices with bandwidths from 1.8 to 6.4 Tb/s, with either 2 or 4 pipelines, and SerDes speeds of 10 and 25 Gb NRZ. The “pipeline folding” technique can be used to increase forwarding resources that can be allocated to inputs/outputs (I/Os), while dividing the number of possible externally facing I/Os in half.

The Intel Tofino 2 Series of P4-programmable Ethernet switch ASICs comprises devices with bandwidths from 4.8 to 12.8 Tb/s, with either 2, 3, or 4 pipelines, and 50 Gb PAM4 SerDes speeds with 10/25 Gb NRZ support. Programmability resource enhancements, advanced flow control, and port mirroring flexibility, along with 400 Gb MAC support, are among the key added features.

The Intel Tofino 3 Series of P4-programmable IFPs comprises devices with bandwidths from 12.8 to 25.6 Tb/s, with either 4 or 8 pipelines, and it offers both 50 Gb and 100 Gb PAM4 SerDes options at each bandwidth. With maximum MAC speeds at 400 Gb and an increased port buffer, this third-generation of the Intel Tofino product family focuses on hyperscaler use case power savings with minor pipeline enhancements.
## Three generations of Intel Tofino IFPs at-a-glance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Intel Tofino 1 (up to 6.4 Tb)</th>
<th>Intel Tofino 2 (up to 12.8 Tb)</th>
<th>Intel Tofino 3 (up to 25.6 Tb)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>16 nm</td>
<td>7 nm</td>
<td>7 nm</td>
</tr>
<tr>
<td>Num of MAU stages/pipe</td>
<td>12</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Total SRAM/pipe</td>
<td>120 Mb</td>
<td>200 Mb</td>
<td>200 Mb</td>
</tr>
<tr>
<td>Total TCM/pipe</td>
<td>6.2 Mb</td>
<td>10.3 Mb</td>
<td>10.3 Mb</td>
</tr>
<tr>
<td>Scheduler</td>
<td>1-level</td>
<td>2-level</td>
<td>2-level</td>
</tr>
<tr>
<td>Number of queues/port</td>
<td>32/100 Gb port</td>
<td>Up to 128/400 Gb port</td>
<td>Up to 128/400 Gb port</td>
</tr>
<tr>
<td>CPU port queues</td>
<td>32</td>
<td>Up to 128</td>
<td>Up to 128</td>
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<tr>
<td>Maximum SerDes speed</td>
<td>25 Gbps</td>
<td>56 Gbps</td>
<td>112 Gbps</td>
</tr>
<tr>
<td>Port speeds supported</td>
<td>100 Gb/50 Gb/40 Gb/25 Gb/10 Gb</td>
<td>400 Gb/200 Gb/100 Gb/50 Gb/40 Gb/25 Gb/10 Gb</td>
<td>400 Gb/200 Gb/100 Gb/50 Gb/40 Gb/25 Gb/10 Gb</td>
</tr>
<tr>
<td>Maximum port contexts</td>
<td>256</td>
<td>256</td>
<td>256</td>
</tr>
</tbody>
</table>

### Intel Tofino 1
100/50/40/25/10 gigabit Ethernet (GbE)
25/10 Gb NRZ SerDes
256-port radix

### Intel Tofino 2
400/100/50/40/25/10 GbE
50 Gb PAM4 and 25/10 Gb NRZ SerDes
256-port radix

### Intel Tofino 3
400/100/50/40/25/10 GbE
100/50 Gb PAM4 and 25/10 Gb NRZ SerDes
256-port radix
Extend capabilities with Intel FPGAs

The Intel Tofino IFP is intended primarily for switching applications—for example, leaf, spine, and top-of-rack switches—and its openness and flexibility through P4 programming unlocks many more applications including packet brokers, load balancers, various types of gateways, and network testers. Some of these applications push the boundaries of what can be placed onto the available silicon area by requiring support for a high number of sessions and tables to store their state and/or deep buffers for traffic scheduling and shaping.

In these use cases, Intel Tofino IFP–based systems can be augmented by adding an FPGA or multiple FPGAs to provide additional resources. With the latest Intel FPGAs, it is possible to get tens of gigabytes of high-speed memory that can be used to implement extra-large tables or extra-large buffers. Intel FPGAs offer other resources as well, including a hierarchy of memories that allow for algorithmic implementations of various functions that can further extend the deployment possibilities of an Intel Tofino IFP–based system. Some examples are cryptography, pattern matching, and floating-point mathematics.

Unleashing network functions with Intel Tofino IFPs and Intel FPGAs

FPGA look-aside to Intel Tofino IFP
- Cloud gateway (LB, NAT, FW, VxLAN)
- Broadband access and 5G gateway
- Carrier-grade security and NFV
- Network packet broker
- AI/ML acceleration

FPGA inline with Intel Tofino IFP

100 GbE data connections
10 GbE control connections
Data-plane traffic path
Look-aside traffic path
## Solutions for Service Providers

Intel has several applications deployed for communications service providers (CoSPs) and cloud service providers (CSPs) around the globe, and others are working with Intel and the ecosystem partners on pilots and proofs of concept (PoCs), many involving 5G.

With the silicon architecture of Intel Tofino IFPs, CoSPs and CSPs can accelerate innovation and services. Network engineers can plan, qualify, and deploy network architecture more simply and rapidly with P4-programmable IFPs—with no need to worry about the compatibility of different systems based on distinct silicon architectures for each network function.

CoSPs and CSPs can rely on Intel Tofino IFPs engineered with agile programmable architecture, enabling customers to deploy customized solutions from ToR switches all the way through the web-scale data centers and across the service-provider networks with a fully unified routing and switching portfolio.

### Intel Tofino IFPs support a wide range of applications

With exponential growth in network usage and transmission bandwidths, one key effort is at the heart of every chip designed and produced by Intel: a methodological approach to lowering power consumption.

Intel Tofino IFPs are the only Ethernet switch devices in the industry to offer a “consume-as-you-need” model and support optimizations for predictable traffic patterns in hyperscaler environments.
With an increase in network traffic and businesses transforming their infrastructures toward private, public, and hybrid clouds, administrators have been asking for tools that will enable them to take more control of their networks. Software-defined networking (SDN) technologies provide initial solutions to this challenge by separating the control plane from the data plane and therefore simplifying network provisioning, management, and troubleshooting. However, due to inflexible fixed-function switching hardware, SDN has not been able to achieve its full potential. The degree to which software can transform IT has been limited by the rigidity of the switching silicon.

Intel has revolutionized the industry with fully programmable Intel Tofino IFPs. Key to enabling this programmability is a robust and flexible Intel® P4 Studio SDE.
Intel Deep Insight Network Analytics Software

Intel Deep Insight Network Analytics Software provides network operators the path and origin of each packet traversing the network, in addition to a precise description of network events and anomalies observed in the network. Intel Deep Insight Network Analytics Software uses INT to track packet flow, remediate problems quickly, and help improve network uptime.

**Real-time network-event and anomaly detection**

Intel Deep Insight Network Analytics Software detects network events like new flows, flow termination, end-to-end latency change, hop latency change, unused link, unused switch, and path change. With insight into the various events occurring in the network, operators can make remediations. Furthermore, these insights can also help with packet-drop analysis, providing packet-drop details with granular and rich information, including: timestamp, drop reason, packet 5-tuple, packet metadata, ingress/egress port, and queue ID.
Congestion analysis

In enterprise data centers, many-to-one communication patterns, commonly found in application frameworks such as Apache Hadoop and HDFS, can result in congestion, queue build-up, and increased latency. Some applications also produce bursty traffic, with short-lived periods of very high throughput. Intel Deep Insight Network Analytics Software can quickly analyze such anomalies and visualize the full dynamics of a congestion event, down to each individual packet.

Applications:
- Financial and trading apps
- Distributed storage apps (Hadoop, MapReduce, HDFS, Cassandra)
- Cloud data center apps (web search, maps, social networks, data warehousing and analytics)

Switch to Intelligence

Intel Tofino Intelligent Fabric Processors deliver a dynamic suite of intelligent, software-defined solutions to transform your network switching infrastructure into an intelligent network fabric. Intel Tofino IFPs are comprehensive solutions with the ability to handle unique workloads across the entire edge-to-cloud spectrum. Furthermore, Intel is committed to advancing the Intel Tofino Intelligent Fabric Processor ecosystem and pushing the boundaries of cloud-native technology to new heights.
Get involved

You can get involved by joining the effort of the P4-programming community (https://p4.org/) at the Open Networking Foundation (ONF) community and the Open Compute Platform (OCP) SONiC Project (Open Compute Platform (OCP) SONiC Project).


Get up to speed quickly