QUICK START GUIDE

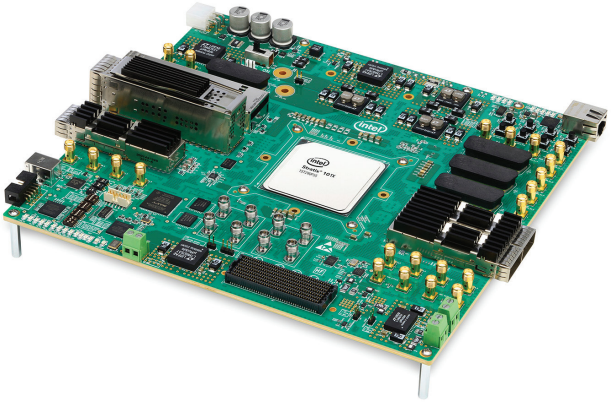
TRANSCEIVER SIGNAL INTEGRITY DEVELOPMENT KIT, INTEL® STRATIX® 10 TX EDITION

A Complete Development Platform for Prototyping

Introduction

Intel's Transceiver Signal Integrity Development Kit, Intel® Stratix® 10 TX Edition helps you thoroughly evaluate the signal integrity of Intel Stratix 10 TX FPGA transceivers. With this kit, you can:

- Evaluate transceiver performance up to 58 Gbps PAM4 and 30 Gbps NRZ
- Generate and check pseudo-random binary sequence (PRBS) patterns via an easy-to-use GUI
- Dynamically change differential output voltage (VOD), pre-emphasis, and equalization settings to optimize transceiver performance for your channel
- Perform jitter analysis
- Verify physical medium attachment (PMA) compliance to 10G/25G/50G/100G/200G/400G Ethernet and other major standards



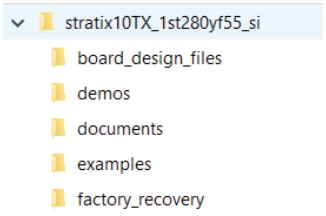
What's in the Box

- Intel Stratix 10 Transceiver Signal Integrity Development Board TX Edition
  - Intel Stratix 10 TX 1ST280EY2F55E1VG
  - Two full-duplex transceiver channels with 2.4 mm SMA connectors
  - 24 full-duplex transceiver channels to FMC+ connector
  - 16 full-duplex transceiver channels to both QSFP-DD 1x2 and QSFP-DD 2x1 optical interfaces
  - Sixteen full-duplex transceiver channels to two QSFP-DD 1x1 optical interface
  - Eight full-duplex transceiver channels to MXP 0 and MXP 1 high-density connectors
  - Ethernet PHY
- AC adapter power supply and 24-pin to 6-pin power adapter cable
- USB type A to B cable
- FMC+ loopback daughtercard
- Ethernet cable
- Printed documentation

You can download the kit installer directly from www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kits-s10-tx-si.html

Download the latest development kit software tools from www.intel.com and unzip the software package to anywhere on your computer.

Directory Structure



Using the Transceiver Signal Integrity Demonstration

The Transceiver Signal Integrity Demonstration consists of a Java-based GUI and an FPGA design. To run the demonstration follow these steps:

1. Connect the Intel FPGA Download Cable from your PC to the board.
2. If the Intel FPGA Download Cable driver is not installed on your PC, install the driver using the instructions in the user guide.
3. Connect 2.4 mm SMA cables from one or more channels on the board to an oscilloscope capable of displaying the data rates you wish to observe. Make sure SW5.1 is set to ON position and power up the board.
4. Launch the **BoardTestSystem.exe** file, located at **stratix10TX_1st280yf55_si\examples\board_test_system**. For optimal viewing, your screen resolution must be 1024x768 or greater.
5. Set PMA options in the Transceiver Channel Controls section.
6. Observe the resulting eye diagram on the oscilloscope and monitor the link statistics shown on the screen.

For information on bit error rate (BER) calculation, equalization settings, and other details regarding this demonstration, refer to the user guide. Visit the Transceiver Signal Integrity Development Kit page (www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kits-s10-tx-si.html) for the latest documentation and designs.

Related Links

- Transceiver Signal Integrity Development Kit homepage
  www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kits-s10-tx-si.html
- Transceiver Technology
  www.intel.com/content/www/us/en/architecture-and-technology/programmable/transceiver/overview.html
- Intel Stratix 10 FPGAs
  www.intel.com/content/www/us/en/products/programmable/fpga/stratix-10.html
- Board Design Resource Center
  www.intel.com/content/www/us/en/programmable/support/support-resources/support-centers/board-design-guidelines.html
- Software Download Center
  www.intel.com/content/www/us/en/programmable/downloads/download-center.html
- Technical Support Center
  www.intel.com/content/www/us/en/programmable/support/support-resources.html
- Development kits
  www.intel.com/content/www/us/en/programmable/products/boards_and_kits/all-development-kits.html
- Intel Forum
  forums.intel.com/s/
- Intel FPGA Wiki
  fpgawiki.intel.com/wiki/Main_Page

Electromagnetic interference caused by any modification made to the kit contents is the sole responsibility of the user. This equipment is designated for use only in an industrial research environment.
Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

CE

FCC NOTICE: This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under FCC Part 5 of CFR Title 47.

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