Assuring safety while saving time and resources

DO-254-certifiable IP cores

With safety at the top of your customers' airborne equipment requirements lists, Altera and our partners are making it easier for you to comply with industry operational-reliability standards. Our recently launched DO-254 Global Partner Network provides a comprehensive environment of DO-254-certifiable intellectual property (IP) cores, in-hardware verification flows, and documentation.

The DO-254 standard gives you design assurance and guidance from conception through initial certification, as well as through post-certification product improvements. With partners Aldec, Geensys, HighRely, and HCELL Engineering, we are committed to delivering specialty solutions and services that enable Altera® FPGA and HardCopy® ASIC solutions to be quickly approved and implemented in avionics and military applications. Our focus is on DO-254 levels A, B, C, and D compliance.

DO-254 design assurance levels

Level	Description	Affected area	Altera solution
A	Failure will cause or contribute to a catastrophic failure of the aircraft	Display unit, switch systems, airborne computing	HardCopy ASIC or FPGA with cyclic redundancy check (CRC) feature
B	Failure will cause or contribute to a hazardous/severe failure condition	Backup power, heads-up display	HardCopy ASIC or FPGA with CRC feature
C	Failure will cause or contribute to a major failure condition	Any	FPGA with or without CRC feature
D	Failure will cause or contribute to a minor failure condition	Any	FPGA with or without CRC feature
E	Failure will have no effect on the aircraft or on pilot workload	Any	FPGA with or without CRC feature

Lowering your risks, raising your design efficiency

Altera offers expertise to help with the DO-254 requirements and delivery process for your projects. We also participate in a DO-254 Users Group to discuss best practices, successful implementation results, difficulties, and other issues with aerospace companies.

Our Cyclone®, Stratix®, and Arria® FPGA families, along with our HardCopy ASICs, are equipped with features suited for military and airborne applications:

- Anti-tampering design security
- End-of-life protection
- Military temperature support
- Quality and reliability levels for rugged environments

The newest additions to our portfolio, the 40-nm Stratix IV FPGAs and HardCopy IV ASICs, also deliver the advantages of the market's smallest technology node. Both device families, available with and without transceivers, are manufactured on our longtime partner Taiwan Semiconductor Manufacturing Company's (TSMC's) 40-nm process. Together, we engaged in a rigorous multi-stage test chip program to ensure device performance and reliability.

Stratix IV FPGAs are based on a proven architecture utilized in previous-generation devices, delivering the highest density, highest performance, and the lowest power. The transceiver-based Stratix IV GX variant provides unprecedented system bandwidth and superior signal integrity, with up to 48 high-speed transceivers supporting data rates up to 8.5 Gbps. HardCopy IV ASICs offer the benefits of both FPGAs and ASICs, with an equivalent transceiver block and package- and pin-compatibility to Stratix IV FPGAs that supports a seamless prototype-to-production path.

Secure soft processor core

Our Nios® II embedded processor is the first DO-254 certified solution in the embedded processor space. To ensure safety of airborne equipment, HCELL Engineering offers the NIOS II_SC, a soft IP package providing a general-purpose RISC processor that can be reused in different airborne electronic hardware. Among its design assurance considerations:

- Architecture mitigation at the IP and user levels
- Monitoring of errors such as an invalid instruction's operation code, division by zero, and division overflow
- Single event upset (SEU) mitigation through SEU immunity of the NIOS II_SC embedded memory

Develop with the NIOS II_SC IP package using our Quartus® II design software, which includes tools that provide VHDL synthesis, as well as FPGA placement and routing, static timing analysis, and programming. With its fast compilation times and high logic utilization, Quartus II software can help you accelerate your design cycle.

Rounding out our portfolio, each partner in our network contributes to a low-risk and highly efficient design environment and validation process:

- Aldec and Mentor Graphics: test and verification of FPGA designs in the target Altera device
- Geensys (Europe) and HighRely (North America): consulting, documentation, and training
- HCELL Engineering: IP cores

Frequently asked questions

How can I get started with DO-254 certified solutions?

You can obtain certified training through HighRely, documentation for Nios II embedded processors from Altera, and a host of IP cores from various partners, outlined in the table below.

DO-254 certifiable IP cores

IP core and function	Provider
Nios II_SC 32-bit microprocessor	HCELL Engineering or Altera
Avalon® system interconnect	HCELL Engineering or Altera
UART, timer, compact flash	HCELL Engineering or Altera
Graphics IP	IMAGEM
Time-triggered protocol	TTTech
10/100 and 10/100/1000 Ethernet	MorethanIP
1553 bus controller/remote terminal	Arion
ARINC 429 bus controller	Arion
32-/66-MHz PCI	PLDA
PCI Express Gen1	PLDA

How does Altera certify its tools for DO-254 compliance?

Hardware and software tool assessment and qualification ensures that the tools are capable of performing a particular design or verification activity to an acceptable level of confidence. Tool performance is also independently assessed.

What kind of documentation does Altera provide for DO-254 certification?

Our recently announced DO-254 certifiable soft processor, NIOS II_SC, offers a high degree of available design documentation. Provided through our partner HCELL Engineering, the NIOS II_SC package was developed under DO-254 design assurance level A as well as safety guidelines outlined in Appendix B of the DO-254 certification. Documents with Plan for Hardware Aspect of Certification (PHAC), conceptual design data, validation and verification data, and traceability matrices are provided in the NIOS II_SC packages.

Want to dig deeper?

For more information about Altera's DO-254 compliant solutions, please contact your local Altera sales representative or FAE, or visit **www.altera.com/military**

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