Product Brief

Acceleration
FPGA

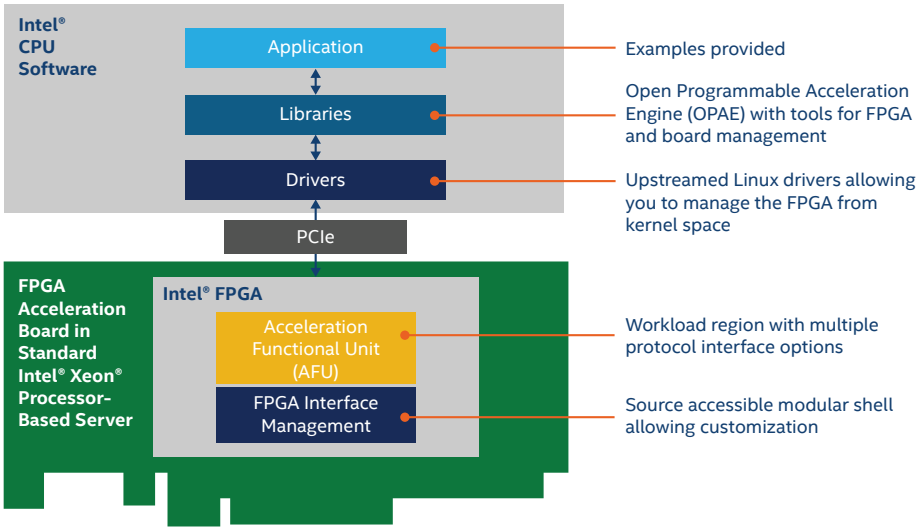
Intel® Open FPGA Stack

Leverage a Source-Accessible Framework to Ease Custom FPGA-based Acceleration Platform Development

Intel® Open FPGA Stack (Intel® OFS) Enables:

- Customization
- Faster Time to Deployment
- Portability
- Ease of Deployment
- Standardization
- Wide-Range of Solutions

Intel® OFS Block Diagram



Intel® Open FPGA Stack (Intel® OFS) is a scalable, source-accessible hardware and software infrastructure that addresses the challenges associated with designing FPGA-based acceleration platform solutions in Intel® Xeon® processor-based servers. Intel OFS eases custom board and workload development by providing a reference infrastructure and UVM verification environment with all the necessary components that you may choose to modify or leverage as-is.

Intel OFS enables software, hardware, and application developers to:

- **Use Standard Interfaces and Application Programming Interfaces (APIs)** to accelerate workload development and enable code reuse
- **Port existing workloads to the Acceleration Functional Unit (AFU) Region** and proliferate across Intel OFS-based platforms for FPGA-based acceleration or CPU offload
- **Utilize a growing ecosystem** of Intel OFS-enabled boards and workloads provided by Intel and third parties
- **Deploy Bare Metal, Virtualized, or Containerized** applications with data center class management for NFV, SmartNIC, VRAN, FSI, and more
- **Build Application Specific FPGA Interface Managers (FIMs)** from the provided reference FIMs using a modular, 'take and tailor' approach
- **Leverage Open-Sourced and Upstreamed Software Code** delivered via Git Repositories with native support from leading software vendors

Board Developers

Use the source-accessible, modular infrastructure to quickly create application specific FPGA Interface Mangers (FIMs) tailored to the differentiated needs of various boards and target workloads.

Software Developers

Leverage the OPAE software development kit, libraries, and APIs along with upstreamed, open-source kernel drivers that target the FIM and accelerate integration into common application frameworks.

Application Developers

Tap into a proven infrastructure and growing ecosystem to achieve greater return on investment and proliferation of workloads across a growing number of Intel® OFS-based platforms.

What's Inside

Hardware

Acceleration Functional Unit (AFU) Region

What it is: The AFU is the algorithm or processing unit that provides FPGA-based acceleration and/or CPU offload.

Why it's important: Workload performance is improved by offloading a computational operation for an application from the CPU to the FPGA's AFU region. The AFU region includes an optional Partial Reconfiguration (PR) region for dynamic configuration. Providing a designated area with specific insertion points for customization allows for cleaner, easier to manage RTL.

FPGA Interface Manager (FIM)

What it is: Reference FIMs provide platform management, functionality, clocks, resets, and standard interfaces to the host and AFU.

Why it's important: These easy-to-use reference FIMs are provided as working examples to help users develop their own custom platforms. They are designed to be modular and scalable, so customers can 'take and tailor' the design blocks relevant to their application.

Board Management Controller (BMC)

What it is: The BMC is responsible for controlling, monitoring, and granting access to board features.

Why it's important: The BMC provides root of trust and authentication to verify that bitstreams come from a trusted source. It interfaces to the server management controller using inudstry standard AXI protocols.

High Level Design (HLD) Shim

What it is: A collection of hardware and software components enabling HLD-based workload support.

Why it's important: HLD abstracts the FPGA hardware and design flow, enabling users to design FPGA custom hardware with familiar programming languages and development environments. HLD also provides extensible code that can be reused across architectures and vendors.

Software

Upstreamed, Open-Source Kernel Drivers

What it is: The Intel OFS kernel drivers are the first layer in the FPGA software stack.

Why it's important: This layer decomposes implemented functionality into sets of individual device features, providing a clean and extensible framework for the creation and integration of additional functionalities and their features. Kernel drivers are being upstreamed to the Linux kernel (kernel.org) to enable native support for Intel OFS by third-party open-source software vendors.

OPAE libraries and APIs

What it is: The OPAE C libraries are lightweight, user-space libraries that provide abstraction for FPGA resources in a compute environment.

Why it's important: This library abstracts hardware and OS specific details, exposing the underlying FPGA resources as a set of features accessible from within software running on the host. The unified C API supports different FPGA integration and deployment models to enable portability across OS's and bare metal, hypervisor, or containerized use models.

OPAE Tools

What it is: OPAE installs tools to expedite development.

Why it's important: These tools provide useful functions such as: displaying FPGA information, implementing a secure firmware update, enabling virtualization, downloading new images to the board, and more.

UVM Test Framework

What it is: The Universal Verification Method (UVM) test framework provides a verification environment for the FIM and AFU.

Why it's important: UVM delivers a modular, reusable, and scalable testbench structure by providing an API framework and unit test cases that can be deployed across multiple projects.

Open-Source Methodology

All Intel OFS hardware and software code has been developed using an open source development methodology, resulting in code organized and delivered through git repositories. We refer to our model as being source-accessible since users are granted access to source code in the git repositories. Technical documentation is co-located with the code itself.

Intel will soon allow contributions back from users who wish to share with the Intel OFS community. This will enable the Intel OFS infrastructure to grow and be enriched more quickly.

Intel FPGA-Based Acceleration Platforms

Intel FPGA-based Infrastructure Processing Units (IPUs) and Programmable Acceleration Cards (PACs) are production-qualified, acceleration hardware solutions designed for telecommunications, cloud services, and other data center environments. Similarly, Intel Acceleration Development Platforms (ADPs) are reference platforms that include all major solution ingredients needed for initial evaluation before porting to a production platform. The Intel FPGA PAC D5005, Silicom FPGA SmartNIC N5010 Series, and Intel N6000 ADP are the first Intel-OFS enabled platforms using the Intel® Stratix® 10 FPGA and Intel® Agilex™ FPGA, with more Intel OFS-enabled platforms to come from our ecosystem partners.

Intel OFS code is developed and validated using the Intel FPGA PAC D5005 and the Intel N6000 ADP as hardware reference platforms for the Intel OFS Intel Stratix 10 and Intel Agilex FPGA code lines. Users are encouraged to leverage the Intel Stratix 10 or Intel Agilex FPGA reference platform with the Intel OFS hardware and software code for initial code bring-up, before modifying and porting to custom hardware. Alternatively, the N6000 ADP full design, including board files and the Intel OFS implementation, can also be licensed. Reference platforms can be leveraged for design of an Intel-FPGA based, third party, or custom platform.

Get Started

- Learn more about Intel Open FPGA Stack
- Learn more about the N6000 Acceleration Development Platform
- Learn more about the Silicom FPGA SmartNIC N5010 Series
- Visit the Open-Source Intel OFS Software GitHub
- See Intel FPGA-Based Acceleration Cards Enabled with Intel OFS

ss-1125-1.2