INTEL® USER-CUSTOMIZABLE SoC FPGAs

DESIGN THE WAY YOU WANT

What if you could select the intellectual property (IP) and peripherals you need to quickly create a custom system on a chip (SoC) tailored to accelerate your application?

What if you could consolidate two or more discrete devices into one, reducing system power, cost, and board size while increasing performance?

What if you could use this chip to differentiate your end product in both hardware and software?

Now you can design that custom device with Intel® SoC FPGAs. SoC FPGAs combine a processor, peripherals and FPGA into a single, user-customizable device. The Intel SoC FPGA portfolio includes SoC versions of our popular 28 nm Cyclone® V and Intel Arria® FPGA families. Based on 20 nm process technology, the Arria 10 SoC offers a performance upgrade for Arria V SoC users and adds enhanced security features. The Intel Stratix® 10 SoC offers users the ultimate in performance with a quad-core ARM* Cortex*-A53 processor built on Intel's leading edge 14 nm Tri-Gate (FinFET) silicon process technology. Regardless which one you choose, Intel SoC FPGAs help you keep up with changing market requirements and interface standards. We include a wide range of system peripherals, Intel FPGA IP, custom IP, and third-party IP that lets you quickly create a custom system using Intel design tools. For your software development needs, Intel and our partners provide comprehensive tools, operating systems, and middleware.

WHAT IS AN INTEL SoC FPGA?

Our SoCs integrate an ARM-based hard processor system (HPS) consisting of a multi-core ARM processor, peripherals, and memory controllers with the FPGA fabric using a high-bandwidth interconnect backbone.

The Intel SoC FPGA is ideal for:

- Accelerating key, application-specific workloads and performing system management tasks to complement the host processor in midrange and high-end systems
- Reducing system power, cost, and board space by integrating multiple chips – processor, DSP, and FPGA – into one
- Improving system performance via high-throughput data paths between the HPS and the FPGA
- Differentiating your end product by customizing in both hardware and software
- Enhancing system reliability with built-in error correction code (ECC) and memory protection that protect your system against potential hardware or software errors
- Developing ARM-compatible software with unmatched target visibility, control, and productivity using Intel's unique FPGA-adaptive debugging
- Improving system performance and power efficiency by implementing complex software algorithms in FPGA logic

WHY DESIGN WITH INTEL SoC FPGAs?

You know that building a product with a strong architecture is the key to ensuring that the final design meets your requirements. With Intel SoC FPGAs, you are already starting with a solid foundation that provides:

Increased System Performance

Our SoCs combine the performance and broad embedded software ecosystem of a ARM multi-core applications processor with the flexibility of Intel's FPGA fabric. Tight integration between the processor and FPGA provides system interconnect performance not possible in two-chip solutions: higher bandwidth interconnect with a more than 125 Gbps (in the Arria V SoC) processor (HPS)-to-FPGA peak bandwidth interface and a high-bandwidth FPGA-to-SDRAM interface. In higher-end applications, the Arria 10 SoC or Stratix 10 SoC can be used to offload the host processor by accelerating application-specific workloads or performing board management tasks. Hardware acceleration with coherent memory access to all system with customized accelerators masters in the FPGA and HPS accelerates critical sections of your code while keeping memory coherent.

Improved Reliability

We built in a variety of features to protect your system against potential hardware or software errors.

- ECC circuitry to make your system more robust and resilient against unexpected data errors or corrupted data
- CPU warm and cold reset initiates without affecting or reprogramming FPGA
- Shared DDR memory controller with an integrated protection unit keeps masters from accessing other memory regions

Increased Flexibility

Why should your design be constrained by your architecture? With our SoCs, you get the ability to optimize your design the way you want.

- Enables you to customize in both hardware and software
- Offers a variety of methods to boot the processor and configure the FPGA for more system design choices
- Dedicated hardened memory controllers in both the processor system and FPGA portion of the device save FPGA resources and guarantee timing closure
- Flexible product portfolio enables easy device migration (vertical and horizontal) with high-speed transceivers in all device densities

Lower System Cost

To help you lower your system cost, we have designed our SoCs so you can reduce design time and bill of materials (BOM) compared to multichip solutions.

- Integrates two or more chips into one (processor, DSP, FPGA) with a single-core processor option available
- Integrated PCI Express* (PCIe*) support runs across all device families
- Cyclone V and Arria V SoCs require no power-off sequencing, eliminating the need for external circuitry.
- Ability to update the FPGA hardware design in the field to track changes in industry standards, customer requirements or add differentiating product features.

FPGA-Adaptive Debugging

The ARM Development Studio 5 (DS-5*) Intel SoC FPGA Edition dynamically adapts your custom configurations of the FPGA within the SoC to seamlessly extend embedded debugging capabilities across the CPU-FPGA boundary. The toolkit delivers an unprecedented level of debugging visibility and control that leads to substantial productivity gains.

- On-silicon debugging infrastructure combines with industry-standard ARM DS-5 tool to offer the best from both worlds—intuitive, easy-to-use debugging interface, and Intel-unique FPGA-adaptive debugging capabilities
- True multicore debugging capabilities, whole-chip visibility and control, and automatic FPGA register view
- Premium JTAG-based debugging capabilities including cross triggering, trace, and correlation of CPU and FPGA events
- gdbserver compatibility enables Linux* application debugging

SoCs: All in

Whatever direction you take your future designs, we'll be there to help. Our SoC portfolio and roadmap spans our high-end, midrange and low-cost product lines, built on leading-edge process technologies from TSMC (28 nm and 20 nm) and Intel (14 nm Tri-Gate). We offer forward migration of software for future devices to protect your software investment. Our average product cycle is 15 years, with many of our products having lifetimes in excess of 20 years, so you can design in our products with confidence.

SoC FPGAs are Smart FPGAs

Intel SoC FPGAs combine the world class capabilities of Intel FPGAs and the integrated intelligence of ARM processors to provide on-chip system management, connectivity control, and FPGA acceleration administration. When utilizing the processors within the SoC FPGA many OAM functions are possible including system performance monitoring, reporting and logging, data flow management, and fault detection. Intel SoC FPGAs also provide the connectivity control and access allowing users to update FPGA configuration and debug the FPGA from a remote location, providing critical access to the device even after being deployed in the field and otherwise inaccessible. In addition, the processors within the SoC FPGA can be deployed to efficiently manage acceleration and DSP algorithms in the FPGA fabric. By integrating standard ARM processors, SoC FPGAs mark the next step in the evolution of FPGAs by making FPGAs smart and provide capabilities that previously were not possible with standard FPGAs.

MAJOR ELEMENTS OF AN INTEL SoC FPGA

ARM-Based Hard Processor System

The HPS consists of a multi-core ARM Cortex MPCore* applications processor, a rich set of peripherals, and a multiport memory controller shared with logic in the FPGA. The HPS gives you the flexibility of programmable logic combined with the performance and cost savings of hard IP.

- Embedded peripherals eliminate the need to implement these functions in programmable logic, leaving more FPGA resources for application-specific custom logic and reducing power consumption
- The hard multiport SDRAM memory controller, shared by the processor and FPGA logic, supports DDR2, DDR3, DDR4, LPDDR2, LPDDR3, RLDRAM 3, and QDR II+ SDRAM devices with an integrated ECC support for high reliability and safety-critical applications.

High-Speed Interconnect

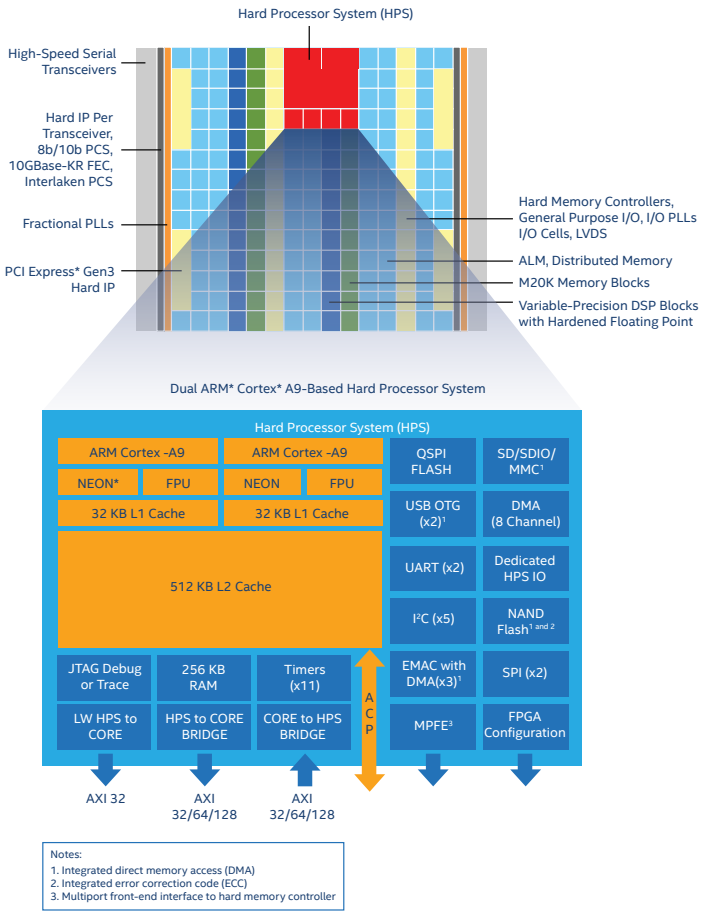
High-throughput data paths between the HPS and FPGA fabric provide a level of interconnect performance that is not possible in two-chip solutions. The tight integration between the HPS and FPGA fabric provides over 125 Gbps peak bandwidth in the Arria V SoC for example with integrated data coherency between the processor and the FPGA.

Flexible FPGA Fabric

The flexibility offered by the FPGA logic fabric, with up to 5.5 million logic elements (MLE) in the Stratix 10 SoC, lets you differentiate your system by implementing custom IP or off-the-shelf preconfigured IP from Intel or its partners into your designs. This allows you to:

- Adapt quickly to varying or changing interface and protocol standards
- Add custom hardware in the FPGA to accelerate time-critical algorithms and create a compelling competitive edge
- Reduce power consumption and FPGA resource requirements by leveraging hard logic functions within the FPGA, including PCIe ports and additional multiport memory controllers

Figure 1 Arria 10 SoC Block Diagram



INDUSTRY-LEADING LINUX SUPPORT

Intel keeps up with the Linux community by upgrading to the latest stable kernel on kernel.org. Additionally, Intel supports a modern release strategy by updating access to public Git trees every two weeks on www.rocketboards.org.

Upstreaming

Intel's approach to Linux for SoC FPGAs is centered on upstreaming fixes and improvements of the SoC FPGA code, primarily to kernel.org and DENX.de. Consequently, Intel assembled a Linux team with upstreaming as a key strategy.

Delivery

In addition to providing the latest stable kernel for the SoC FPGA architecture, Intel also supports U-Boot, LTSI kernel with and without PREEMPT_RT, and a Yocto Project layer (meta-Altera). This code runs (and was tested on) the Yocto-compatible, Angstrom distribution. You can access the code via the github repositories repositories via RocketBoards.org, which is a "one-stop-shop" for Linux developers working on Intel SoC FPGAs.

Rocketboards.org repositories include: latest stable kernel, LTSI kernel, LTSI kernel with PREEMPT_RT, U-Boot, Meta-Altera layer for Angstrom Distribution and many design examples.

With RocketBoards.org, accelerate development by exchanging ideas with the Linux community, discover the right resources for your embedded solutions, get your questions answered, show off your latest SoC FPGA projects , start your own wiki page, and edit an existing wiki page.

Unified Extensible Firmware Interface (UEFI) source code for the Arria 10 SoC FPGA is available via github at: https://github.com/altera-opensource/uefi-socfpga

Ongoing Innovation

Intel contributes to the Linux kernel, kernel.org. Specifically, Intel SoC FPGA innovates by augmenting the Linux kernel with new features, such as an FPGA manager framework for programming and reconfiguring the FPGA. Furthermore, Intel is enhancing the kernel to better handle memory map reconfiguration via dynamic device trees.

INDUSTRY-LEADING ECOSYSTEM SUPPORT

Commercial Operating Systems

In addition to open-source Linux, there are over 20 commercial operating systems available for the Intel SoC FPGAs including Wind River VxWorks, Green Hills Software Integrity RTOS and Micrium µC/OS- II and µC/OS-III. For the latest list of Intel SoC FPGA operating system support for Cyclone V and Arria V SoC, visit www.altera.com/products/soc/ecosystem.html. For Arria 10 SoC, visit www.altera.com/products/soc/portfolio/arria-10-soc/ecosystem.html#squares-box-1.

Broad Ecosystem

To help get your design to market quickly and reliably, Intel SoC FPGAs are surrounded and supported by a broad ecosystem provided by industry experts. For more information on development tools, IP cores, Nios II soft processor, design services, standalone boards, development kits, and System on Modules (SoMs) for Intel SoC FPGAs. For Cyclone V and Arria V SoCs, visit www.altera.com/products/soc/ecosystem.html. For Arria 10 SoCs, visit www.altera.com/products/soc/portfolio/arria-10-soc/ecosystem.html#squares-box-2.

SoC FPGAs: A FULL RANGE PRODUCT PORTFOLIO

Intel offers a full-range SoC FPGA product portfolio spanning high-end, midrange, and low-end applications.

SoC FPGAs for All Your Needs

Stratix 10 SoCs offer breakthrough advantages in bandwidth and system integration, including a next-generation hard processor system (HPS). Stratix 10 devices feature the revolutionary HyperFlex™ architecture and are manufactured on the Intel 14 nm Tri-Gate process, delivering breakthrough levels of performance and power efficiencies that were previously unimaginable. When coupled with 64 bit quad-core ARM Cortex-A53 processor and advanced heterogeneous development and debug tools such as the Intel FPGA SDK for OpenCL™[1] and Intel SoC FPGA Embedded Design Suite (EDS), Stratix 10 devices offer the industry's most versatile single-chip heterogeneous computing platform.

Arria 10 SoCs deliver optimal performance, power efficiency, small form factor, and low cost for midrange applications. The Arria 10 SoCs, based on TSMC's 20 nm process technology, combine a dual-core ARM Cortex-A9 HPS with industry-leading programmable logic technology that includes hardened floating-point digital signal processing (DSP) blocks. By building on the architecture of the dual-core ARM Cortex-A9 processor from the Arria V SoC, the Arria 10 SoC offers an easy performance upgrade and software migration path for Arria V and Cyclone V SoC designs. The architectural innovation in the implementation of IEEE 754 single-precision hardened floating-point DSP blocks in Arria 10 SoCs enables processing rates up to 1.5 TFLOPs (tera floating-point operations per second) and power efficiency up to 40 GFLOPs/Watt†.

Arria V SoCs balance cost and power with performance for midrange applications, such as remote radio heads, LTE base stations, and multifunction printers. You get high system performance due to a fast FPGA fabric, fast I/Os, and fast transceiver data rates. The DSP-rich Arria V FPGA fabric delivers up to 1,600 GMACS and 300 GFLOPS performance† while helping you meet your cost and power requirements for applications in this space.

The Arria V SoC family comes in two tailored options:

- Arria V SX SoC with ARM-based HPS and 6.5536 Gbps transceivers
- Arria V ST SoC with ARM-based HPS and up to 10.3125 Gbps transceivers

Cyclone V SoCs provide the industry's lowest system cost and power†, along with performance levels that make the device family ideal for differentiating your high-volume applications. You get up to 40 percent lower total power versus the previous generation FPGAs†, efficient logic integration capabilities, and integrated transceiver options. You also get up to 150 GMACS and 100 GFLOPS DSP performance with our variable-precision DSP blocks. Cyclone V SoCs offer a single- or dual-core Cortex-A9 processor, depending on your performance needs.

The Cyclone V SoC family comes in three tailored options:

- Cyclone V SE SoC with ARM-based HPS
- Cyclone V SX SoC with ARM-based HPS and 3.125 Gbps transceivers
- Cyclone V ST SoC with ARM-based HPS and 6.144 Gbps transceivers

Note 1: OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission by Khronos.

WHERE YOU CAN USE INTEL SoC FPGAs

We understand the requirements of end market solutions that drive silicon and IP development. That's why we optimized our SoCs for real-world applications. Example applications ideally suited for Stratix 10, Arria 10, Cyclone V, and Arria V SoCs:

Typical Applications for SoC FPGAs by Device

			Cyclone V SoC				Arria V SoC		Arria 10 SoC							Stratix 10 SoC										
Industry	**Target Applications**	**Key Functions**	**25**	**40**	**85**	**110**	**350**	**470**	**160**	**220**	**270**	**320**	**480**	**570**	**660**	**500**	**650**	**850**	**1100**	**1650**	**2100**	**2500**	**2800**	**4500**	**5500**
Factory Automation	Industrial I/O	Sensor interfaces, safety	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Industrial networking	Industrial communication/network protocol bridging, safety	●	●	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Programmable logic controllers (PLCs)/ human machine interface (HMI), drives, servos	Control loop, energy efficient inverter, communication protocols, I/O, safety	●	●	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Smart Energy	Renewable energy, transmission and distribution, secure communication	Inverter, power management, protection relays, communication standards, security, and safety	●	●	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Video Surveillance	IP camera	WDR, HD video, advanced video analytics	–	–	●	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Automotive	Advanced driver assistance, infotainment	Video processing, video analytics, communication	●	●	●	●	–	–	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Consumer	Portable devices, professional gaming machines, signage and display walls, drones, VR/AR	Video processing, video analytics, codec, vision processing, system management and controls, security	●	●	●	●	–	–	●	●	–	–	–	–	–	●	●	–	–	–	–	–	–	–	–
Wireless Infrastructure	• Remote radio unit, standalone unit	Signal processing and digital front end (filtering, etc), modem and ethernet switch and OAM	–	–	–	●	●	●	●	●	●	●	●	●	●	●	●	●	●	–	–	–	–	–	–
	• Remote radio unit ASIC coprocessor		–	–	–	–	–	–	●	●	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–
	• LTE mobile backhaul		–	–	–	–	–	–	●	●	●	●	●	–	–	•	–	–	–	–	–	–	–	–	–
Wireline Communications	Router, access, edge equipment	Routing protocols, link management, OAM	–	–	–	●	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Broadcast	Studio, video conferencing, professional audio/visual (A/V)	Codec, video over IP, edge QAM, PCIe capture	–	–	–	●	●	●	●	●	●	●	●	●	●	●	●	●	●	–	–	–	–	–	–
Defense and Aerospace	Night vision, secure communications	Vision and waveform processing	–	–	–	–	●	●	●	●	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–
	Intelligence, cybersecurity	High-performance computing	–	–	–	–	–	–	–	–	–	–	●	●	●	●	●	●	●	●	●	●	●	–	–
Medical	Diagnostic imaging, instrumentation	Ultrasound imaging, signal processing	–	–	–	●	●	●	●	●	●	●	●	●	●	●	●	●	●	–	–	–	–	–	–
Compute and Storage	Multifunction printer, chassis management	Image processing pipeline	●	●	●	●	–	–	●	●	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Data Center and Flash Storage	Server acceleration, server connectivity, flash cache	• Server acceleration – accelerate search / sort, encryption / decryption, compression / decompression, filtering, special algorithms like CNN • Server connectivity – 25G connectivity, cluster networking • Flash cache – storage controller for NAND memory expansion	–	–	–	–	●	●	–	–	–	–	●	●	●	●	●	●	●	●	●	●	●	●	–
ASIC Prototyping	Off-the-shelf solution for protoyping ASIC and ASSP designs	Verification of both register transfer level (RTL) design and initial software development	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	●	●	●	●	●	●	●	●

Notes:

● Well suited for application

– May or may not be suited for application

SoC FPGA PORTFOLIO OVERVIEW

Family	HPS Max. Freq.	KLE	Block Memory Bits (Mb)	Var. Prec. Multiplier Blocks	Max. FPGA User I/Os	HPS Dedicated I/Os	Max. Transceivers (GP)	Per-Transceiver Max. Data Rate (Gbps)	SoC Hard Memory Controller	FPGA Hard Memory Controllers	Hard PCIe
Cyclone V SoC	925 MHz	25	1.4	36	145	181	6	3	1	1	2 ea, Gen1
		40	2.7	58	145	181	6	3	1	1	2 ea, Gen1
		85	4.0	87	288	181	9	6.144	1	1	2 ea, Gen2
		110	5.6	112	288	181	9	6.144	1	1	2 ea, Gen2
Arria V SoC	1.05 GHz	350	17.3	809	528	208	30 / 16	6 / 10	1	3	2 ea, Gen2
		460	22.8	1,068	528	208	30 / 16	6 / 10	1	3	2 ea, Gen2
Arria 10 SoC	1.50 GHz	160	9	156	288	17	12	17.4	1	4	1 ea, Gen3
		220	11	191	288	17	12	17.4	1	4	1 ea, Gen3
		270	15	830	384	17	24	17.4	1	4	2 ea, Gen3
		320	17	985	384	17	24	17.4	1	4	2 ea, Gen3
		480	28	1,368	492	17	36	17.4	1	4	2 ea, Gen3
		570	35	1,523	588	17	48	17.4	1	4	2 ea, Gen3
		660	42	1,688	588	17	48	17.4	1	4	2 ea, Gen3
Stratix 10 SoC	1.50 GHz	500	43	1,152	488	48	24	28	1	10	1 ea, Gen3
		650	50	1,440	488	48	24	28	1	10	1 ea, Gen3
		850	68	2,016	736	48	48	28	1	14	2 ea, Gen3
		1,100	86	2,520	736	48	48	28	1	14	2 ea, Gen3
		1,650	114	3,145	704	48	96	28	1	14	4 ea, Gen3
		2,100	127	3,744	704	48	96	28	1	14	4 ea, Gen3
		2,500	195	5,011	1,160	48	144	28	1	24	6 ea, Gen3
		2,800	229	5,760	1,160	48	144	28	1	24	6 ea, Gen3
		4,500	137	1,980	1,640	48	72	28	1	34	3 ea, Gen3
		5,500	137	1,980	1,640	48	72	28	1	34	3 ea, Gen3

Cyclone V and Arria V SoC Packages

		Non-Transceiver Devices (FPGA User I/Os)			Transceiver Devices (FPGA User I/Os, Transceivers)				
Family	KLE	U484-WB 19x19 mm	U672-WB 23x23 mm	F896-WB 31x31 mm	U672-WB 23x23 mm (I/O, 3G/5G)	F896-WB 31x31 mm (I/O, 3G/5G)	F896-FC 31x31 mm (I/O, 6G, 10G)	F1152-FC 35x35 mm (I/O, 6G, 10G)	F1517-FC 40x40 mm (I/O, 6G, 10G)
Cyclone V SoC	25	66	145	–	145, 6	–	–	–	–
	40	66	145	–	145, 6	–	–	–	–
	85	66	145	288	145, 6	288, 9	–	–	–
	110	66	145	288	145, 6	288, 9	–	–	–
Arria V SoC	350	–	–	–	–	–	170, 12, 4	350, 18, 8	528, 30, 16
	460	–	–	–	–	–	170, 12, 4	350, 18, 8	528, 30, 16
HPS I/O		161	181	181	181	181	208	208	208

Arria 10 SoC Small Form Factor Packages

Device	U19 (U484) (19x19 mm)	F27 (F672) (27x27 mm)	F29 (F780) (29x29 mm)
	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR
10AS016	192, 48, 72, 6	240, 48, 96, 12	288, 48, 120, 12
10AS022	192, 48, 72, 6	240, 48, 96, 12	288, 48, 120, 12
10AS027	–	240, 48, 96, 12	360, 48, 156, 12
10AS032	–	240, 48, 96, 12	360, 48, 156 , 12
10AS048	–	–	360, 48, 156, 12

192, 48, 72, 6 Numbers indicate general purpose I/O (GPIO) count, high-voltage I/O count, LVDS pairs, and transceiver count.

Arria 10 SoC I/O and Transceiver (XCVR)-Optimized Packages

Device	F34 (35x35 mm²) (H = 24 XCVRs)	F35 (35x35 mm²) (K = 36 XCVRs)	F40 (40x40 mm²) (N = 48 XCVRs)	F40 (40x40 mm²) (K = 36 XCVRs)
	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR
10AS027	384, 48, 168, 24	384, 48, 168, 24	–	–
10AS032	384, 48, 168, 24	384, 48, 168, 24	–	–
10AS048	492, 48, 222, 24	396, 48, 174, 36	–	–
10AS057	492, 48, 222, 24	396, 48, 174, 36	588, 48, 270, 48	648, 96, 324, 36
10AS066	492, 48, 222, 24	396, 48, 174, 36	588, 48, 270, 48	648, 96, 324, 36

384,48,168,24 Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Stratix 10 SoC Packages

Device	F1152 (35x35 mm)	F1760 (42.5x42.5 mm)	F2112 (47.5x47.5 mm)	F2112 (47.5x47.5 mm)	F2112 (47.5x47.5 mm)	F2112 (47.5x47.5 mm)	F2397 (50x50 mm)	F2397 (50x50 mm)	F2397 (52.5x52.5 mm)	F2912 (55x55 mm)
	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR	GPIO, 3 V I/O, LVDS, XCVR
10SX050	344, 8, 172, 24	488, 8, 240, 24	–	–	–	–	–	–	–	–
10SX065	344, 8, 172, 24	488, 8, 240, 24	–	–	–	–	–	–	–	–
10SX085	–	688, 16, 336, 48	736, 16, 360, 48	–	–	–	–	–	–	–
10SX110	–	688, 16, 336, 48	736, 16, 360, 48h	–	–	–	–	–	–	–
10SX165	–	688, 16, 336, 48	–	648, 24, 312, 72	464, 32, 216, 96	–	–	704, 32, 336, 96	–	–
10SX210	–	688, 16, 336, 48	–	648, 24, 312, 72	464, 32, 216, 96	–	–	704, 32, 336, 96	–	–
10SX250	–	688, 16, 336, 48	–	648, 24, 312, 72	–	–	1160, 8, 576, 16	704, 32, 336, 96	432, 48, 216, 144	–
10SX280	–	688, 16, 336, 48	–	648, 24, 312, 72	–	–	1160, 8, 576, 16	704, 32, 336, 96	432, 48, 216, 144	–
10SX450	–	–	–	–	–	648, 24, 312, 72	1256, 8, 624, 16	–	–	1640, 8, 816, 16
10SX550	–	–	–	–	–	648, 24, 312, 72	1256, 8, 624, 16	–	–	1640, 8, 816, 16

344,8,172,24 Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

SoC DEVELOPMENT KITS AND BOARDS

Intel SoC FPGAs are supported by a full range of development kits available from Intel and our ecosystem partners.

Cyclone V SoC Development Kit

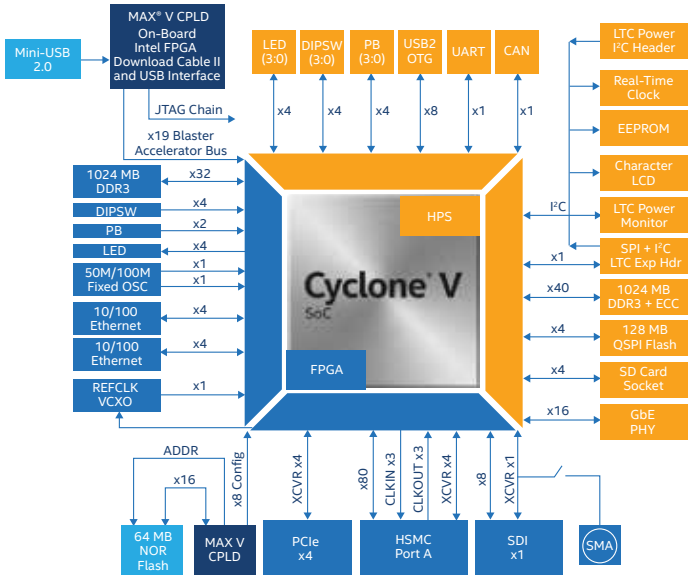
The Cyclone V SoC Development Kit offers a development platform to rapidly create custom ARM processor-based SoC designs. The kit includes a Cyclone V SoC development board and the Intel SoC FPGA EDS featuring the ARM DS-5 for Intel SoC FPGAs.

The development board includes the following features and interfaces:

- Cyclone V SX SoC - 925 MHz, 110K LE
- 2 GB DDR3 SDRAM (1 GB processor and 1 GB FPGA)
- Ethernet, USB 2.0 On-The-Go (OTG), CAN, I2C, and UART interfaces
- Integrated Intel FPGA Download Cable II circuitry
- PCIe (rootport and endpoint support)
- Power supply and all cables
- Boots Linux on power up
- Expansion header (HSMC)[1]
- ARM DS-5 Intel SoC FPGA Edition Toolkit with 1-year maintenance

Note 1: Application-specific daughtercards, available separately, support a wide range of I/O and interface standards.

Board Block Diagram



For more details on the Cyclone V SoC Development Kit, visit www.altera.com/products/boards_and_kits/dev-kits/altera/kit-cyclone-v-soc.html or contact your local Intel sales representative.

Ecosystem Development Kits, Boards and SOMs

For a list of the latest Development Kits, Boards and System on Modules (SOMs) available from our ecosystem partners, visit www.altera.com/products/soc/ecosystem.html or contact your local Intel sales representative.

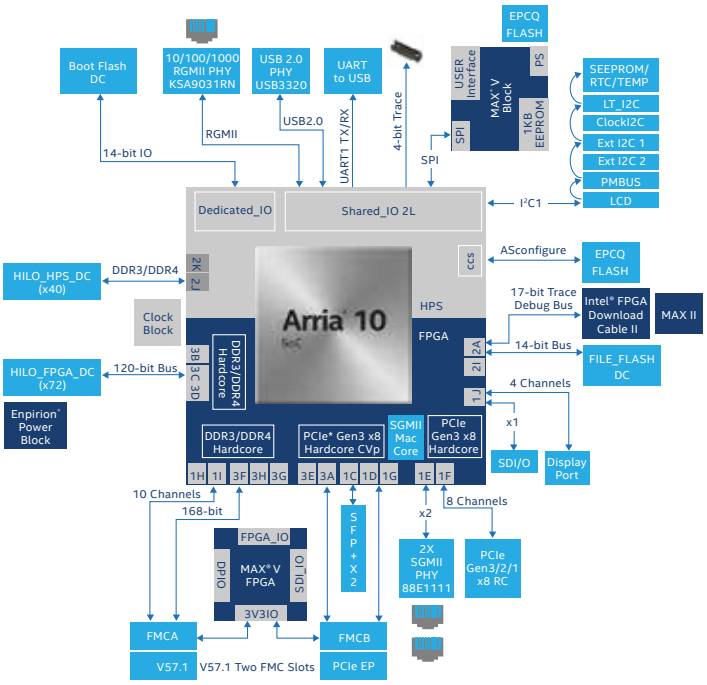
Arria 10 SoC Development Kit

The Intel Arria 10 SoC Development Kit offers a quick and simple approach for developing custom ARM processor-based SoC designs. Design productivity is one of the driving philosophies of the Arria 10 SoC architecture. The Arria 10 SoCs offers full software compatibility with previous generation SoCs, a broad ecosystem of ARM software and tools, and the enhanced FPGA and DSP hardware design flow.

The development board includes the following features and interfaces:

- Arria 10 SX SoC - 1.0 GHz, 660K LE
- Embedded Intel FPGA Download Cable II II for hard processor system (HPS) or FPGA programming
- PCIe Gen3 x8, Dual FPGA mezzanine card (FMC) expansion headers
- Two 10/100/1000 SGMII Ethernet ports and one 10/100/1000 RGMII Ethernet port
- Two 10GbE small form factor pluggable (SFP) cages
- 1 FMC loopback card
- USB On-The-Go (USB OTG) port
- 1GB DDR4 HPS HILO memory card
- NAND, QSPI, and SD/MICRO boot flash cards
- 1GB DDR4 HILO memory card
- Display port and SDI port
- Quartus® Prime Pro software with 1-year license
- ARM DS-5 Intel SoC FPGA Edition Toolkit with 1-year maintenance

Board Block Diagram



For more details on the Arria 10 SoC Development Kit visit www.altera.com/products/boards_and_kits/dev-kits/altera/arria-10-soc-development-kit.html or contact your local Intel sales representative

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COMMON DEVELOPMENT TOOLS MAKE DESIGN EASIER

Intel® Quartus® Prime

Design Software

Intel® Qsys

System Integration Tool

Software Tools

A set of common software tools and design resources equips you to swiftly turn your concepts into revenue-generating applications. Our SoC FPGAs inherit the rich software development ecosystem available for ARM Cortex-A9 and Cortex-A53 MPCore processors, including software development tools, operating systems, and middleware. This ecosystem compatibility ensures you can stay productive with familiar tools and reuse legacy software to shorten the development cycle.

You can follow the same software development process for our SoC FPGAs that you do with other embedded processors. Intel and its ecosystem partners provide tool choices for each step of the process, from board bring-up to building Linux kernels to debugging application software.

We provide comprehensive operating system (OS) support including Linux, Wind River VxWorks, and more. Using our reference Linux kernel or board support packages for other operating systems, you can immediately start OS-based application development.

For development tools, you can use the Intel SoC FPGA EDS for hardware-to-software handoff, Linux development, bare metal usage, and FPGA-adaptive debugging.

Hardware Tools

Our productivity-enhancing Quartus Prime software development environment, featuring the Qsys system integration tool, makes development easier for hardware designers. Qsys saves you time and effort in the FPGA design process, simplifying development of complex hardware systems.

Faster Development

- Easy-to-use GUI interface enables quick integration of IP functions and subsystems
- Automatic generation of interconnect logic and automatic HDL generation of your system
- Hierarchical design flow enables scalable designs, supports team-based design, and maximizes design reuse
- Support for a wide range of IP interface standards including ARM AMBA*/AXI*, Avalon® Memory-Mapped, and Avalon Streaming interfaces
- Automatic generation of a simulation model, software header file, and data sheet to expedite development across hardware and software teams

Faster Timing Closure

- High-performance Qsys interconnect based on the network-on-a chip (NoC) architecture
- User control of pipelining to meet f_{MAX} and latency system requirements

Faster Verification

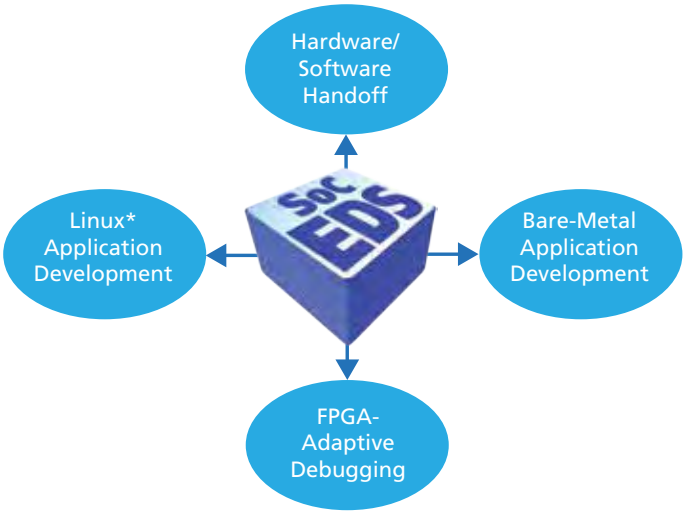
- Automatic testbench generation and verification IP suite let you start your simulation faster
- Ability to bring your board up faster by sending read and write transactions into a live system for debug

JUMP START SOFTWARE DEVELOPMENT

In any embedded system development project, software design typically takes up the bulk of time and resources. With the Intel SoC FPGA EDS, you get all the tools you need to work more productively, improve your software quality, and ultimately get to market faster.

The SoC EDS is a comprehensive tool suite for embedded software development on Intel SoC FPGAs. It contains development tools, utility programs, run-time software, and application examples to jump start firmware and application software development.

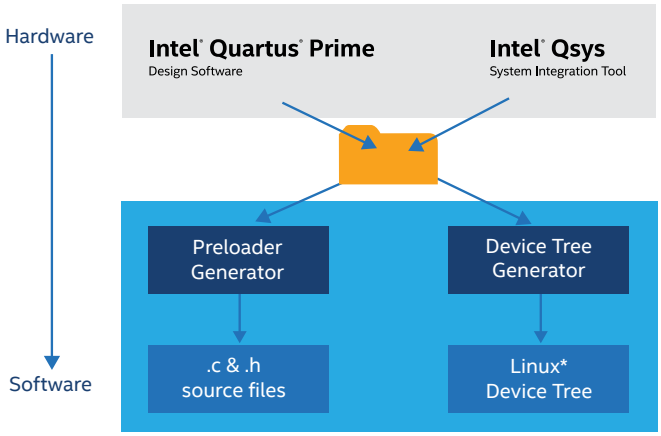
Intel SoC FPGA Embedded Design Suite



Hardware-to-Software Handoff

As part of the SoC EDS, the hardware-to-software handoff utilities allow FPGA and software design teams to work independently and follow their familiar design flows. These utilities take the Intel Quartus Prime software and Qsys output files and generate handoff files for the software design flow. As software engineers steer clear of FPGA development, they can focus on software design and be more productive.

Hardware-to-Software Handoff Utility Tools



Linux Application Development

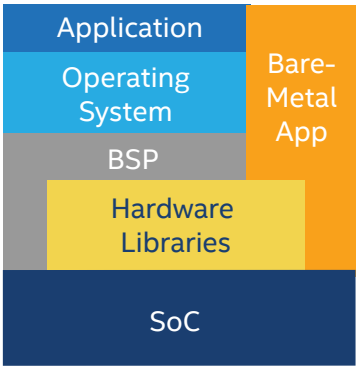
Intel contributes to the Linux community to enable our SoC FPGA customers via the community portal RocketBoards.org. We provide a kernel, U-boot, and a meta-Altera layer for Angstrom and the Yocto Project. Intel contributes to the open source community to enable the Linux kernel to run on its SoC FPGA architectures. Contributions include improvements to the general kernel as well as new SoC FPGA specific functions, such as the FPGA manager framework. By nature, these improvements benefit everyone in the Linux community.

Bare Metal Development

The SoC EDS' SoC hardware libraries support bare metal usage such as board bring-up support, device driver development, and optimized hardware access.

The SoC hardware libraries provide a low-level software interface to the underlying SoC hardware implementation. This application programming interface (API) provides easy access, configuration, and control of SoC hardware resources.

Hardware Libraries Abstract SoC Hardware



SoC EDS Editions

The SoC EDS is available in two editions: Standard Edition and the free Lite Edition. Designed for firmware and bare-metal developers, Standard Edition enables full FPGA-adaptive debugging via an Intel FPGA Download Cable II connection. For Linux software developers, the free Lite Edition allows application development over an Ethernet connection.

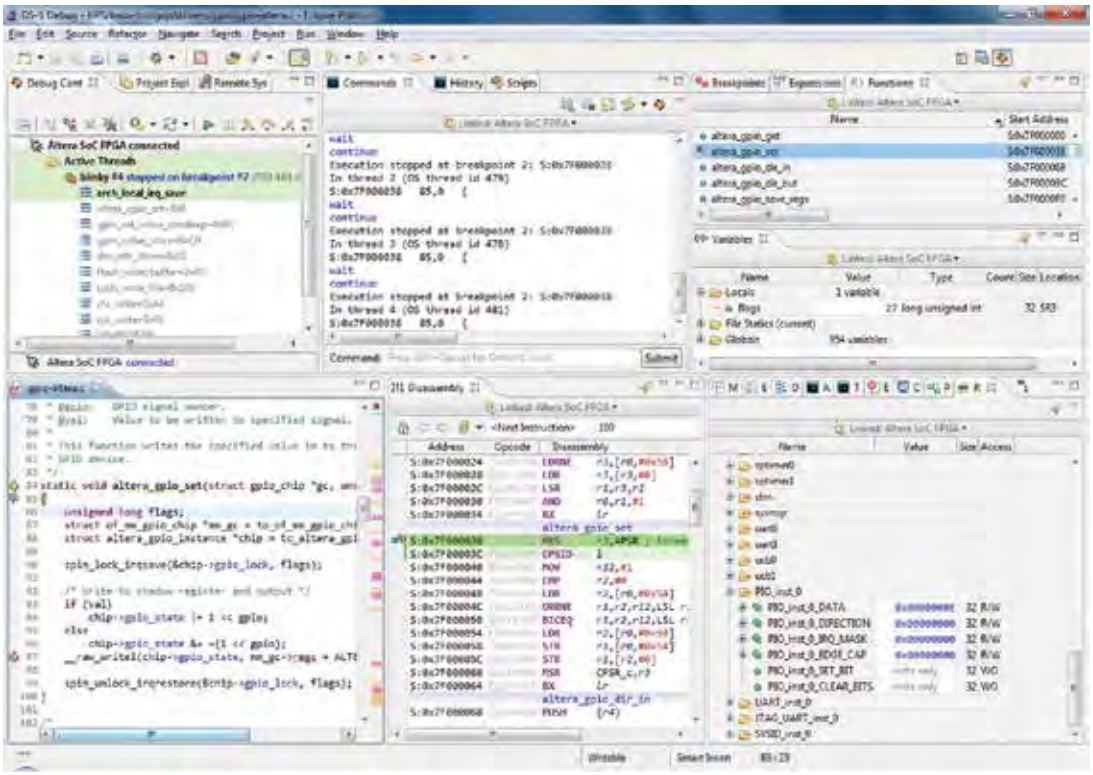
SoC EDS Editions

Application/Use Case	Lite Edition	Standard Edition
Board Bring-up		Yes
Device Driver Development		Yes
Operating System Porting		Yes
Bare-Metal Programming		Yes
Linux Application Development	Yes	Yes
Multicore Debugging		Yes
System Debugging		Yes

FPGA-Adaptive Debugging

At the heart of the SoC EDS is the ARM DS-5 for Intel SoC FPGAs. By combining the ARM DS-5 advanced multicore debugging capabilities with FPGA-adaptivity and a seamless link to the Intel's SignalTap™ II logic analyzer, the toolkit provides you with an unprecedented level of full-chip visibility and control.

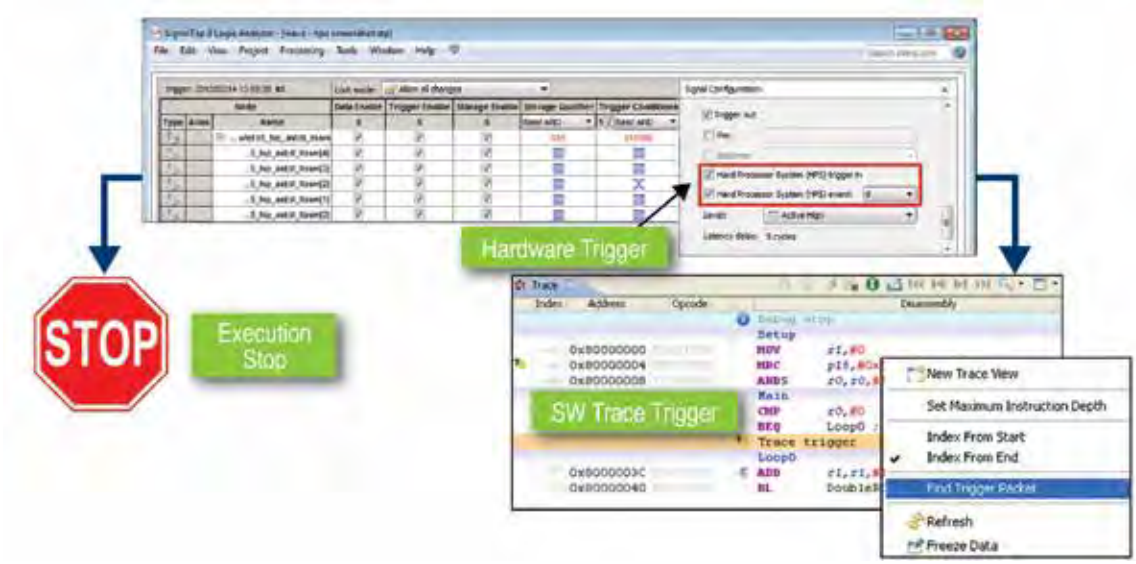
ARM DS-5 Intel SoC FPGA Edition



The toolkit displays pre-configured CPU subsystem peripheral register views and enables automatic generation of register views for peripherals in the FPGA fabric. All register views are self-documenting and organized by peripherals, registers, and bit fields.

Working with the SignalTap II Logic Analyzer, the toolkit provides advanced, signal-level hardware cross- triggering between the CPU and FPGA domains. Using this capability, software and FPGA designers can analyze the captured trace and co-debug across the hardware-to-software boundary.

Cross-Triggering Between CPU and FPGA Domains



With the ARM DS-5 Intel SoC FPGA Edition, you can efficiently debug code running on the dual-core CPU subsystem as well as IP synthesized into the on-chip SoC's FPGA fabric for higher productivity, better software quality, and faster time to market.

Key features include:

- Support for board bring-up, driver development, OS porting, bare-metal, and Linux application development
- Development and debugging support for systems running in symmetric multiprocessing (SMP) and asymmetric multiprocessing (AMP) modes
- Simultaneous debug and trace connection for ARM Cortex-A9 processors as well as any custom cores with ARM CoreSight* trace macrocells synthesized on the FPGA fabric
- Allows non-intrusive capture and visualization of signal events in the FPGA fabric, time- correlated with software events and processor instruction trace
- Supports advanced, signal-level hardware cross-triggering between the CPU and FPGA logic domains, enabling software execution to stop on any FPGA hardware event and hardware execution to stop on any software event
- ARM Streamline Performance Analyzer with performance counters from the SoC and FPGA domains to enable full system-level analysis
- Requires only a single cable for the DS-5 Debugger and other Intel JTAG-based tools to the Intel SoC FPGA target via the Intel FPGA Download Cable II or the ARM DSTREAM debug and trace unit.

READY TO LEARN MORE?

With Intel's ARM-based SoCs, you can reduce board size, system power, and system cost while increasing system performance. Our 28 nm SoC portfolio continues to reinvent programmable logic, enabling you to create differentiated and more complex solutions with less time and effort. Our 20 nm and 14 nm Tri-Gate SoC FPGAs offer blazing fast processor speeds and interface capabilities to give your design a competitive edge. If you're ready to learn more or get your hands on a development kit, contact your local Intel representative or visit our website for white papers, webcasts, and development kit ordering information.

Visit: www.altera.com/soc

† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

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