

A man in a light blue long-sleeved shirt and safety glasses is working on a blue industrial robotic arm. He is wearing grey gloves and is focused on adjusting a component on the arm. The background shows a factory environment with metal structures and safety fencing.

ACCELERATING INDUSTRIAL IoT INNOVATION

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ACCELERATE IoT INNOVATION

From factory and process automation to energy infrastructure and machine vision systems, industrial products help improve our world. Traditional Industrial market where PLCs, motor control, safety and security solutions are used, Intel FPGAs enable the industrial products to be safe, reliable, adaptable, helping the Industrial manufacturers design products that are future-proof and first to market.

Evolution from Industry 3.0 to Industry 4.0 will require Industrial devices to be connected in real-time, collecting data to make smart decisions and use advanced compute to build intelligent systems: Connected-Smart-Autonomous. Time-Sensitive Networking providing the deterministic connectivity and OPC-UA enabling interoperability, the unconnected devices on the factory floor can be connected. The data collected from the real-time connected devices, will be analyzed, controlled and some of that data will be send to cloud to be processed or stored. The Machine Learning analytics will enable the Smart factories and will lead to fully autonomous factories which heavily depend on Deep Learning analytics.

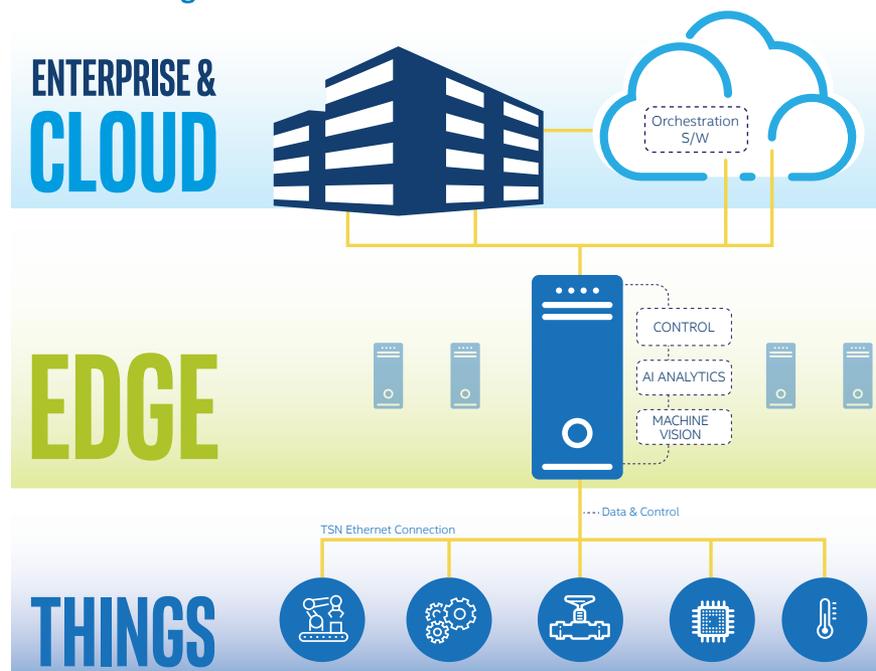
Next generation smart factories need to be more connected, secure, safe, and operate with greater efficiency than ever before. Intel® FPGAs transform industrial automation equipment into smart factories. The technologies and services to enable this transformation require changes to hardware and software architectures combined with artificial intelligence (AI)-based analytics. Learn how your next-generation automation systems can benefit from high-performance, low-latency features, with connectivity and accelerator or AI solutions with Intel FPGAs.

Figure 1 depicts a cloud-enabled industrial complex that addresses specific requirements. Larger installations involve layers including cloud, on-site, and edge networks.

Aside from the traditional control demands such as **Functional Safety (IEC61508)** and **Control (IEC61131)**, new emerging requirements related to connectivity **Time-Sensitive Networking (TSN)**, **interoperability OPC Unified Architecture (OPC UA)**, **acceleration, and security** need to be added throughout the networks. Architectures requiring the use of edge analytics and distributed control must employ networks orchestration software for the precise control of motion and other manufacturing processes.

This brochure provides an overview of solutions for various industrial systems using Intel FPGAs.

Figure 1. Industrial Automation Architecture



THE INDUSTRIAL IoT

End-to-end connectivity from sensors and actuators on the factory floor, to Edge, and to the Enterprise Cloud have opened up the possibility of unprecedented operational efficiencies that can be achieved by combining this ubiquitous connectivity with autonomous operation.

To realize the vision of Industry 4.0 the 'things' at the factory floor will get smarter and connected. At the same time, the 'edge' will become more powerful by integrating capabilities that were only available in the cloud so far such as artificial intelligence. Edge compute is driven by the need for:

- Real-time connectivity
- Increased availability
- Higher security, reduced risk
- Local intelligence
- Ability to process, condition and use large amounts of data
- Less reliance on expensive cloud infrastructure

Figure 2. Technology Pillars Enabling Industrial IoT

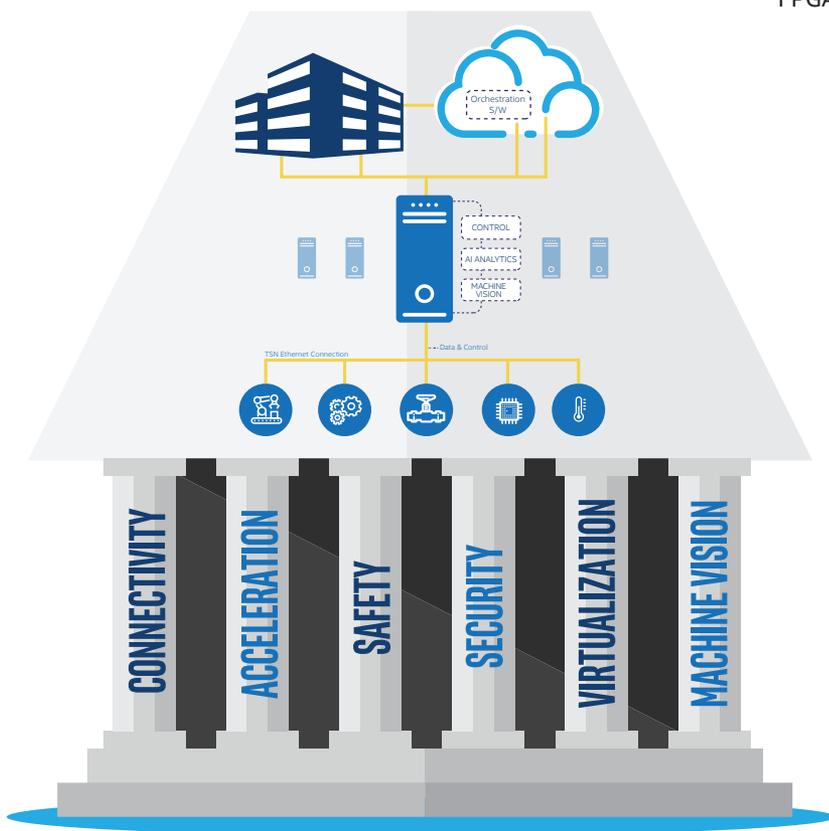


Figure 9 shows the architecture of an Edge gateway implementation that can be realized using Intel's CPU and FPGA solutions.

FPGA Value in Industrial IoT

Intel FPGAs and SoC FPGAs play a pivotal role in providing flexible connectivity options, scalable compute power for analytics, and high fabric performance for accelerating interoperability, manageability, and security algorithms; and they are able to do this at a power profile considerably less than conventional processors. The scalability of Intel processors, combined with the flexibility and performance of Intel FPGAs, provide the best solution for the industrial Internet of Things (IoT).

Wired connectivity for the smart factory should support the need for new standards on new standards, such as IEEE 802.1 TSN and software frameworks OPC-UA. A variety of FPGA-based TSN solutions provide deterministic connectivity, flexibility for mixing and matching different industrial equipment.

CONNECTIVITY

Time-Sensitive Networking (IEEE 802.1 – TSN)

TSN is proving to be a key enabling technology for Industrial IoT and Industry 4.0 by acting as one of the networking standards for deterministic Ethernet communication in many end markets, such as industrial automation, substation automation, machine vision, autonomous vehicle networking, and robotics.

By integrating TSN solutions based on Intel FPGAs into your end product, you can build PLCs, I/O controllers, industrial gateways/PCs/servers that offer users the full benefits of guaranteed real-time Ethernet communication. Intel FPGA-based TSN solutions will be compliant to the following IEEE 802.1 standards:

- 802.1Qbv
- 802.1Qcc
- 802.1AS
- 802.1ASrev
- 802.1Qbu
- 802.1CB
- 802.1Qci

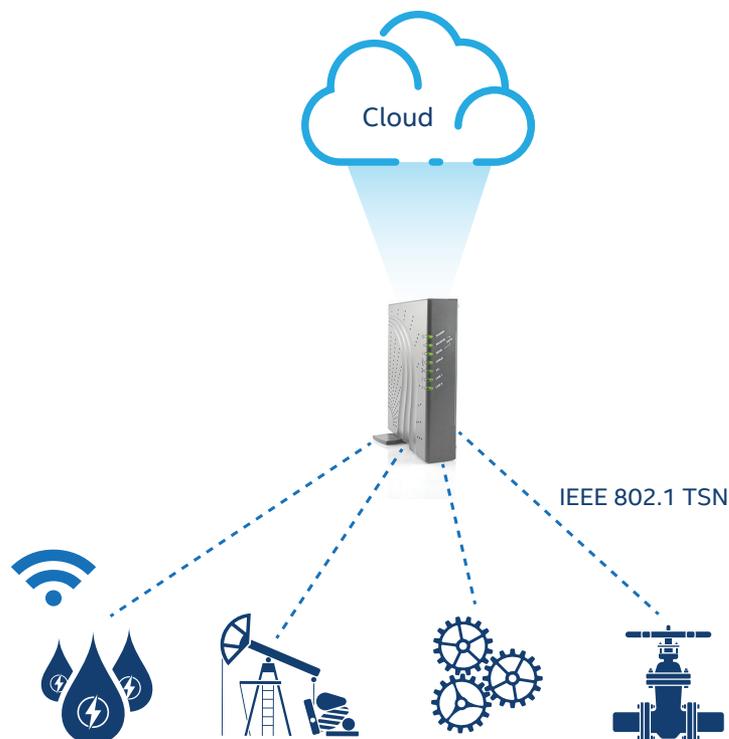
Intel has partnered with TTEch, leader in real-time networking platforms and safety controls. TTEch's TSN IP reference design offering for Intel FPGAs provides real-time connectivity solutions. TTEch's TSN IP supports multiple TSN sub-standards and enables deterministic connectivity between industrial equipment.

Interoperability

OPC UA: Essential Open Data Connectivity for Industrial IoT and Industry 4.0

Secure, reliable open data connectivity is the central factor Industry 4.0 and the Industrial IoT relies on to deliver the unprecedented business and operational improvements end users and device vendors have come to expect. Recognized as the key data connectivity method in Industry 4.0 applications, the OPC UA protocol provides the flexibility, security, and scalability needed for the job. Designed to tackle current and evolving Industrial IoT and Industry 4.0 data connectivity challenges, OPC UA provides an elegant solution to the question of how diverse Industrial IoT components can all share meaningful (context rich) data securely and efficiently.

Figure 3. Real-time Connectivity from Things to Cloud



Key Characteristic of OPC UA

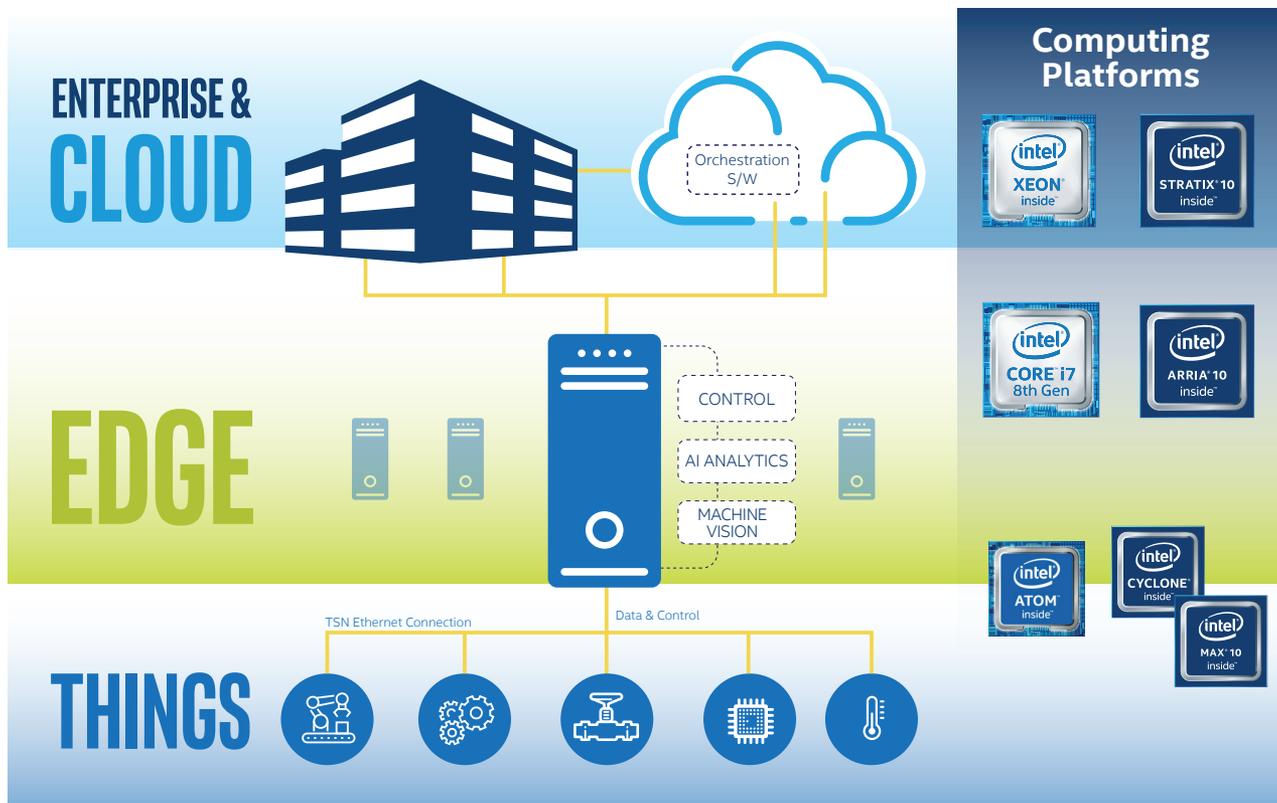
Scalability: OPC UA can run on virtually all networked sensors, devices, controllers, or applications. Taking into account that a small smart sensor will not have the computing power of a controller or a PC (both of which can sustain over a million updates per second), the OPC UA Standard groups OPC UA Server capabilities into profiles. This allows vendors to choose the right level of functionality and performance they need to implement for their specific applications.

Security: Designed from ground up using IT and OT security best practices - OPC UA addresses both IT and OT related issues (for example: ensuring data sources are secure while their data remains accessible ensuring maximum factory floor uptime). Beyond standard IT security concerns - OPC UA security employs best practices based on Public Key Infrastructure (PKI) to establish trust between systems and encryption and signing to guarantee data confidentiality and integrity right from the source.

Flexibility: With the advantage of being operating system (OS) and platform independent - OPC UA can be implemented on various platforms and any OS: from bare-metal systems with no OS, to custom real-time operating systems (RTOSs) and mainstream operating systems, such as Linux* and Windows*. OPC UA is flexible enough to make it usable on virtually any new or existing networked product.

Future Friendly: Addressing the rapid evolution of networking and IT security practices - OPC UA makes it possible to upgrade the underlying transport protocols, such as binary, HTTPS, and Advanced Message Queuing Protocol (AMQP), without disrupting previous OPC UA implementations – preserving your return on investment (ROI).

Figure 4. Industrial Automation and Intel Offerings



Industrial Ethernet

With the need to support multiple variants of Industrial Ethernet protocols, designing industrial systems can be far from simple. These protocols often must be implemented as a deeply embedded function to meet shrinking system costs, form factors, and power budgets. It is commonplace for a developer to obtain IP protocols in which they must negotiate with different vendors, usually requiring them to pay up-front licensing fees, and sometimes adding the complexity of tracking end-product sales to pay royalties.

Intel FPGAs offer an integrated Industrial Ethernet function with a simplified licensing structure. Therefore, developers have access to most of the common Industrial Ethernet protocols enabling them to focus efforts on other aspects of the design.

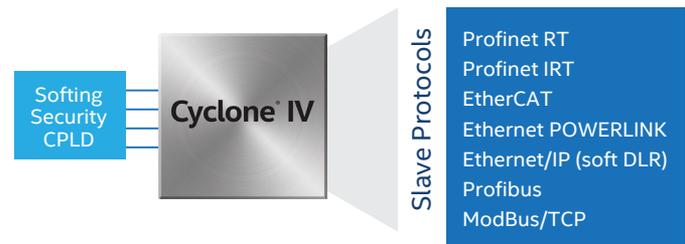
Intel has partnered with Softing Industrial Automation GmbH, the world leader in Industrial Ethernet IP protocols. The combination of Intel FPGAs and a security CPLD provides an easy and inexpensive way for developers to implement Industrial Ethernet and fieldbus connectivity platforms with:

- No license negotiation
- No up-front licensing costs
- No per-unit royalty reporting
- Easy-to-use two-chip solution with "No Hassle" licensing

Figure 5. Industrial Ethernet IP on Cyclone V SoC



Figure 6. Security CPLD Enables License for Selected Ethernet IP



ACCELERATION STACK

Enhanced Performance, Simplified

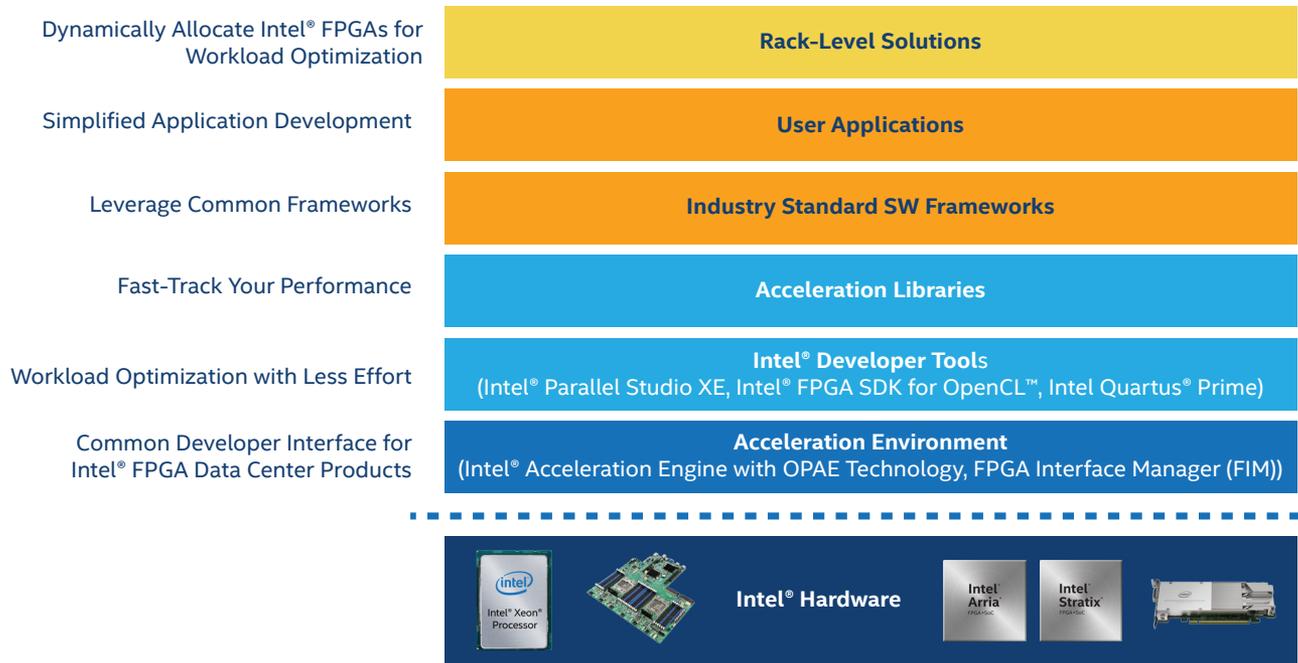
The Acceleration Stack for Intel Xeon CPU with FPGAs is a robust collection of software, firmware, and tools designed and distributed by Intel to make it easier to develop and deploy Intel FPGAs for workload optimization in the data center. The Acceleration Stack for Intel Xeon CPU with FPGAs provides multiple benefits to design engineers, such as saving time, enabling code-reuse, and enabling the first common developer interface.

The Acceleration Stack for Intel Xeon CPU with FPGAs provides optimized and simplified hardware interfaces and software application programming interfaces (APIs), saving developers time so they can focus on the unique value-add of their solution.

The Acceleration Stack for Intel Xeon CPU with FPGAs provides multiple benefits to design engineers:

- Saves developer time to focus on unique value-add of their solution
- Enables code-reuse across multiple Intel FPGA form-factor products
- Establishes the world's first common developer interface for Intel FPGA data center products
- Offers optimized and simplified hardware and software APIs provided by Intel
- Growing adoption by Intel partner ecosystem, further broadening appeal and simplifying use

Figure 7. Acceleration Stack



Open Programmable Acceleration Engine (OPAE) Technology

Open Programmable Acceleration Engine (OPAE) technology is a software programming layer that provides a consistent API across FPGA product generations and platforms. It is designed for minimal software overhead and latency, while providing an abstraction for hardware-specific FPGA resource details. To foster an open ecosystem and encourage the use of FPGA acceleration for data center workloads, Intel has open sourced the technology for the industry and developer community.

OPAE technology features:

- Provides a lightweight user-space library (libfpga)
- Provides license: FPGA API (BSD), FPGA driver (GPLv2)
 - FPGA driver being upstreamed into a Linux* kernel
- Supports both virtual machines and bare-metal platforms
- Enables faster development and debugging of accelerator functions with the included AFU Simulation Environment (ASE)
- Provides guides, command-line utilities, and sample codes

Figure 8. OPAE Technology

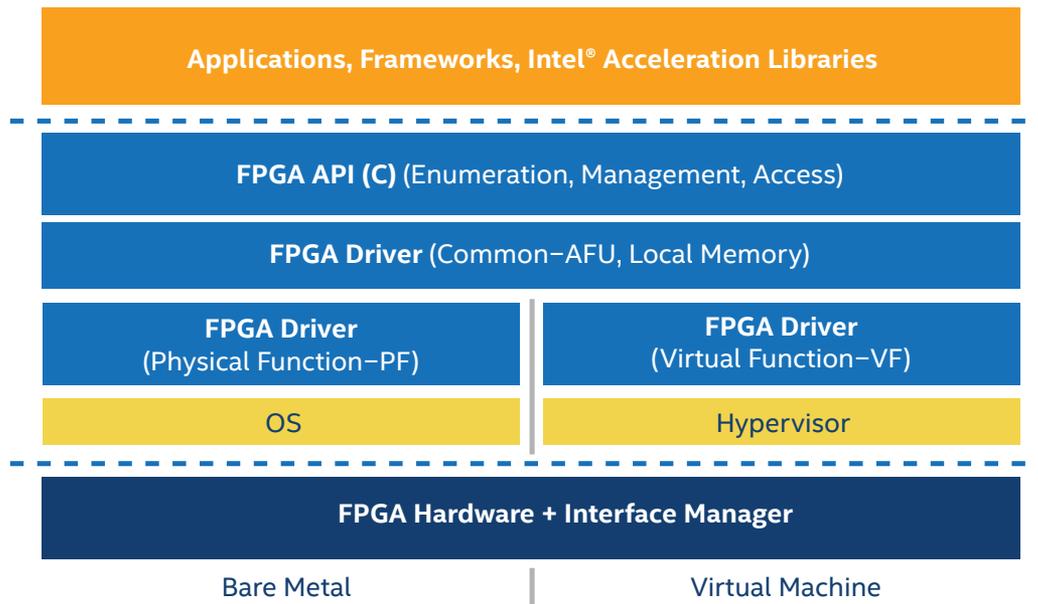
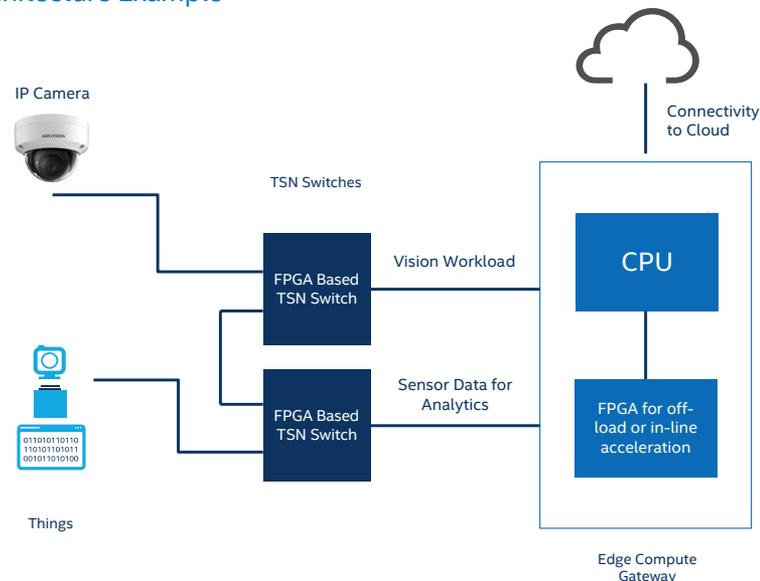


Figure 9. Edge Compute Architecture Example



SAFETY

IEC 61508 functional safety is increasingly a central requirement for industrial systems in the machinery, transportation, and process automation sectors. Government directives to reduce the risk of operator injuries and the demand for improved operational efficiencies are driving the need for more comprehensive functional safety features.

Safety imposes an increase in overall complexity with considerations such as:

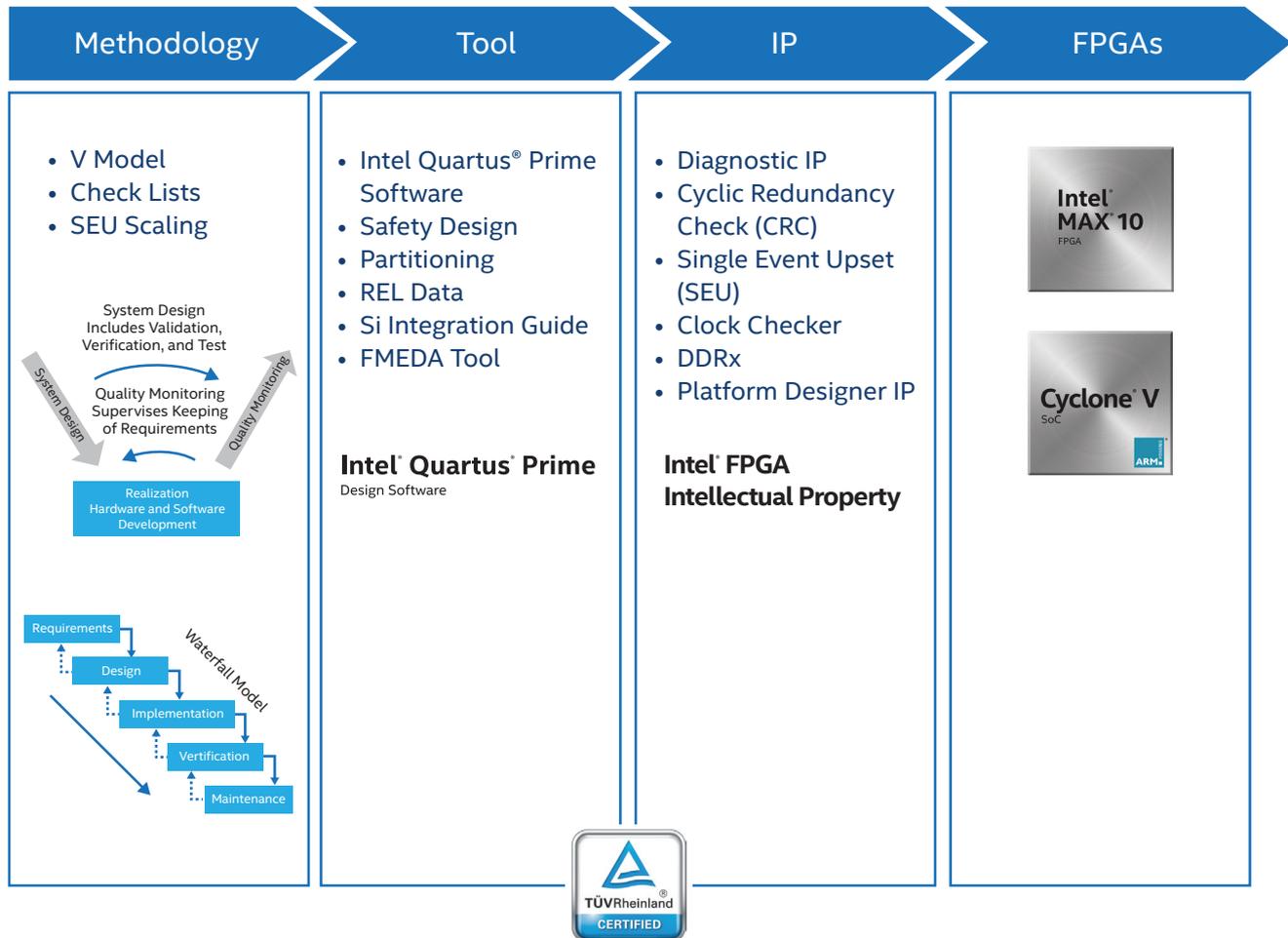
- On-schedule and in-budget product certification meeting the appropriate Safety Integrity Level (SIL) as defined by IEC 61508 and derivative industry-specific standards
- Flexibility to design for today's diverse requirements while meeting evolving requirements over the product lifetime
- Cost and risk reduction through integration of safe and non-safe functionality into fewer discrete devices

To simplify and speed up your certification process, we worked closely with TÜV Rheinland to gain approval for IEC 61508 SIL 3, making Intel the first FPGA supplier offering a complete safety package across tools, tool flows, devices, and reliability

data. Intel FPGA TUV-qualified safety package simplifies and speeds up your system-level certification process through availability of the following solutions:

- Certified **IEC 61508** tool flow mapped to FPGA specific V-flow
- Certified software tool chain —Intel Quartus® Prime software
- Diagnostic IP with **IEC 61508** standard documentation and source code to monitor the integrity of your design
- Nios® II Lockstep, SIL 3 certified Smart Comparator IP to enable safety certified software implementations
- Safety Separation Design Partitioning—Tool flow retaining the FPGA benefits of quick upgrades or bug fixes while reducing the need for full design re-certification
- Safety Reference Board— Provides board and design examples for implementing SIL 3 safety systems
- FMEDA (Failure modes, effects, and diagnostic analysis) —Provides comprehensive and detailed IEC 61508 specific failure rate calculations, simplifying customer certification data generation

Figure 10. Functional Safety Data Package



SECURITY

Security combined with safety and reliability are key requirements for the Industrial IoT, involving security approaches beyond simple methods such as link encryption. The functional view of the security framework includes:

Endpoint protection implements defensive capabilities on devices at the edge and in the cloud. Primary concerns include physical security functions, cyber security techniques, and an authoritative identity.

Communications and connectivity protection uses the authoritative identity capability from endpoint protection to implement authentication and authorization of the traffic. Cryptographic techniques for integrity and confidentiality secure the data flowing over the communications.

Brownfield describes environments where new solutions and components must co-exist and interoperate with existing legacy solutions. The term is used in contrast to Greenfield, where legacy systems are absent, removing such constraints. Implementing security for existing brownfield deployments should be as non-invasive as possible. In the case of Brownfield end points the primary consideration is not to disrupt the existing business process with added security control.

The most common technique for implementing security quickly and effectively is to deploy a security gateway that provides security capabilities to the devices behind it. Common functionality includes:

- Storing and managing identity
- Mutual authentication
- Authorizing network traffic
- Confidentiality and integrity controls

Intel FPGAs offer the capability to not only secure Greenfield environments, but also to Brownfield environments, by the creation of a secure gateways that not only adds the required security but also enables connectivity to legacy buses.

FPGA implementation is well suited to accelerating software encryption functions, providing whitelisting and firewall functionality.

FPGA acceleration of Internet Protocol Secure (IPsec) connections has been shown by Silex Insight to reduce the CPU usage by factor of 4X¹ and accelerate the throughput by greater than 7X¹.

Figure 11. Security Platform

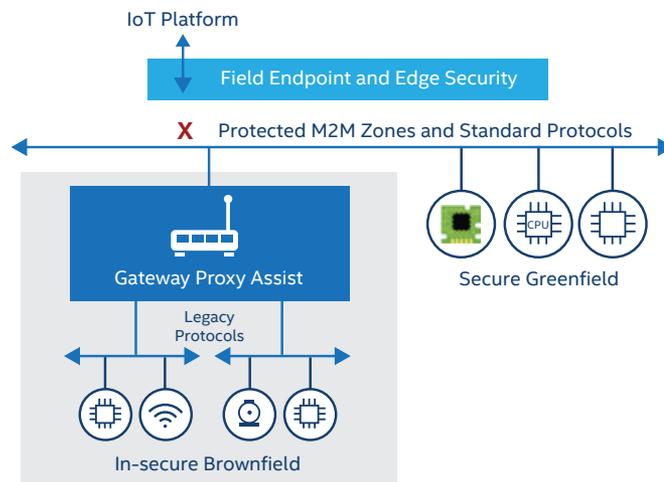
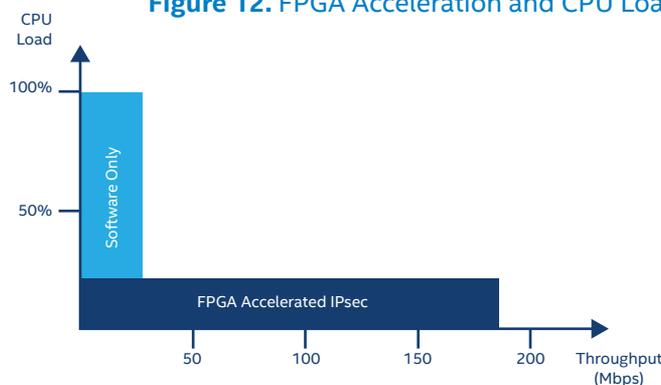


Figure 12. FPGA Acceleration and CPU Load



CONTROL

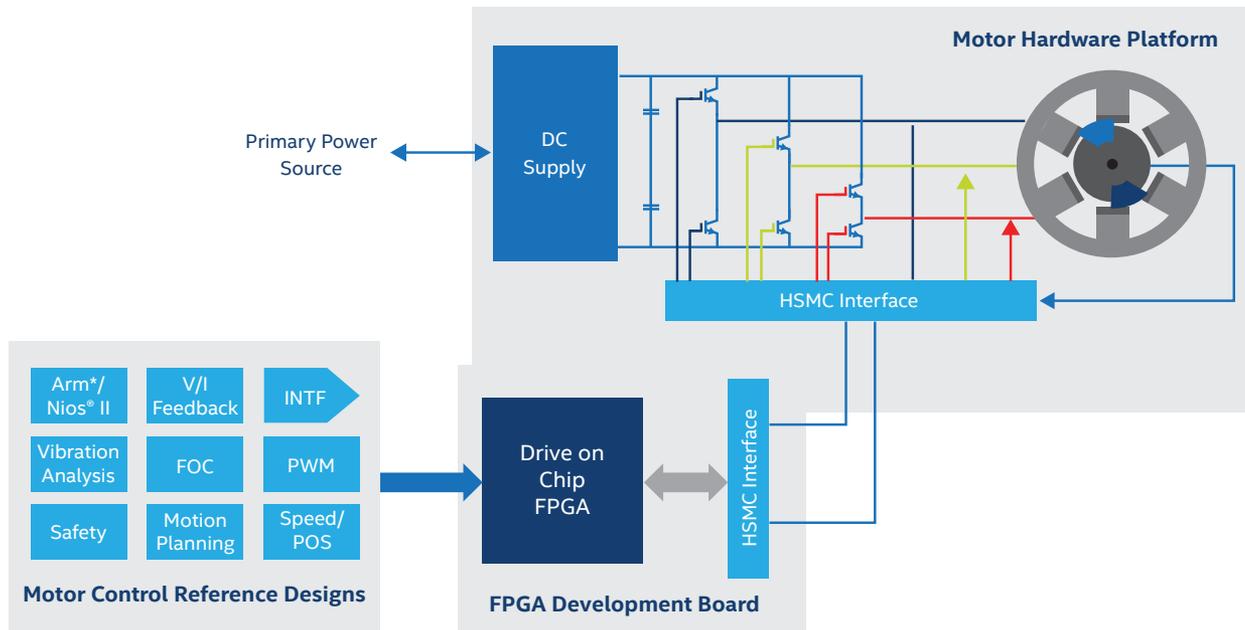
Factory Automation – Drives

Motor Control Solutions

Motor and motion control designs face with unique challenges for each application. To address the needs of motor control design engineers, Intel provides a Motor Control Development

Framework consisting of a Motor Hardware Platforms, an appropriate FPGA development board, and motor control reference designs as shown in Figure 11.

Figure 13. Intel's Motor Control Development Framework

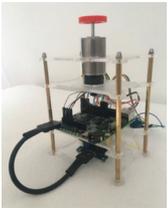


Motor Hardware Platform

The Motor Hardware Platform enables motor drive hardware engineers to quickly develop solutions without the need to design prototypes. The Motor Hardware Platform connects

an FPGA development board of choice via the high-speed mezzanine card (HSMC) interface.

TABLE 2. MOTOR HARDWARE PLATFORM OPTIONS

HARDWARE PLATFORM	DESCRIPTION	POWER STAGE	FEEDBACK/FEATURES
 <p>https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=1026#</p>	<p>Motor Types: PMSM, BLDC, stepper, software reluctance</p> <p>Axis: 2</p> <p>Applications: industrial, automotive, high-speed</p> <p>FPGA interface: HSMC</p> <p>Available Q1 2017</p>	<p>Power stage: 48V MOSFET</p> <p>Motor phases: 3</p> <p>Isolation: No</p> <p>EMI filter: No</p> <p>PF correction: No</p>	<ul style="list-style-type: none"> • DC link voltage measurement • Motor current measurement • Resolver, encoder, hall, Sensorless feedback • Power conversion or motor control (bi-directional converter)
 <p>https://shop.alizem.com/products/alizem-motor-control-reference-design-kit</p>	<p>Motor Types: PMSM, BLDC and DC motors.</p> <p>Axis: 1 in basic kit with multi-axis option available.</p> <p>Applications: medical, industrial, automotive, aerospace.</p> <p>FPGA interface: PMOD and GPIOs.</p> <p>IoT option available.</p> <p>Available Q4 2018</p>	<p>Power Stage: 10.8V MOSFET</p> <p>Motor phases: 3</p> <p>Over-current protection: Yes</p> <p>Isolation: No</p> <p>EMI filter: No</p> <p>PF correction: No</p>	<ul style="list-style-type: none"> • Easy to use software: no need for advanced expertise in motor control nor FPGA • Customizable to any power level (30W-100kW) with same software • Kit built with low-cost COTS components • Two phases current measurement • Incremental encoder with single-ended channels

Motor Control Reference Design

Intel's motor control reference design provides engineers with key software and hardware intellectual property (IP) cores to design the motor control algorithms quickly and easily. Thus, reducing design time of the motor control to focus on system-level customization.

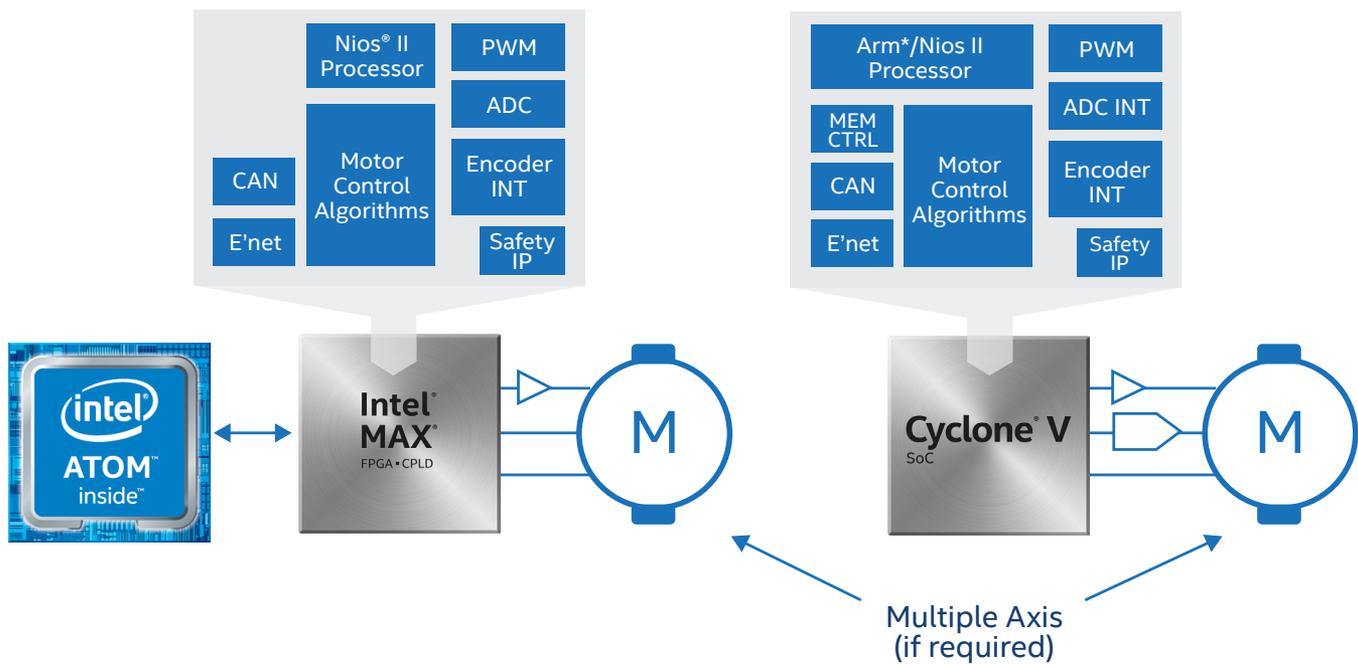
[AN 773: Drive-On-Chip Reference Design for MAX® 10 Devices](#) and [AN 669: Drive-On-Chip Reference Design for Cyclone® V SoC Devices](#) shows how to download and use the reference designs. The reference design itself is free to download at <https://cloud.altera.com/devstore/platform/>.

When combined with other IP from Intel or one of its partners, highly precise, cost-effective motor and motion control solutions with safety, connectivity, and security features are implemented on a single FPGA, speeding time to market.

Motor Control Use Cases

Figure 12 provides two common FPGA use cases. Drive designs typically incorporate programmable logic either as a companion device, shown on the left, or in a 'drive-on-a-chip' configuration, shown on the right. In both cases the programmable logic is closely coupled with the motor hardware enabling the system designer to take advantage of the FPGAs unique capabilities.

Figure 14. Motor Control FPGA Use Cases



PWM = pulse-width modulation
 ADC = analog-to-digital converter

Factory Automation – PLCS

FPGA Use Cases for PLC

Figure 13 and Figure 14 illustrate two common FPGA use cases for programmable logic controllers (PLCs). In Figure 13, the FPGA serves as a companion device to an Intel processor and provides hardware acceleration and specialized connectivity features (e.g., IEEE 802.1 TSN or Industrial Ethernet).

This architecture is highly scalable as the appropriate Intel processor can be chosen to meet the needs of a specific

family of PLCs. In this instance, FPGAs are particularly useful if the design employs emerging technologies in which standards are somewhat fluid; allowing for updates after equipment deployment. Figure 14 illustrates a single-chip PLC and shows the main features of a development kit from one of Intel's industrial partners, Exor International. An Arm* architecture provides processing, while core functionality, required for a mid-range PLC, is implemented within the Cyclone® V SoC. This architecture is particularly useful for cost-sensitive designs.

Figure 15. FPGAs as a PLC Companion Device (Intel Architecture)

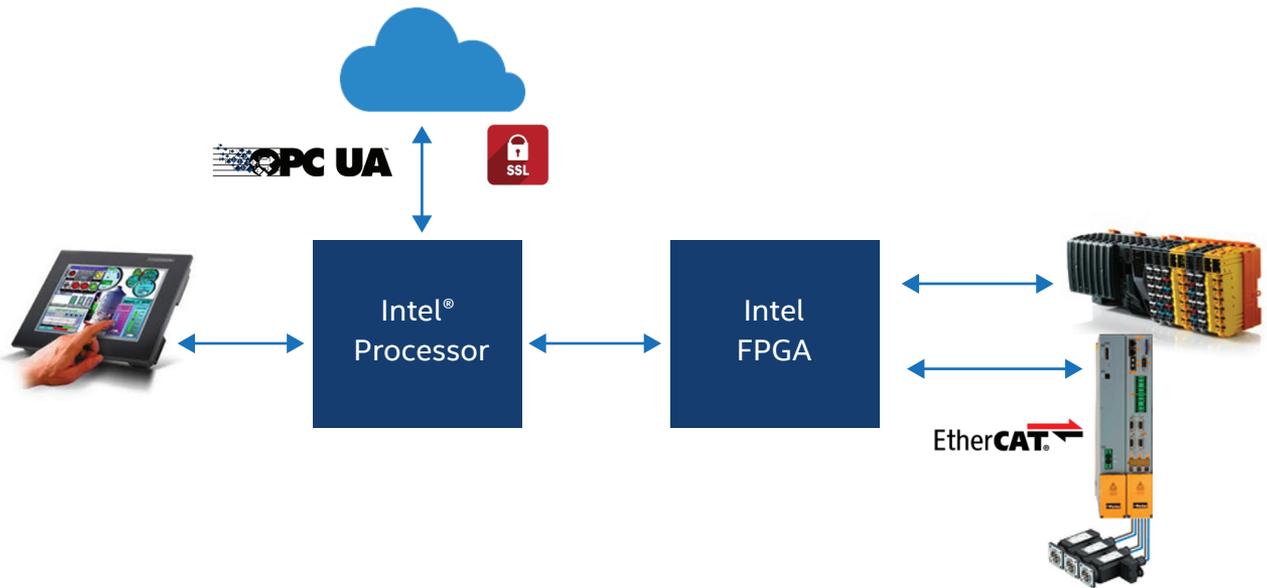


Figure 16. Cloud-Enabled PLCs and I/O Modules

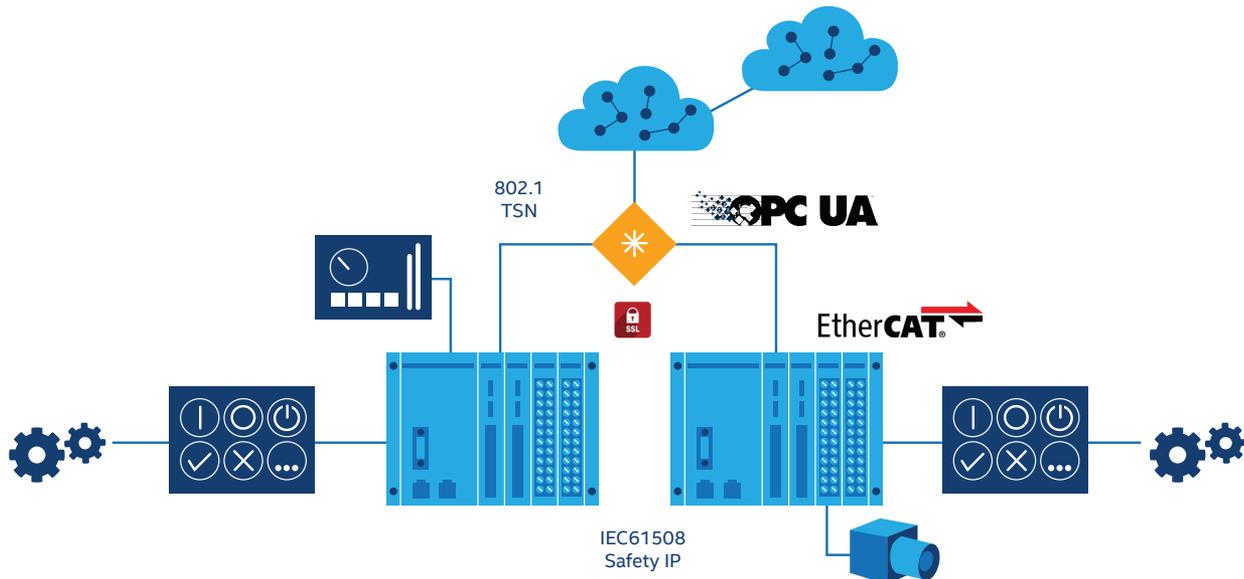
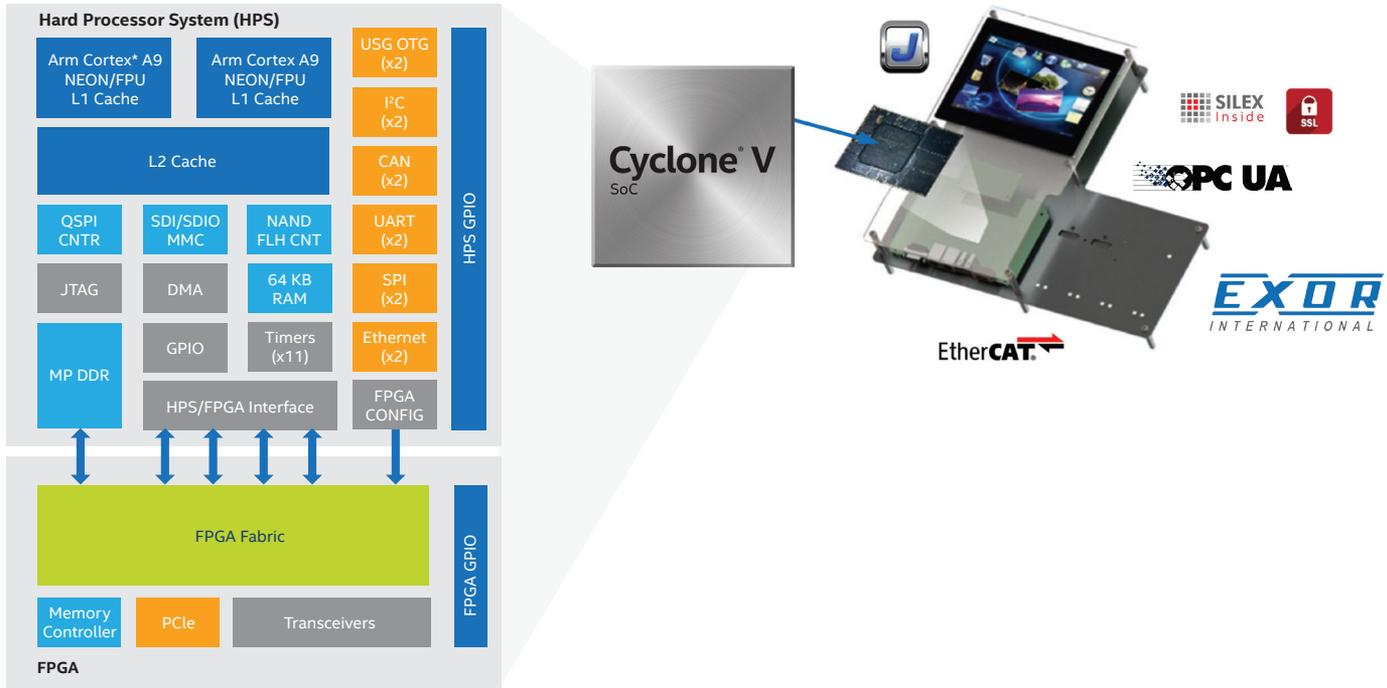


Figure 17. Single-Chip PLC Development Platform (Arm Architecture)



FPGA Benefits in PLC Applications

Programmable logic provides several key benefits for PLC architectures:

- Scalable performance
- Increased security
- Reduces development costs and accelerates time to market

FUNCTION	CYCLONE® V SoC SECTION	COMMENT
Operating System	HPS	Linux* Kernel 3.8 RT
Control	HPS	CODESYS
Connectivity	HPS	Ethercat
Security	HPS + FPGA	Hardware Accelerated OpenSSL
Interoperability	HPS	OPC UA
Human Machine Interface (HMI)	FPGA	Video Controller
HMI	HPS	Graphics Engine (JMOBIL)
Connectivity	HPS	Fieldbus Interfaces

Machine Vision

Machine-based image inspection and analysis is proliferating at an unprecedented rate throughout many industrial applications. Manufacturers can speed production processes, minimize defects, and reduce costs.

Intel FPGAs provide the highest degree of I/O connectivity and programming flexibility, drastically simplifying integration of a wide range of image sensors, enabling use of tightly tuned image pipelines in many use cases.

When coupled with Computer Vision Analytics, a high level of understanding from digital images or videos can be realized to achieve object recognition in applications, such as intelligent surveillance, collision avoidance in autonomous drones, and beyond.

Intel architecture and FPGAs bring together a high-performance heterogeneous compute platform to optimally execute image sensor pipelines and vision analytics in one system.

In doing so, Intel simplifies the design flow by abstracting the heterogeneity of the architecture through a user-friendly Vision SDK. At the same time, it still provides unrestricted extensibility through OpenCL™ for customers who want fine-grained control.

Figure 18. Intel Architecture and Intel FPGA

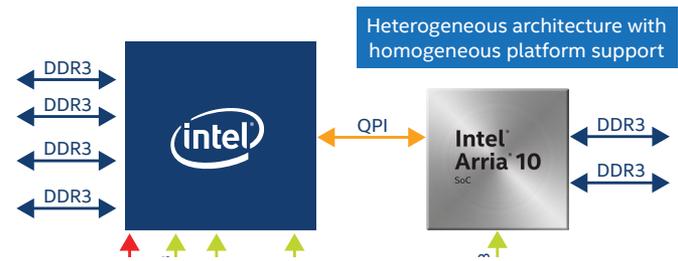
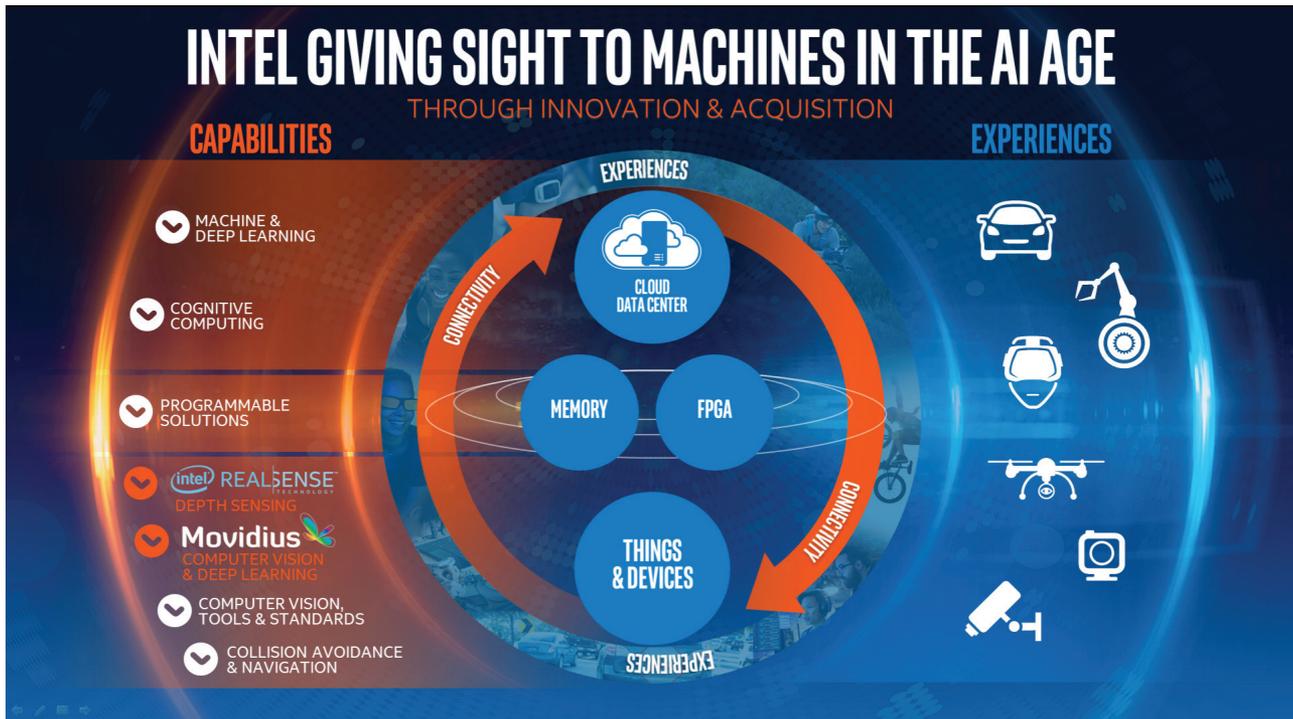
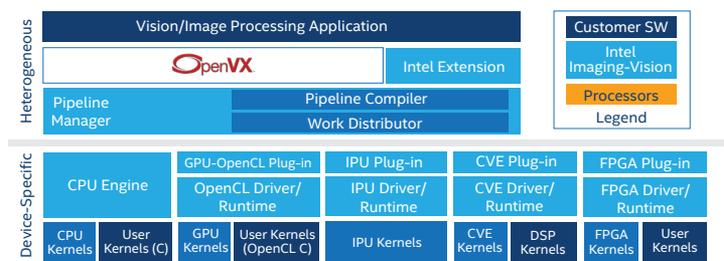


Figure 19. Intel OpenVINO Toolkit Architecture

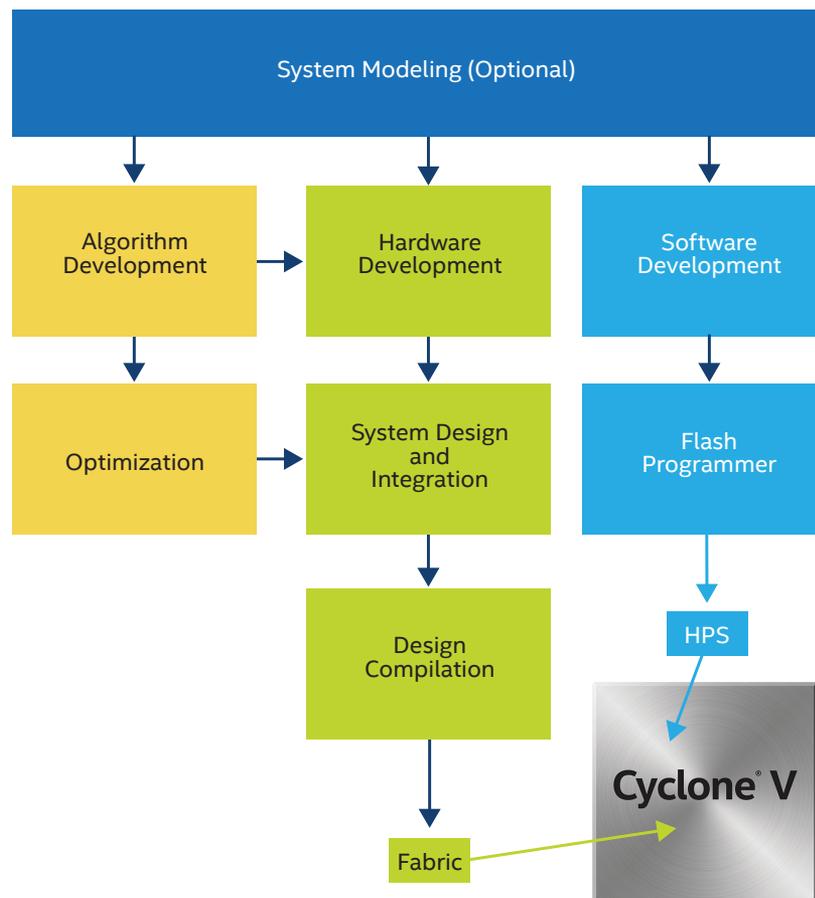


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DEVELOPMENT ENVIRONMENTS AND TOOLS

Figure 18 illustrates the various development flows supported by Intel FPGA development tools. Whether you work in the software domain, the hardware domain, or on modeling, Intel has the tool suite to model, develop algorithms, and build your system.

Figure 20. Intel FPGA System Development Environments



Standard Software Development Tools for High Productivity



Develop software targeting integrated Arm and Nios II processors on Intel SoC and FPGAs using the Arm Development Studio 5* (DS-5*) for Intel SoC FPGAs and other standard Eclipse-based software development and debug tools.

Model-Based Software and Hardware Design Flows



DSP Builder for Intel® FPGAs

Simulate models of complete systems and use C/C++ and HDL code generation tools from MathWorks and Intel to directly target FPGA and SoCs. MathWorks* Embedded Coder, HDL Coder, and DSP Builder for Intel FPGAs tools shorten your design cycle, from algorithm development and system modeling, to software hardware design partitioning exploration and optimized system implementation.

Intellectual Property

Intel® FPGA Intellectual Property

Together with our partners, we offer a broad IP portfolio in areas such as Industrial Ethernet, motor control, and functional safety in addition to optimized standard communication, memory controller, and DSP functions

Intel® Quartus® Prime Software Development Tools

Platform Designer

(formerly Qsys)

Intel® Quartus® Prime

Design Software

The Platform Designer, which is part of the Intel Quartus Prime Software, lets you integrate coprocessors, interface IP, and on-chip Arm and Nios® II processors. It allows for system-level specification of design topology, peripheral addressing and interrupts, and AXI* interconnect generation to meet required throughput, latency, and area constraints.

The Intel Quartus Prime Software is revolutionary in performance and productivity for FPGA, CPLD, and SoC design synthesis, place and route, and static timing analysis.

Intel HLS Compiler

Intel® HLS Compiler

The Intel HLS Compiler is a high-level synthesis (HLS) tool that takes untimed C++ as input and generates production-quality register transfer level (RTL) code optimized for Intel FPGAs. This tool accelerates verification time over RTL by raising the abstraction level for FPGA hardware design. Models developed in C++ are typically verified orders of magnitude faster than RTL.

Intel FPGA SDK for OpenCL Overview

Intel FPGA SDK for OpenCL enables software developers to accelerate their applications by targeting heterogeneous platforms with Intel CPUs and FPGAs. This environment combines Intel's state-of-the-art software development frameworks and compiler technology with the revolutionary, new Intel Quartus Prime software to deliver next-generation development environment that abstracts FPGA details while delivering optimized results. Intel FPGA SDK for OpenCL enables you to fully leverage the unique capabilities of FPGAs to deliver acceleration performance with power efficiency and low latency.

OpenVINO

OpenVINO Toolkit

Develop applications and solutions that emulate human vision with the Intel® Distribution of OpenVINO™ toolkit. Based on convolutional neural networks (CNN), the toolkit extends workloads across Intel® hardware (including accelerators) and maximizes performance.

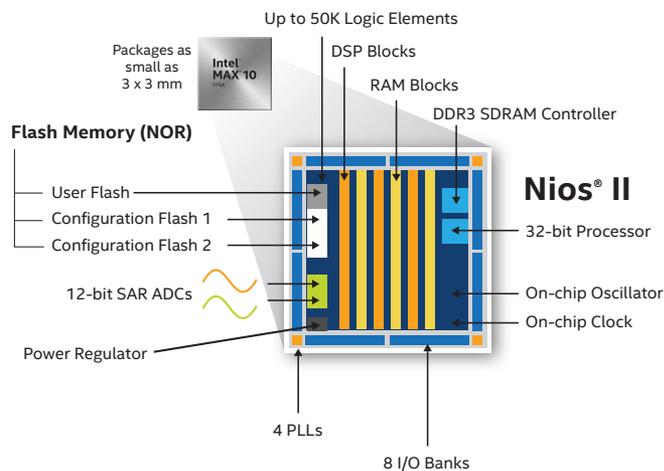
- Enables CNN-based deep learning inference on the edge
- Supports heterogeneous execution across computer vision accelerators—CPU, GPU, Intel® Movidius™ Neural Compute Stick, and FPGA—using a common API
- Speeds time to market via a library of functions and preoptimized kernels
- Includes optimized calls for OpenCV and OpenVX*

SELECT INDUSTRIAL PRODUCTS

Intel® MAX® 10 Device Family

The Intel MAX 10 device family is a versatile 'hybrid' product family possessing some qualities of a CPLD and is also a full-featured FPGA. The on-board flash memory provides device configuration registers, which can be used for parameters and/or code/ data storage for a Nios II soft processor. The Intel MAX 10 FPGA is highly integrated with traditional FPGA circuitry (fabric, RAM, DSP, phase-locked loops (PLLs), and I/O) but can also include analog blocks (voltage regulators, analog-to-digital converters (ADCs), and temperature sensors). Use cases range from implementing a simple block of logic to a companion device that handles pulse-width modulator (PWM) channels and industrial communications to a fully integrated one-chip solution, such as an I/O module, a 4-axis drive with industrial Ethernet, or an industrial Ethernet switch.

Figure 21. Intel MAX 10 FPGA Architecture



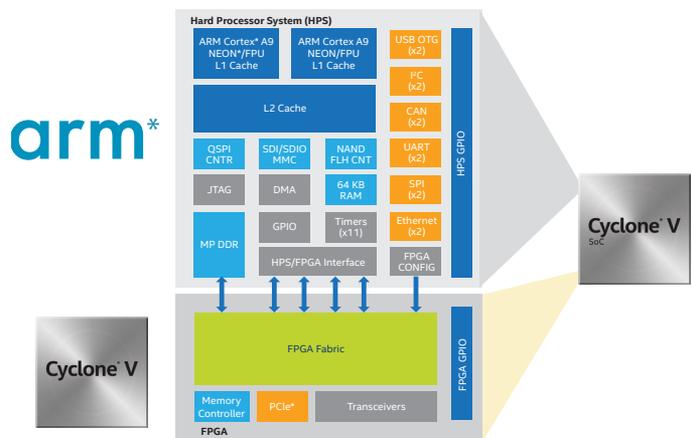
Intel® Arria® 10 Device Family

Intel Arria device family delivers optimal performance and power efficiency in the midrange. The Intel Arria device family has a rich feature set of memory, logic, and digital signal processing (DSP) blocks combined with the superior signal integrity of up to 25.78 Gbps transceivers that allow you to integrate more functions and maximize system bandwidth. Furthermore, the SoC variants in the Arria V and Intel Arria device families offer an ARM*-based hard processor system (HPS) for even higher integration and power savings.

Intel Cyclone® Device Family

The Intel Cyclone device family has been a workhorse in the industrial segment for decades. The industrial segment requires a careful balancing act between cost, performance, and power consumption. SoC device family members represent the latest trend in programmable logic technology, combining FPGAs with on-chip embedded CPU systems while the benefits from the perspectives of cost and size are obvious, there are notable advantages to implementations employing a Cyclone V SoC over a (a processor and companion FPGA) architecture. The coupling between the processor cores and the fabric are much tighter than a two-chip approach enabling the fabric to provide function acceleration rather than offloading the processor. The bandwidth between the HPS and the FPGA fabric is very high; and, blocks implemented in the fabric can share parameters with the processor cores via the L2 cache while maintaining cache coherency. Additionally, the development and debug environment is far superior, which enables much faster architecture development when there is significant interaction between the processor and fabric.

Figure 22. Cyclone V SoC





**Powering Industrial IoT:
Intel Enpirion® Power Solutions**



Intel Enpirion® Power Solutions were the first to deliver power supply-on-chip (PwrSoC) DC-DC converters with a high level of integration and ultra-small footprint that addresses the entire breadth of industrial application requirements.

Higher Efficiency and Thermal Performance

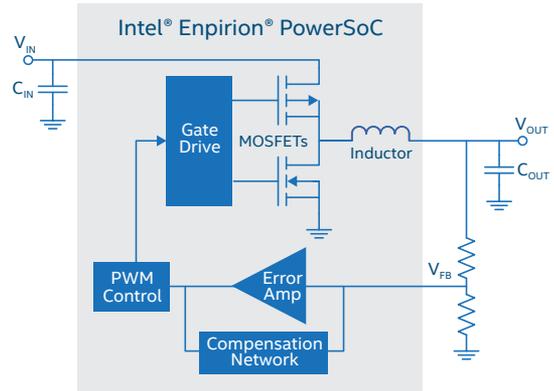
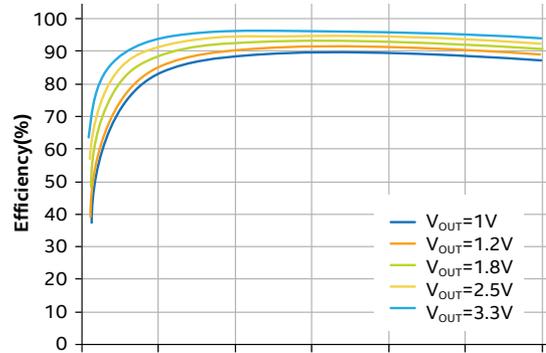
Industrial electronics must deliver increasingly higher levels of performance in smaller form factors. Conventional thermal management devices are typically not an option. Intel Enpirion Power Solutions' highly efficient, point-of-load approach reduces system thermal load greatly increasing system reliability and reducing costs.

High Power Density and Small Footprint

Intel Enpirion PwrSoCs integrate the controller, power stages, critical passive loop components, and inductor into a single device. Electromagnetic interference (EMI) emissions are ultra-low due to compact module size.

Ease of Design, High Reliability

Intel Enpirion PwrSoCs are fully validated designs providing engineers with turnkey solutions. This can save engineers over 40%† less design time than discrete power solutions. More importantly, higher levels of integration lead to improved mean time between failures (MTBF) and failure in time (FIT) rates that help reduce a common cause of system failures.



Intel® Enpirion® Power Solutions

Up to 600 mA 2.25 mm x 2.5 mm	600 mA to 1.5 A 3 mm x 3 mm	1.5 A to 3 A 4 mm x 6 mm	3 A to 4 A 4 mm x 7 mm	4 A to 8 A 8 mm x 8 mm	8 A to 12 A 10 mm x 11 mm	Digital up to 40A 11 mm x 17 mm
EP5357/58	EP53A7/A8/F8	EN5319/29/39	EN6337/47	EN6362/82	EN63A0	EM2120/30/40

cm 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

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† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

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