Reliability of heterogeneously integrated hybrid lasers for optical compute interconnects

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***Abstract*—Intel's Silicon Photonics (SiPh) components including its hybrid-lasers have been proven to achieve good performance and reliability[1], an important consideration for the reliable deployment of silicon photonics in optical compute interconnects (OCI) and co-packaged optics (CPO). In this paper, the impact of packaging-assembly-induced thermo-mechanical (TM) stress effects on the lasers during the packaging-assembly process is discussed. Particularly, a method to determine the thermal budget for packaging the lasers without impacting their reliability in the final products is proposed.**

Silicon photonics technology, silicon photonics hybrid lasers, thermo-mechanical stress, thermal budget, reliability.

I. INTRODUCTION

I-A. Intel's SiPh Technology[2]

The silicon photonics research-development-manufacturing at Intel in the last 2 decades has enabled new optical transceiver products for network infrastructure interconnect application within data centers. Utilizing silicon as optical transmission medium and processes compatible with typical CMOS fabrication processes, integration of optical and electronic devices in the same photonic integrated circuit can be done without steps to assemble individual devices resulting in high volume manufacturing and more reliable components.

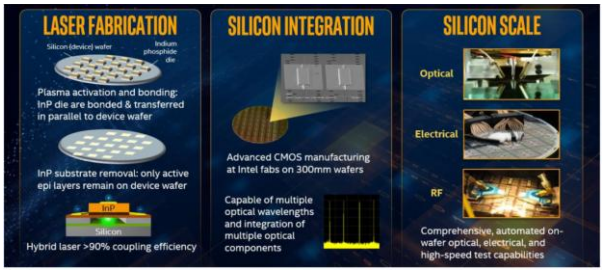


Figure 1: Overview of Intel's SiP research, development, nd manufacturing components for optical transceiver modules, OCI, and CPO applications[2].

I-B. Reliability of Intel's SiPh hybrid lasers

It was reported previously[1] that, Intel's hybrid lasers were intrinsically immune to several failure modes of conventional discrete distributed feedback lasers, namely, (1) without exposed III-V facets, there was no catastrophic optical mirror damage, (2) without III-V re-growth steps, the epitaxial interface defects were significantly reduced, and (3) standardized 300mm wafer handling and assembly process eliminated the possibility of handling-assembly-induced electrostatic discharge damages leading to latent failures. In addition, for elimination of other failure modes due to crystalline defects such as dark line dislocations and catastrophic optical bulk damage, every laser was tested using a wafer-scale, high-volume manufacturing burn-in test system to screen out early life failures prior to field deployment. Specifically, the reliability of Intel's lasers was demonstrated with 45,000 hours of high temperature operating life testing on 32 units with negligible observed degradation. A failure rate in time of < 0.1 FIT was demonstrated with accelerated life testing of over 55 thousand lasers and validated as 0.05 FIT by analyzing field deployment data collected from more than 6 million hybrid lasers with 100% Failure Analysis (FA) confirmation over a period of 3 years.

I-C. Packaging-assembly induced TM stress

The packaging process to integrate the hybrid lasers into final products would expose them to different thermal profiles, hence, induced thermal stress on them and could potentially alter their quality and reliability behaviors.

One of those thermal profiles was the standard IPC/JEDEC J-STD-020F lead-free solder reflow profile with typical max temperature of 250C; see figure 2. Other thermal profiles could have a max temperature up to 300C but with much shorter exposure time.

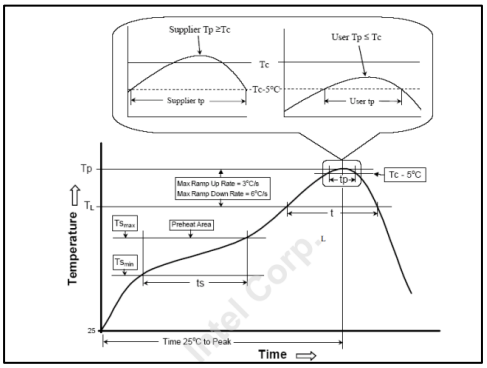


Figure 2: IPC/JEDEC J-STD-020F lead-free solder reflow classification profile (not to scale.)

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II. THERMAL BUDGET FOR INTEGRATING THE HYBRID LASERS DEVELOPMENT

II-A. Thermal expense definition

After fabrication, the SiPh wafers with the Photonic Integrated Circuits (PIC) die would go through additional manufacturing assembly processes similar to the packaging processes for the conventional semiconductor IC technology including wafer backside metallization, solder bumping, SMT, die-attach, solder reflow and others until production complete. The temperature and duration of those processes were different and could affect hybrid-lasers' quality and performance.

An actual lead-free solder reflow profile following the IPC/JEDEC J-STD-020F standard was shown in figure 3. The lasers could experience many rounds of this reflow profile during the production manufacturing.

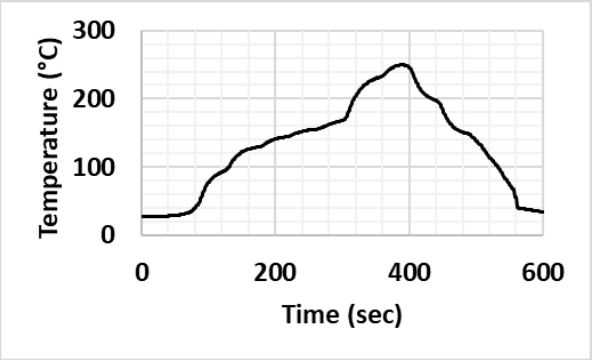


Figure 3: An actual lead-free solder reflow profile following the IPC/JEDEC J-STD-020F standard.

Conceptually, if one could correlate the laser characteristic changes with a quantity representing the impact of the packaging thermal profiles, safe conditions for packaging could be determined. One approach to achieve such goal was to utilize Fick's law of diffusion where temperature and exposure time were input factors. Accordingly, a proxy reflecting the packaging's thermal profile impact on the lasers, namely ***the thermal expense***, could be defined as shown below:

$$Thermal\ Expense \overset{\text{def}}{\equiv} \sum_{Step\ i} \left(dt_i \times D_0 e^{\frac{E_A}{kT_i}} \right)_i$$

where:

dt_i: exposure time to the temperature profile at ***step i***.

k: Boltzmann's constant, 8.6173×10^{-5} eV/K.

T_i: Temperature (K) at ***step i***.

Note that in the above definition, for engineering practical purposes, the pre-exponential constant ***D_0*** and the activation energy of proton diffusion ***E_A*** of the Fick's law were normalized, i.e. setting to equal 1. In parallel, if the change in laser characteristics after each of the process steps were also documented, a ***thermal budget,*** that is the maximum thermal expense when the change in laser characteristics was still within acceptable limit, can be determined.

II-B. DOE, Results, and Discussion

To demonstrate such approach, a DOE was carried out, where laser test structures were subjected to different thermal profiles and the structure's characteristic change was captured as shown in figure 4. Based on this data, a plot of the change using 95%ile data points of the distributions vs. thermal expense was obtained; see figure 5. With the obtained plot, the thermal budget was thus can be determined providing that characteristics change would not be allowed to exceed certain criteria. As a case study, Intel's hybrid lasers were exposed to the IPC/JEDEC J-STD-020F standard's lead-free solder reflow profile multiple times; the results showed insignificant change to their characteristic behaviors, confirming that the lasers should be fully compatible to any heterogeneous integration of electronic ICs and photonic ICs (Co-Packaged Optics) schemes utilizing existing conventional electronic IC packaging technologies.

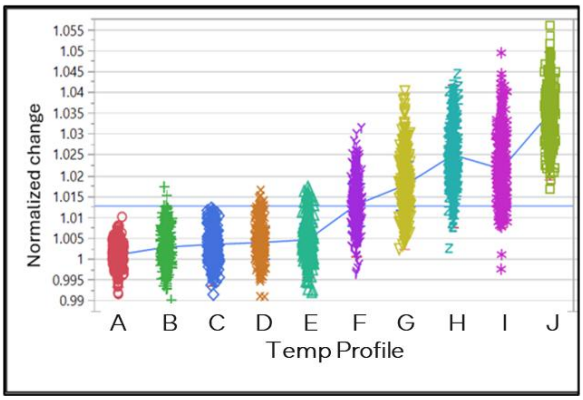


Figure 4: Temp-Profile-DOE where laser test structures were subjected to different thermal profiles and the structure's characteristic change was captured. The temp profiles have temp and duration increased in order from A→B→C→…→J.

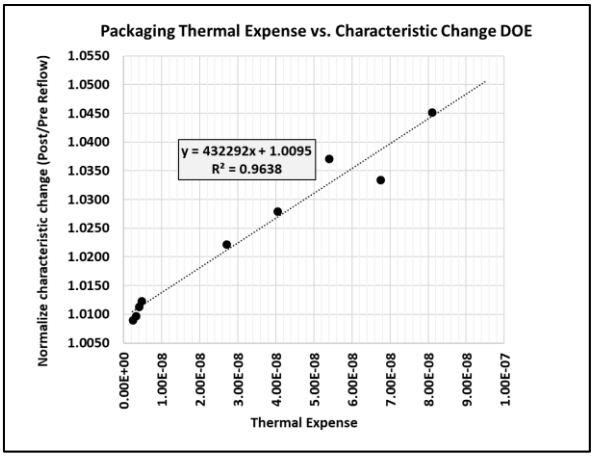


Figure 5: Calibration curve, using the 95%ile data points of the distributions from the Temp-Profile-DOE, to determine thermal budget for integrating the hybrid lasers into Co-Packaged Optics.

III. CONCLUSTION

A method to determine the impact of packaging-assembly-induced thermo-mechanical (TM) stress effects on the hybrid lasers during the packaging-assembly process was discussed. Particularly, the thermal budget for packaging was proposed.

IV. REFERENCES

1. Felipe Vallini, Karthik Narayanan, Christopher Helms, Wendai Wang, George Ghiurcan, Pierre Doussiere, Richard Jones, Isako Hoshino, Quan Tran, Kishore Kamath, "Reliability of III-V/Si heterogeneously integrated lasers," Proc. SPIE 13371, Silicon Photonics XX, 1337106 (20 March 2025); https://doi.org/10.1117/12.3043449.
2. Robert Blum, "Integrated silicon photonics for high-volume data center applications," Proc. SPIE 11286, Optical Interconnects XX, 112860M (28 February 2020) DOI: 10.1117/12.2550326.