intel foundry

Technology Brief

Foveros Direct 3D

Foveros Direct 3D revolutionizes chip integration for AI and HPC

Foveros Direct 3D advanced packaging technology uses ultra-high density interconnects via direct copper-to-copper bonding to enable increased performance.

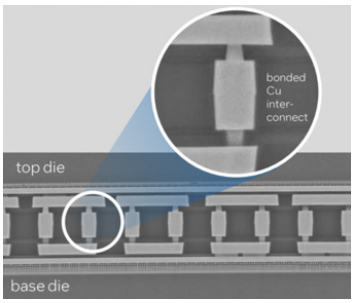

Figure 1. Foveros Direct 3D with advanced hybrid bonding interconnect.

Processor designs for artificial intelligence (AI) accelerators, high-performance computing (HPC), and advanced mobile applications demand maximum performance and power efficiency in compact designs. Available only on Intel Foundry process nodes, Foveros Direct 3D enables true vertical die stacking with unprecedented interconnect density — delivering improvements in bandwidth, power efficiency, and form factor.

This method builds on our Foveros 2.5 technology, which pioneered face-to-face (F2F) chip-on-chip bonding. Foveros Direct 3D takes it further by eliminating traditional solder microbumps used in die-to-die connections. By utilizing direct copper-to-copper hybrid bonding, Foveros Direct 3D achieves sub-10 micron (µm) pitch — up to 10x finer interconnect density compared to conventional microbump technologies.

Hybrid bonding combines mechanical interconnection and electrical conduction into a single process by bonding copper pads directly between dies. This creates a more robust interface by eliminating the resistance and parasitic effects of solder bumps while enabling far tighter pitch. These density improvements translate into orders of magnitude more interconnects per unit area, fundamentally changing what's possible in chip architecture and allowing more sophisticated heterogeneous integration designs.

Embedded Multi-die Interconnect Bridge (EMIB) enables even greater flexibility in product design when combined with Foveros 2.5D chip-on-chip bonding and Foveros Direct 3D hybrid bonding to make EMIB 3.5D. The hybrid architecture utilizes the vertically stacked chiplets of Foveros with the silicon-embedded bridge of EMIB to deliver an optimized balance of package size, compute performance, power usage, and cost savings.

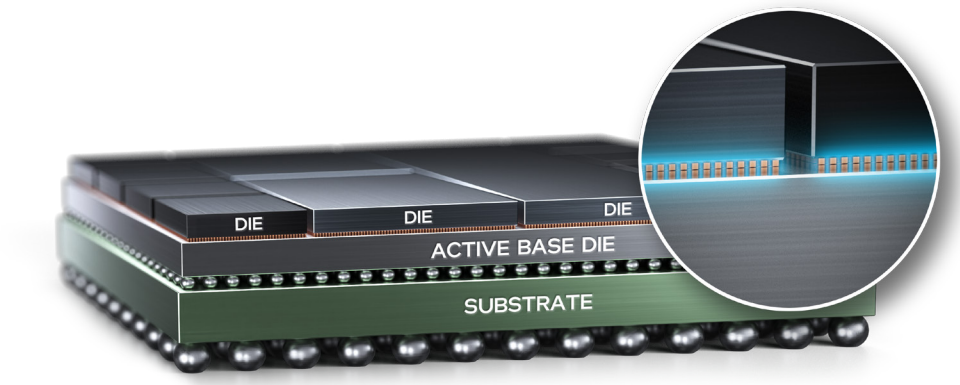

Figure 2. Foveros Direct 3D eliminates traditional solder microbumps, enabling direct copper-to-copper hybrid bonding between chiplets.

Enabling heterogeneous integration at scale

Using Foveros Direct 3D, you can integrate multiple intellectual property (IP) chiplets, memory technologies, and specialized compute elements in a true 3D stack — achieving system-level performance that far exceeds traditional 2D or 2.5D approaches.

Foveros Direct 3D offers the following key benefits:

1. **Performance optimization:** Dramatically reduces latency and improves bandwidth by minimizing signal path distances. The sub-10 µm pitch enables memory and logic to communicate with greater efficiency, critical for AI accelerators and data-intensive workloads.

2. **Enhanced thermal management:** Direct bonding creates continuous thermal paths between dies, enabling more efficient heat dissipation compared to traditional packaging approaches. This allows for higher power densities and better sustained performance in demanding applications.

3. **Space efficiency:** Achieves compact designs through vertical integration rather than horizontal spreading. This is valuable for mobile and edge computing applications where board space is at a premium.

4. **Cost-effective heterogeneous design:** Enables combining small specialized chiplets on advanced nodes with proven IP blocks on mature, cost-effective nodes. Each die can be manufactured on its optimal Intel Foundry process node and yielded independently, improving overall manufacturing economics.

5. **Scalability:** The technology supports multiple stacking levels and various die sizes, providing a scalable platform for future product generations and diverse application requirements.

Finding the right advanced packaging solution for your business

Foveros Direct 3D represents the most advanced technology in Intel Foundry's comprehensive packaging portfolio, complementing 2.5D technologies to address the full spectrum of integration challenges.

Intel Foundry offers a range of packaging solutions:

- **Foveros (S/R/B) 2.5D:** Side-by-side die placement with 36 µm microbump interconnects, utilizing silicon interposers or redistribution layer (RDL) technology for horizontal integration.
- **EMIB 2.5D:** The industry's first 2.5D interconnect solution using bridges embedded in the substrate.
- **EMIB 3.5D:** This hybrid design addresses the downsides of thermal warping, reticle size limits, and interconnect constraints.
- **Foveros Direct 3D:** True vertical die stacking with sub-10 µm hybrid bonding for maximum integration density and performance.

This portfolio is fully compatible with the Universal Chiplet Interconnect Express (UCIe) specification, enabling standardized die-to-die communication. As a founding member of UCIe, Intel Foundry ensures seamless integration of chiplets from multiple sources while leveraging the performance advantages of advanced packaging.

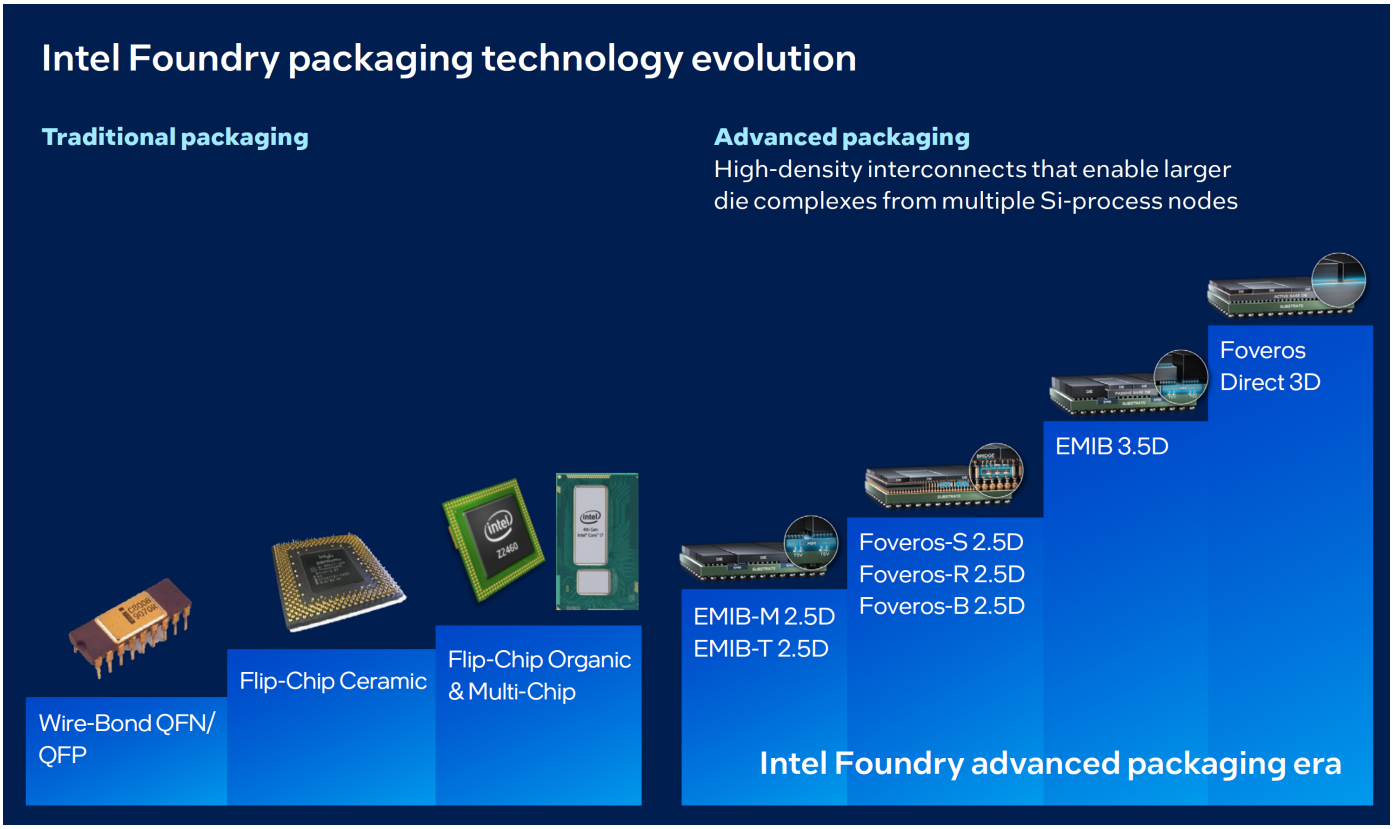

Figure 3. Evolution of Intel packaging technology, from traditional to advanced packaging.

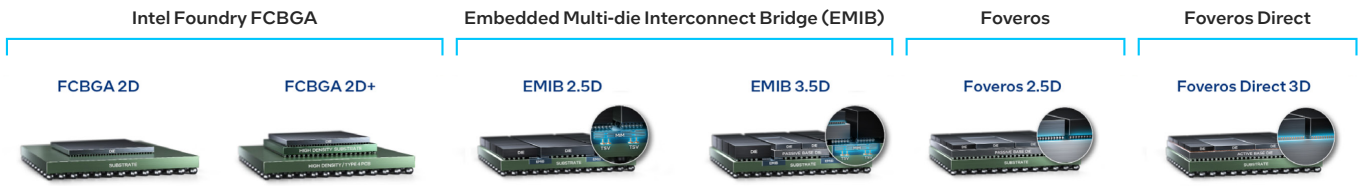

Figure 4. Intel Foundry's systems of chips advanced packaging.

About Intel Foundry Advanced System Assembly & Test

Intel Foundry Advanced System Assembly & Test (Intel Foundry ASAT) is a key industry innovator, with a robust portfolio of advanced packaging technologies, end-to-end data-forward testing services, and geographically diverse capacity to deliver your most complex silicon solutions with exceptional yields.

Start your journey with Intel Foundry

Intel Foundry offers full-stack solutions for accelerated time to market, leading the industry transition from "system on chip" to "systems of chips." As a pioneer in enabling disaggregated, chiplet-based solutions, Intel Foundry is not only advancing packaging technology but also driving die-to-die interface standards such as UCIe, which supports both asynchronous and synchronous communication methods.

A full suite of offerings supports Intel Foundry's process nodes and advanced packaging technologies. We deliver complex systems of chips that increase density and performance for AI accelerators and other demanding use cases. Intel Foundry also has services and ecosystem partners available to help with systems technology co-optimization (STCO), addressing broader system design needs.

To learn more about Intel Foundry, visit intel.com/foundry

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