intel foundry

Technology Brief

Foveros

Foveros 2.5D packaging technology enables complex chip designs

Foveros 2.5D advanced packaging technology enables more compact chip designs, with chip-on-chip bonding for interconnect density.

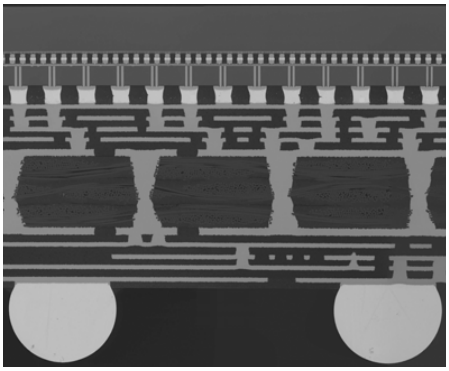

Figure 1. Foveros 2.5D advanced chip-on-wafer stacking technology in HVM.

Processor designs for increasing workloads must deliver performance and power efficiency in compact designs. Foveros 2.5D improves die density, so you can add more functionality without significantly increasing the footprint of the package.

Because you can layer advanced nodes on mature nodes, Foveros 2.5D enables more cost-effective chip designs, combining multiple types of dies based on your silicon requirements.

First introduced in 2019, Foveros 2.5D is an advanced die-stacking packaging process technology (see Figure 1). It incorporates two or more chiplets assembled together, and it comprises a passive base die with active die attached on top. The active die could be logic, memory, or a field-programmable gate array (FPGA). The base die is enabled with through-silicon via (TSV) technology and is also known as a silicon interposer.

A key feature of Foveros 2.5D is face-to-face (F2F) chip-on-chip bonding through an extremely fine microbump pitch of 36 µm (see Figure 2). F2F bonding delivers the interconnect density and lower wire parasitics required in today's high-performance chip designs. Wire parasitics are electrical properties such as resistance, capacitance, and inductance that impair performance and arise due to the physical layout of interconnects.

The benefits of Foveros 2.5D chip-on-chip bonding are amplified when complemented with Embedded Multi-die Interconnect Bridge (EMIB). These two technologies are combined to make EMIB 3.5D, which can address even more complex packaging needs. The EMIB connects passive dies to each other to help expand the reticle limit.

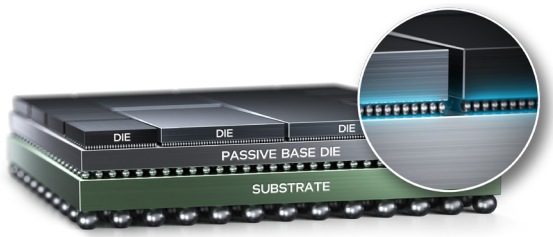

Figure 2. Foveros-S 2.5D provides an extremely fine microbump pitch of 36 µm, enabling face-to-face chip-on-chip bonding.

Enabling a package of heterogeneous chiplets

Using Foveros 2.5D packaging, you can mix and match different intellectual property (IP) chiplets with various memory and input/output (I/O) device elements—all in a small physical package, for significantly reduced board size.

Our 2.5D packaging approach has three key benefits:

1. It reduces latency and improves overall performance by minimizing the distance signals need to travel between components.
2. It helps optimize space with more compact designs, achieved by stacking components rather than spreading them horizontally.
3. It can potentially reduce manufacturing costs by using small specialized dies on advanced nodes while reusing proven IP blocks on mature nodes improves yields.

Discover the range of Foveros 2.5D solutions

Intel Foundry offers a range of Foveros 2.5D packaging solutions:

- **Foveros-S 2.5D** places multiple chips side-by-side on a silicon interposer that acts as the interconnect bridge. This approach improves performance and power efficiency compared to traditional packaging methods that do not involve vertical stacking of dies.
- **Foveros-R 2.5D** helps you optimize for cost and interconnect density. This solution has no interposer, uses fanout with redistribution layer (RDL), and can enable flexible heterogeneous systems with up to three RDLs.
- **Foveros-B 2.5D** can apply active and passive silicon bridges combined with RDLs for solutions requiring multiple base die chiplets. Future designs can include cache disaggregation, Integrated Voltage Regulator (IVR), or Metal Insulator Metal (MIM).

The portfolio of Foveros (S/R/B) 2.5D advanced packaging configurations is compatible with the UCIe specification. UCIe is an open industry-standard interconnect technology that makes high-density integration of chips from various sources possible, such as from different IP vendors or manufacturers. As a founding member of UCIe, Intel Foundry is committed to helping you access all the advantages of advanced packaging with UCIe. Foveros 2.5D makes full use of UCIe to improve energy efficiency and increase bandwidth.

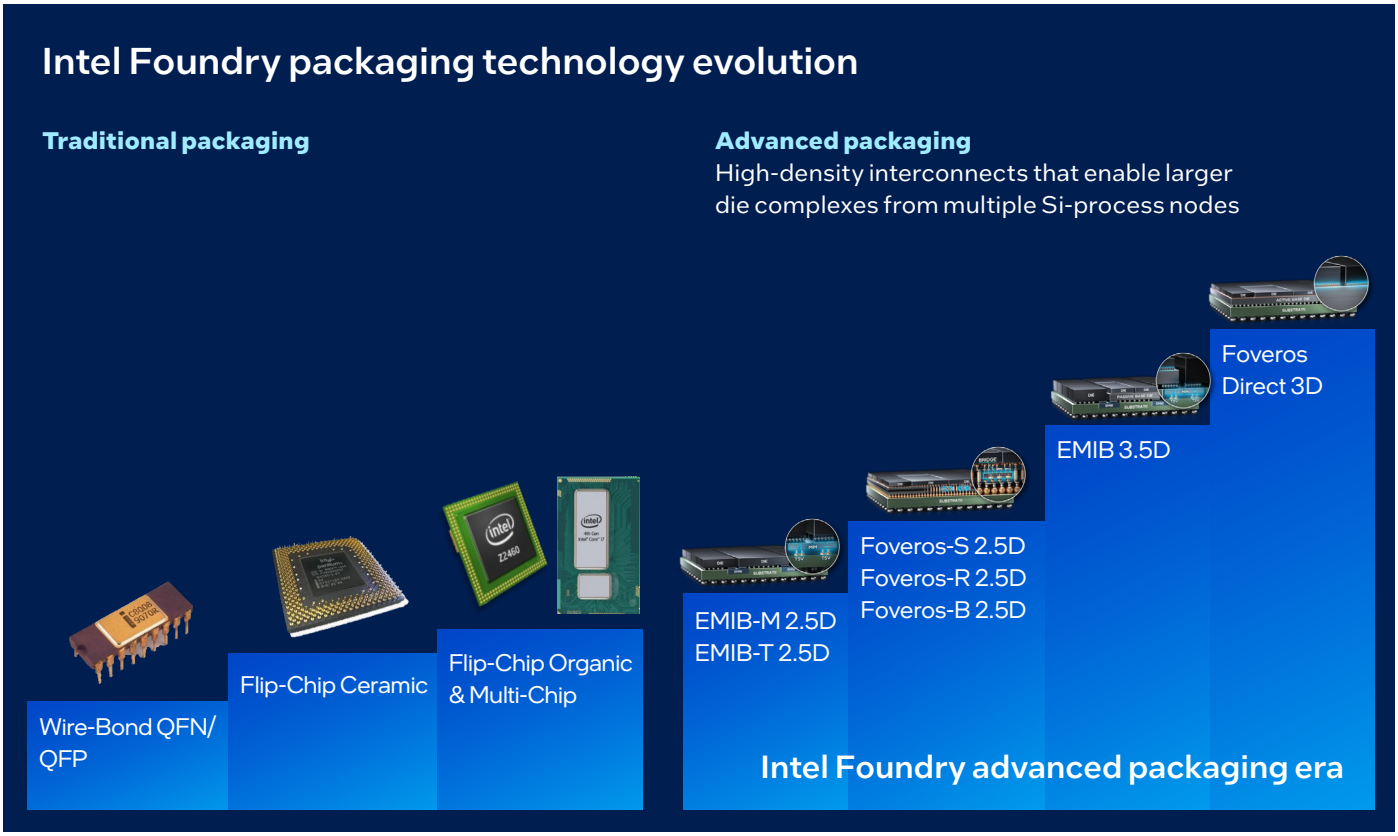

Figure 3. The Intel packaging technology revolution, from traditional to advanced packaging.

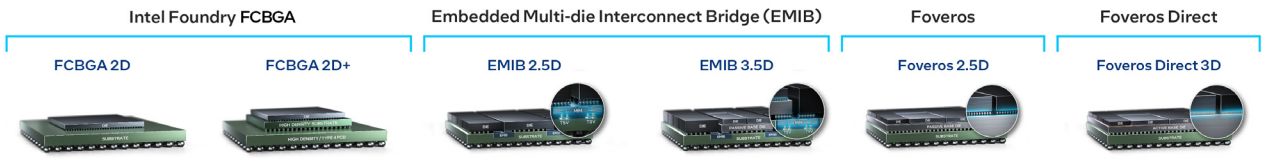

Figure 4. System of chips advanced packaging.

About Intel Foundry Advanced System Assembly & Test

Intel Foundry Advanced System Assembly & Test (Intel Foundry ASAT) is a key industry innovator, with a robust portfolio of advanced packaging technologies, end-to-end data-forward testing services, and geographically diverse capacity to deliver your most complex silicon solutions with exceptional yields.

Start your journey with Intel Foundry

Intel Foundry offers full-stack solutions for accelerated time to market, leading the industry transition from "system on chip" to "systems of chips." As a pioneer in enabling disaggregated, chiplet-based solutions, Intel Foundry is not only advancing packaging technology but also driving die-to-die interface standards such as UCIe, which supports both asynchronous and synchronous communication methods. A full suite of offerings supports Intel Foundry's process nodes and advanced packaging technologies. We deliver complex systems of chips that increase density and performance for AI accelerators and other demanding use cases. Intel Foundry also has services and ecosystem partners available to help with systems technology co-optimization (STCO), addressing broader system design needs.

To learn more about Intel Foundry, visit intel.com/foundry

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