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Technology Brief

EMIB

Embedded Multi-die Interconnect Bridge (EMIB) revolutionizes chip packaging interconnect technology

Discover how EMIB delivers high-bandwidth communications when integrating multiple dies (chips) into a single package.

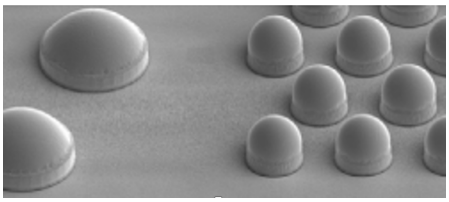

Figure 1. Embedded Multi-die Interconnect Bridge (EMIB) requires a tight microbump pitch at the bridge, but the rest of the die-core region can have a loose pitch.

Advanced applications, such as AI, machine learning (ML), and high-performance computing (HPC), require high data throughput and low latency. Embedded Multi-die Interconnect Bridge (EMIB) improves semiconductor designs' performance, power efficiency, and flexibility. EMIB enables you to integrate more components as needed, making it easier to scale up performance and functionality without complete system redesigns.

EMIB is the industry's first 2.5D interconnect solution using bridges embedded in the substrate. In high-volume manufacturing since 2017, EMIB features in products used in the server, network and HPC segments.

The EMIB process uses standard semiconductor package-assembly flows, with the only difference being the manufacturing of the substrate. EMIB places bridges in the substrate cavity where they are held in place with adhesives. The process adds dielectric and metal build-up layers.

Combining two different bump pitches on the die enables cost-efficient heterogeneous integration and scaling for very large complexes. EMIB requires a tight microbump pitch at the bridge only, which allows the rest of the die-core region to retain a loose pitch, as shown in Figure 1.

Why choose EMIB?

As shown in Figure 2, EMIB uses a very small bridge die with multiple routing layers, instead of the large silicon interposer typically used in other approaches that embed multiple routing layers in an organic substrate.

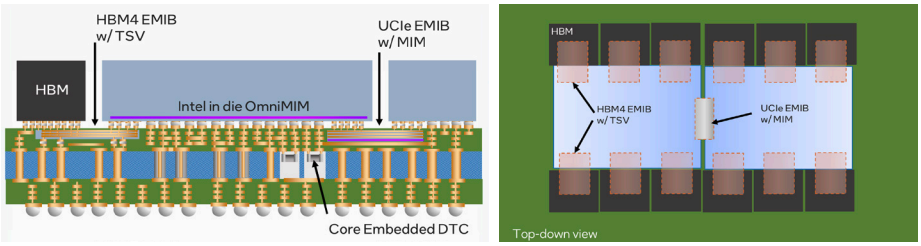

Figure 2. Overview of Embedded Multi-die Interconnect Bridge (EMIB) construction.

The small footprint of EMIB means that the balance of the input/output (I/O) signal and the power-integrity characteristics are unaffected. This contrasts with a full silicon interposer, which requires all signal and power vias to traverse through the interposer.

As the demand for improved power delivery has increased, Intel Foundry has expanded the EMIB portfolio. EMIB-M incorporates Metal Insulator Metal (MIM) capacitors into the silicon bridges to enhance power delivery. The demand for high-bandwidth memory (HBM) has increased the need for vertical power delivery with minimal DC and AC noise. To respond to this, Intel Foundry has added through-silicon vias (TSVs) to the EMIB-T solution. This architecture also enables design conversion from other packaging technologies.

A locally embedded bridge offers more cost-effective options for solutions requiring logic-logic and logic–HBM communication, providing the flexibility to select the right bridge type for different interconnects.

EMIB designs are used in high-volume manufacturing, using both Intel and external silicon. They achieve assembly yields comparable to a standard flip chip ball grid array (FCBGA) of equal complexity.

EMIB has three key benefits:

- It enables large, heterogeneous die complexes with highly customizable layouts.
- It supports high-data-rate signaling between adjacent dies while using simple driver/receiver circuitry.
- It allows optimizing each die-to-die link individually by customizing the bridge for each link.

Adding Foveros to create EMIB 3.5D

EMIB enables even greater flexibility in product design when used with Foveros 2.5D and Foveros Direct 3D to make EMIB 3.5D, as shown in Figure 3.

EMIB 3.5D is a hybrid design that combines EMIB with the Foveros advanced die-stacking packaging process technology in a single package. The hybrid architecture utilizes the vertically stacked chiplets of Foveros with the silicon-embedded bridge of EMIB to deliver an optimized balance of package size, compute performance, power usage, and cost savings. EMIB 3.5D addresses the downsides of thermal warping, reticle size limits, and interconnect constraints, enabling a significantly expanded surface area of silicon for building highly complex systems of chips.

Figure 3. The Intel packaging technology revolution, from traditional to advanced packaging.

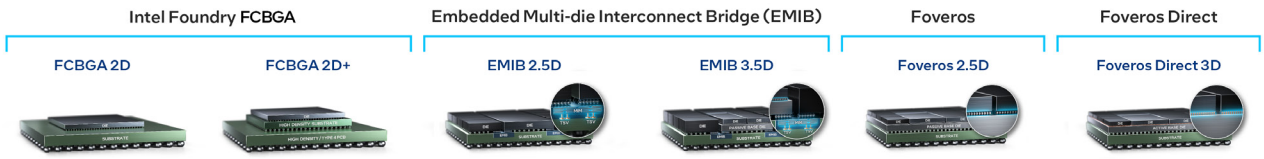

Figure 4. System of chips advanced packaging.

About Intel Foundry Advanced System Assembly & Test

Intel Foundry Advanced System Assembly & Test (Intel Foundry ASAT) is a key industry innovator, with a robust portfolio of advanced packaging technologies, end-to-end data-forward testing services, and geographically diverse capacity to deliver your most complex silicon solutions with exceptional yields.

Start your journey with Intel Foundry

Intel Foundry offers full-stack solutions for accelerated time to market, leading the industry transition from "system on chip" to "systems of chips." As a pioneer in enabling disaggregated, chiplet-based solutions, Intel Foundry is not only advancing packaging technology but also driving die-to-die interface standards such as UCIe, which supports both asynchronous and synchronous communication methods. A full suite of offerings supports Intel Foundry's process nodes and advanced packaging technologies. We deliver complex systems of chips that increase density and performance for AI accelerators and other demanding use cases. Intel Foundry also has services and ecosystem partners available to help with systems technology co-optimization (STCO), addressing broader system design needs.

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