Investor Meeting 2022

intel

Investor Meeting 2022

Technology Development

Dr. Ann Kelleher

Executive Vice President and General Manager
Technology Development

intel

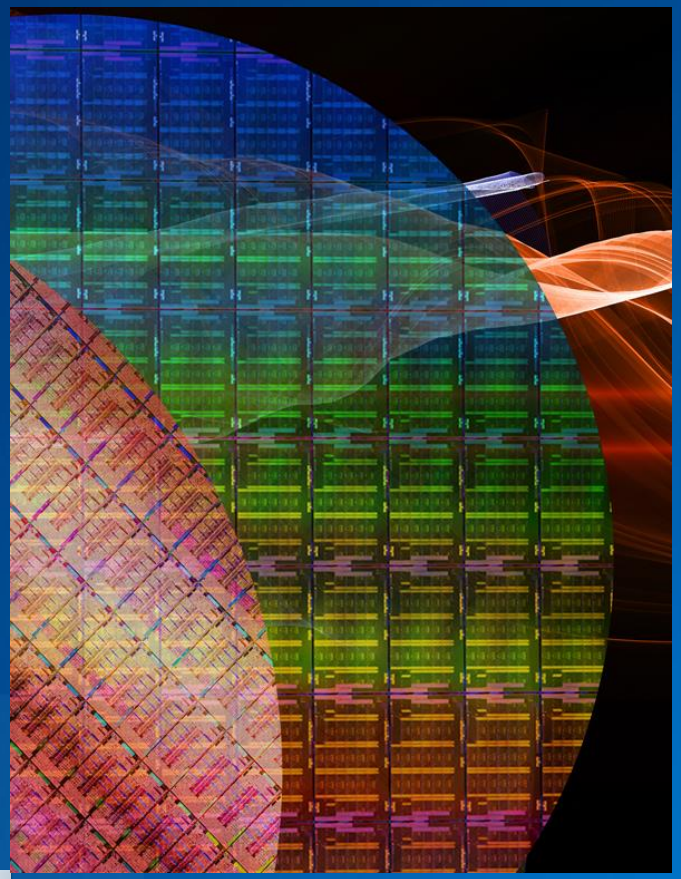
Notices and Disclaimers

Future node performance and other metrics, including power and density, are projections and are inherently uncertain and, in the case of other industry nodes, are derived from or estimated based on publicly available information. Intel's node numbers do not represent the actual dimension of any physical feature on a transistor or structure. They also do not pinpoint a specific level of improvement in performance, power or area, and the magnitude of a decrease from one node number to the next is not necessarily proportionate to the level of improvement in one or more metrics. Historically, new Intel node numbers were based solely on improvements in area/density; now, node numbers generally reflect a holistic assessment of improvement across metrics and can be based on improvement in one or more of performance, power, area, or other important factors, or a combination, and will not necessarily be based on area/density improvement alone.

Statements in this presentation contain forward-looking statements relating to Intel's business outlook, future plans and expectations, including with respect to Intel's process and packaging technology roadmap and schedules; innovation cadence; future technology, services, and products and the expected benefits and availability of such technologies, services, and products, including PowerVia and RibbonFET technologies, future process nodes, and other technologies and products; future use of EUV and other manufacturing tools and technologies; expectations regarding suppliers, partners, and customers; Intel's strategy and its anticipated benefits; product and manufacturing plans, goals, timelines, ramps, progress, and future product and process leadership and performance; future manufacturing capacity; manufacturing expansion and investment plans; plans and goals related to Intel's foundry business; business plans; financial projections and expectations; total addressable market (TAM) and market opportunity; future economic conditions; future impacts of the COVID-19 pandemic; future legislation; future capital offsets; pending or future transactions; the proposed Mobileye IPO; supply expectations including regarding industry shortages; future external foundry usage; expectations regarding customers, including designs, wins, orders, and partnerships; projections regarding competitors; ESG goals; and anticipated trends in our businesses or the markets relevant to them, including future demand, market share, industry growth, and technology trends. Such statements involve a number of risks and uncertainties. Words such as "anticipates," "expects," "intends," "goals," "plans," "believes," "seeks," "estimates," "commits," "continues," "may," "will," "would," "should," "could," "strategy," "progress," "path," "positioned," "ramp," "momentum," "accelerate," "on-track," "roadmap," "pipeline," "cadence," "schedule," "forecast," "likely," "guide," "potential," "next gen," "future," and "deliver" and variations of such words and similar expressions are intended to identify forward-looking statements. Statements that refer to or are based on estimates, forecasts, projections, and uncertain events or assumptions also identify forward-looking statements. Such statements involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in these forward-looking statements. Important factors that could cause actual results to differ materially from the company's expectations include, among others, Intel's failure to realize the anticipated benefits of its strategy and plans; changes in plans due to business, economic, or other factors; actions taken by competitors, including changes in competitor technology roadmaps; changes impacting our projections regarding our technology or competing technology; delays in development or implementation of our future manufacturing technologies or failures to realize the anticipated benefits of such technologies, including expected improvements in performance and other factors; delays or changes in the design or introduction of future products; changes in customer needs and technology trends; our ability to rapidly respond to technological developments; delays, changes in plans, or other disruptions involving manufacturing tool and other suppliers; and other factors set forth in Intel's earnings release dated January 26, 2022, which is included as an exhibit to Intel's Form 8-K furnished with the Securities and Exchange Commission (SEC) on such date, and in Intel's other reports filed or furnished with the SEC, including the company's most recent reports on Forms 10-K and 10-Q. Copies of Intel's SEC filings may be obtained by visiting our Investor Relations website at www.intc.com or the SEC's website at www.sec.gov. All information in this presentation reflects management's views as of February 17, 2022, unless an earlier date is indicated. Intel does not undertake, and expressly disclaims any duty, to update any statement made in this presentation, whether as a result of new information, new developments or otherwise, except to the extent that disclosure may be required by law.

Intel technologies may require enabled hardware, software or service activation. No product or component can be absolutely secure. Your costs and results may vary. Product and process performance varies by use, configuration and other factors. Learn more at www.Intel.com/PerformanceIndex and www.Intel.com/ProcessInnovation. Future product and process performance and other metrics are projections and are inherently uncertain.

Key Takeaways



Process

We expect to reach performance per watt parity in 2024 and leadership in 2025

Packaging

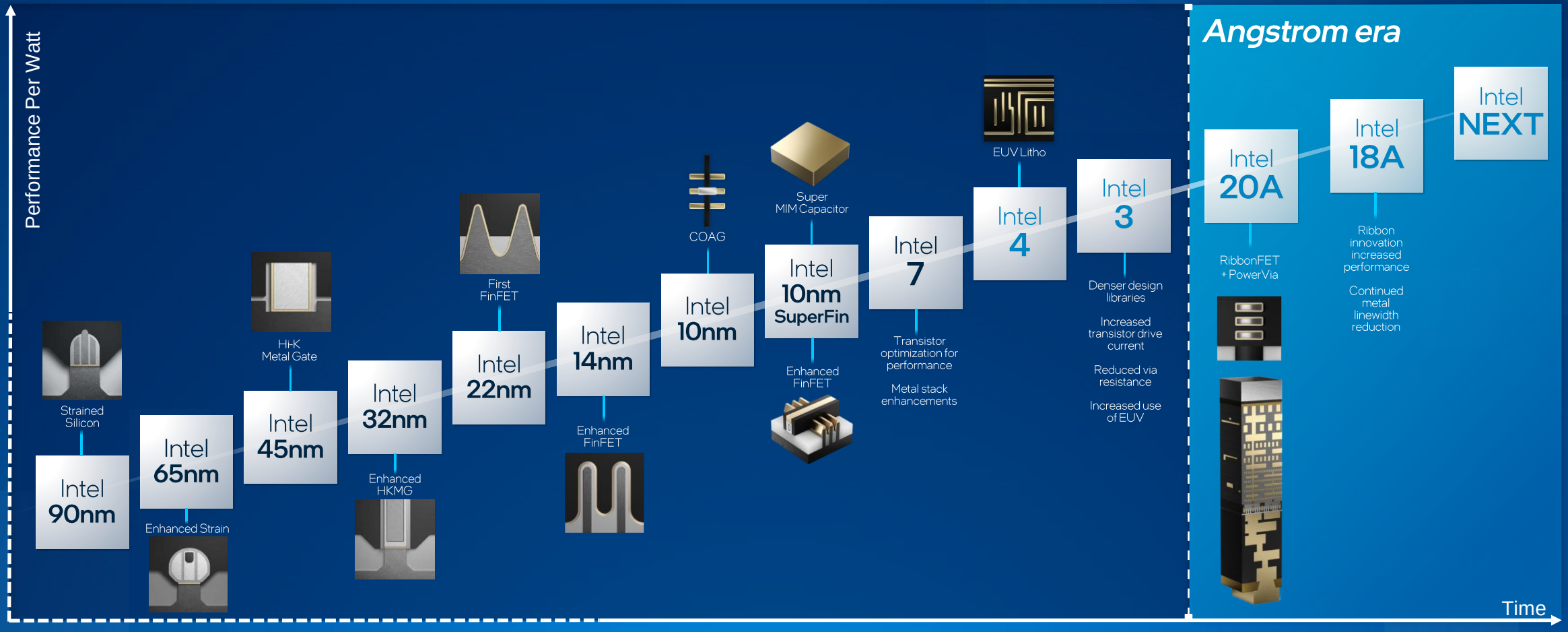
We deliver leadership packaging for our products and our foundry customers' products

Innovation

Moore's Law is about innovation and innovation continues unabated

Process Technology

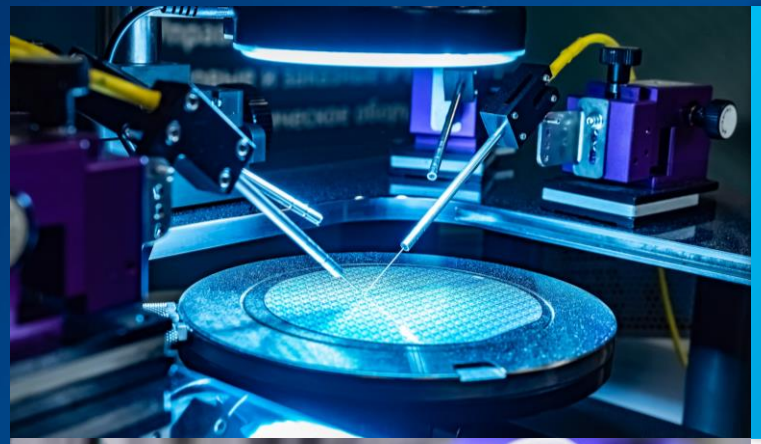
Intel Process Technology



Every major transistor innovation in the past 20 years delivered by Intel and we are driving the next with RibbonFet & PowerVia

*Graphic is for illustrative purposes only and is not to scale

Added Focus



Predictable Execution

- Modular, incremental, parallel: “tick-tock” like
- Flow simplification
- Built-in contingencies

Innovation and Ecosystem

- Deep & active engagement with industry partners
  - equipment, materials, electronic design automation (EDA)
- Embracing industry best practices and standards

We added focus in key areas while investing ~$1.5B more in people & equipment

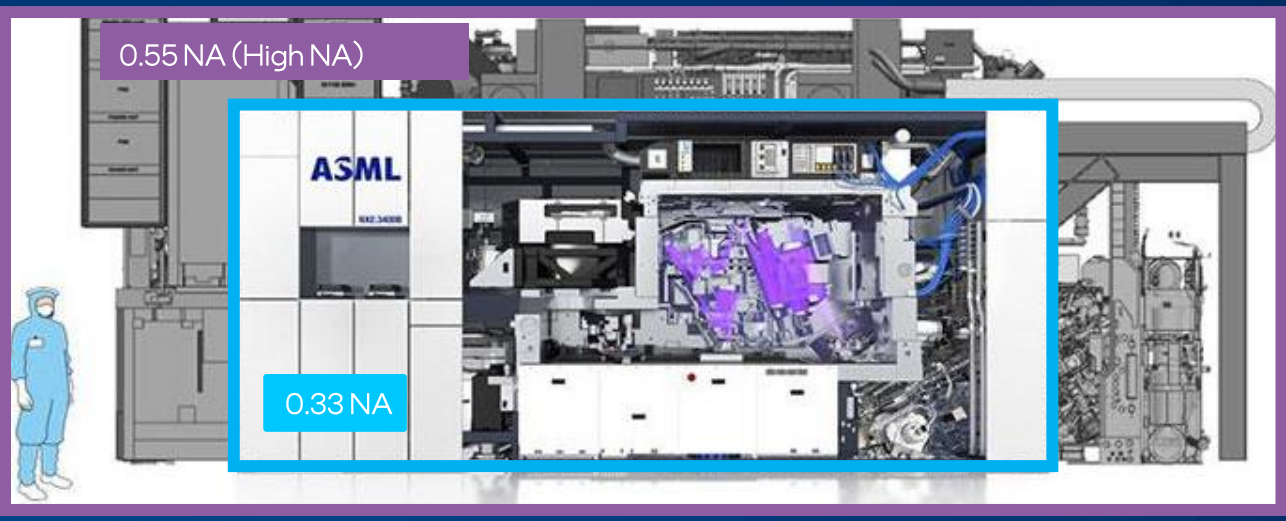
EUV Update

0.33 NA:
Plan of record for Intel 4, Intel 3, Intel 20A, Intel 18A

- NXE 3400C → NXE 3600D → NXE 3800E
- Direct print capability of >30nm pitch metal lines.

0.55 NA (High NA):
Next major generation of lithography

- EXE 5000 → EXE 5200
- Direct print capability of ≤ 30nm pitch metal lines
- Current intercept is 2025 for high volume manufacturing

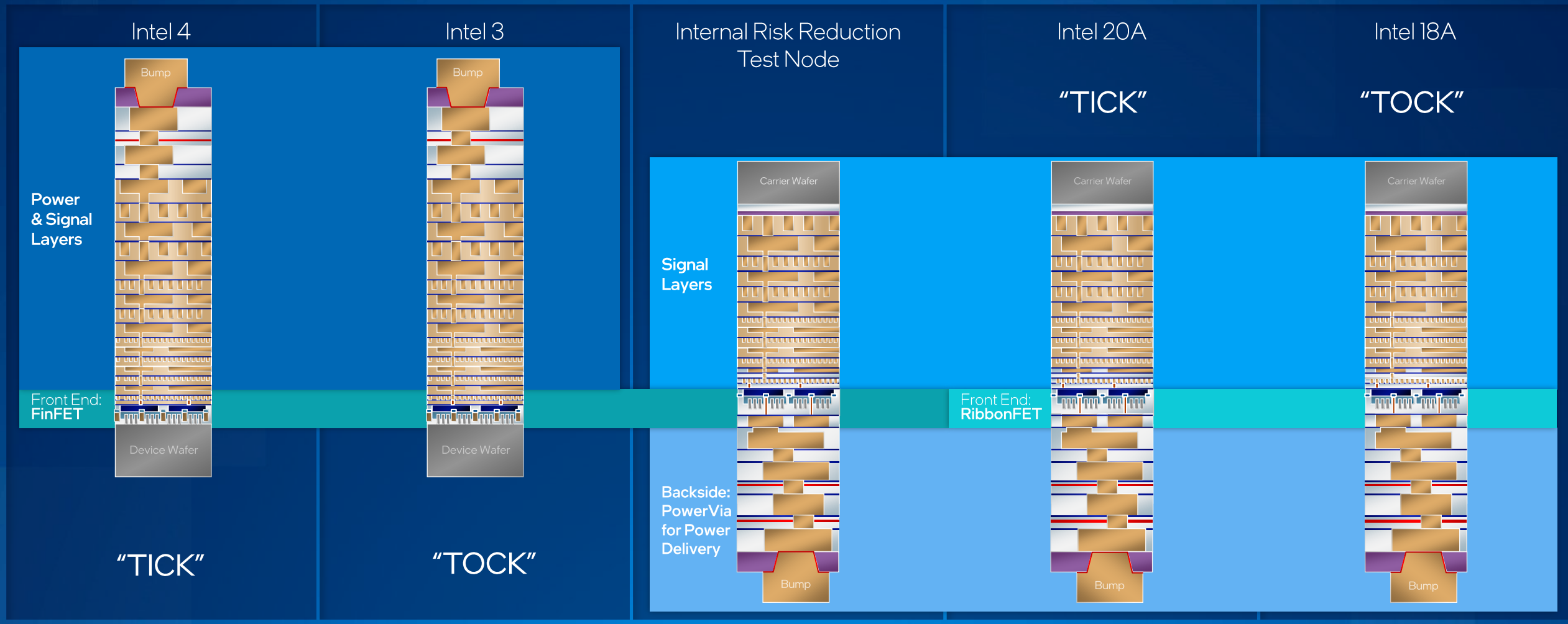


"Intel's vision and early commitment to ASML's High-NA EUV technology is proof of its relentless pursuit of Moore's Law."
Martin van den Brink, ASML President and CTO, January 2022

Committed to Lithography Leadership

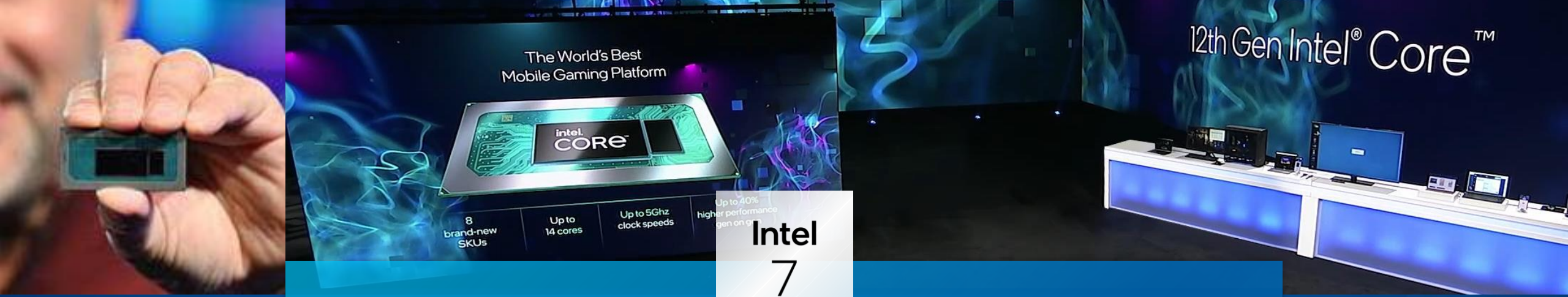
*images courtesy of ASML

Modular Design



Tick-tock + modular, parallel design increases learning and reduces risk

*Graphic is for illustrative purposes only and is not to scale



Intel 7

12th Gen Intel Core (Alder Lake) processors

client

- ~10% improvement in performance per watt
- More thick metal layers and MIMs, new lower-k dielectric
- Novel high-density patterning and thin barrier

Intel 7 now in production with the first product shipping in volume

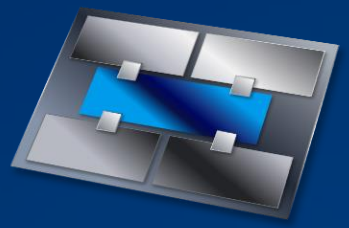
*Graphics for illustrative purposes only and is not to scale

Internal estimates, results may vary. Process readiness timing does not necessarily indicate product production timing. Learn more at www.intel.com/PerformanceIndex. Results may vary.

Intel 4

manufacturing ready **H2 2022**
select products shown

Meteor Lake
client



Custom ASIC
networking

- ~20% improvement in performance per watt
- First use of EUV; significant increase in density over Intel 7
- 2022: Meteor Lake CPU tile production stepping tape out (H2)

Intel 3

manufacturing ready **H2 2023**
select products shown

Future Xeon
data center

- ~18% improvement in performance per watt
- Higher performance library, optimized drive current & metal stack
- 2022: lead product test wafers running in fab (H2)

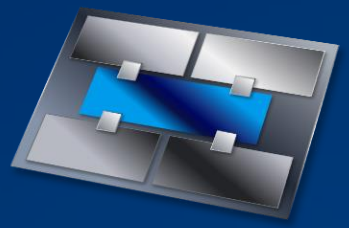
Our next generation FinFET processes are healthy and will be manufacturing ready on schedule

*Graphics for illustrative purposes only and is not to scale
Internal estimates, results may vary. Process readiness timing does not necessarily indicate product production timing. Learn more at www.intel.com/PerformanceIndex. Results may vary.

Intel 4

manufacturing ready **H2 2022**
select products shown

Meteor Lake
client



Custom ASIC
networking

- ~20% improvement in performance per watt
- First use of EUV; significant increase in density over Intel 7
- 2022: Meteor Lake CPU tile production stepping tape out (H2)

Intel 3

manufacturing ready **H2 2023**
select products shown

Future Xeon
data center

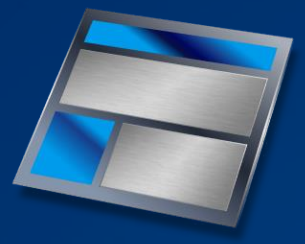
- ~18% improvement in performance per watt
- Higher performance library, optimized drive current & metal stack
- 2022: lead product test wafers running in fab (H2)

Our next generation FinFET processes are healthy and will be manufacturing ready on schedule

*Graphics for illustrative purposes only and is not to scale
Internal estimates, results may vary. Process readiness timing does not necessarily indicate product production timing. Learn more at www.intel.com/PerformanceIndex. Results may vary.

Intel 20A

manufacturing ready **H1 2024**
select products shown

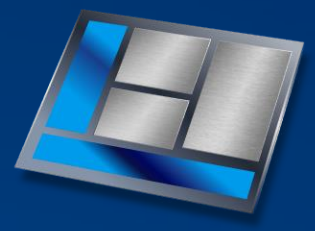


Future Product
client

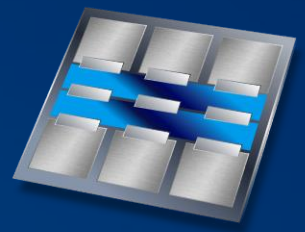
- Up to 15% improvement in performance per watt
- Introduction of RibbonFET & PowerVia
- 2022: IP test wafers running in fab (H2)

Intel 18A

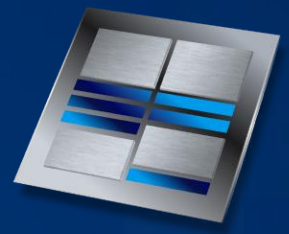
manufacturing ready **H2 2024**
select products shown



Future Product
client



Future Xeon
data center



Foundry Customer

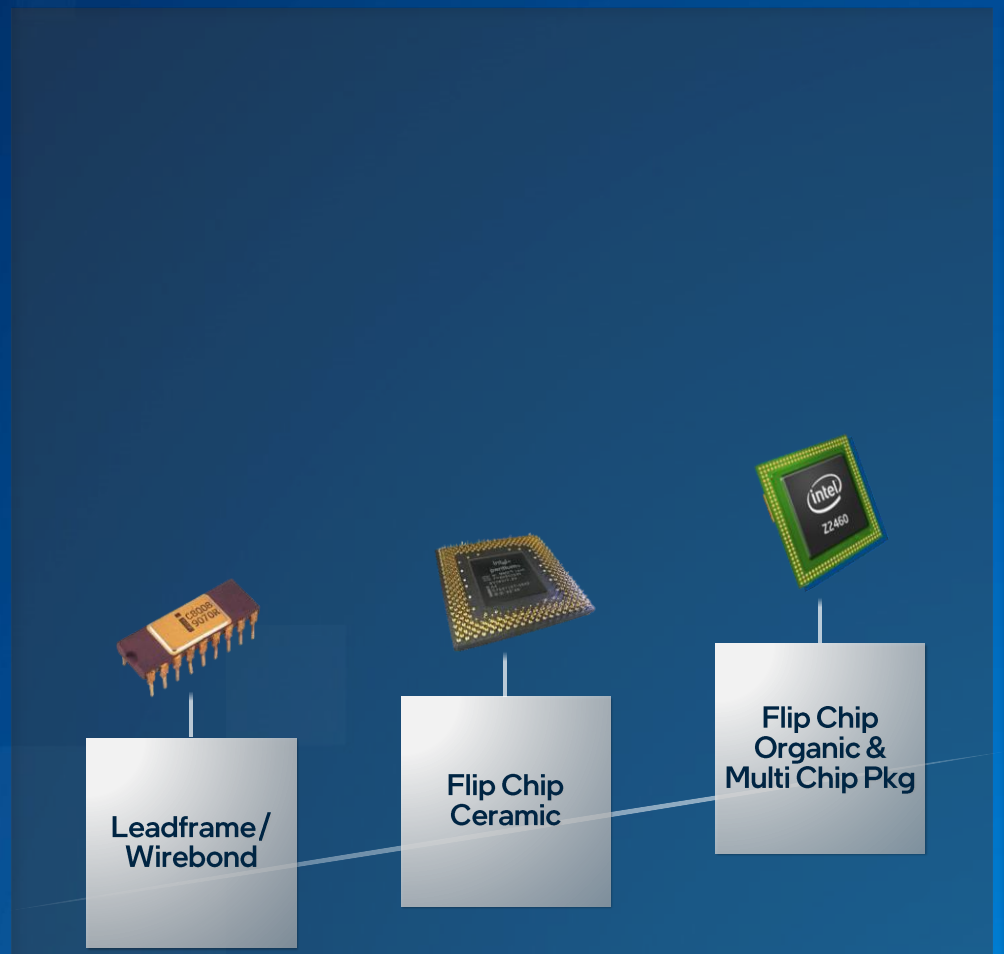
- Up to 10% improvement in performance per watt
- Ribbon innovation for design optimization, line width reduction
- 2022: foundry customers' test chips (H1); first IP shuttle (H2)

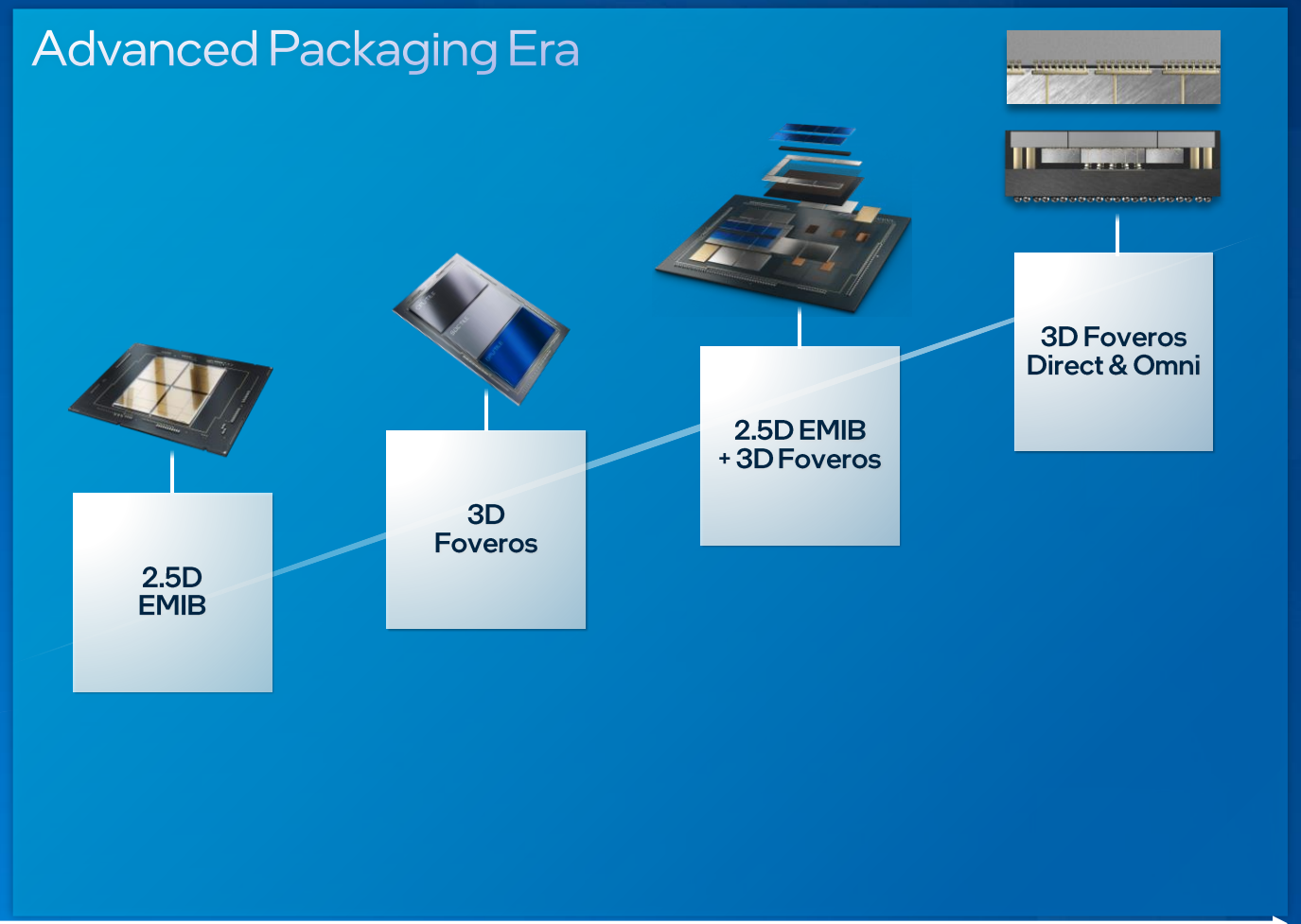
Our first generation RibbonFET with PowerVia processes are demonstrating early health and will be manufacturing ready on schedule

*Graphics for illustrative purposes only and is not to scale
Internal estimates, results may vary. Process readiness timing does not necessarily indicate product production timing. Learn more at www.intel.com/PerformanceIndex. Results may vary.


Packaging Technology

Intel Package Technology





Package main function: provide power and signaling from motherboard to die

Added Package value: high density interconnects that enable larger die complexes from multiple process nodes

*Graphic is for illustrative purposes only and is not to scale

What does packaging leadership mean?

Die to Die Interconnects - 2D, 2.5D, 3D
Large packages, large die complexes, TSV scaling, mixed top and base

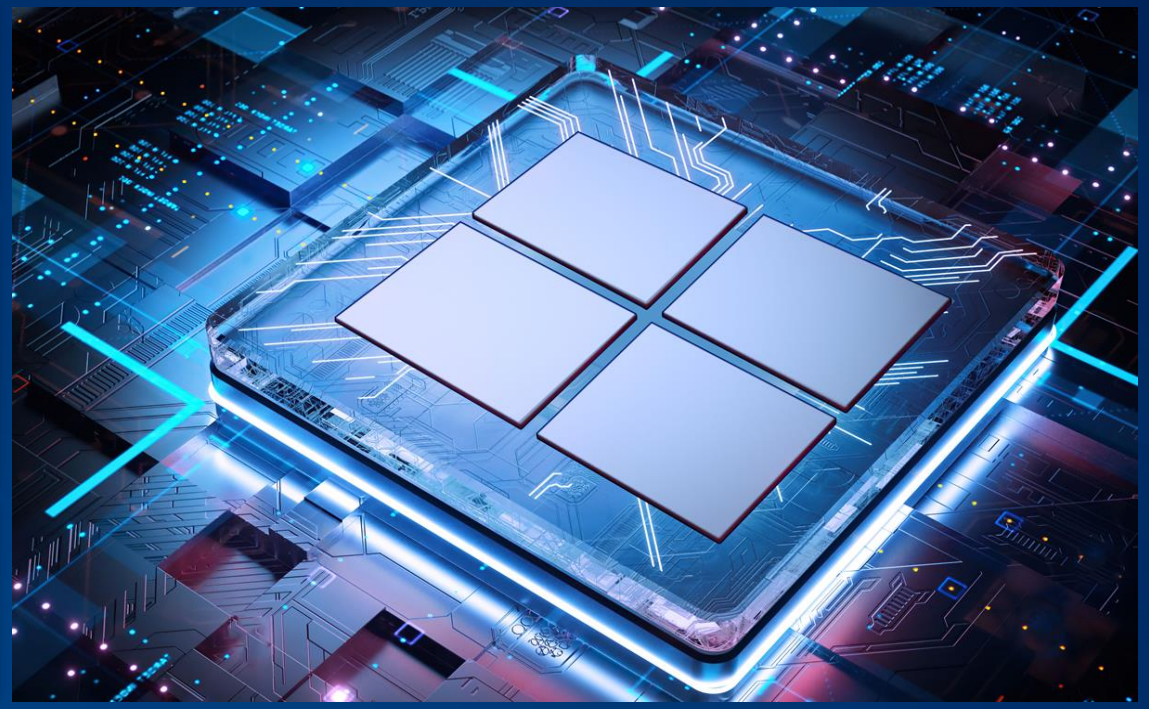
Thermals

Power Delivery

High Speed Signaling / Optical

Power & Performance

Advanced Sort & Test Capabilities
Known good die test capability for packages with many die



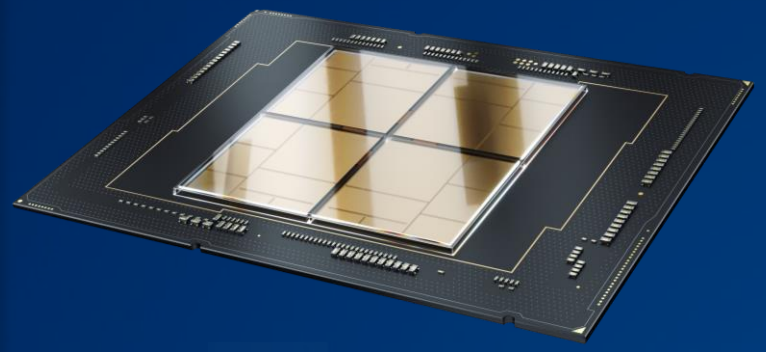
Everything at high yield, high volume, and high reliability

Leadership in packaging

provides multiple technology choices, validated in high volume,
for designers and architects to build leadership products

2022 Packaging Leadership

EMIB 55um
with Sapphire Rapids

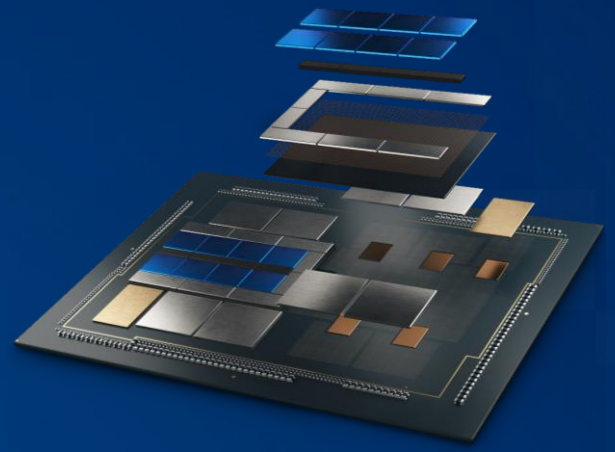


Projected to be the highest volume advanced packaging product ever in the data center

Next Gen Foveros 36um
with Meteor Lake

Projected to ship 100's of millions of units in its lifetime

EMIB 55um + Foveros 36um
with Ponte Vecchio



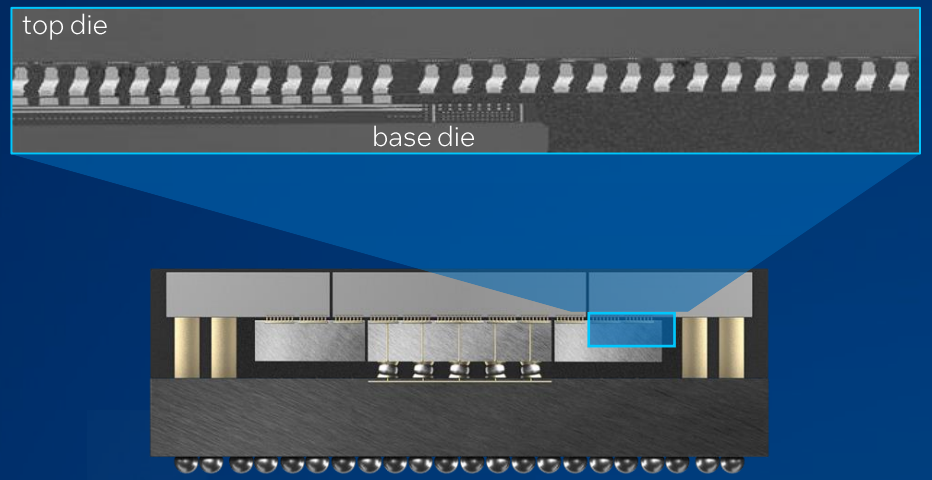
Shipping this year - the most advanced package in history

*Graphics for illustrative purposes only and is not to scale. Learn more at www.intel.com/PerformanceIndex. Results may vary.

Future Leadership

Foveros Omni

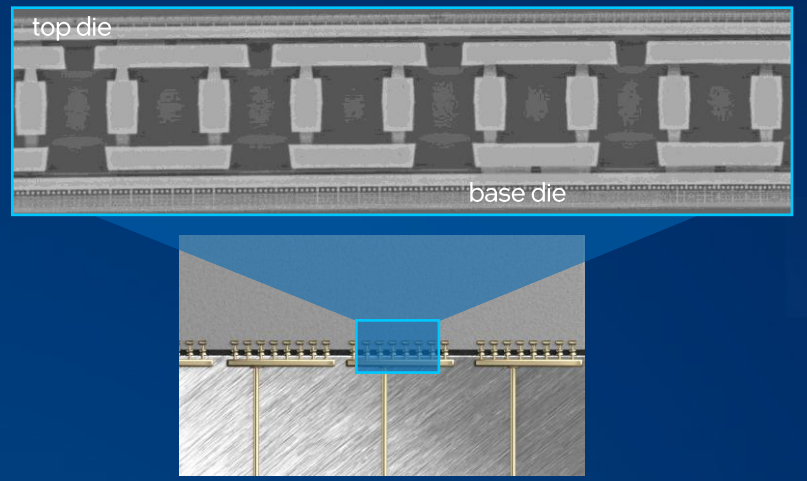
manufacturing ready **H2 2023**



- ‘Mix and match’ chiplets in base die complex
- 4x higher interconnect bump density vs EMIB

Foveros Direct

manufacturing ready **H2 2023**



- >10x higher interconnect bump density vs Foveros
- Higher bandwidth at lower latency, power, and die area

The era of advanced packaging allows us to combine our expertise in wafer processing and packaging

*Graphics for illustrative purposes only and is not to scale

Internal estimates, results may vary. Package readiness timing does not necessarily indicate product production timing. Learn more at www.intel.com/PerformanceIndex. Results may vary.

The Stewards of Moore's Law

Multiple paths of innovation enabling Moore's Law

Essential Technologies, New Capabilities, New Concepts

Transistors RibbonFET, stacked CMOS, 2D materials

Power Delivery PowerVIA, GaN-based power switch

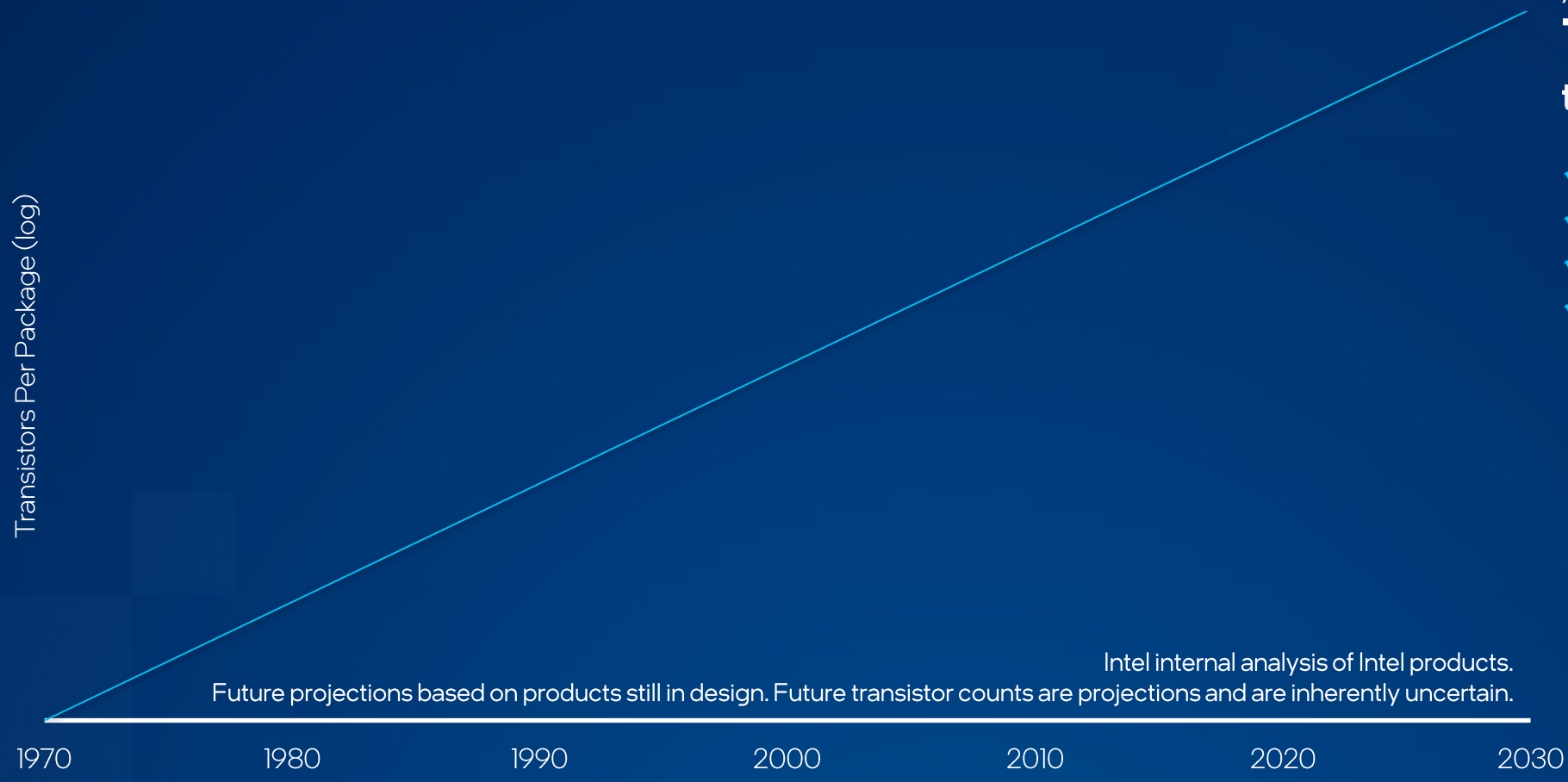
Lithography High NA, Directed Self Assembly

Packaging Foveros Omni, Foveros Direct, Interconnect density improvements

Quantum Magneto-Electric Spin-Orbit Device, SiMOS & Si / SiGe

A rich portfolio of future innovation in multiple areas delivering Moore's Law

Moore's Law



Intel internal analysis of Intel products.
Future projections based on products still in design. Future transistor counts are projections and are inherently uncertain.

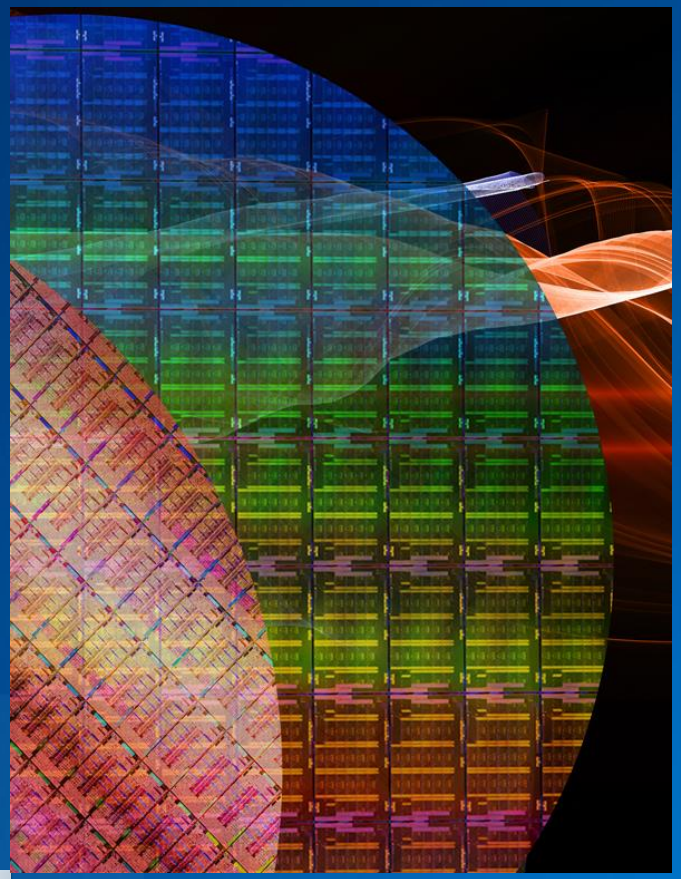
Aspiring to
1 Trillion
transistors in 2030

- ✓ RibbonFET
- ✓ PowerVia
- ✓ High NA
- ✓ 2.5 / 3D packaging

Moore's Law continues

when combining the power of processing and packaging innovation

Summary



Process

We expect to reach performance per watt parity in 2024 and leadership in 2025

Packaging

We deliver leadership packaging for our products and our foundry customers' products

Innovation

Moore's Law is about innovation and innovation continues unabated


intel