White Paper

FPGAs and SoCs

Intel Agilex® 5 FPGAs and SoC FPGAs Are Ideal for Midrange Applications Requiring Higher Performance, Lower Power, and Smaller Form Factors

Continuing the innovation that started with Intel Agilex® 7 FPGAs

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Executive Summary

Rapid transformation across diverse markets—from edge to core to data center—requires solution providers, application developers, industries, and businesses to deliver massive innovation at unprecedented speed. This is evident at the edge as embedded devices are expected to deliver near-real-time, actionable intelligence; in the network core, with network function virtualization (NFV) to aggregate and process massive amounts of data; and in data centers grappling with increasing analytics, memory, and storage requirements. Essentially, data is inundating infrastructure at each critical point from edge to core to data center. The rate of change reinforces the need for flexibility as all market sectors seek to structure and process this data.

Computationally intensive workloads—for example, workloads that employ artificial intelligence (AI) and machine learning (ML) algorithms—are increasingly migrating out from data centers to the network's edge, where localized concurrent processing and analysis are needed to meet demanding, system-level latency requirements. At the same time, power is more constrained in many embedded and edge applications, which means the implementation technology employed must be power efficient while providing the required performance attributes.

In 2019, Intel Introduced the Intel Agilex® 7 FPGAs and SoC FPGAs (formerly Intel Agilex FPGAs) to service the extreme capacity and performance requirements demanded by the network core and data centers. The first members of the Intel Agilex 7 device family, the F-Series and I-Series FPGAs, were built using (what was at that time) Intel's leading-edge 10 nm SuperFin process technology. In 2022, Intel introduced the Intel Agilex 7 FPGAs M-Series, which is built using the current leading-edge Intel 7 process technology. The M-Series FPGA expands upon F-Series and I-Series FPGA features by offering in-package high-bandwidth memory (HBM), interfaces for external DDR5 SDRAM, and a hard Network-on-Chip (NoC) to maximize memory bandwidth.

Following tremendous market acceptance of the Intel Agilex 7 device families, Intel continues to innovate by bringing the high-performance capabilities of Intel Agilex 7 devices into new mid-range Intel Agilex® 5 FPGAs and SoC FPGAs (Figure 1). All members of the new Intel Agilex 5 device family including performance-optimized D-Series and power-optimized E-Series devices are manufactured on Intel 7 technology, have a monolithic construction, and come in smaller sizes (both in terms of numbers of logic elements (LEs) and in terms of physical packages), which allows them to deliver the excellent performance per watt characteristics needed to meet embedded and edge application requirements.

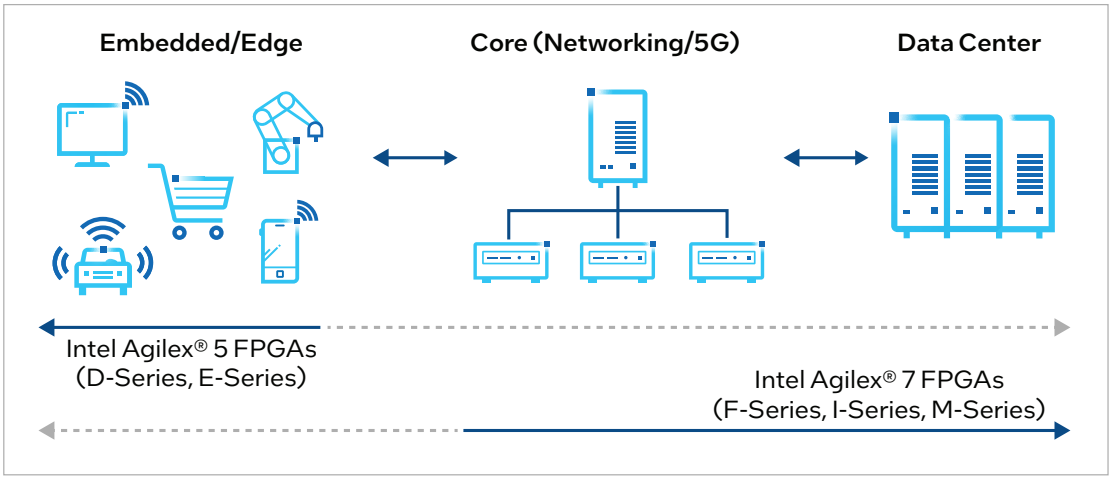

Figure 1. The Intel Agilex 5 device family is ideally suited for embedded and edge applications.

Embedded/Edge Challenges

With a wide range of businesses and industries tied to the Internet of Things (IoT), and the installed base of connected devices expected to reach nearly 31 billion by 2020, more and more data is being created, processed, and transmitted at the edge.[1] This brings an expectation that embedded devices at the network edge will be acting on structured and unstructured data and generating insight in near-real-time. Processing raw, unfiltered data, structuring it, and conducting deep learning inference at the edge demands new levels of performance, capacity, and flexibility.

Drowning in data

The world is becoming more digitized and connected every day, with vast amounts of new data being generated 24 hours a day, 7 days a week, and 365 days a year. There's a competitive imperative to analyze all this data to extract value from it and to produce actionable insights. We've entered the era of big data, which is a world that gets bigger and more complex by the minute. Having said this, companies currently analyze only 12% of the available data, according to a widely quoted Forrester Research paper.[2]

According to the IDC, 64.2 zettabytes (ZB) of data were created in 2020 and less than 2% of that data was saved or retained into 2021.[3] From 2020 to 2025, the IDC forecasts that new data will be created at a compound annual growth rate (CAGR) of 23%, resulting in approximately 175 ZB of annual data creation by 2025.[4] Clearly, there's more than enough data to analyze. What is needed are better, faster ways to analyze this data, to derive actionable insights, and to create additional value from these analyses. This data analysis demands increased agility and flexibility to handle the exploding diversity in data types and to implement new data-analysis algorithms and methods including artificial intelligence (AI) and machine learning (ML) techniques.

Requirement for safety and reliability

Functional Safety (FuSa) is defined as the absence of unreasonable risk due to hazards caused by malfunctioning behavior of Electrical and/or Electronic (E/E) systems. The mission of functional safety is to avoid that a failure in the electronic systems harm the human life. In particular, the objective of functional safety is freedom from unacceptable risk that can affect human lives directly or indirectly (e.g., chemical pollution). Functional safety copes with systematic failures (i.e., failures related to design bugs or manufacturing process, operational procedures, or documentation flaws) and random hardware failures (i.e., failures that can occur unpredictably during the lifetime of a hardware element and can be due to physical phenomena).

In FuSa standards based on the IEC 61508 standard, four safety integrity levels (SILs) are defined. SIL3 is the highest safety integrity level that is economically feasible for most industrial operations.

Need for flexible I/O

One aspect of embedded and edge-based systems is that they have to interface with a wide variety of sensors with various interface characteristics. Also, these systems tend to be composed of multiple silicon chips, including application processors (APs), each of which may employ different electrical interfaces and communications protocols.

All this results in a need for devices like FPGAs to provide high-speed general-purpose input/output (GPIO) banks with single-ended and differential I/O support for a variety of interface standards, high-voltage I/O banks that support interfaces to legacy devices, and high-speed SerDes transceivers that support a variety of serial interface standards including Ethernet and PCI Express (PCIe).

Demand for optimal power and performance

As embedded and edge developers expand their service offerings and solutions, there is a need for highly customizable processing of data wherever it is generated, processed, transported, or stored. Processing at this level requires specific functionality to achieve the optimal power and performance.

Because of their flexible nature and ability to implement nearly any sort of processing architecture, programmable logic devices, namely FPGAs, have been on the forefront of advanced data-processing systems for more than three decades. Along the journey, FPGAs accumulated several powerful capabilities such as fast on-chip memory, high-speed serial transceivers, and hardened intellectual property (IP) blocks including digital signal processing (DSP) functions, fast SDRAM memory controllers, and multi-core microprocessor system.

Introducing Intel Agilex 5 FPGAs and SoC FPGAs

The first Intel Agilex 7 FPGA and SoC families were presented to the market in early 2019. Back then, EE Journal's Founder and Editor-in-Chief Kevin Morris wrote, "Intel Agilex® is a milestone in the evolution of FPGA technology, and it brings substantial new capabilities to the party."5 The market quickly realized the advantages of those new capabilities, which have made Intel Agilex 7 devices extremely successful. Expanding this evolutionary architecture into additional markets—where power efficiency (performance per watt) and smaller packaged device size are just as important as raw performance—inspired the development of the Intel Agilex 5 device family.

Intel Agilex 5 devices incorporate many new features such as an upgraded hard processor system (HPS), Enhanced DSP with AI Tensor Block, MIPI I/O support, and a hardened Time Sensitive Networking (TSN) controller. These features make Intel Agilex 5 devices ideal for midrange FPGA applications requiring performance, lower power, and smaller board level footprints.

Intel has taken advantage of its in-house manufacturing capabilities for the Intel Agilex 5 device family to provide lower logic densities, lower power consumption, and smaller form factors than were previously available. Intel Agilex 5 devices are manufactured using Intel 7 technology, which is the same leading-edge process Intel uses to manufacture central processing units (CPUs), including the 12th generation Intel® Core™ processors and the 4th generation Intel® Xeon® Scalable processors.

Intel Agilex 5 FPGAs and SoC FPGAs inherit many strong and proven architectural features from the initial Intel Agilex 7 device families, including the second-generation Intel® Hyperflex™ FPGA Architecture and SmartVID power-management technology that significantly improve performance and reduce power consumption within the programmable-logic fabric. Intel 7 technology permits Intel to create programmable-logic devices that integrate fast input/output (I/O) circuits—including 28 Gbps transceivers and flexible general-purpose I/O banks—along with programmable logic and hardened IP blocks, all on one monolithic silicon die. A further advantage of Intel 7 technology is that it allows the Intel Agilex 5 devices to have both high-speed I/O banks and high-voltage I/O banks that can support 3.3 V operation. These capabilities help Intel Agilex 5 devices provide excellent power-efficient performance while offering lower densities and smaller package options.

In addition, Intel Agilex 5 devices incorporate several hard IP blocks that are new to the Intel Agilex device family, including an Enhanced DSP with AI Tensor Block, a TSN controller, a MIPI interface, and an upgraded HPS that includes two Arm Cortex-A76 processor cores and two Arm Cortex-A55 processor cores.

When coupled with high-performance, low-power programmable-logic fabric, these new hardware features make Intel Agilex 5 devices ideal for use in midrange FPGA applications across many embedded and edge markets, including wireless and wireline communications, video and audio broadcast equipment, industrial applications, test and measurement products, medical electronics, and military/aerospace applications.

An Architecture Optimized for Embedded and Edge applications

The programmable-logic fabric in the Intel Agilex 5 device family uses essentially the same architecture that is used in the high-performance Intel Agilex 7 device family. For example, the same second-generation Intel Hyperflex FPGA Architecture, which uses Hyper-Registers throughout the programmable fabric to maximize throughput and performance and to minimize power consumption. Intel Agilex 5 FPGAs and SoC FPGAs bring these advanced capabilities into the midrange FPGA realm.

Extensive Set of Connectivity Options

Intel Agilex 5 devices also feature multiple I/O capabilities that can handle nearly any I/O task needed in equipment used in embedded and edge applications, including:

- High-speed SerDes transceivers capable of operating at data rates as fast as 28.1 Gbps that support a variety of interface standards including Ethernet and PCI Express (PCIe) 4.0.
- High-speed general-purpose I/O (GPIO) banks with single-ended support for a variety of interface standards including 1.05 V, 1.1 V, and 1.2 V LVCMOS; differential I/O support for LVDS and MIPI D-PHY applications; and key I/O functions such as a hard memory controller for DDR4, LPDDR4, DDR5, LPDDR5, and QDR-IV SRAM.
- High-voltage I/O banks that support up to 3.3 V, single-ended LVCMOS voltage levels to support interfaces to legacy devices.

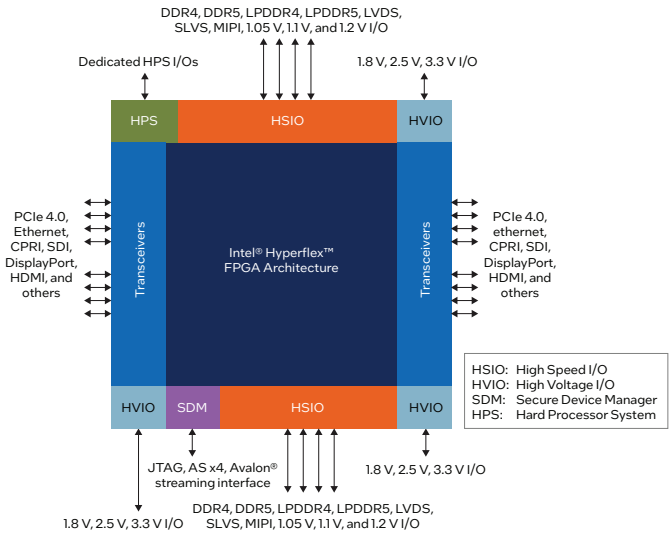

Figure 2. The advanced Intel 7 technology allows Intel to manufacture Intel Agilex 5 devices—including the programmable-logic fabric, hard processor system, high-speed and high-voltage I/O ports (HSIO and HVIO), and high-speed serial transceivers.

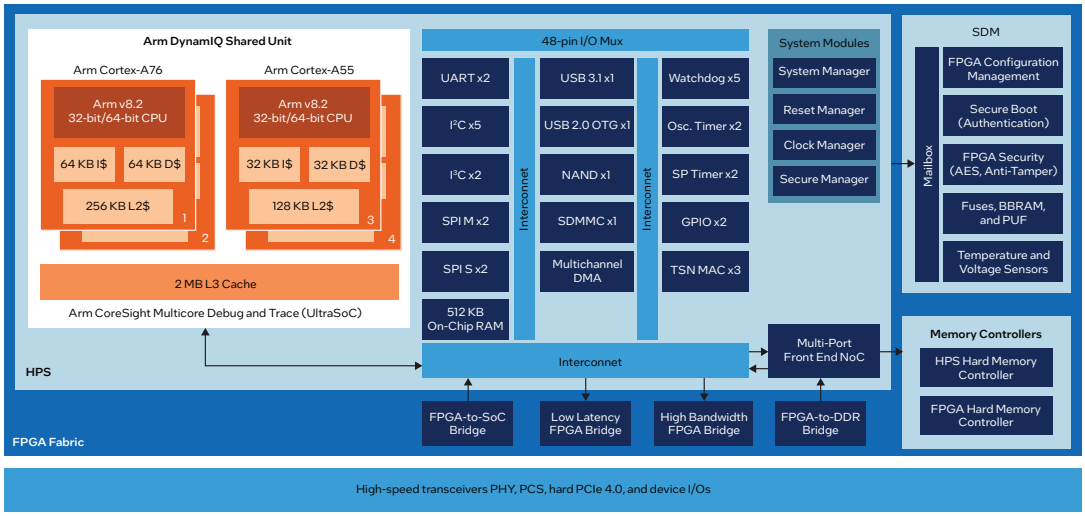

Figure 3. The HPS in Intel Agilex 5 SoC FPGAs incorporates two Arm Cortex-A76 processor cores, two Arm Cortex-A55 processor cores, and many peripheral IP blocks to support varied I/O requirements.

In addition, Intel Agilex 5 FPGAs and SoC FPGAs incorporate several hard IP elements that are new to the Intel Agilex FPGA family including the following:

An Upgraded HPS

Intel Agilex 5 SoC FPGAs introduce an upgraded HPS to the Intel Agilex device families. This upgraded HPS incorporates two 32/64-bit Arm Cortex-A76 and two 32/64-bit Arm Cortex-A55 processor cores. The Arm Cortex-A76 cores in the HPS operate at clock speeds as fast as 1.8 GHz and the Arm Cortex-A55 cores operate at clock speeds as fast as 1.5 GHz. This upgraded HPS includes a system memory management unit (MMU) that enables system-wide hardware virtualization.

The HPS also incorporates many hard peripheral IP blocks to support a wide range of I/O requirements. The processor cores used in the HPS for Intel Agilex 5 SoC FPGAs employ Arm's DynamIQ multi-core processor technology, which allows software to combine the Arm Cortex-A76 and Cortex-A55 CPUs into a single, fully integrated processor cluster that delivers additional power and performance benefits to applications ranging from portable devices to infrastructure gear from the network's edge to its core.

High-Speed, Monolithic Transceivers

Intel Agilex 5 devices are equipped with high-speed non-return-to-zero (NRZ) transceivers that support data rates ranging from 1 Gbps to 28.1 Gbps. These transceivers exhibit low latency and are optimized for a wide variety of applications, including long-reach backplanes.

Enhanced DSP with AI Tensor Block

The DSP blocks incorporated into the programmable-logic fabric of Intel Agilex 5 devices inherit the design of the variable-precision DSP blocks in the Intel Agilex 7 device families. In addition to those capabilities, the DSP blocks in Intel Agilex 5 devices add features derived from the tensor block used in Intel® Stratix® 10 NX FPGAs. It is important to note that these new DSP blocks have been completely redesigned from the ground up to provide a 5X performance boost (see Table 1) while maintaining the same die size area compared to the prior generation of DSP blocks, thereby significantly increasing the performance-per-watt metric.

The Enhanced DSP with AI Tensor Block introduces two new important operations: tensor processing capability for AI and complex number support for signal processing applications such as fast Fourier transform (FFT) and complex finite impulse response (FIR) filters.

Applications	Multiplier	Capabilities per DSP Block		Improvement*
		Earlier Intel Agilex Devices	Enhanced DSP with AI Tensor Block*	
AI, Signal Processing	INT8	4 OPS	20 OPS	5X
	INT9	4 Multipliers	6 Multipliers	50%
Signal Processing	16-bit Complex Multiplier	Needs 2 DSP Blocks	1 DSP Block	2X

Table 1. The Enhanced DSP with AI Tensor Block provides an order of magnitude increase in AI and DSP compute density.

The first mode enhances AI with the INT8 tensor mode, which provides twenty INT8 multiplications within one Enhanced DSP with AI Tensor Block and increases INT8 compute density by 5X versus Intel Agilex 7 device families. The tensor mode uses a two-column tensor structure with both INT32 and FP32 cascade and accumulation capability. It also supports a block floating exponent for improved inference accuracy and low-precision training. In addition, the AI capability of the variable-precision DSP functionality has also been enhanced. The vector mode has been upgraded from four INT9 multipliers to six INT9 multipliers. These modes are extremely useful for AI-centric tensor math and for various DSP applications.

The second new mode, the complex-number operation, doubles the performance of the tensor block when performing complex-number multiplication. Previously, two DSP blocks were needed for complex-number multiplication, but this new family of Intel Agilex 5 devices can multiply 16-bit, fixed-point, complex numbers within one Enhanced DSP with AI Tensor Block.

Time Sensitive Networking

Time Sensitive Networking (TSN) is a set of standards developed by the Time-Sensitive Networking task group of the IEEE 802.1 working group. These standards define mechanisms for the time-sensitive transmission of data over deterministic Ethernet networks and are needed by applications throughout the network to synchronize systems ranging from IoT devices to servers, and everything in between.

The hard Ethernet MACs in Intel Agilex 5 devices implement TSN endpoint functionality compliant to IEEE 802.1AS-2020, Qav, Qbv, Qbu, and IEEE 802.3br standards. Previously, TSN was implemented in programmable logic. However, TSN usage has now become so widespread that it made sense to build TSN capabilities directly into the hard Ethernet MACs of the Intel Agilex 5 devices.

MIPI D-PHY

Intel Agilex 5 devices incorporate MIPI IP to support a wide range of video applications. This IP supports MIPI D-PHY v2.5 at data rates as fast as 3.5 Gbps for MIPI's standard reference channel and as fast as 2.5 Gbps for MIPI's long reference channel.

The IP also supports MIPI D-PHY high-speed and low-power signaling modes without requiring external components. The MIPI IP's D-PHY implementation supports MIPI's Camera Serial Interface (CSI) version 3.0 and Display Serial Interface (DSI) version 2.0.

Functional Safety

Intel Agilex 5 FPGAs and SoC FPGAs are produced using rigorous quality-controlled procedures and processes. The safety certification of Intel's tools, methodologies, and IPs is provided by a trusted, independent external review body, TÜV Rheinland, which is one of the world's leading testing service providers. TÜV independently verifies that Intel's systems, tools, and described methodologies are suitable for use in safety applications up to SIL3.

Intel Agilex 5 Product Family Options

The Intel Agilex 5 product family includes both D-Series and E-Series devices with a range of options, including FPGAs (without an HPS) and SoC FPGAs (with an HPS).

D-Series devices deliver an industry-leading performance/watt fabric targeted at high-performance, low-density applications such as network and video/vision. For example, D-Series devices have a higher DSP/M20K ratio and a higher fabric speed than do their E-Series device counterparts. D-Series device features include the following:

- Same performance as Intel Agilex 7 FPGAs (F-Series/I-Series) with 15% lower power normalized for density.
- Up to 40% lower total power consumption vs. Intel Stratix 10 FPGA*
- Up to 1.5X fabric performance compared to Intel Stratix 10 FPGA*
- First FPGA for midrange applications to include AI Tensor Block

E-Series devices are optimized for I/O connectivity and offer best-in-class power-efficient performance with advanced next-generation features for power-, space-, and cost-sensitive embedded, edge, and IoT applications. E-Series device features include the following:

- Flexible and most capable set of I/O options compared to prior generation of products
- Up to 50% lower total power* consumption vs. Cyclone® V FPGA. Up to 2.5X fabric performance vs. Cyclone V FPGA*
- Up to 39% lower total power* consumption vs. Intel® Arria® 10 FPGA. Up to 34% higher fabric performance vs. Intel Arria 10 FPGA
- First edge-optimized FPGAs to include AI Tensor Block

Accelerating Application Development for Intel Agilex 5 FPGAs and SoC FPGAs

Design development support for Intel Agilex 5 devices is provided via multiple options. The first is with Intel® Quartus® Prime Software tools, which include everything required to design Intel® FPGAs and SoC FPGAs, from design entry and synthesis to optimization, verification, and simulation. Dramatically increased capabilities for Intel's latest-generation devices provides designers with the ideal platform to meet next-generation design opportunities.

In addition, Intel is opening up FPGA development access to software developers starting with the Intel® Distribution of OpenVINO™ toolkit and continuing with oneAPI toolkit. Intel's oneAPI development environment simplifies the programming of diverse computing engines across CPUs, graphics processing units (GPUs), neural processing units (NPUs), FPGAs, other accelerators. The oneAPI platform includes a comprehensive, unified portfolio of developer tools for mapping software to the hardware that can best accelerate the optimized applications, middleware, and frameworks.

The Intel® FPGA Add-on for oneAPI Base Toolkit will allow more designers to take advantage of Intel Agilex 5 FPGAs. With oneAPI toolkit, developers can explore different implementations of a design across diverse hardware choices, so they can understand the power and performance capabilities of each implementation and ultimately choose the best fit for their specific needs.

Example Use Cases

Intel Agilex 5 devices target the acceleration and compute needs for a wide range of embedded and edge applications—customized for specific market segments and applications—wherever data is generated, transported, stored, or processed.

It is important to understand that although Intel Agilex 5 devices are predominantly of interest for embedded and edge applications, they may also find employment in core infrastructure and data center applications.

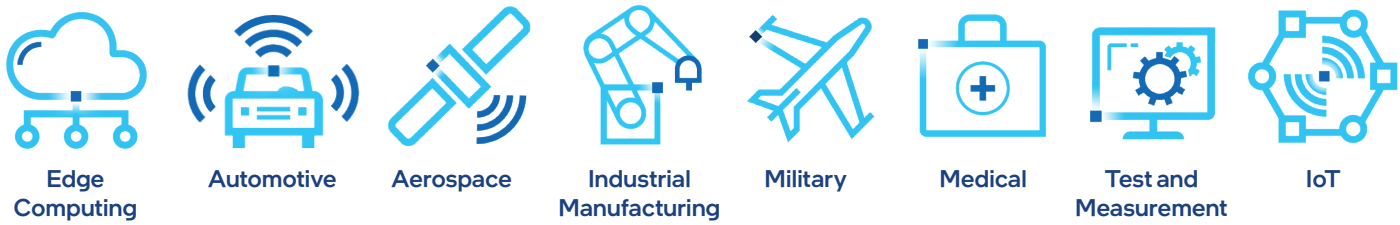

Figure 4. Example applications for Intel Agilex 5 FPGAs and SoC FPGAs.

In addition to a broad range of embedded applications across industrial, broadcast, medical, consumer, test and measurement, and military, aerospace, and government (MAG), target use cases for Intel Agilex 5 FPGAs D-Series include wired and wireless communications (next-generation radio, I/O expansion, ASIC co-processing) and cloud infrastructure (system management controller, root of trust, platform CPLD).

Target applications for Intel Agilex 5 FPGAs E-Series include industrial (camera interfaces, industrial drives, robot controllers, programmable logic controllers (PLCs), and IoT 4.0 gateways and edge compute), wireline/wireless (sidecar board controller, control OTN, I/O bridging), broadcast/medical (interactive white boards (IWBs), AV networking, cameras and video, and ultrasound, X-ray, MRI, and endo/laparoscopes), and test/measurement/retail (display automatic test equipment, terminal devices (parking meters, lightning, and environmental sensors), multi-camera systems, and video analytics).

Conclusion

With the power and performance efficiency provided by industry-leading Intel 7 process technology, Intel Agilex 5 FPGAs and SoC FPGAs are optimized for a wide range of applications that require lower power and higher performance. Devices in the Intel Agilex 5 product family include many features needed to develop systems for edge and core applications, including the following:

- Up to sixteen 28.1 Gbps serial transceivers capable of supporting up to 25 Gbps Ethernet ports.
- High-bandwidth processor interface interconnects, including PCIe 4.0 x8.
- Scalable integrated memory controllers with support for DDR4, DDR5, LPDDR4, and LPDDR5 SDRAM.
- Variable-precision, AI-enabled DSP or tensor blocks capable of executing as many as 40 TFLOPS.
- Hardware support for Advanced Encryption Standard (AES) cryptography for bitstream encryption.
- A HPS with two Arm Cortex-A76 processor cores running at clock speeds to 1.8 GHz and two Arm Cortex-A55 processor cores running at clock speeds 1.5 GHz.
- Second-generation Intel Hyperflex FPGA Architecture for faster implementations in the FPGA fabric.
- Support for multiple high-speed video I/O standards including MIPI D-PHY v2.5 at up to 3.5 Gbps per lane, serial digital interface (SDI), DisplayPort, and high-definition multimedia interface (HDMI).
- High-speed I/O (HSIO) ports supporting voltage levels of 1.05 V to 1.3 V and high-voltage I/O (HVIO) ports supporting voltage levels from 1.8 V to 3.3 V.

All these features combined provide developers of systems for embedded and edge applications with a comprehensive toolkit of hardware, software, IP, and reference designs that can tackle a tremendous number of design challenges. For more information about Intel Agilex 5 FPGAs and SoC FPGAs, view the resources listed below or contact your local Intel sales representative.

Learn More

- Intel Agilex 5 FPGA and SoC FPGA website
- Intel Agilex 5 FPGAs and SoCs D-Series product table
- Solutions for Intel Agilex 5 E-Series FPGAs

References

[1] www.statista.com/statistics/471264/iot-number-of-connected-devices-worldwide

[2] Brandon Purcell, "Q&A: The Secrets of Successful Segmentation Revealed", Forrester, January 1, 2018.

[3] IDC, "Data Creation and Replication Will Grow at a Faster Rate than Installed Storage Capacity, According to the IDC Global DataSphere and StorageSphere Forecasts", March 24, 2021.

[4] IDC Report, "Worldwide Global DataSphere Forecast, 2021–2025: The World Keeps Creating More Data—Now, What Do We Do with It All?" (Doc #US46410421), March 2021

[5] Kevin Morris, "Inside Intel Agilex FPGAs," EEJournal.com, April 9, 2019.