ICA-XFG-001
Introduction to Data Plane Programmability

Course Prospectus

ICA-XFG-001 is free, 1-unit preparatory, instructor-led course that provides a quick introduction to the exciting technology of high-speed programmable packet processing. This course is recommended to anyone who wants to attend the introductory academy courses such as ICA-XFG-101 to learn about P4 Language, Intel® P4 Studio, and Intel Tofino™ Family of Intelligent Fabric Processors (IFP) but would like to have more background about the underlying technology and its applications.

ICA-XFG-001 is a part of Intel® Connectivity Academy XFG course series and can be taken either in-person or online.

Course Goals

Upon the completion of the course, the students will:

1. Understand the general architecture of telecommunication systems with the emphasis on the role of the data plane in system functionality and performance
2. Understand the concept of data plane programming and its benefits
3. Understand the typical functionality offloaded to the data plane programs
4. Understand the role of the control plane and control plane APIs
5. Get a roadmap for future education and exploration

Detailed Schedule

The course consists of a 2-hour-long lecture (presentation) with one break. There are no labs due to the introductory nature of the course.

Both morning and evening (Pacific Time) sessions are offered to accommodate students from different time zones.

Course Outline

- Introduction
- How are network devices built?
- Why do we need devices with programmable data planes?
- Is it possible to build high-speed devices with programmable packet processing algorithms?
- What packet processing algorithms do and how one can express them?
- What is the role of the control plane and how it can communicate with the data plane
- Intel Connectivity Academy training roadmap

Target Audience

This course is suitable for everyone who wants to learn about programmable networking and might be considering attending other Intel Connectivity Academy courses.

Pre-requisites

- General understanding of networking

How to Register

Class dates and times are announced on the Academy Calendar Page ahead of time and you can register right on the site.

Please, note that most courses require all the participants to have a valid NDA and SLA in place. Their existence will be verified after the purchase, and you will be notified if additional steps are required, or the ticket will be refunded.

Logistics

To attend an online presentation, you will need to create a **free Zoom account, associated with your work email address**. Upon the registration, you will receive a link to the online event. You will also receive invitations to establish accounts on Slack and the Academy Support Portal for lab support and materials access, also **associated with your work email address**.

A high-speed internet connection is required to attend the online presentation. Call-in numbers for higher voice quality might be provided, depending on the region. Please, connect to the online meeting 5-10 minutes before the start to work out all potential connection problems.

All necessary materials, including the presentation PDFs and lab exercises will be available through the Academy Support Portal a day before the start of the class. We highly recommend that you print the presentation PDFs and use them to take notes. Alternatively, these presentations can be loaded on a tablet, where the notes can be taken with an electronic pen.

Contact

For more information, please contact connectivity.academy@intel.com.

Important Notes

Intel® P4 Studio SDE is a software product, developed independently from the software, available via p4.org. Some components of the SDE were contributed by Intel to p4.org, others rely on the code from p4.org, but the goals of the projects, the tools, and the workflows are different. P4.org software is a community-supported project with many resources freely available. This class covers Intel® P4 Studio SDE and **not** p4.org software. Specifically, not covered are the Behavioral Model (BMv2), v1model and PSA $P4_{16}$ architectures and neither is P4Runtime protocol.

$P4_{16}$ compiler for Intel® Tofino™ and Intel® Switch Runtime Interface APIs are in active development as is the course module material. While Intel® Connectivity Academy team strives to introduce Intel customers to the leading-edge software, bugs, errors and omissions may occur. The later versions of these course modules might significantly differ from the earlier ones.

The course module material covers both Tofino and Tofino2 devices. Relevant enhancements and differences are emphasized and discussed whenever applicable.

The availability of each course is announced separately. Please, visit Intel® Connectivity Academy website for more information.

The online presentations may be recorded and may be published, in whole or in part, in various media, including print, audio and video formats without further notice. If you do not want to participate, you may choose to either keep your audio and video connections muted or turned off or leave the call. By choosing to remain, you are consenting to the recording of the session.