**Table 1: Board Setting Configuration [SW6]**

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| --- | --- | --- | --- |
| **Switch** | **Schematic Signal Name** | **Description** | **Settings** |
| 1 | CLK\_SEL | **ON** for 100Mhz on-board clock oscillator selection**OFF** for SMA input clock selection | ON |
| 2 | CLK\_EN | **OFF** for setting CLK\_ENABLE signal high to the MAXV | OFF |
| 3 | Si516\_FS | **ON** for setting the SDI REFCLK frequency to 148.35Mhz**OFF** for setting the SDI REFCLK frequency to 148.5Mhz | Depends on the source of video to SDI II Receiver (Channel 0),ON for NTSC,OFF for PAL |
| 4 | FACTORY | **ON** to load user design from flash**OFF** to load factory design from flash | ON |
| 5 | ZQ\_B2K | **ON** for setting RZQ resistor of Bank 2K to 99.17ohm**OFF** for setting RZQ resistor of Bank 2K to 240ohm | OFF |

**Table 2: DIP Switches**

|  |  |
| --- | --- |
| **DIP Switch** | **SW2** |
| 8 | 0 = 75% colorbars1 = 100% colorbars |
| 7 | 0 = output colorbars1 = output pathological test pattern |
| 6 | 0 = output color1 = output no color |
| 5 | 0 = PAL rate1 = NTSC rate |
| 4:1 | 4’b0000: SD – 525i4’b0001: SD – 625i4’b0010: HD – 1080i60/59.944’b0011: HD – 1080i504’b0100: HD – 1080p24/23.964’b0101: HD – 720p60/59.944’b0110: HD – 720p30/29.974’b0111: HD – 1080p30/29.974’b1000: HD – 1080p254’b1001: 3Ga – 1080p60/59.944’b1010: 3Ga – 1080p504’b1011: 3Gb – 2x1080p604’b1100: 3Gb – 2x720p30/29.974’b1101: 3Gb – 2x1080p60/59.944’b1110: 3Gb – 1080p60/59.944’b1111: 3Gb – 1080p50 |

**Table 6: User LEDs**

|  |  |
| --- | --- |
| **User LEDs** | **Description** |
| D3 | The heartbeat of the transmitter clock out for channel 0 |
| D4 | The heartbeat of the receiver recovered clock out for channel 0 |
| D5 | Frame locked for channel 0 |
| D6 | TRS locked for channel 0 |
| D7,D8 | RX signal standard for channel 0:* SD :[D7,D8] = 00
* HD :[D7,D8] = 01
* 3Ga :[D7,D8] = 11
* 3Gb :[D7,D8] = 10
 |
| D9,D10 | Internal pattern generator signal standard for channel 1:* SD :[D9,D10] = 00
* HD :[D9,D10] = 01
* 3Ga :[D9,D10] = 11
* 3Gb :[D9,D10] = 10
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