

Tutorial: Write Raw Programming Data (.rpd) into Flash Devices

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Introduction

This tutorial describes the flow to write Raw Programming Data (.rpd) files into flash devices using Stratix 10 Serial Flash Mailbox Client Intel FPGA IP Core. The tutorial is demonstrated using system console.

Requirements

The following are the hardware and software requirements for the design example:

- Stratix 10
- Intel Quartus Prime Pro Edition software version 18.0 and later
- Intel FPGA Download Cable II
- Flash devices

- *Note: This design example is tested on Stratix 10 SoC Development Kit and Micron MT25QU02G.*

Theory of Operation

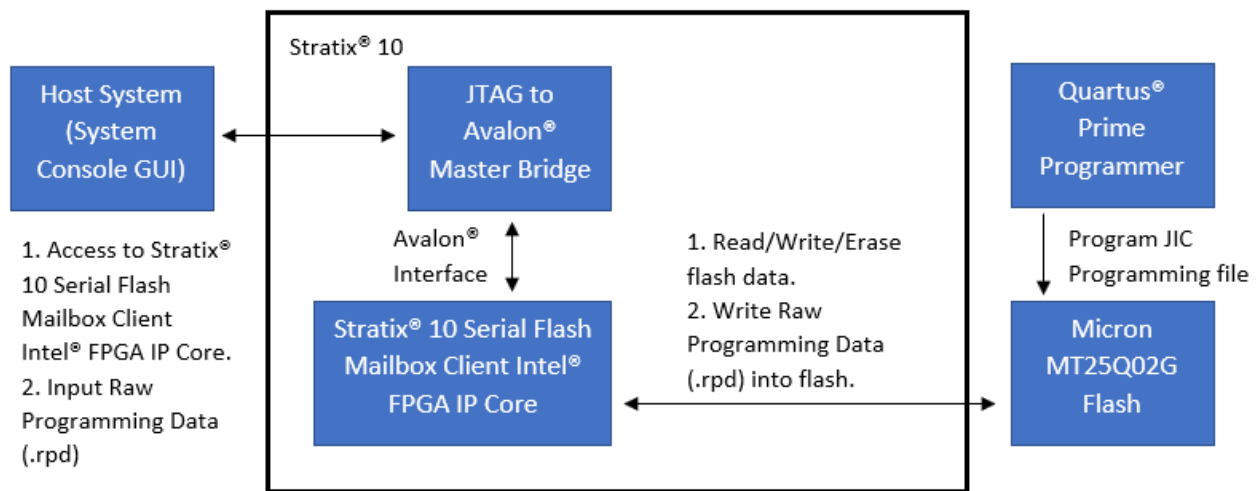


Figure 1. Block diagram of modules in the reference design

Figure 1 shows the high-level modules in the reference design and the interfaces among the modules. First, FPGA programming file with Stratix 10 Serial Flash Mailbox Client Intel FPGA IP Core and JTAG to Avalon Master Bridge IP Core instantiated is programmed into flash memory. Then, another design is created and then converted to Raw Programming Data (.rpd) programming file. System Console Graphics User Interface (GUI) is used to access to Stratix 10 Serial Flash Mailbox Client Intel FPGA IP Core

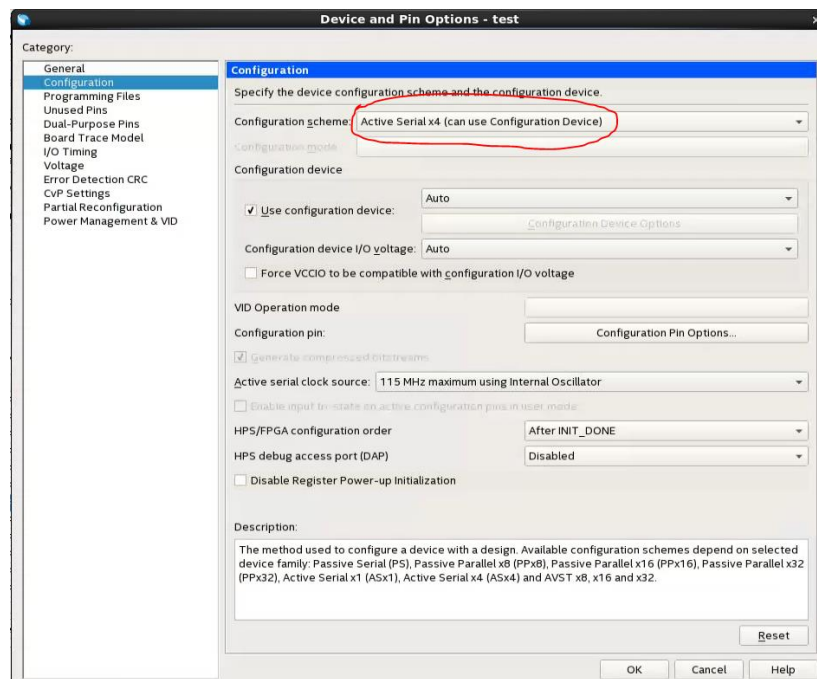
to perform simple memory operation such as read and write from and to flash devices. Finally, System Console GUI is used to write Raw Programming Data into flash devices.

Creating Hardware Design

1. To create a hardware project with JTAG master as host, instantiate a Serial Flash Mailbox Client Intel FPGA IP and connect to JTAG to Avalon Master Bridge in Intel Quartus Prime Pro Edition software.

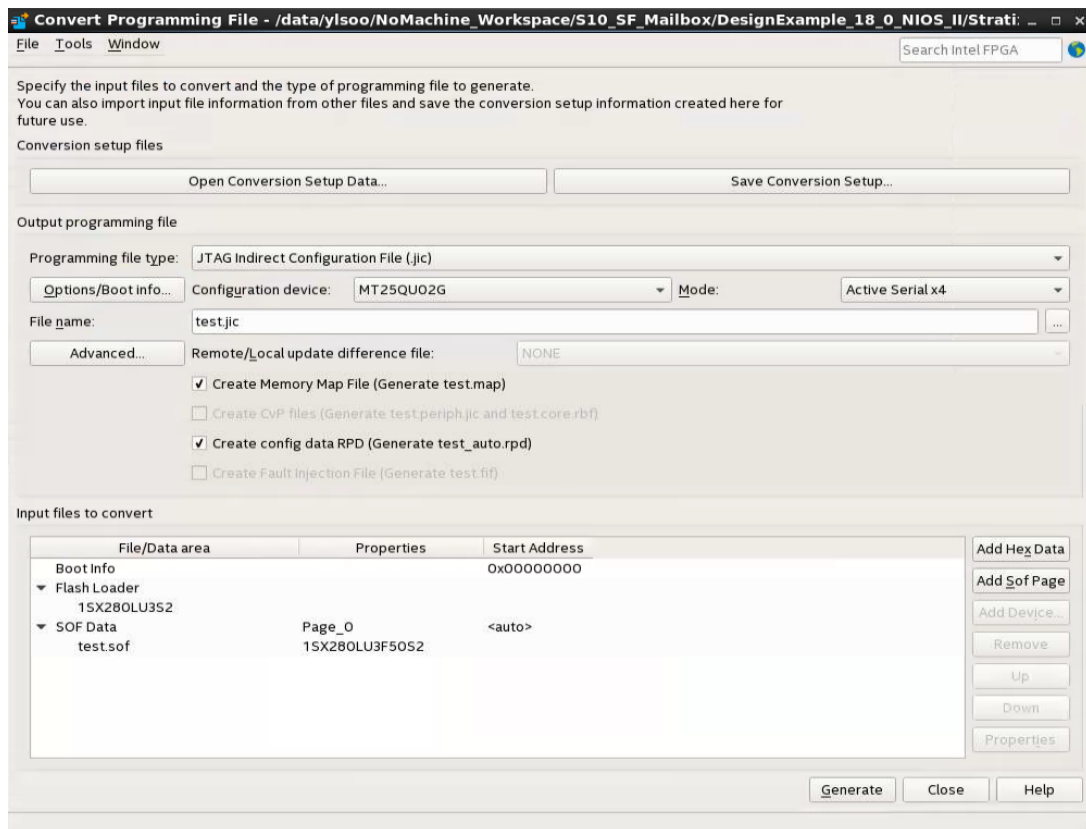
Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	clock_in	Clock Bridge Intel FPGA IP	clk	exported			
		in_clk	Clock Input	Double	clock_in_0...			
		out_clk	Clock Output					
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	reset_in	Reset Bridge Intel FPGA IP	reset	clock_in_...			
		clk	Clock Input	Double	[clk]			
		in_reset	Reset Input	Double	[clk]			
		out_reset	Reset Output	Double	[clk]			
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	strax10_serial_flash_client_0	Stratix 10 Serial Flash Mailbox Client Intel FPGA IP					
		clk	Clock Input	Double	clock_in_...			
		csr	Avalon Memory Mapped Slave	Double	[clk]	# 0x0000_0000	0x0000_01ff	
		irq	Interrupt Sender	Double	[clk]			
		rd_mem	Avalon Memory Mapped Slave	Double	[clk]	# 0x0000_0248	0x0000_024f	
		reset	Reset Input	Double	[clk]			
		wr_mem	Avalon Memory Mapped Slave	Double	[clk]	# 0x0000_0240	0x0000_0247	
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	master_0	JTAG to Avalon Master Bridge Intel FPGA IP					
		clk	JTAG Input	Double	clock_in_...			
		clk_reset	Reset Input	Double	[clk]			
		master	Avalon Memory Mapped Master	Double	[clk]			
		master_reset	Reset Output	Double	[clk]			

2. Set base address for **csr**, **rd_mem** and **wr_mem**.
- *Note: You may refer to design example for the hardware design.*
3. Configure the configuration scheme to Active Serial x4 in Intel Quartus Prime Pro Edition software by selecting **Assignments -> Device -> Device and Pin Options -> Configuration**.



Generating .jic and .rpd programming file

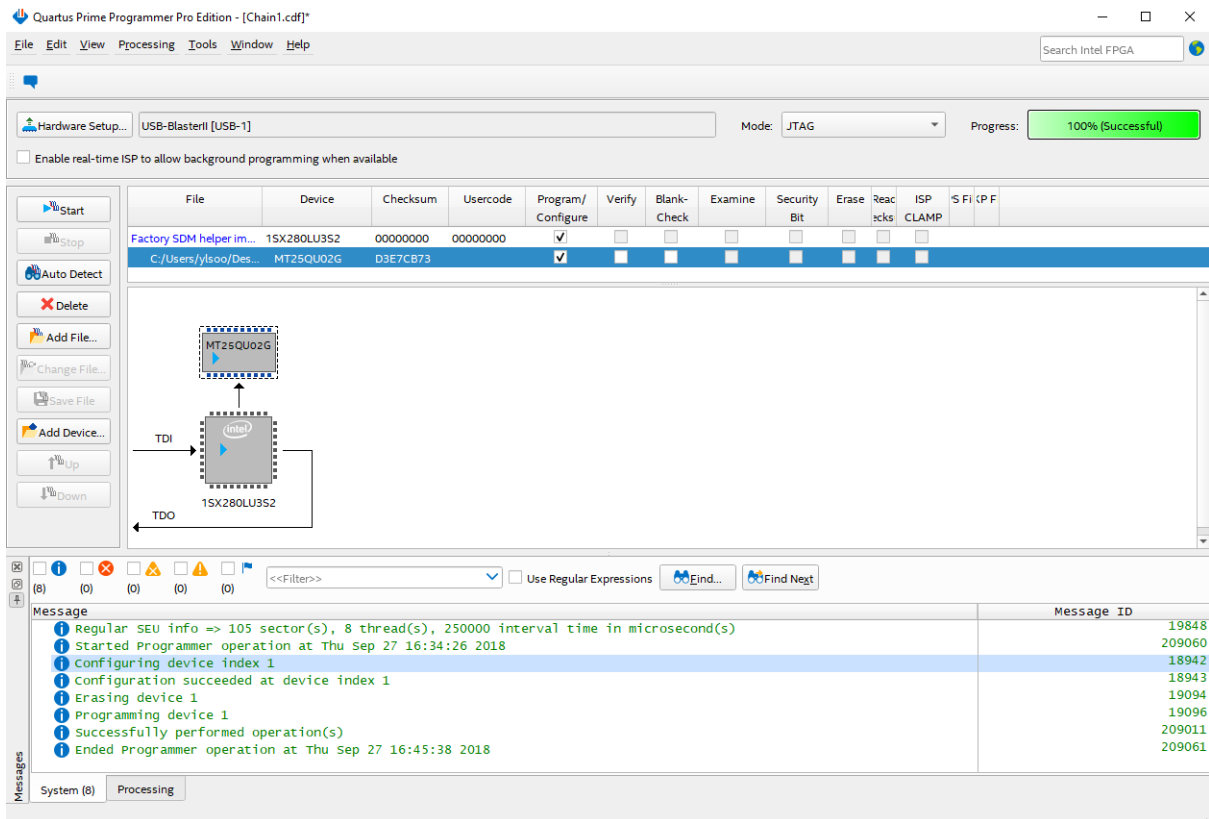
1. Open Intel Quartus Prime Pro Edition software.
2. On the **File** menu, click **Convert Programming Files**.
3. Select **JTAG Indirect Configuration File (.jic)** from **Programming file type** drop-down list.
4. Select the configuration device from **Configuration device** drop-down list.
 - *Note: The configuration device depends on the type of configuration device used in the board.*
5. Select **Active Serial x4** from **Mode** drop-down list.
6. Add SOF programming file into **SOF Data**.
7. Add Device used into **Flash Loader**.
 - *Note: The device used must be the same as the device used in Intel Quartus Prime Pro Edition software.*
8. Tick Create config data RPD to enable the generation of RPD file.
9. Click **Options/Boot** info and select **little Endian**.



10. Click **Generate** to generate both .jic and .rpd programming file.

Programming flash devices with .jic programming file

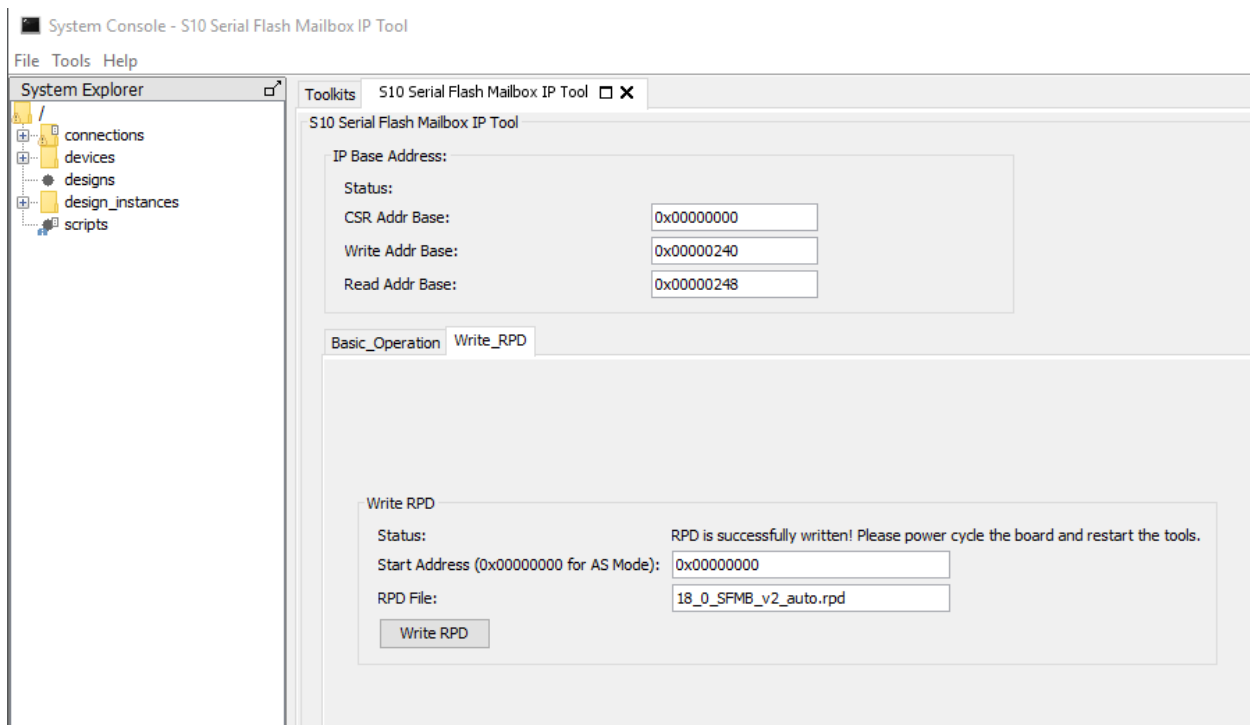
1. Open **Programmer**, click **Add File**, select the generated JIC programming file (.jic) and click **Open**.
2. Check the **Program/Configure** check box for the attached .jic file.
3. Click **Start** to start programming the flash devices.
4. Configuration is complete when the progress bar reaches 100%. Power cycle the board and the Intel Stratix 10 device is automatically configured with the image file via the Active Serial configuration scheme.



Running the system console

1. Open Intel Quartus Prime Pro Edition software.
2. On the **Tools** menu, select **System Debugging Tools** and click **System Console**.
3. In System Console, execute **S10_SerialFlash_Mailbox_TCL_GUI.tcl** by selecting **File** and clicking **Execute Script**.
 - *Note: You may find **S10_SerialFlash_Mailbox_TCL_GUI.tcl** TCL script in the design example.*

4. A Graphic User Interface (GUI) will be opened and we may perform some simple operation such as read flash devices ID, read and write from and to flash devices.
5. To write RPD into flash devices, select **Write_RPD** tab in the GUI and fill in the information in the GUI such as base address for **csr**, **rd_mem** and **wr_mem**, start address to 0x00000000 and the RPD file name.
 - *Note: Base address for **csr**, **rd_mem** and **wr_mem** must be the same as base address configured during the Serial Flash Mailbox Client Intel FPGA IP initialization.*
6. Click **Write RPD** button to execute RPD writing.
 - *Note: Writing of RPD file to flash devices might takes some time. Please do not disconnect the Intel FPGA Download Cable II or perform any memory operation to avoid failure in writing .rpd programming file.*
7. The **Status** bar in the GUI will inform user once the .rpd programming is successfully written into the flash devices, user may power cycle the devices to see the design change.



References

- Stratix 10 Serial Flash Mailbox Client Intel FPGA IP Core User Guide
<https://www.intel.com/content/www/us/en/programmable/documentation/kcn1519199783802.html>

Revision History

Date	Version	Changes
November 28, 2018	1.0	Initial Release
December 04, 2018	2.0	Updated "Requirements"