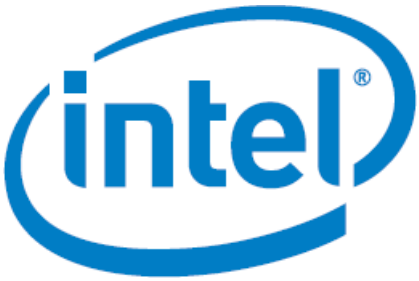

Cyclone 10 GX XCVR Toolkit Reference Design v17.1.1 User Guide

Date: January 2018

Revision: 1.0

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Introduction

The objective of this reference design is to enable transceiver (XCVR) toolkit usage demonstration via Cyclone 10 GX development kit board. This user guide documentation will assist user to use XCVR toolkit to perform XCVR channel bit error rate (BER) check via on board XCVR TX channel to RX channel loopback test and serial loopback test in step by step guidance. BER is a typical measurement parameter used to inspect and build the confidence level of the signal integrity quality of XCVR channel in industry. This reference design utilizes one ATXPLL IP to clock one XCVR NativePHY IP 1.25Gbps XCVR duplex channel.

Requirement

The reference design requires the following hardware and software to run the hardware test:

• Quartus® Prime Software Version: 17.1.1 Pro Edition

• Cyclone 10 GX Development Kit Board

https://www.altera.com/products/boards_and_kits/dev-kits/altera/cyclone-10-gx-development-kit.html

• FPGA Mezzanine Card (FMC) loopback card

Theory of Operation

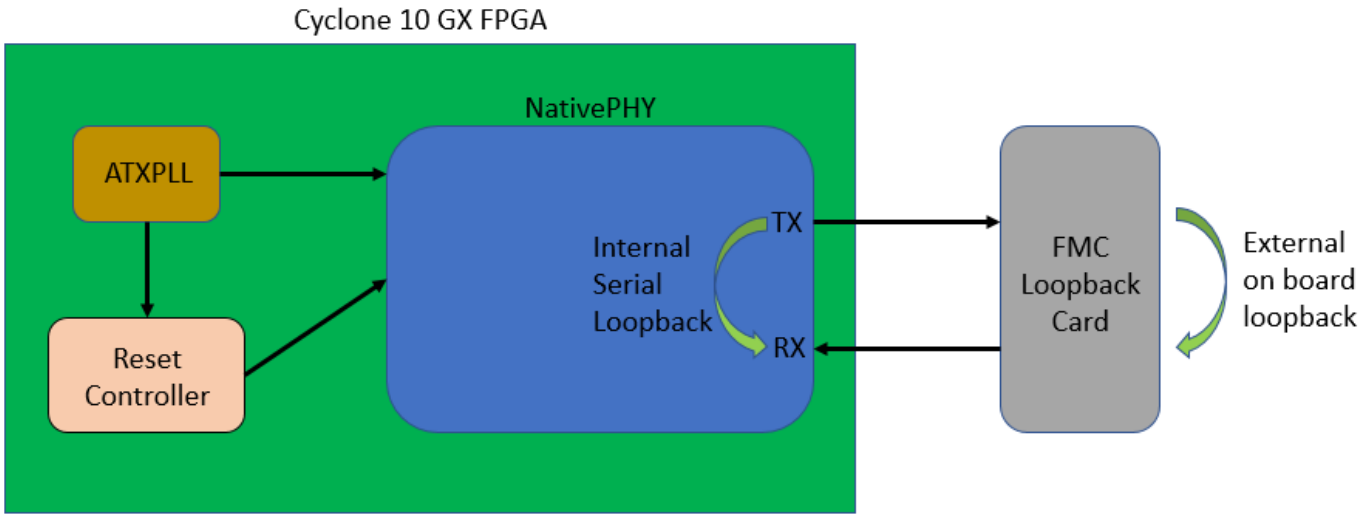

Figure 1. Block diagram of modules in the reference design

Figure 1 shows the high-level modules in the reference design as well as the interfaces among the modules. The Cyclone 10 GX XCVR NativePHY IP is used to generate one 1.25Gbps XCVR duplex channel. The XCVR Reset Controller IP is used to perform the reset to the XCVR channel and ATXPLL. The ATXPLL IP serves as XCVR PLL to provide clock source to NativePHY IP XCVR channel.

XCVR channel TX to RX loopback test can be done in 2 ways which is either via internal serial loopback test in Physical Medium Attachment (PMA) block or via external on board loopback using the FPGA Mezzanine Card (FMC) loopback card.

Figure 2 indicates the overview diagram of serial loopback path within PMA block.

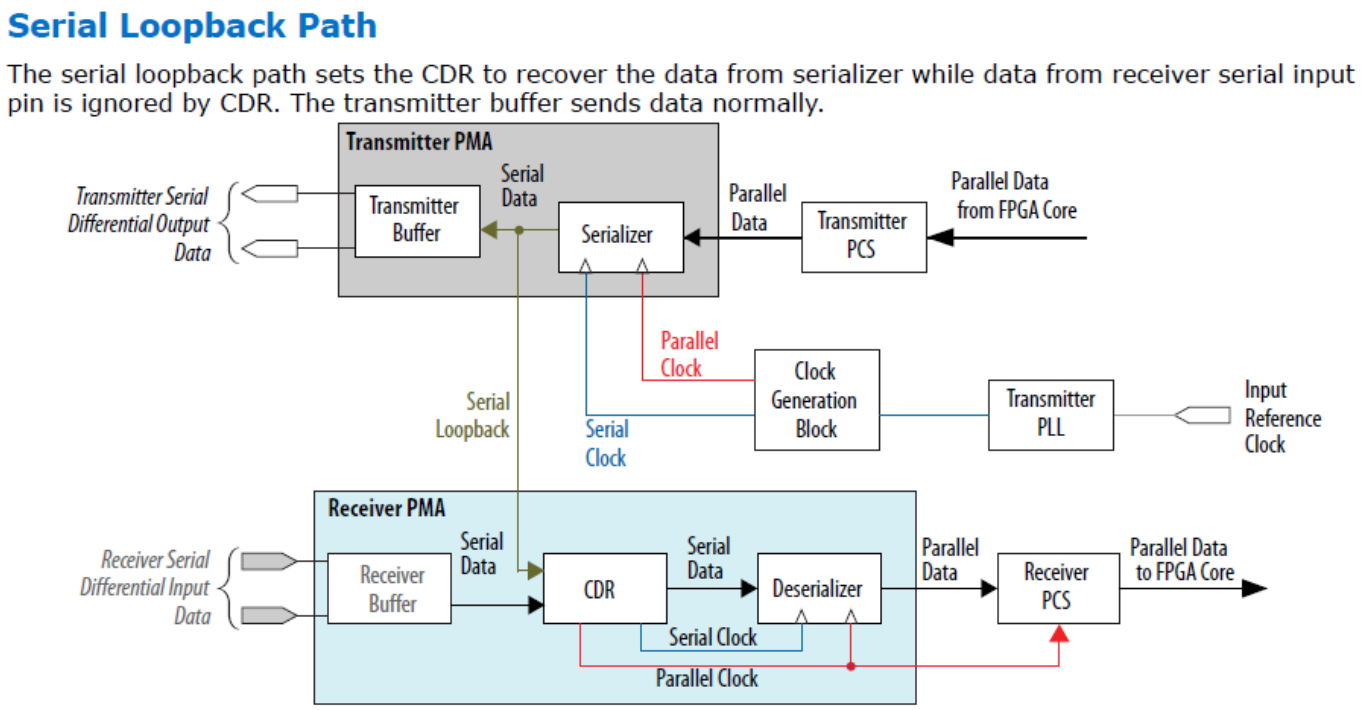

Figure 2. Overview diagram of serial loopback path

In the XCVR toolkit, user needs to select preferred loopback mode before starting the BER testing.

This design example will exercise following loopback mode test.

- Loopback mode = off (user to manually perform on board external loopback via FPGA FMC loopback card)
- Loopback mode = serial loopback (activate serial loopback path within XCVR PMA block)

How to Setup the Development Kits for XCVR Loopback Test

Follow these steps to setup the hardware to run the reference design:
1. Connect the FMC loopback card to the FMC port on the Cyclone 10 GX Development Kit Board
2. Ensure Switch 9 (S9) settings of the Development Kit Board is set to “on” position
3. Connect the Micro USB cable to the USB Blaster connector on the Development Kit Board
4. Connect the power adapter shipped with the Development Kit Board to power supply jack
5. Turn On the power for the Development Kit Board. The hardware system is now ready for testing.

How to Reconstruct and Run the Reference Design

Hardware setup:

1. Follow the instruction in the Design Store to prepare the design template and load the design into your Quartus software
2. Perform full compilation with the Quartus design
3. Carry out following steps to reduce the JTAG frequency from default 24MHz to 16MHz to avoid JTAG connection issue

   a. Launch NIOS II command shell from Windows Quartus Pro v17.1 startup menu

   b. Follow the commands in Figure 3 to configure the JTAG frequency

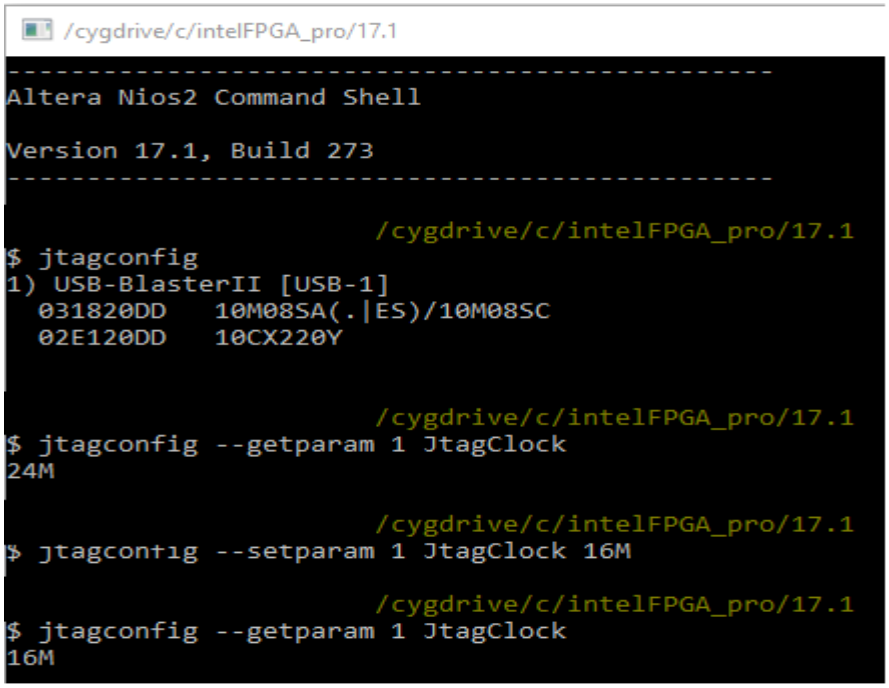

Figure 3. Commands to reduce the JTAG Frequency to 16M

4. Only execute step 4 if your C10 GX Development Kit Board belongs to 1st prototype build with board serial number within 0000001-0000030 else skip to step 5. For 1st prototype board, by default after power up the development kit board, the programmable clock generator (Si5332) used for the transceiver channel in this design is disabled. Do the following to enable and configure the output clock frequencies correctly

   a. Download and unzip "Kit Collateral.zip" design package from below link
   https://www.altera.com/products/boards_and_kits/dev-kits/altera/cyclone-10-gx-development-kit.html
   b. Launch Quartus software first then run the ClockController.exe from
   cyclone-10-gx-kit-collateral\examples\board_test_system
   c. By default, the Clock Controller GUI should look like Figure 4

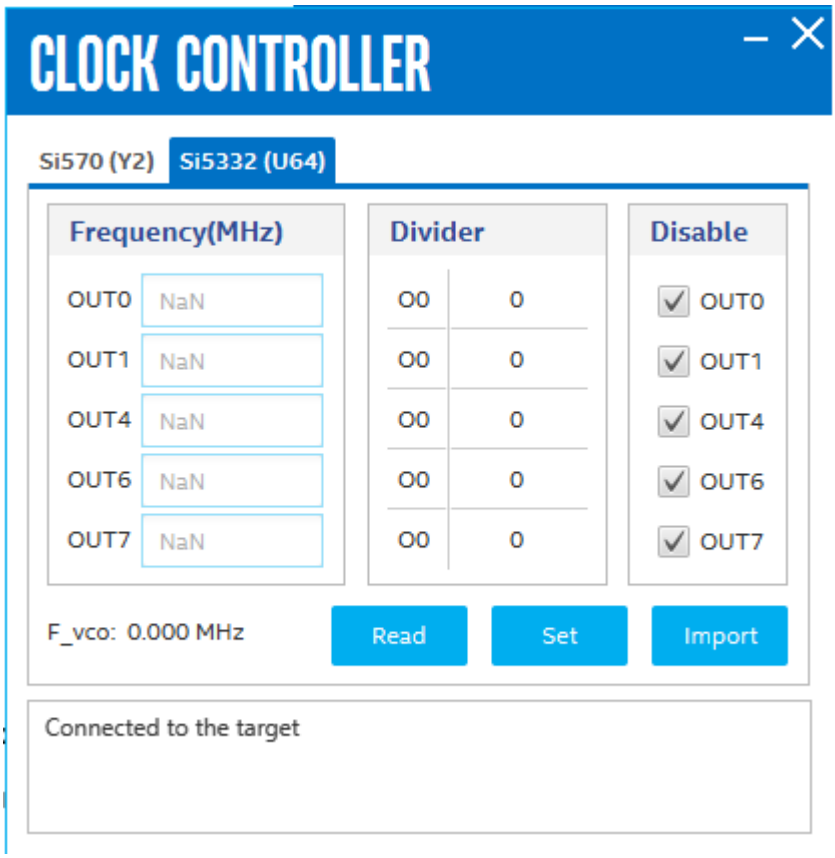

Figure 4. Default Clock Controller GUI for Si5332

   d. Click the "Import" button in Clock Controller GUI and select the "U64-Registers.txt" in cyclone-10-gx-kit-collateral\examples\board_test_system folder to configure the output clock frequencies

e. After successful configuration, the Clock Controller GUI should look like Figure 5

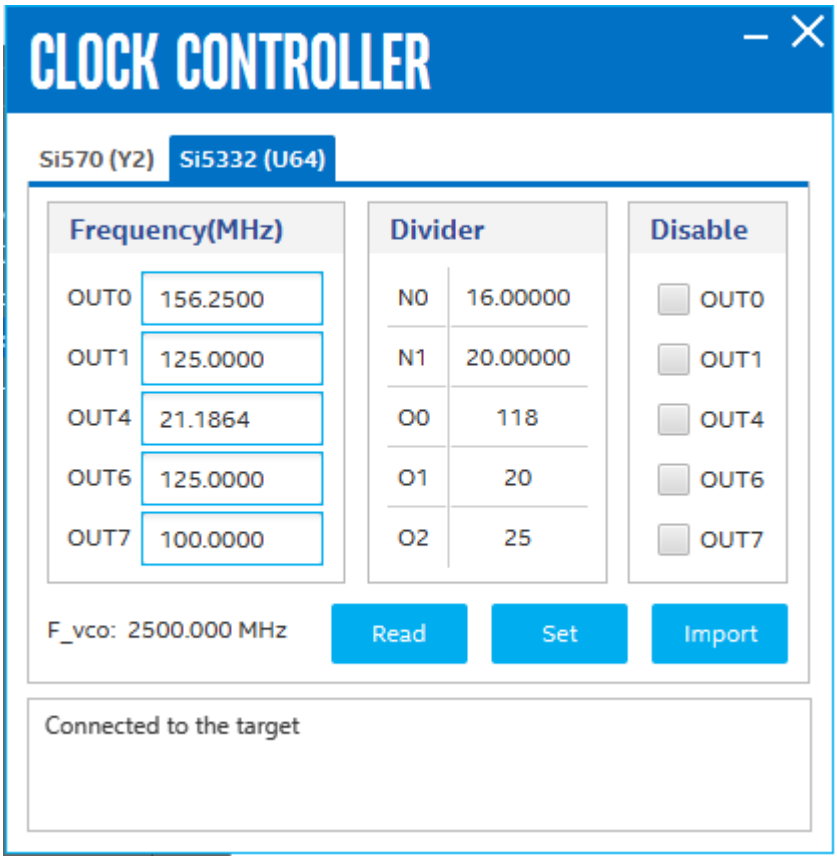

Figure 5. Clock Controller GUI for Si5332 after Successful Configuration

f. Close the Clock Controller application

g. Note that you would need to reconfigure the Si5332 using step 4(b) -> 4(f) each time the Development Kit Board is power-cycled

5. Program the SOF file generated into the Development Kit Board

XCVR Channel Loopback Test Run Procedure :

1. Launch Transceiver toolkit
2. In Quartus software, goto Tools -> System Debugging Tools -> Transceiver Toolkit
3. Click “Load Design” and select the programmed SOF file.
4. Toolkit should initialize one XCVR duplex channel as shown in Figure 6.

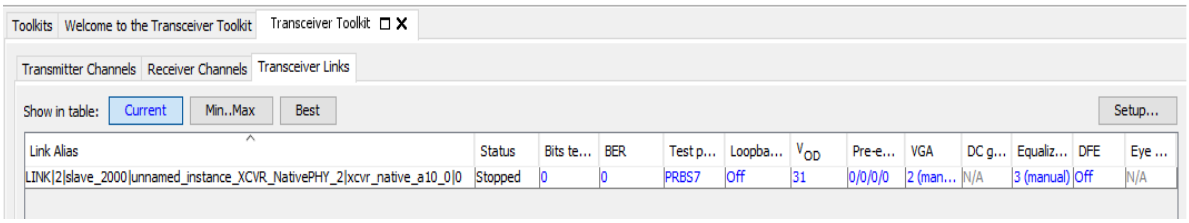

Figure 6. XCVR channel initialization in toolkit

5. Click the XCVR channel under “Link Alias” then click on “Control Transceiver Link”
6. Procedure to test Internal Serial Loopback
   a. Set Loopback Mode to “Serial loopback” as shown in Figure 7

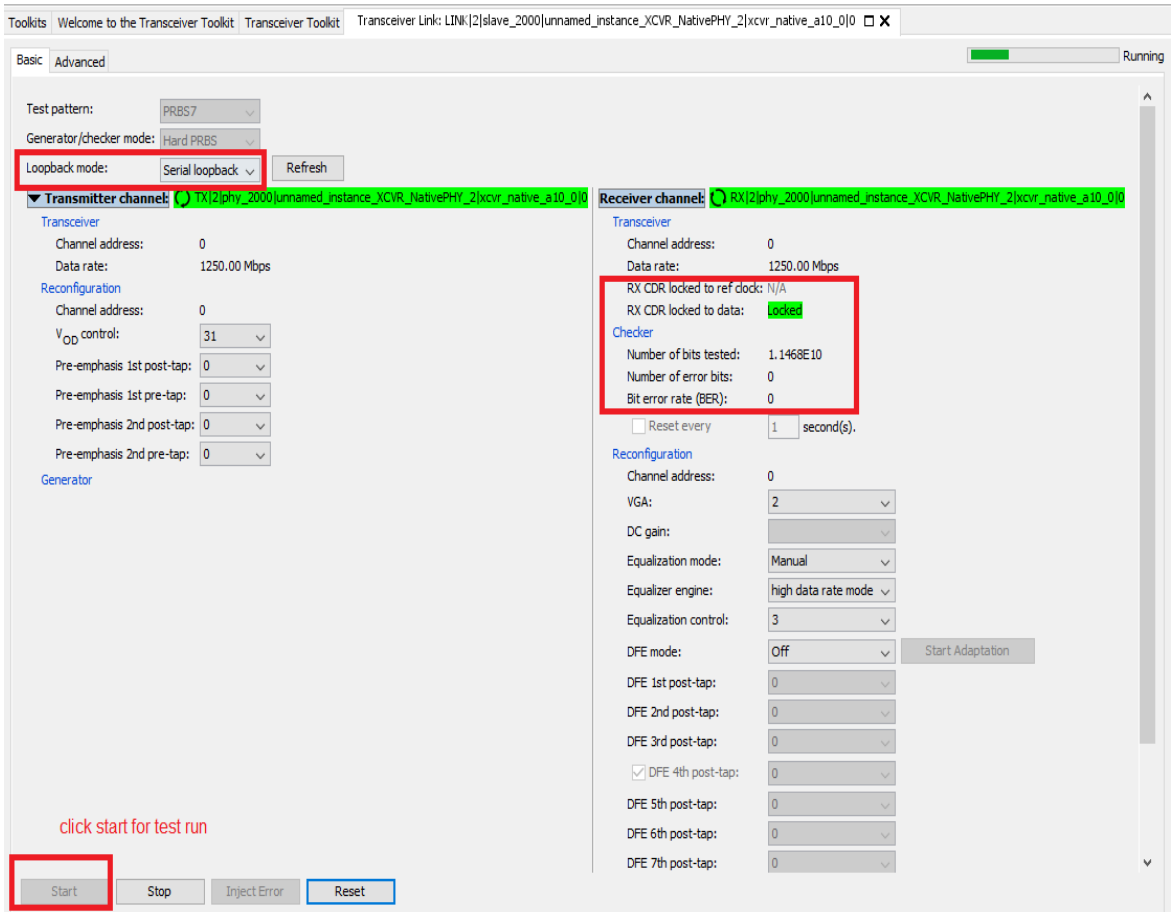

Figure 7. Test run with Internal Serial Loopback Mode

b. Click “Start” button and monitor CDR lock status, number of bits tested and Bit Error Rate (BER)

c. Test is considered pass when CDR is locked and BER result is zero

d. Test run is continuous. Click “Stop” and then click “Reset” to stop test.

7. Procedure to test External On Board Loopback with (FMC Loopback Card plugged on board)

a. Set Loopback Mode to “Off” as shown in Figure 8

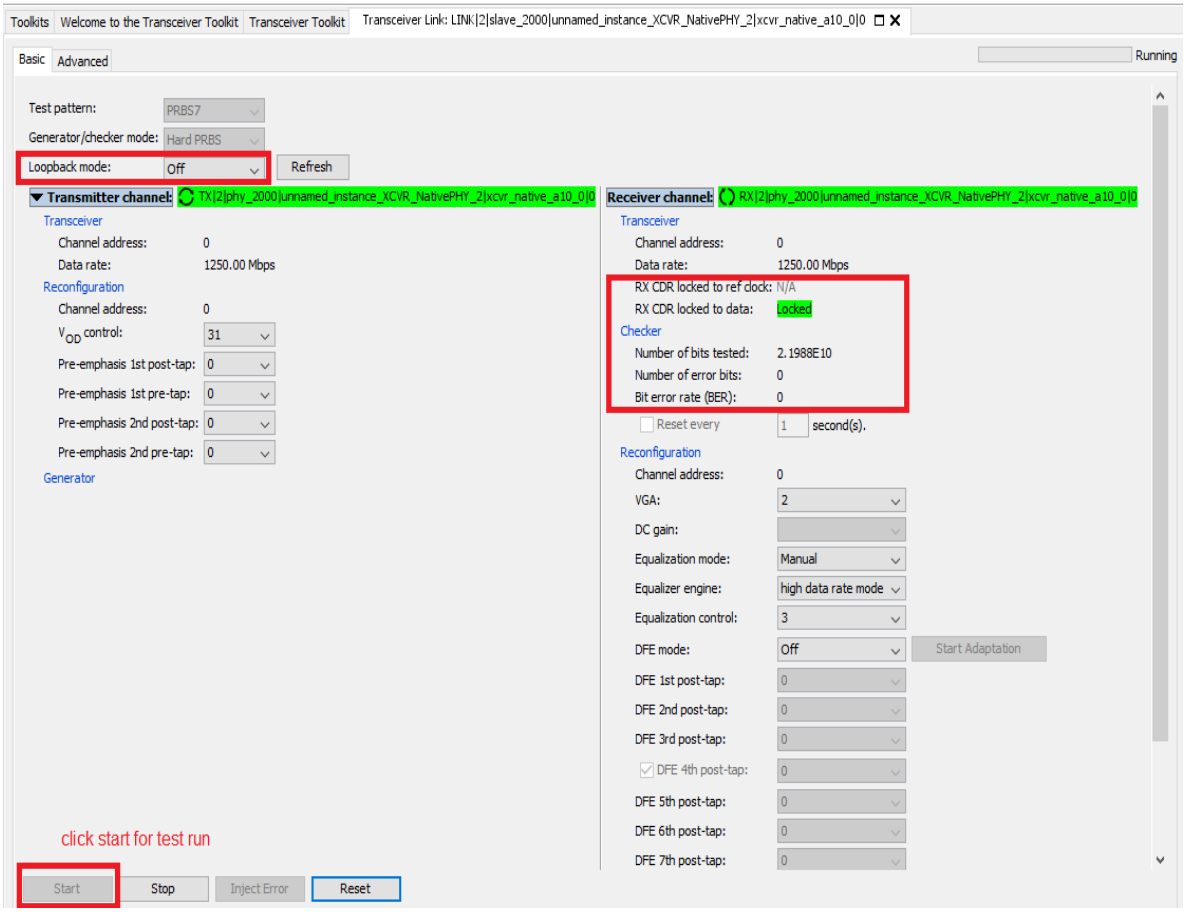

Figure 8. Passing test run with External On Board Loopback Mode

b. Click “Start” button and monitor CDR lock status, number of bits tested and Bit Error Rate (BER)

c. Test is considered pass when CDR is locked and BER result is zero

d. Test run is continuous. Click “Stop” and then click “Reset” to stop test.

8. Procedure to test External On Board Loopback with (FMC Loopback Card removed from board)
    a. Power down Development Kit Board
    b. Remove FMC Loopback Card from Development Kit Board and power on the board
    c. Follow hardware setup guide to reduce JTAG clock and configure Clock Controller GUI if necessary
    d. Follow test run procedure to bring up XCVR toolkit
    e. Set Loopback Mode to “Off” as shown in Figure 9

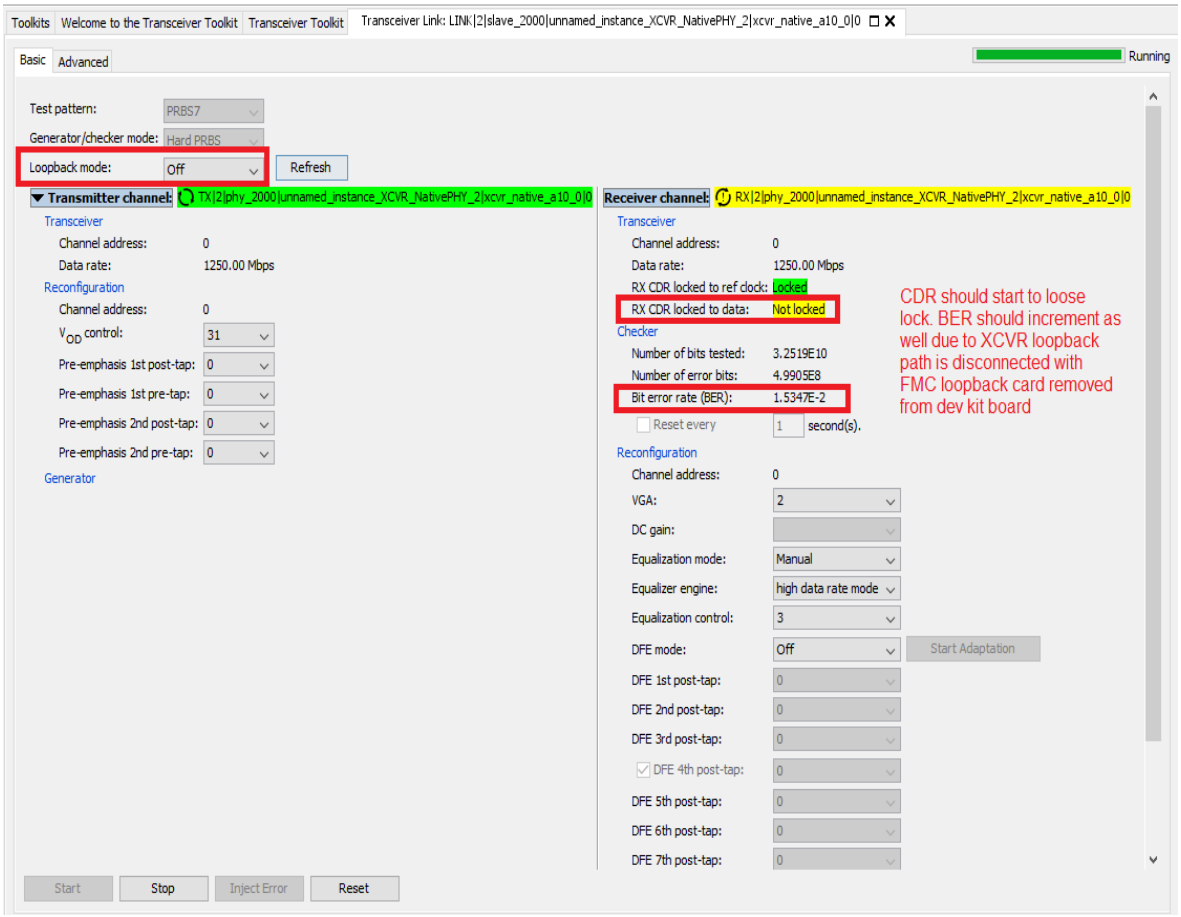

Figure 9. Failing test run with External On Board Loopback Mode

    f. Click “Start” button and monitor CDR lock status, number of bits tested and Bit Error Rate (BER)
    g. Test is expected to fail with CDR loose lock and BER increment due to on board loopback path connection is broken by FMC loopback card removal
    h. Test run is continuous. Click “Stop” and then click “Reset” to stop test.

Conclusion

This reference design provides user a quick start guide to perform XCVR channel hardware test verification in transceiver toolkit by using simple NativePHY IP design.

References

- Intel Cyclone 10 GX Transceiver PHY User Guide
  https://www.altera.com/documentation/hki1486507600636.html
- Intel Cyclone 10 GX Development Kit Board Website
  https://www.altera.com/products/boards_and_kits/dev-kits/altera/cyclone-10-gx-development-kit.html

Revision History

Date	Version	Changes
Jan, 2018	**1.0**	**Initial Release**