OpenLDI Interface Blocks for Qsys

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1. Introduction

OpenLDI is a common video interface found in many applications. It was an LVDS interface that was originally known as FPD-Link from National back in the early 1990s. National invented both FPD-Link and LVDS. Eventually TI second sourced it with their FlatLink family. This standard evolved to Open LDI (LVDS Display Interface) targeted at both Notebook and Monitor displays. It is a reduced pin count interface (compared to parallel RGB888) and uses LVDS levels for lower EMI. This interface is found as a common video output on many sources, and is also used as inputs to many displays. Altera FPGAs and CPLDs can not only be used to economically interface with OpenLDI devices, but to process the video data and perform countless other system functions as well. These interface blocks are designed to connect seamlessly with the Video and Image Processing Suite (VIP Suite) Clocked Video Input II (CVI) and Clocked Video Output II (CVO) components.

2. Overview of the Design Archive

Once extracted (you may double-click on the embedded icon below), the OpenLDI IP archive (OpenLDI_IP.zip) contains the following directories:

source

Contains all design files for the OpenLDI interface IP. This directory may be referenced by your “user_components.ipx” file, in your top-level Qsys directory.

3. Architecture

The OpenLDI RX block accepts and deserializes 18/24-bit single or dual pixel mode unbalanced OpenLDI video inputs (utilizing either JEIDA 24 bpp or SPWG/PSWG/VESA 18/24 bpp data mapping), and reformats the data into RGB 8:8:8 or RGB 6:6:6 mapping. The OpenLDI TX block preforms the same operation, but in reverse. It accepts RGB data, reformating it into an OpenLDI output stream.

3.1. OpenLDI Receive Interface

The OpenLDI RX interface is comprised of three blocks: *OpenLDI_RX*, , *Des_Align_SM*, and *openldi2rbg. OpenLDI_RX* contains the hard deserialization block to convert the differential 3-, 4-, 6-, or 8-lane OpenLDI data input into a parallel 21-, 28-, 42- or 56-bit data stream. The *Des_Align_SM* block is a state machine controller that is used to initially provide the correct word alignment on the OpenLDI receive interface. Upon power-up, the state machine will reset the alignment of the deserializer to a known state and then provide the required bit slipping to achieve alignment. In addition, it also allows the user to dynamically provide additional bit-slipping via the SLIP_ALIGNR input (in case there is unexpected skew on the receive interface that is beyond what is allowed per the OpenLDI spec). The default amount of bit-slip can be set via the "Default bit slip" parameter for the interface. Next, the data is sampled by a bank of flip-flops, to control skew and maintain timing. Lastly, it is decoded into RGB data by the *openldi2rbg* block.

3.1.1. RGB Conversion

The *openldi2rbg* block accepts parallel 21-, 28-, 42-, or 56-bit OpenLDI data, and decodes it into 18-, 24-, 36-, or 48-bits of RGB data and control. The mapping is configurable, and can use either SPWG/PSWG/VESA 18/24 bpp, or JEIDA 18/24bpp Unbalanced Data Mapping.

When designing a system that is either in 18bpp mode, or interfaces to components that are in 18bpp mode, it is important to understand how the data will be received by the OpenLDI IP blocks. Specifically, how was the data transmitted, is the data 24 or 18 bits wide, and should the MSBs be dropped to provide 18bpp, or the LSBs be zeroed to provide 24bpp for processing by the internal logic.

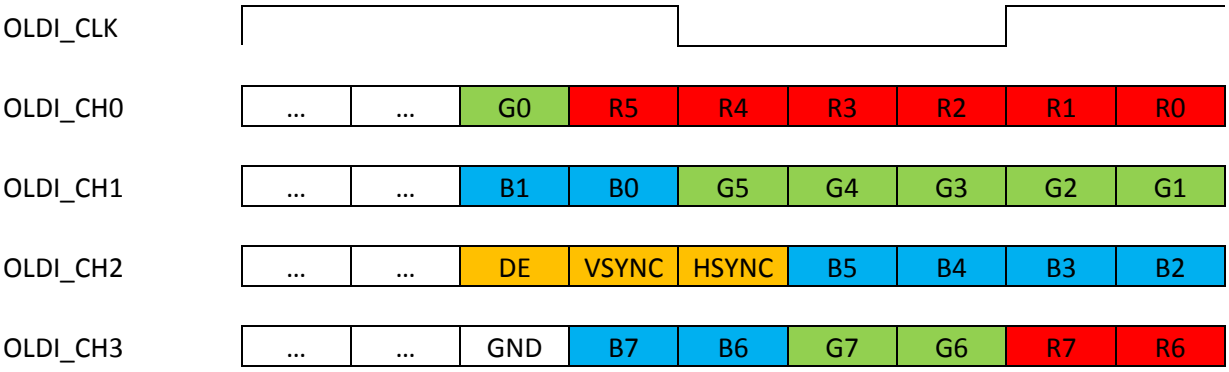

Figure 1: OpenLDI SPWG/PSWG/VESA 18/24 bpp data mapping and timing

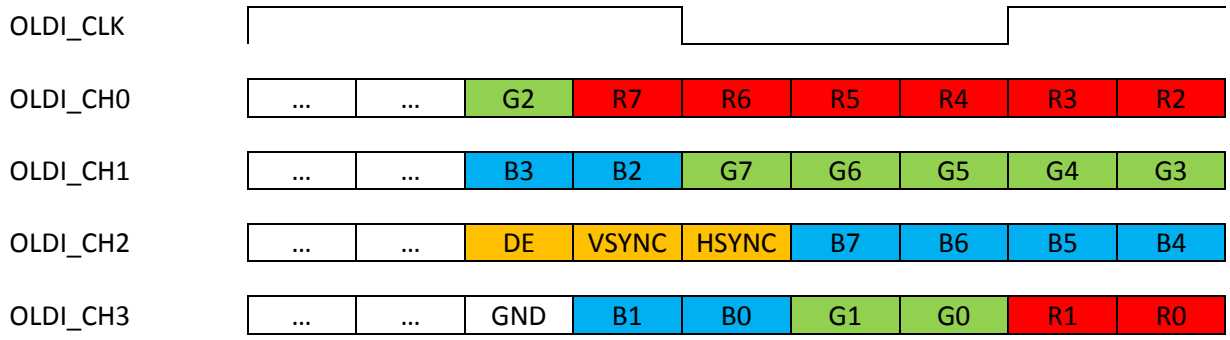

Figure 2: OpenLDI JEIDA 24 bpp data mapping and timing

3.1.2. Word Alignment State Machine

The *Des_Align_SM* allows the designer to adjust the alignment of the 7-bit OpenLDI words that are received by the LVDS interface. This can be done by either adjusting the initial (power-on) alignment via the "Default bit slip" parameter in the interface (shown below in Figure 5), or by sending pulses on the "SLIP_ALGNR" signal. Bit slipping is edge-sensitive, and each rising edge will cause the deserializer to shift the data right by one bit position. Once the state machine detects a rising edge on SLIP_ALGNR, it will respond via a handshake signal by asserting SLIP_ACK (as shown in Figure 3). At this point, the user may deassert SLIP_ALGNR.

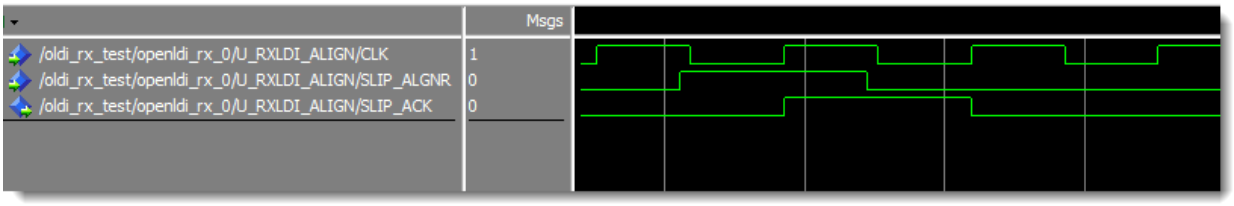

Figure 3: Word Alignment Control Timing

The appropriate number of shifts should ultimately be determined on your hardware system, and can most easily be determined by monitoring the RGB data, looking at the DE, VSYNC, and HSYNC values on the output of channel 2. For example, the data around and before the yellow cursor in Figure 4 below shows what appears to be the HSYNC signal present on VSYNC. According to the OpenLDI specification (described previously in Figure 1 and Figure 2), we know that we would need to shift the data by one position to the right for the correct word alignment. After asserting SLIP_ALGNR for one pulse, the data is now properly aligned with the HSYNC signal occurring regularly once per line of video.

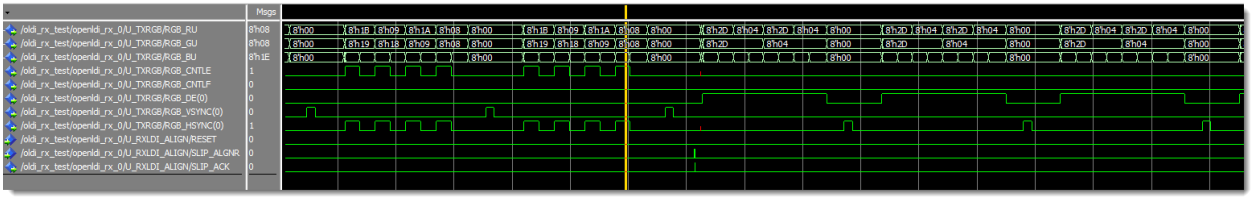

Figure 4: Effect of single bit-slip on RGB Data

3.1.3. IP Catalog GUI Parameterization for OpenLDI_RX

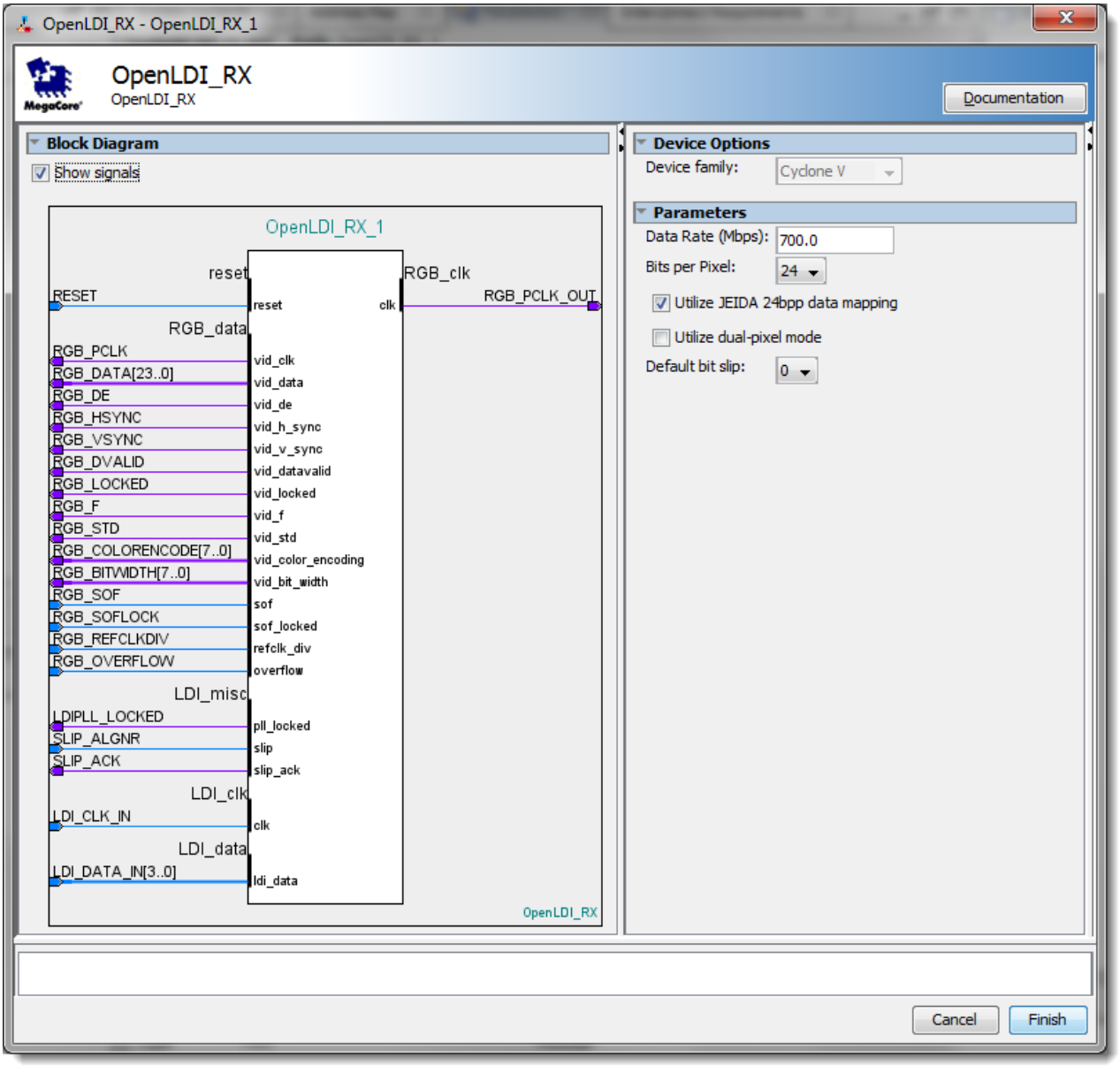

Figure 5: IP Catalog Parameterization for OpenLDI_RX

The following table describes the parameters available in the GUI.

PARAMETER	DESCRIPTION
Data Rate (Mbps)	Data Rate for the Open LDI interface, which should be 7x the pixel clock rate.
Bits per Pixel	Number of bits used per pixel (18 or 24 are the only legal values).
Utilize JEIDA 24bpp data mapping	Allows you to select either JEIDA or SPWG/PSWG/VESA data mapping for 24bpp mode.
Utilize dual-pixel mode	Dual-pixel mode will utilize a 6 or 8 channel LVDS interface, instead of a 3 or 4 channel interface.

PARAMETER	DESCRIPTION
Default bit slip	Number of bits the LVDS interface should slip after device configuration, in order to achieve byte alignment. This should be a static amount for your system, depending on clock/data skew, and is not normally required to be adjusted. Due to differences in the serializer, the following values are recommended defaults for the following device families: Max 10: 5 Cyclone IV: 5 Cyclone V: 1 Arria V: 1 Arria 10: 1 Stratix V: 1

Table 1: OpenLDI RX Parameter Description Table

3.2. OpenLDI RX Signal Description

The following table describes the I/O for the OpenLDI RX component.

NAME	DIRECTION	DESCRIPTION
RESET	Input	Global hardware reset. This signals flushes out the data path and state machines on the OpenLDI interface. Active high input.
LDI_CLK_IN	Input	Clock signal for OpenLDI receive interface (LVDS).
LDI_DATA_IN	Input	Data signals for OpenLDI receive interface (LVDS).
RGB_PCLK_OUT	Output	Pixel clock for RGB interface (additional copy of clock present in the RGB_Data Conduit)
LDI_Misc Conduit		
LDIPLL_LOCKED	Output	Indicates that the RX PLL is locked to the LDI_CLK_IN signal
SLIP_ALIGNR	Input	Asynchronous request to slip the data (rotate right) by one bit. It is rising-edge sensitive.
SLIP_ACK	Output	Acknowledge signal, indicating that the slip request was processed and can be released.
RGB_Data Conduit		Conduit that interfaces the RGB data to the Clocked Video Input (CVI) II component
RGB_PCLK	Output	Pixel clock for RGB interface
RGB_DATA	Output	RGB Pixel data. Depending on configuration, this can either be single or dual pixel data, as RGB 8:8:8 or RGB 6:6:6
RGB_DE	Output	RGB Data Enable signal
RGB_VSYNC	Output	Vertical Sync
RGB_HSYNC	Output	Horizontal Sync
RGB_DVALID	Output	RGB video data valid signal.
RGB_LOCKED	Output	RGB video locked signal.
RGB_F	Output	RGB video field signal.
RGB_STD	Output	Required by the CVI II component – set to zero.
RGB_COLORENCODE	Output	Required by the CVI II component – set to zeroes.
RGB_BITWIDTH	Input	Required by the CVI II component – set to zeroes.
RGB_SOF	Input	Unused - Start of frame signal from the CVI II component.
RGB_SOFLOCK	Input	Unused - Start of frame locked signal from the CVI II component.

NAME	DIRECTION	DESCRIPTION
RGB_REFCLKDIV	Input	Unused - A single cycle pulse, in-line with the rising edge of the HSYNC, from the CVI II component.
RGB_OVERFLOW	Input	Unused - Clocked video overflow signal from the CVI II component.

Table 2: OpenLDI RX Signal Table

3.3. OpenLDI Transmit Interface

The OpenLDI TX interface is comprised of two blocks: *OpenLDI_TX* and *rgb2openldi. OpenLDI_TX* contains the hard serialization block to convert the parallel 21-, 28-, 42- or 56-bit data stream into a differential 3-, 4-, 6-, or 8-lane OpenLDI data output. The *rgb2openldi* block encodes the RGB data according to the OpenLDI specification, prior to it being serialized by the *OpenLDI_TX* block.

3.3.1. RGB Conversion

The *rgb2openldi* block accepts 18-, 24-, 36-, or 48-bits of RGB data and control, and encodes it into parallel 21-, 28-, 42-, or 56-bits of OpenLDI data. The mapping is configurable and can use either SPWG/PSWG/VESA 18/24 bpp, or JEIDA 18/24bpp Unbalanced Data Mapping (as shown in Figure 1 and Figure 2).

When designing a system that is either in 18bpp mode, or interfaces to components that are in 18bpp mode, it is important to understand how the data will be transmitted from the OpenLDI IP blocks. Specifically, is the data 24 or 18 bits wide, and should the MSBs be dropped, or the LSBs be zeroed. For example, if the design is using VIP suite components that are set to 6 bits per pixel per color plane, it is necessary to deselect “Utilize JEIDA 24bpp data mapping”, since bits 5:0 are significant, not bits 7:2.

3.3.2. IP Catalog GUI Parameterization for OpenLDI_TX

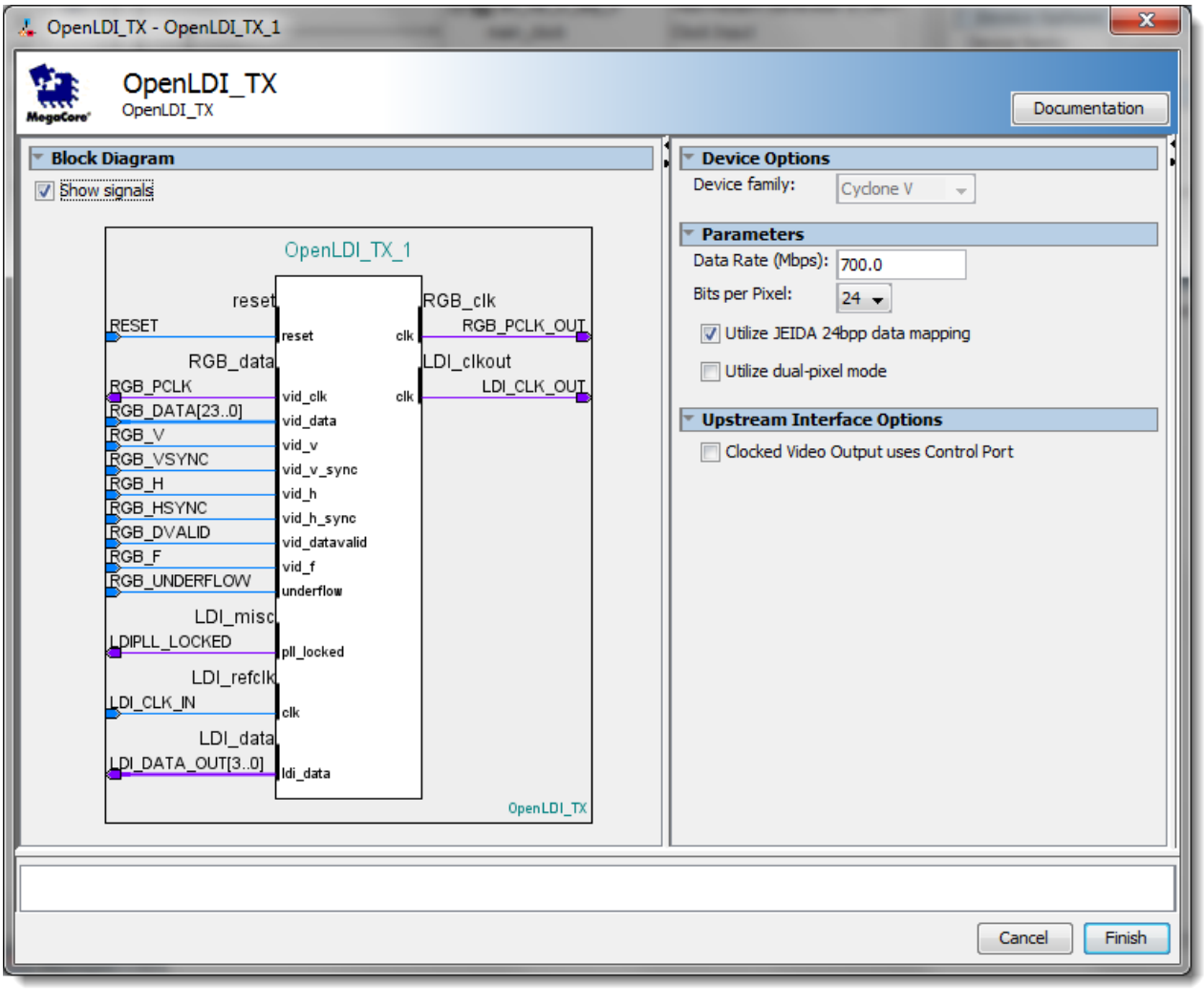

Figure 6: IP Catalog Parameterization for OpenLDI_TX

The following table describes the parameters available in the GUI.

PARAMETER	DESCRIPTION
Data Rate (Mbps)	Data Rate for the Open LDI interface, which should be 7x the pixel clock rate.
Bits per Pixel	Number of bits used per pixel (18 or 24 are the only legal values).
Utilize JEIDA 24bpp data mapping	Allows you to select either JEIDA or SPWG/PSWG/VESA data mapping for 24bpp mode.
Utilize dual-pixel mode	Dual-pixel mode will utilize a 6 or 8 channel LVDS interface, instead of a 3 or 4 channel interface.
Clocked Video Output uses Control Port	If your CVO II block uses the control port, you need to check this box in order to allow the RGB_data conduit to directly connect to the clocked_video port on CVO II.

Table 3: OpenLDI TX Parameter Description Table

If you receive errors in Qsys similar to *Error: alt_vip_cl_cvo_0.clocked_video has a vid_mode_change signal, but OpenLDI_TX_0.RGB_data does not*, you need to check the box for “Clocked Video Output uses Control Port”

3.4. OpenLDI TX Signal Description

The following table describes the I/O for the OpenLDI TX component.

NAME	DIRECTION	DESCRIPTION
RESET	Input	Global hardware reset. This signals flushes out the data path and state machines on the OpenLDI interface. Active high input.
LDI_CLK_IN	Input	Reference clock signal for OpenLDI transmit interface (LVDS). This needs to be equivalent to the pixel clock rate (1/7 the frequency of the data rate).
LDI_DATA_OUT	Output	Data signals for OpenLDI transmit interface (LVDS).
LDI_CLK_OUT	Output	Clock output signal for the OpenLDI transmit interface (LVDS).
RGB_PCLK_OUT	Output	Pixel clock for RGB interface (additional copy of clock present in the RGB_Data Conduit)
LDI_Misc Conduit		
LDIPLL_LOCKED	Output	Indicates that the TX PLL is locked to the LDI_CLK_IN signal
RGB_Data Conduit		Conduit that interfaces the RGB data to the Clocked Video Output (CVO) II component
RGB_PCLK	Output	Pixel clock for RGB interface
RGB_DATA	Input	RGB Pixel data. Depending on configuration, this can either be single or dual pixel data, as RGB 8:8:8 or RGB 6:6:6
RGB_V	Input	When 1, indicates that the video is in a vertical blanking period.
RGB_VSYNC	Input	Vertical Sync
RGB_H	Input	When 1, indicates that the video is in a horizontal blanking period.
RGB_HSYNC	Input	Horizontal Sync
RGB_DVALID	Input	Unused: RGB video data valid signal.
RGB_F	Input	Unused: RGB video field signal.
RGB_UNDERFLOW	Input	Unused - Clocked video underflow signal from the CVO II component.
RGB_VID_CHANGE	Input	Unused, and only visible when “CVO uses control port” option is checked. It indicates a change to the video mode.
RGB_VID_STD	Input	Unused, and only visible when “CVO uses control port” option is checked. It indicates the current video standard that is being used.

Table 4: OpenLDI TX Signal Table