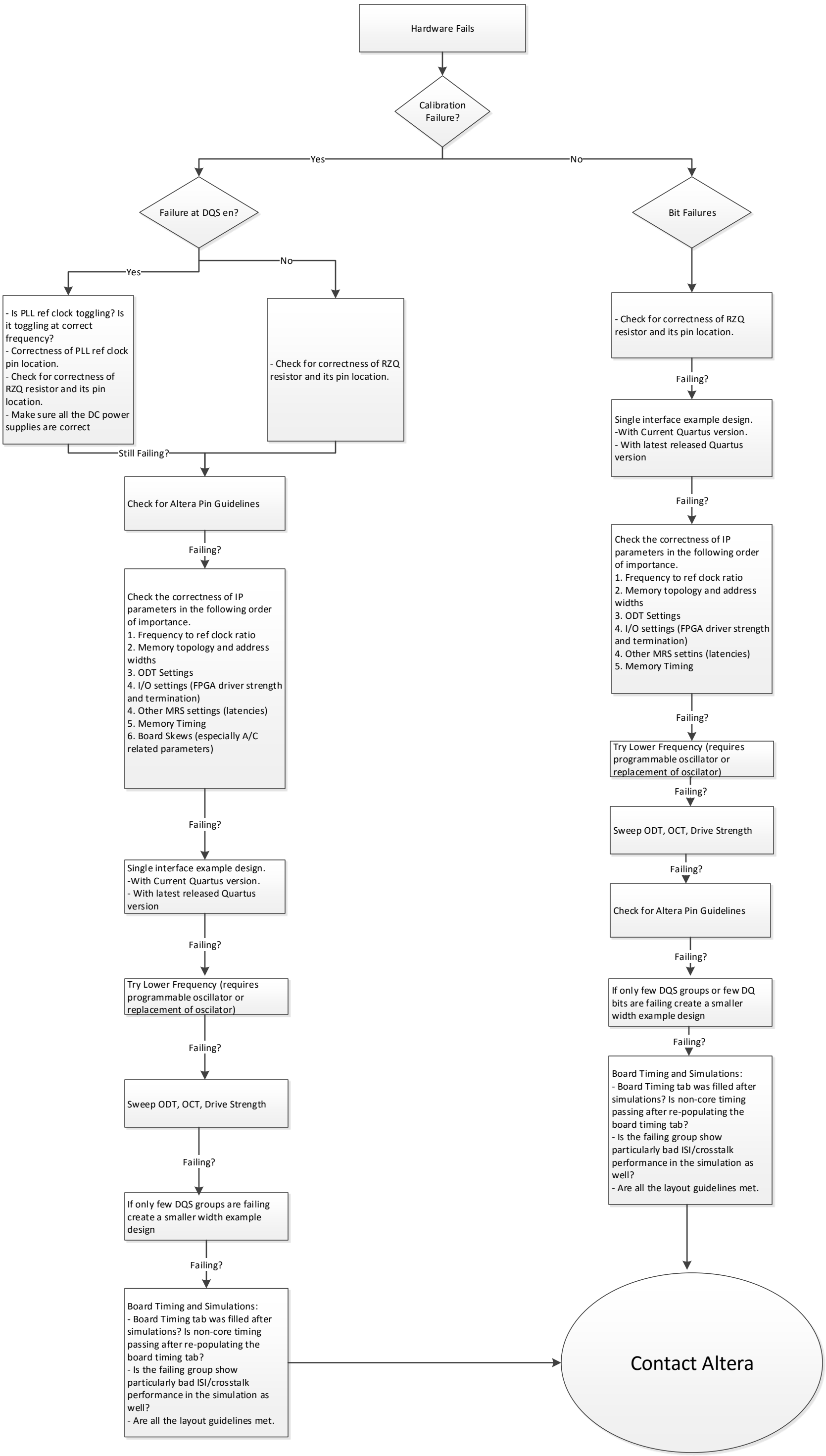
Hardware Fails
Calibration Failure?
Yes
No
Failure at DQS en?
Bit Failures
Yes
No
- Is PLL ref clock toggling? Is it toggling at correct frequency?
- Correctness of PLL ref clock pin location.
- Check for correctness of RZQ resistor and its pin location.
- Make sure all the DC power supplies are correct
- Check for correctness of RZQ resistor and its pin location.
Still Failing?
Check for Altera Pin Guidelines
Failing?
Check the correctness of IP parameters in the following order of importance.
1. Frequency to ref clock ratio
2. Memory topology and address widths
3. ODT Settings
4. I/O settings (FPGA driver strength and termination)
4. Other MRS settings (latencies)
5. Memory Timing
6. Board Skews (especially A/C related parameters)
Failing?
Single interface example design.
-With Current Quartus version.
- With latest released Quartus version
Failing?
Try Lower Frequency (requires programmable oscillator or replacement of oscilator)
Failing?
Sweep ODT, OCT, Drive Strength
Failing?
If only few DQS groups are failing create a smaller width example design
Failing?
Board Timing and Simulations:
- Board Timing tab was filled after simulations? Is non-core timing passing after re-populating the board timing tab?
- Is the failing group show particularly bad ISI/crosstalk performance in the simulation as well?
- Are all the layout guidelines met.
- Check for correctness of RZQ resistor and its pin location.
Failing?
Single interface example design.
-With Current Quartus version.
- With latest released Quartus version
Failing?
Check the correctness of IP parameters in the following order of importance.
1. Frequency to ref clock ratio
2. Memory topology and address widths
3. ODT Settings
4. I/O settings (FPGA driver strength and termination)
4. Other MRS settins (latencies)
5. Memory Timing
Failing?
Try Lower Frequency (requires programmable oscillator or replacement of oscilator)
Failing?
Sweep ODT, OCT, Drive Strength
Failing?
Check for Altera Pin Guidelines
Failing?
If only few DQS groups or few DQ bits are failing create a smaller width example design
Failing?
Board Timing and Simulations:
- Board Timing tab was filled after simulations? Is non-core timing passing after re-populating the board timing tab?
- Is the failing group show particularly bad ISI/crosstalk performance in the simulation as well?
- Are all the layout guidelines met.
Contact Altera