WHITE PAPER

FPGA

Understanding and Meeting FPGA Power Requirements

Power is a system-level concern; developers should create power consumption estimates and power trees to meet design requirements as early as possible.

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Introduction

With all the advantages of an FPGA's flexible implementation comes one growing challenge: powering the FPGA to ensure seamless operation. This white paper aims to identify the sources of complexity with powering an FPGA, describes what trade-offs in designing the FPGA power tree must be considered, and explores how and why FPGA power is truly—and increasingly—a system-level concern.

What determines FPGA power requirements?

The power consumption needs of an FPGA are determined by the sum of fixed and variable conditions: the static power consumption, driven by process technology and silicon design, and the dynamic power consumption, driven by each design's unique utilization.

The dynamic power is a product of the quantity and specific use of each resource, and is a function of the additional power consumption caused by signals toggling and capacitive loads charging and discharging. As a result, more heavily loaded FPGA designs as well as designs with higher clock frequencies will consume more power. For example, the use of general-purpose I/O pins and high-speed serial transceivers impacts the total power requirements since considerations like I/O standards used and data rates expected determine how fast the I/Os toggle and how fast the logic must be clocked. As expected, the faster the data rates and the higher the clock frequency required, the higher the power consumption as the loads must be charged and discharged more frequently. With multiple factors determining an FPGA's power requirements, it is expected that these power requirements will vary broadly, both across different FPGA families as well as for different use cases of the exact same FPGA.

Because understanding the power requirements of an FPGA design can be complex—and is important—most FPGA suppliers offer power estimation tools. Intel provides a suite of PowerPlay power analysis tools, including the PowerPlay Early Power Estimator spreadsheet that estimates the power consumption of an FPGA system early in the design process, and the PowerPlay Power Analyzer tool embedded within the Intel® Quartus® Prime software that outputs an accurate analysis of power after the design is complete to ensure that thermal and supply budgets are not violated.

Translating FPGA power consumption to power converter requirements

Understanding the raw power requirements for each power rail of an FPGA is only the first step in designing an appropriate power tree; a variety of additional

requirements and considerations must be evaluated to maximize the performance of a design, given its specific resource utilization.

Core power

The most power-hungry input on an FPGA will usually be the core power rail, often denoted as V_{CC}. This is understandable because the core power rail drives the logic, the use of which is central to any FPGA design. As FPGA offerings push logic quantities to extraordinary levels, so too is the potential power required growing.

For example, Intel's Generation 10 FPGAs and SoCs, the Intel Arria® 10 and Intel Stratix® 10 series, take advantage of higher densities associated with smaller process geometries to offer devices with over 1 million logic elements (LEs). And, while the power consumption of each logic element is lower than previous generations, highly utilized, high-frequency designs could require core currents in excess of 100 A.

In addition to being able to meet high power demands, core power supplies must also meet stringent steady-state and transient power rail requirements. The steady-state requirement is the ability to maintain the steady-state DC voltage of the core input, regardless of how the core logic is utilized—or, in simpler terms, how accurately the power supply regulates to the core input voltage. As depicted in Table 1, the actual requirement for a given FPGA is usually found in the data sheet or DC Operating Characteristics and is shown as the tolerance—or minimum and maximum deviation—for the expected V_{CC} voltage value. As FPGA technology advances to shrinking process nodes, so too has the allowed tolerance shrunk, putting even more importance on understanding and considering core rail power supplies.

The steady-state DC regulation of a power supply is impacted primarily by two items: voltage regulation accuracy and output voltage ripple. Voltage regulation accuracy of a power supply is straightforward and found in any power converter datasheet. As a rule of thumb, a typical or good converter accuracy will be at or better than ±2%. Output voltage ripple is the small, unwanted variation on the output voltage that occurs as a result of the load energy transfers during the on and off cycles of a switching converter. This means ripple is impacted not only by the converter integrated circuit (IC) design but also system design considerations including layout and external components that introduce parasitic capacitances and inductances. Together, the accuracy and ripple of an acceptable power converter must be less than the core tolerance requirement.

- For more details about meeting core voltage rail static power requirements, see the video Power Management For FPGA Users: Core Power Requirements.

The dynamic load requirements of the core rail are driven by the ability of FPGAs to quickly engage and disengage resources, which can result in very large and fast changes in the immediate input power requirements. For example, the need for significantly more logic to carry out a function could drastically change the dynamic power consumption of the core input. There are bulk capacitors near each FPGA power rail whose purpose are to provide instantaneous current during load steps; however, the transient response of a power supply used for the core power rail must also adjust to the load change quickly in order to ensure that the power rail voltage stays within the acceptable range and the bulk capacitors are recharged. Achieving the right balance of bulk capacitance and fast power converter transient response is especially critical for the core power rail.

The ideal power converter for the core power rail will combine high regulation accuracy, low-ripple, and fast-transient response. One way to achieve these requirements is to use a switching converter with a high switching frequency, which provides multiple advantages. First, a higher switching frequency enables the use of smaller, lower value inductors and capacitors and allows for a dense layout that reduces parasitic inductance and capacitance. Secondly, a higher switching frequency also enables wider control loop bandwidth, which in turn means that a converter can respond to load changes more quickly and, coupled with smaller bulk capacitance, operate with less over- or undershoot. Not only will the faster transient response ensure seamless operation, reducing bulk capacitance saves significant board space and cost as bulk capacitors are generally large and expensive. The benefit is demonstrated in Figure 1, which shows a Cyclone® V SoC design using standalone switching regulators compared to the same design with Intel Enpirion® Power Solutions. Enpirion Power Solutions are designed to operate at high switching frequency and utilize unique magnetics and package integration to deliver a very dense footprint with minimal inductance and capacitance, which allows the devices to achieve low-ripple and fast-transient response. When used with the Cyclone V SoC design, the Enpirion Power Solution shrank the power supply footprint by 22%, reduced power loss by 35%, and cut the required bulk capacitance in half by eliminating the need for five large, expensive tantalum capacitors.†

Noise-sensitive inputs

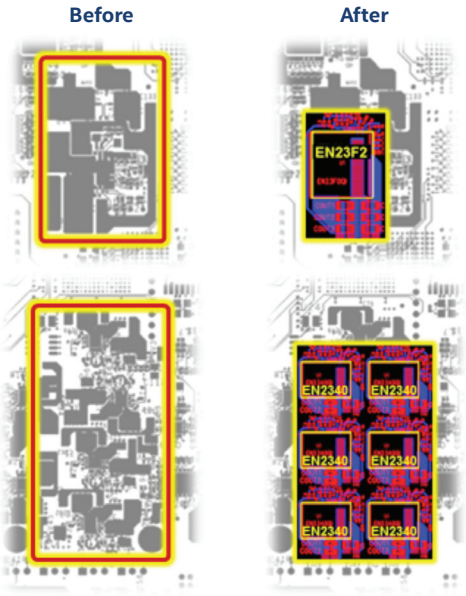
While logic is the primary building block of an FPGA's fabric, FPGAs also implement a number of additional blocks like phase-locked loops (PLLs), which are used inside the FPGA to align the rising edge of the reference input clock to a feedback clock, and high-speed transceivers, which are integral to many network, communications, storage, and

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply (C1, C2, and 12 speed grades)	—	0.87	0.90	0.93	V
	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, 13, 13L, and 14 speed grades)	—	0.82	0.85	0.88	V

[1] Example V_{CC} core voltage power supply operating conditions for the Stratix V FPGA, as shown in Table 6 of the Stratix V data sheet. In this example, the Stratix V core input must be supplied with either 0.9 V or 0.85 V, depending on the speed grade variant, with ±30 mV allowable steady-state DC voltage tolerance.

Table 1. Example VCC Core Voltage Power Supply Operating Conditions (1)

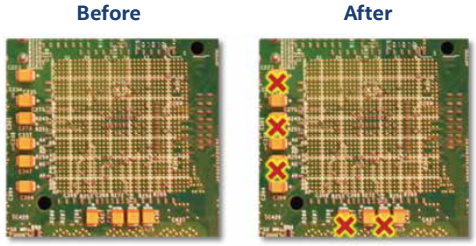
(2a)



(2b)

Measured Results	Before	After
Power Conversion Efficiency	79%	85%
DC/DC Converter Consumption (Normalized)	1.00	0.65

(2c)



Replacing the existing power supply solution with Enpirion Power Solutions on the Cyclone V SoC Development Kit shrank the power supply footprint by 22%† (2a), reduced power loss by 35%† (2b), and cut the required bulk capacitance in half, reducing size and cost by eliminating expensive tantalum capacitors† (2c).

Figure 1. Using Enpirion Power Solution

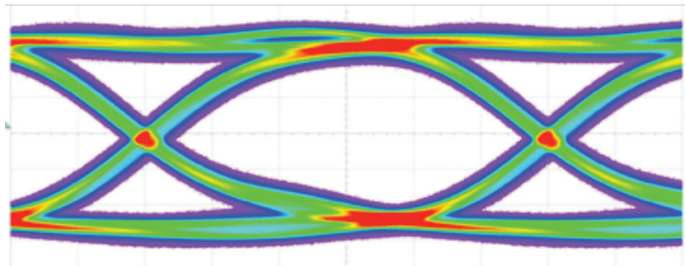
other electronic systems. These circuit blocks are sensitive to power supply noise because it can lead to jitter generation, which can in turn cause an unacceptably high bit error rate (BER) and poor circuit performance. The challenge of maintaining signal integrity is made more difficult as FPGAs and the end applications that they are used for continue to drive increasingly faster edge rates.

As a result, the power supply inputs for these blocks in the FPGA require special care to ensure power rail noise is minimized. Occasionally, if the sensitive power rail shares the same voltage requirement as another regulated power rail in the system, a small, cheap filter such as a ferrite bead can be used. In many cases, though, a power converter with sufficiently low output noise is required to deliver a specific, regulated voltage. Traditionally, FPGA board designers have simply used Low Drop-Out linear regulators (LDOs), which often have high Power Supply Rejection Ratio (PSRR) and, by definition, generate no switching noise. However, linear regulators are also extremely inefficient, and as transceiver power consumption demands rise and total system power budgets get increasingly more constrained, the power waste and excess heat generated can cause even worse system challenges.

To address this challenge, many of Enpirion's Power Solutions can be used with sensitive FPGA power rails because they have been designed to deliver the noise performance of an LDO while maintaining the high efficiency of a switching regulator. This is shown in Figure 2 by the wide open eye diagram of a high speed signal on a Stratix V GX FPGA board, for which an Enpirion Power Solution is used to supply the transceiver power rails. This low-noise performance is achieved through a combination of high-frequency silicon design, efficient switch FET technology that minimizes switch loss even at high-frequency operation, and unique package construction that minimizes parasitic inductance.

Power is a system-level concern

With power rails that often have special hardware and interoperability requirements and current requirements that vary depending on each user's unique design, it is important to consider FPGA power management as early in the design process as possible. System-level decisions including power supply grouping and sequencing, digital control, and hardware design have higher level system performance, cost, and design time implications with risks that can be mitigated with proper planning.



Low T_J = 19.32 ps
Efficiency > 80%†

Eye diagram of an 11.3 Gbps signal on a Stratix V GX FPGA board. An EN6337QI Enpirion Power Solution was used to convert V_{IN} = 3.3 V to V_{OUT} = 1.0 V for the VCCRT_GXB and VCCA_GXB transceiver pins. An LDO tested under identical conditions resulted in T_J = 19.89 ps with only 30% efficiency.†

Figure 2. Eye Diagram

Power rail grouping and sequencing

An FPGA will have a number of input pins that require power, but it is not necessarily required for each FPGA power rail input to have a dedicated power supply. For each FPGA, Intel provides a Pin Connection Guidelines document that, in addition to providing details about every pin, also includes recommended power trees that group various similar power rails. This Pin Connection Guideline document is found through each FPGA device's product page on www.altera.com. An example recommended power tree is shown in Figure 3.

Together, all the power supplies needed for an FPGA design create an FPGA power tree that may also have special requirements which impact the selection and use of power converters. For example, many advanced FPGAs require sequencing—by which, different resources within the FPGA, and therefore different voltage rails, must be powered on before other resources can be powered on. This requires that each power supply have an enable pin and the ability to communicate when the power supply is on and regulating to the desired voltage. Several Enpirion devices, such as the EN6360QI, support this with a Power OK or Power Good pin that can be used to signal to a system controller or sequencing device that the power supply has turned on the specific FPGA input and the next sequence step can begin.

Digital control

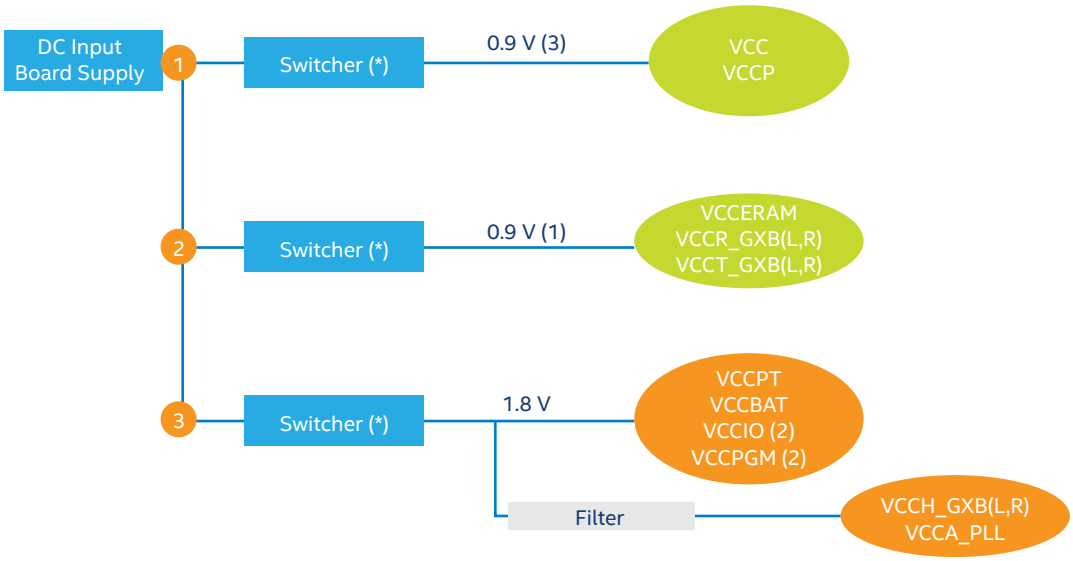
Another common system power requirement is the ability to perform telemetry—a process by which system parameters are remotely measured and communicated to a receiving system for monitoring. Parameters like input voltage, output voltage, output/load current, and temperature are all valuable pieces of information to enable more intelligent system power monitoring and optimization. For example, a system designer may want to monitor the load current and temperature to ensure that the FPGA is operating as expected, and flag a system monitor to investigate or replace an FPGA board that is operating erroneously or is too hot. Another example is that a system designer may want to log power consumption of an FPGA over a variety of use cases and use that knowledge to dynamically throttle a specific FPGA's performance or portions of a system that may not be needed in order to reduce system power for a greener, more cost effective piece of end equipment. This kind of system condition monitoring can be implemented in a few ways, but the easiest, cheapest, and most compact way is by using a power regulator with integrated telemetry and an appropriate communication bus.

Intel Arria 10 FPGAs and SoCs also integrate power reduction features that deliver the lowest power when combined with advanced power converters. The primary example is Smart Voltage ID (SmartVID), a feature by which the FPGA communicates with a compatible power supply to dynamically adjust the core voltage rail to the lowest possible level without sacrificing system performance. A compatible power supply supports this communication with industry-standard interfaces and controls, such as a parallel VID interface or PMBus interface, to perform the output voltage adjustment. Figure 4 provides an example of how SmartVID is implemented in an FPGA system.

An example solution is Intel's ED8101P0xQI single-phase digital controller with PMBus support that, when paired with the ET4040QI high-current powertrain, enables FPGA users to implement a wide range of telemetry and power reduction features. This includes:

- Monitoring of system input and output parameters, such as voltage, current, and temperature
- Monitoring for system faults, such as over- and under-voltage and over-temperature conditions
- Dynamic output voltage adjustment to support SmartVID

To implement SmartVID, the FPGA determines the desired V_{CC} voltage and communicates to the voltage regulator system using the PMBus interface, where the voltage



Example recommended power tree for an Arria 10 GX with transceiver data rate ≤11.3 Gbps and using the SmartVID feature.

Figure 3. Arria 10 GX Recommended Power Tree

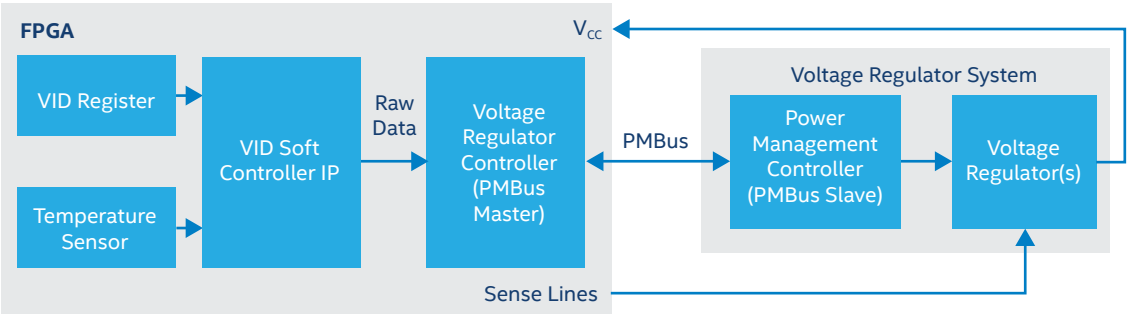


Figure 4. SmartVID Implementation

regulator system is the total core power rail power converter solution. Using these Enpirion solutions, the power management controller can be implemented using the ED8101P0xQI and the voltage regulator(s) can be implemented using the ET4040QI.

Hardware design

Early planning of the power tree for an FPGA design is critical because there are many system hardware design implications that can impact design complexity, cycle time, and cost. While exact power requirements are impossible to know at the onset of a design, putting careful thought in to FPGA power consumptions estimates enables the user to create a power tree that is close to the final, optimal design. The first benefit of this is that the hardware designer will be able to properly place the required power converters even on the initial board designs. This is important because FPGA systems face increasing printed circuit board (PCB) density challenges as users add more functionality, and therefore more components, while shrinking form factors. If the power tree is not planned during PCB layout, then users face the risk of having to place the power converters in a non-ideal location far from the FPGA with several disadvantages. For example, users may be forced to fit in appropriate power converters in limited PCB space in the wrong area of the board where cooling, solution profile, and distance from the FPGA can present difficult hardware challenges including the need for larger, more expensive bulk capacitors and degraded performance. Worse yet, the user risks not having sufficient space for the power converters at all.

The second benefit of early power tree planning is achieving enough design flexibility to meet the power consumption requirements of the final FPGA design without requiring significant redesign. A core competency of an FPGA is the ability to integrate features and capabilities, even within the design cycle, and greater integration leads to greater power consumption. Scaling and optimizing an initial power tree that is close to the final design is significantly easier and faster than designing a new power tree when an initial design was too inaccurate. In a world where companies are under pressure to deliver in the shortest possible cycle time, minimizing the risk, cost, and extra time needed for board spins to change a poorly planned power tree is a huge advantage that can enable system designers to get products to market, and revenue, faster than their competition.

Intel provides a number of tools for planning and creating an FPGA power tree, described in Table 2.

Tool	Overview
PowerPlay Early Power Estimator (EPE)	Estimates power consumption of an initial FPGA design and integrates FPGA power rail groupings with power converter recommendations
PowerPlay Power Analyzer	Delivers accurate power consumption analysis after FPGA design complete, ideal for ensuring power tree and thermal design meet final requirements
PowerPlay Power Tree Designer	Enables user to create a system power tree block diagram by simply uploading a completed EPE or entering initial power rail requirements
Power Distribution Network (PDN) design tools	Enables user to optimize the board level power distribution network by determining the required network of bulk and ceramic decoupling capacitors

Table 2. Intel FPGA Power Consumption Planning and Power Tree Design Tools

Conclusion

While the question about how a user powers their FPGA can only be answered with "it depends," understanding how FPGA design and usage impacts the power consumption and power supply requirements can bring better clarity and less design frustration. FPGA power consumption is driven by static and dynamic power requirements, the second of which depends heavily on each unique FPGA design. Regardless of the design, however, there are certain common requirements for FPGA power supply design that can be used to simplify and guide system design decisions. Intel's Enpirion power solutions have been designed to meet these challenging FPGA power requirements.

Utilizing low-ripple, fast-transient response power converters from Enpirion, for example, can ensure that the stringent static and dynamic core voltage requirements are met for seamless operation during all load conditions. Similarly, using low-noise Enpirion Power Solutions instead of linear regulators for sensitive FPGA voltage rails can ensure that signal integrity, power efficiency, and thermal budget goals are met. And lastly, implementing differentiated system features such as telemetry and power reduction is possible by using advanced power converter solutions such as Enpirion's ED8101P0xQI digital controller with PMBus and ET4040QI high-current powertrain.

With the flexibility of an FPGA design, power is truly a system-level concern requiring the effort to estimate an FPGA's power consumption and architecting a power tree to meet the design's unique requirements as early as possible. The benefit will be a more optimal system design that can be completed more quickly, with fewer resources, and with the right performance characteristics to deliver a strong competitive edge.

Further information

[1] www.altera.com/support/devices/estimator/pow-powerplay.jsp
[2] www.altera.com/support/software/power/sof-qts-power.html?GSA_pos=9&WT.oss_r=1&WT.oss=power%20analyzer
[3] www.altera.com/servlets/power-designer
[4] www.altera.com/technology/signal/power-distribution-network/sgl-pdn.html?GSA_pos=5&WT.oss_r=1&WT.oss=pdn

Where to get more information

For more information about Intel and Enpirion Power Solutions, visit **https://www.altera.com/products/power/overview.html**

† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.