

This white paper examines how Altera's optimized and verified intellectual property (IP) blocks can simplify your design, reduce design issues, and shorten time to market. It also explains how Altera's Generation 10 FPGAs enables broad portfolio of complex IP—the broadest portfolio in the industry—to achieve a 50 percent reduction in size while achieving twice the performance of current devices.

Introduction

As electronic designs have become increasingly complex, designers are required to incorporate different types of functionality that they may not have the expertise, resources, or time to create. This has given rise to the semiconductor intellectual property (SIP) market, which is estimated to reach \$5.7 billion by 2017 ⁽¹⁾. With some complex designs utilizing as many as 100 different SIP blocks, integrating them into a design and then verifying that they work optimally with the underlying hardware is a major issue—one that grows more difficult at each new process node.

In addition, interoperability issues are compounded when using SIP blocks from multiple vendors because there is no standard to guide how these blocks are written or to be used in a particular design. Each of these blocks is likely to reflect different trade-offs between speed, power, and die size, not all of which can then be adequately addressed by the system on a chip (SOC) designer. Achieving an optimal design using multivendor IP blocks is a painstaking process at best.

Finally, if the industry keeps on the trajectory that it has been on for the last decade, implementing a 400 gigabits per second (Gbps) system will take up almost an entire 1 million logic elements (LEs) FPGA. This is an impossible situation for customers. Altera has seen this coming, and has re-architected its highest performing IP from scratch not only to make it faster in order to support exploding data rates, but also to provide smaller, more efficient IP. The new innovative architecture has resulted in IP blocks that are twice as fast but 50 percent smaller than anything previously available.

The Need for Speed

The explosive Internet growth has made high-speed data processing a critical capability. According to the international telecommunications Union (ITU) as of 2011 one third of the world's 7 billion people are using the Internet, generating network traffic at the rate of 80 terabits per second (Tbps), a 45 percent increase over the previous year ⁽²⁾.



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The next wave of Internet use is machine to machine (M2M) communications, the so-called Internet of Things (IoT). The IoT encompasses a wide variety of devices, including smart meters, wireless sensor nodes, industrial supervisory control and data acquisition (SCADA) systems, gateways, and highway toll tag readers. All of these will contribute heavily to data traffic on both public and private infrastructure. The IoT market was worth \$44 billion in 2011 and is expected to grow by 30 percent per year to \$290 billion by 2017 ⁽³⁾.

With consumers all having mobile phones and expecting the rest of their gadgets to be wireless, mobile communications accounted for 55 percent of IP traffic in 2011—and it is growing at 66 percent per year. This represents a huge challenge for telecommunications companies, who are building 4G networks as quickly as possible ⁽⁴⁾. Base stations are increasingly reliant on high-speed FPGAs for the core performance needed to process complex functions over a wide range of frequencies. FPGAs also help safeguard the investment in 4G base stations by providing the flexibility to accommodate regional variations in a still-evolving standard.

According to Cisco—who makes many of the routers that make all this possible—Internet protocol traffic will exceed a Zettabyte (10^{21}) per year by the end of 2016 ⁽⁴⁾.

Data centers will be particularly hard-pressed to handle the increased traffic. While the trend to multicore processors addresses the power consumption issue, the bandwidth to external memory and data is not keeping pace with the increasing computing power. Here FPGAs can profitably be used for data access, algorithm, and networking acceleration, relieving the data access bottleneck. This will be increasingly important as cloud computing and software as a service (SaaS) continues to grow.

Next-generation FPGAs will leverage high-speed serial transceivers to overcome the bandwidth, latency, and power limitations of parallel memory interfaces. Arria® 10 FPGAs will be able to easily handle 100 Gbps and 200 Gbps data streams. Stratix® 10 FPGAs with multiple 56 Gbps transceivers will be able to process both 400 Gbps Ethernet (GbE) and 500 Gbps Interlaken traffic.

Altera IP: We've Got You Covered

While FPGAs can relieve the memory and I/O interface bottlenecks in 4G base stations and data center channel cards, an increase in datapath bandwidth and frequency is normally accompanied by a linear increase in power consumption. This is a key trade-off that Altera sets out to address—along with bandwidth and die size—across its wide range of IP cores.

Memory access is critical for any application. Altera® FPGAs provide an abundance of on-chip internal SRAM memory, but for those applications that require fast access to off-chip memory, Altera and its partners provide memory controller IP cores, reference designs, and design examples. All are hardware-tested drop-in design blocks that greatly simplify local interface to complex memory devices. Supported standards include:

- SDR SDRAM
- RLDRAM 2 or RLDRAM 3
- DDR SDRAM
- DDR2 SDRAM

- DDR3 SDRAM
- DDR4 SDRAM

Memory technology is moving forward rapidly and Altera is keeping pace. Micron's 3-D Hybrid Memory Cube (HMC) delivers up to 15 times the bandwidth of a DDR3 SDRAM module and uses 70 percent less energy while requiring 90 percent less board space than existing technologies. Altera and Micron recently demonstrated interoperability between Altera's 28 nm Stratix V FPGAs and Micron's HMC. Forthcoming Arria 10 and Stratix 10 FPGAs will all include an HMC interface.

For chip-to-chip, board-to-board, or box-to-box connectivity, Altera and its partners provide over 175 different connectivity IP cores and reference designs that leverage the transceivers integrated into their FPGA and ASIC devices—the list of Ethernet IP cores alone runs to almost 60 solutions. These interface protocols are available as licensable IP cores and reference designs, as well as free megafunctions and design examples. See Altera's All Intellectual Property web page for a complete listing of IP cores.

PCI Express® (PCIe®) is a leading backplane interconnect standard used in data centers. Altera makes PCIe Gen1 (2.5 Gbps) and Gen2 (5.0 Gbps) IP available throughout its Cyclone®, Arria, and Stratix FPGA product lines. The PCIe Gen3 (8.0 Gbps) is available in Stratix V FPGA with the protocol stack embedded as a hard IP block. The PCIe standard continues to be a focus in Generation 10 FPGAs as well. With the hardened implementation of the PCIe block, you get a resource savings of 8,000 to 30,000 LEs per IP instance, faster timing closure, shorter design and compile times, and substantial power savings relative to a soft IP core with equivalent functionality. All PCIe cores are verified to conform to the appropriate PCI Express Base Specification.

Smaller, Faster, Better

Altera's new low-latency 10GbE IP core is the first to benefit from the Generation 10 FPGA architecture. IP optimizations increase core performance from 156.25 MHz to 312.5 MHz. Table 2 compares the existing standard 10GbE IP cores with the new low-latency core. The size is 36 percent smaller and the speed 24 percent faster. This is impressive, but is only the beginning. The low-latency 40GbE IP core extends this benefit to a 40 percent reduction in both size and latency while the low-latency 100GbE IP core breaks conventional thinking with a 55 percent smaller footprint and 70 percent reduction in roundtrip latency. These IP cores show a dramatic improvement compared to the already outstanding core and truly best-in-class IP.

Table 1 lists the difference in size and speed for both standard and low-latency 10GbE IP core.

Table 1. 10GbE Core Size and Speed

	Standard 10GbE IP	Low-Latency 10GbE IP
10GbE MAC size	3,560	2,800
10GbE MAC + 10 GBASE-R PHY size	3,740	2,980
10GbE TX + RX latency	141 ns	60 ns
10GbE + 10 GBASE-R PHY latency	340 ns	260 ns

Table 2 lists the difference in size and speed for both standard and low-latency 40GbE IP core.

Table 2. 40GbE IP Core Size and Speed

	Standard 40GbE IP	Low-Latency 40GbE IP
40GbE MAC size	3,660 ALM	2,670 ALM
40GbE MAC+ PCS size	10,460 ALM	6,010 ALM
40GbE TX + RX latency	102.4 ns	70 ns
40GbE + PHY TX + RX latency	323.2 ns	179.2 ns

Table 3 lists the difference in size and speed for both standard and low-latency 100GbE IP core.

Table 3. 100GbE IP Core Size and Speed

	Standard 100GbE IP	Low-Latency 100GbE IP
100GbE MAC size	10,770 ALM	6,260 ALM
100GbE MAC + PCS size	34,450 ALM	15,300 ALM
100GbE TX + RX latency	212 ns	63.7 ns
100GbE + PHY TX + RX latency	519 ns	160.7 ns

The scalable Interlaken Protocol enables chip-to-chip packet transfers and rates from 10 Gbps to 100 Gbps and beyond. Interlaken was designed for multiterabit routers and switches for access, carrier Ethernet, and data center applications that demand high IP configurability to optimize for system performance and interoperability. Altera's Interlaken IP cores use a hardened PCS in Stratix V and Arria V FPGAs, saving 30 to 50 percent of logic resources compared to soft IP. Altera's IP cores have been through extensive simulation verification to ensure conformity with the Interlaken Protocol Specification v1.2. Table 4 summarizes the features and benefits of Altera's Interlaken IP:

Table 4. Features and Benefits of Altera's Interlaken IP

Features	Benefits
Data rates of up to 14 Gbps	Maximizes platform flexibility to increase bandwidth and insures scalability over time
Multilane configuration of up to 40 lanes	
Interleave (segment) mode and packet mode support	Flexible data handling enables improvements to overall system performance
Dual segment support	
Up to 256 logical channels	
In-band and out-of-band flow control (calendar page options)	Resilient data transmission due to unexpected failures or glitches and reliable data integrity over multiple media
Retransmission	
Tunable pre-emphasis and equalization settings	

While the low-latency 10GbE IP core is available today, the Interlaken and 40GbE and 100GbE IP cores are available for early access, with general availability scheduled for early 2014.

With hundreds of Altera IP solutions to choose from—all of which are thoroughly tested, verified, and optimized to work on the underlying hardware—designers can avoid integration headaches and get to market quickly with applications built around complex IP blocks that are guaranteed to play well together.

As data rates continue to rise and 100 Gbps bandwidth is quickly consumed, new high-speed protocols for 400 Gbps systems will represent a major hurdle for current hardware. With innovations in its Generation 10 FPGA architecture, Altera will be able to deliver 1 GHz FPGAs that yield a dramatic improvement in bandwidth while actually decreasing power consumption and die size. The Stratix 10 FPGAs will be able to process 400GbE and even 500 Gbps Interlaken.

Architecting Around Trade-offs

The question at this point is how Altera achieved such drastic latency and size improvements so quickly and on so many IP cores. The answer lies in both the architecture of the IP and in the architecture of the underlying FPGA silicon. In truth, it is the coupling of both that provides the outstanding improvements seen across the board. In the case of the underlying silicon, it is generally accepted that chip design inevitably involves uncomfortable, even painful trade-offs between speed, power, latency, and die size. By rearchitecting its FPGAs, starting with 28 nm, Altera has been able to produce chips that are at once much faster, lower power, and smaller than previous-generation FPGAs, providing designers with a lot more latitude than they have enjoyed in the past.

The midrange Arria 10 FPGAs and SoCs are the first device families to roll out as part of the Generation 10 portfolio. The device family sets a new bar for midrange programmable devices, delivering both the performance and capabilities of current high-end FPGAs at the lowest midrange power. Leveraging an enhanced architecture that is optimized for TSMC's 20 nm process, Arria 10 FPGAs and SoCs deliver higher performance at up to 40 percent lower power compared to the previous device family.

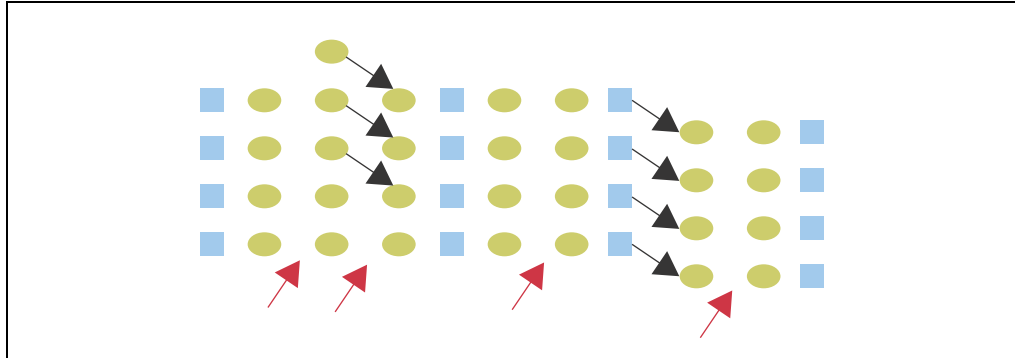
Arria 10 devices offer more features and capabilities than today's current high-end FPGAs, at 15 percent higher performance. Reflecting the trend toward silicon convergence, the Arria 10 FPGAs and SoCs offer the highest degree of system integration available in midrange devices, including 1.15 million LEs, integrated hard IP, and a second-generation processor system that features a 1.5 GHz dual-core ARM® Cortex™-A9 processor. The Arria 10 FPGAs and SoCs also provide 4 times greater bandwidth compared to the current generation, including 28 Gbps transceivers, and 3 times higher system performance, including 2,666 megabits per second (Mbps) DDR4 SDRAM support and up to 15 Gbps HMC support.

High-end Stratix 10 FPGAs and SoCs—with a core performance of up to 1 GHz—will offer over 10 TeraFLOPS, a performance level that has never been available in any off-the-shelf device.

As for the rearchitecture of the IP that is layered over these silicon platforms, Altera's engineers reworked the datapath to reduce the pipeline and paid rigorous attention to optimizing control structures. In doing so, they were able to double the clock speed with no change in latency.

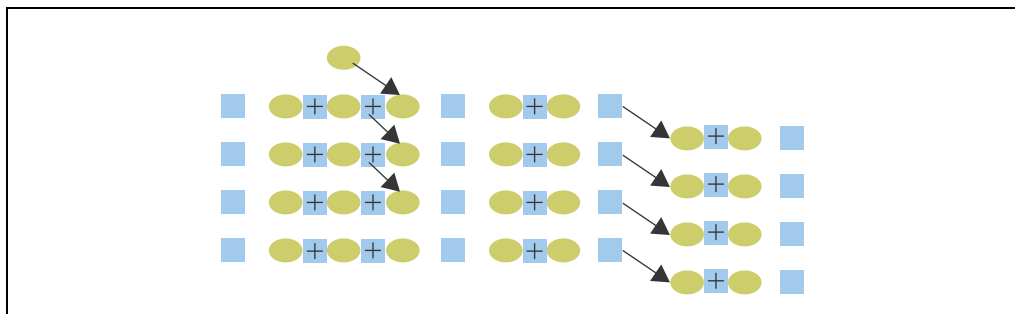
Looking at Altera logic cells, they observed that in a traditional pipeline there were often three or more LUTs between register levels. The existing hardware architecture had an excess of registers, making it possible to increase the registering without increasing the post place-and-route area (refer to [Figure 1](#)).

Figure 1. Altera Logic Cells, with Every Unregistered LUT Next to an Unused Register



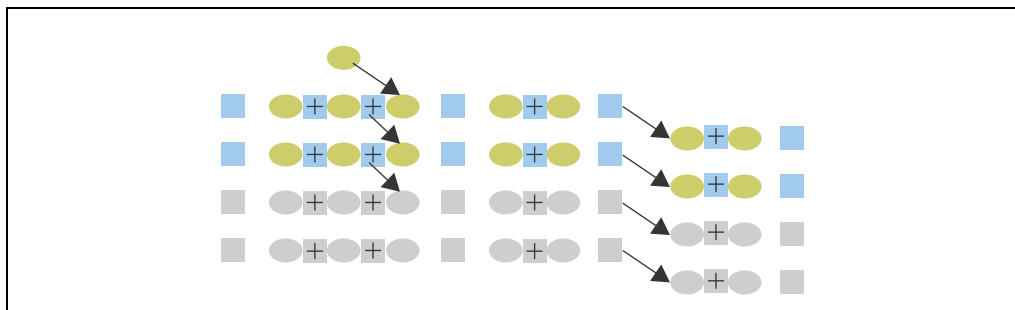
Matching unregistered LUTs with registers resulted in doubling the bandwidth of the circuit while retaining the same area. For example, a 100GbE could run at 200 Gbps. Applications engineers now had the option of either running two independent streams or running one stream on half the circuitry (refer to [Figure 2](#)).

Figure 2. Matching Unregistered LUTs with Unused Registers



The final option involves deleting half of the width and retaining the original bandwidth. For highly parallel circuitry, this is the stopping point: twice the clock rate, same latency, and half the area (refer to [Figure 3](#)).

Figure 3. Now That Efficiency Has Been Increased, Limiting Bandwidth Can Result in a Major Die Shrink



All of these architectural innovations have been applied to the Stratix V, Arria 10, and Stratix 10 FPGAs and SoCs. They are the primary reason all the IP listed earlier got smaller, faster, and better. These discoveries have Altera's general good practice to be implemented in all new IP cores that Altera will release. Altera's design software has also been updated to ensure full device support and a seamless migration path for legacy designs.

Conclusion

With Altera's Generation 10 FPGAs, we can address the limitations to scalability of total system throughput and latency while scaling back on power requirements.

Circuit designers will be able to choose from a wide range of Generation 10 Arria and Stratix FPGAs that reflect different emphases on bandwidth, latency, power, and die size. However for any given application their performance will far exceed what they've encountered to date, bringing design trade-offs back within their comfort zone.

Utilizing Altera's broad portfolio of best-in-class IP—instantiated in Generation 10 FPGAs—designers will be able to get leading-edge products to market quickly, secure in the knowledge that they'll maintain that edge for many years to come.

References

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Further Information

- White Paper: *Meeting the Performance and Power Imperative of the Zettabyte Era with Generation 10*:
www.altera.com/literature/wp/wp-01200-power-performance-zettabyte-generation-10.pdf
- White Paper: *The Breakthrough Advantage for FPGAs with Tri-Gate Technology*:
www.altera.com/literature/wp/wp-01201-fpga-tri-gate-technology.pdf
- White Paper: *Expect a Breakthrough Advantage in Next-Generation FPGAs*:
www.altera.com/literature/wp/wp-01199-next-generation-FPGAs.pdf
- Generation 10 FPGAs and SoCs web page:
www.altera.com/technology/system-tech/next-gen-technologies.html

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Document Revision History

Table 5 lists the revision history for this document.

Table 5. Document Revision History

Date	Version	Changes
November 2013	1.0	Initial release.