White Paper

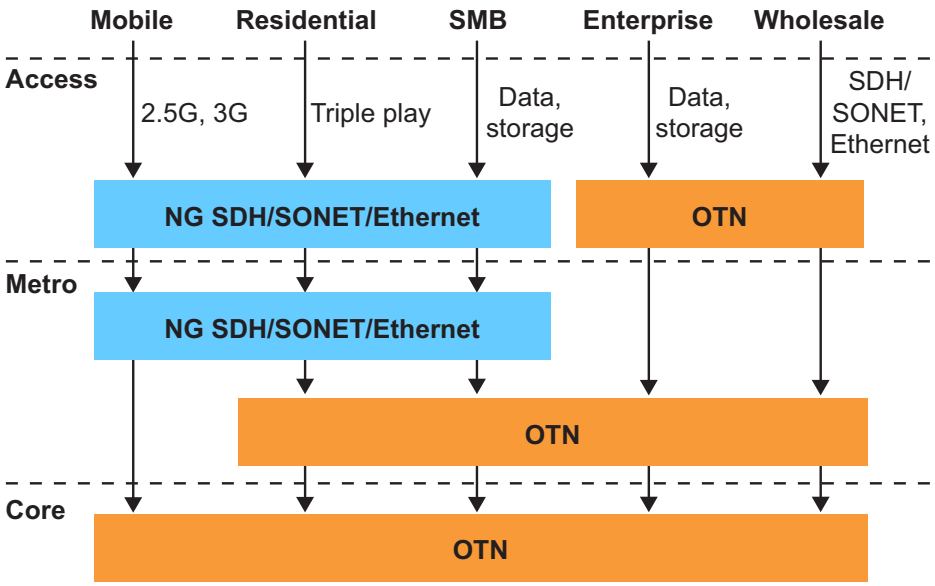
Enabling 100-Gbit OTN Muxponder Solutions on 28-nm FPGAs

The rapid growth in bandwidth required to support video and broadband wireless is straining communication networks. The current 10-Gbit OTN infrastructure is facing bandwidth exhaustion as the channels approach their maximum capacity. Faced with higher capital expenditure, higher operating expenditure, and shrinking revenue growth, service providers are turning to 100-Gbit OTN solutions to scale their current 10-Gbit-based networks by a factor of ten. However, there are large numbers of legacy OTN, SONET, Ethernet, and storage systems operating at lower data rates, which need to be plugged into the emerging optical infrastructure using 100-Gbit OTN muxponders. Altera's Stratix V FPGA family contains a number of key innovations that directly address the needs of 100-Gbit OTN muxponder solutions.

Introduction

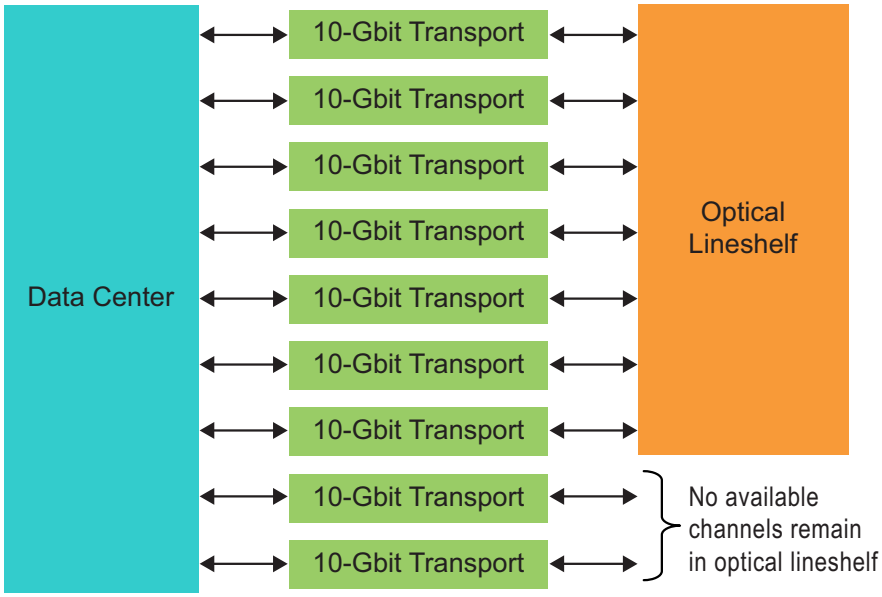
The explosive demand for bandwidth in the metro and long-haul networking space is forcing service providers to find ways to utilize their wavelength division multiplexing (WDM) networks more efficiently. Figure 1 shows the increasing services and bandwidth demands being made of today's Optical Transport Network (OTN) infrastructure.

Figure 1. Demands Being Made of Today's OTN Infrastructure



This demand for ever-increasing bandwidth is driven by endless new applications such as peer-to-peer sharing, social networking, digital video transmission, broadband wireless handsets and video conferencing and messaging. In the past, service providers have attempted to keep up with this growth by simply adding more channels to their existing WDM networks, as shown in Figure 2. However, this scheme exhausted the available channels, leaving service providers to face higher capital expenditure, higher operating expenditure, and shrinking revenue growth. The reality is that conventional 10-Gbit OTN architectures do not facilitate cost-effective implementations that optimize bandwidth usage in greenfield deployments.

Figure 2. Traditionally, Service Providers Added More Channels as Bandwidth Demands Increased



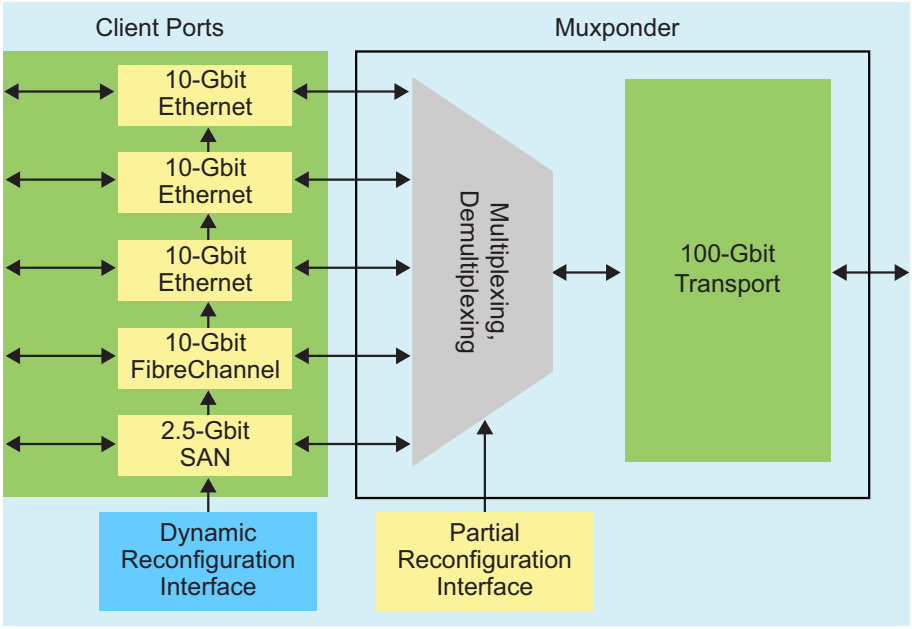
With the introduction and adoption of 40-/100-Gbit Ethernet, and the acceptance of OTN standards, service providers are now turning to 100-Gbit OTN solutions to scale their channel capacity by a factor of ten. However, there are a large number of legacy OTN, SONET, Ethernet, and storage systems operating at lower data rates, which somehow must be connected into the emerging OTN infrastructure. One way to achieve this, in a way that maximizes the available bandwidth while reducing space and power, is to aggregate multiple lower data-rate client channels onto a single wavelength at a higher data rate. This is the role of the 100-Gbit OTN multiplexing transponder (muxponder).

100-Gbit OTN Muxponder Solution

Traditionally, OTN systems have line cards that interface with one or more client ports and aggregate them to an optical transport port. Each line card is designed to meet the requirements of a particular client protocol, and specific client and transport data rates. In an environment where there are many different client port types, many different line cards are required in each chassis. This is not a cost-, area-, power-, or management-efficient solution, and results in the individual client payloads being transported on different wavelengths, which reduces the overall efficiency of the fiber-optic cable.

For 100-Gbit OTN systems, a more desirable situation is to deploy a single line card that supports many different protocols and data rates. This line card can be reconfigured in-service to meet a client's changing requirements without affecting the operation of the other clients on the same card. The line card can also take several lower speed client signals and combine them into, and separate them out of, a single 100-Gbit optical transport signal. This multiplexing and demultiplexing is the primary function of a 100-Gbit OTN muxponder (Figure 3).

Figure 3. Block Diagram of 100-Gbit OTN Muxponder Card



Muxponder cards currently exist in some dense wavelength-division multiplexing (DWDM) reconfigurable optical add-drop multiplexer (ROADM) systems, but these are based on older, multichip solutions that do not support the latest requirements in key service growth areas, such as storage area networking (SAN) and high-definition (HD) video transport. To address these markets, equipment manufacturers must update their platforms to support the new, higher speed interfaces such as 40-/100-Gbit Ethernet, 10-Gbit Fibre Channel, HD-SDI, and 3G-SDI.

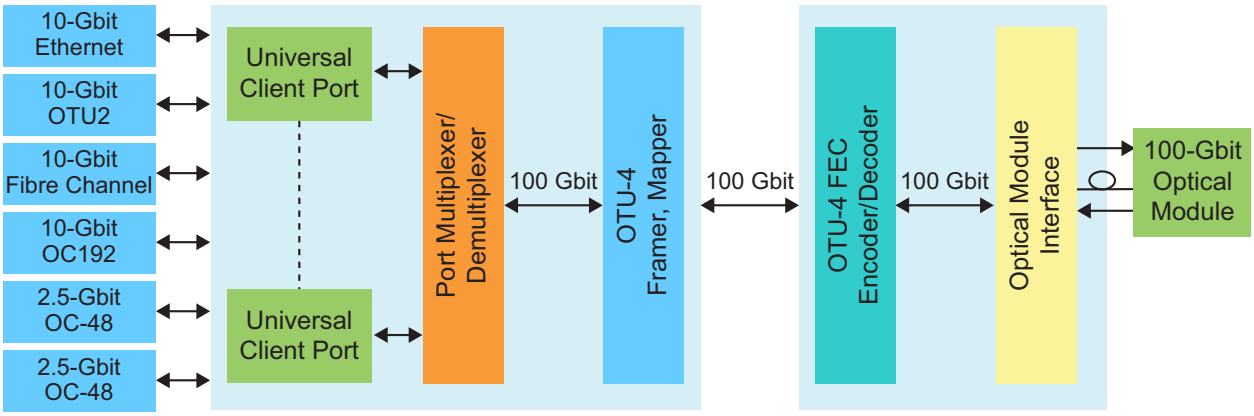
The Altera® Stratix® V FPGA family provides the bandwidth, level of integration, and innovative features required to enable a new generation of cost-effective 100-Gbit OTN muxponder solutions. Muxponder cards based on Stratix V FPGAs can efficiently address all service types including Ethernet, SONET/SDH, SAN, and HD-video. This allows equipment manufacturers to add new services to existing platforms, and consolidate multiple service-specific cards, while reducing board space, complexity, and power. Additional benefits include lower system-operating and -maintenance costs and increased reliability and uptime.

Implementing 100-Gbit OTN Muxponders in Stratix V FPGAs

Altera's 28-nm Stratix V FPGAs are designed with a number of significant innovations that lead to the highest bandwidth, highest system integration, and greatest flexibility available today in a single FPGA. The implementation of 100-Gbit OTN muxponders in Stratix V FPGAs (Figure 4) makes use of the following new and enhanced device features:

- Integrated serial transceivers support both line-side and client-side interfaces, with options covering a continuous range from 600 Mbps to 12.5 Gbps and a continuous range from 20 Gbps to 28 Gbps
- Integrated fractional-synthesis PLLs using 24-bit delta-sigma (ΔΣ) modulation eliminate the need for expensive voltage-controlled crystal oscillators (VCXOs) to generate the client reference frequencies
- Partial reconfiguration of core logic allows protocol logic for each individual client to be added, dropped, or modified without affecting the operation of the other clients, thus maximizing system uptime
- Dynamic reconfiguration of transceivers allows changes to the analog physical medium attachment (PMA) settings for every transceiver, without affecting the operation of any other transceivers
- High-performance, high-density, low-power FPGA core fabric, with redesigned adaptive logic module (ALM) and enhanced MultiTrack routing architecture, provides the throughput necessary to support wide parallel buses in the user logic

Figure 4. Block Diagram of a 100-Gbit OTN Muxponder Implemented in a Stratix V FPGA



Integrated Serial Transceivers

Stratix V FPGAs have up to 66 transceivers operating at data rates up to 28 Gbps. Each transceiver includes programmable pre-emphasis, equalization, and differential output voltage. At data rates up to 12.5 Gbps, a comprehensive physical coding sublayer (PCS) is included that provides support for a wide range of industry-standard and proprietary protocols.

For 100-Gbit OTN muxponder applications, the line-side interface uses a group of 10 of these transceivers, driven by a common transmit PLL. Stratix V FPGAs include low-jitter inductor-capacitor (LC) transmit PLLs which are ideal for meeting the tight jitter requirements of line-side protocols. The line-side data rate depends on the required forward error correction (FEC), and is generally in the range of 9.9 Gbps to 12.5 Gbps. Future implementations are expected to use four transceivers operating in the range 25 Gbps to 28 Gbps, and this configuration is also supported by Stratix V FPGAs.

The client-side interface uses 10 or more transceivers, each independently clocked using its own transmit PLL. The transceiver clocking architecture in Stratix V devices allows for independent clocking of channels, as well as the channel bonding required by the line-side interface. The client-side data rates depend on the various client protocols, and are generally in the range of 614 Mbps to 11.3 Gbps. With continuous operating ranges of 600 Mbps to 12.5 Gbps and 20 Gbps to 28 Gbps, the transceivers in Stratix V FPGAs are ideal for this application.

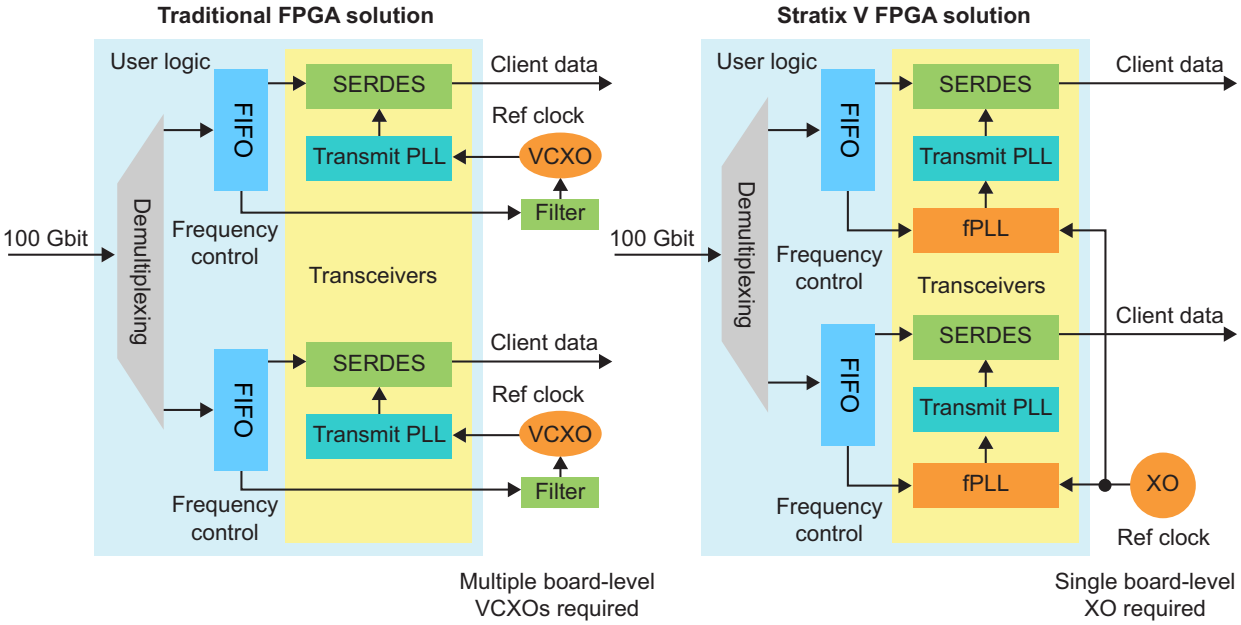
Integrated Fractional Synthesis PLLs

In 100-Gbit OTN muxponder applications, when the client data streams are multiplexed together to form a single 100-Gbit aggregate data stream, information about the client frequency is added into the data stream and transmitted along with the data on the line side.

When a muxponder receives this 100-Gbit aggregate data stream, it uses the individual client-frequency information embedded in the data stream to synthesize the required client frequencies and separate out each of the original client data streams. Traditionally, this process requires a bank of expensive, board-level VCXOs. However, in Stratix V FPGAs, these VCXOs are replaced by the integrated fractional synthesis PLLs. This reduces the area, complexity, and bill of material (BOM) cost for the circuit board.

Stratix V FPGAs integrate up to 32 fractional-synthesis PLLs (fPLLs) that use 24-bit, third-order, ΔΣ modulators. This corresponds to a resolution of about 1 part in 16 million, which results in frequency synthesis precise enough to replace the board-level VCXOs. Figure 5 shows a bank of VCXOs on the board being replaced by the integrated fPLLs in a Stratix V FPGA.

Figure 5. Using ΔΣ fPLLs in Stratix V FPGAs to Replace VCXOs

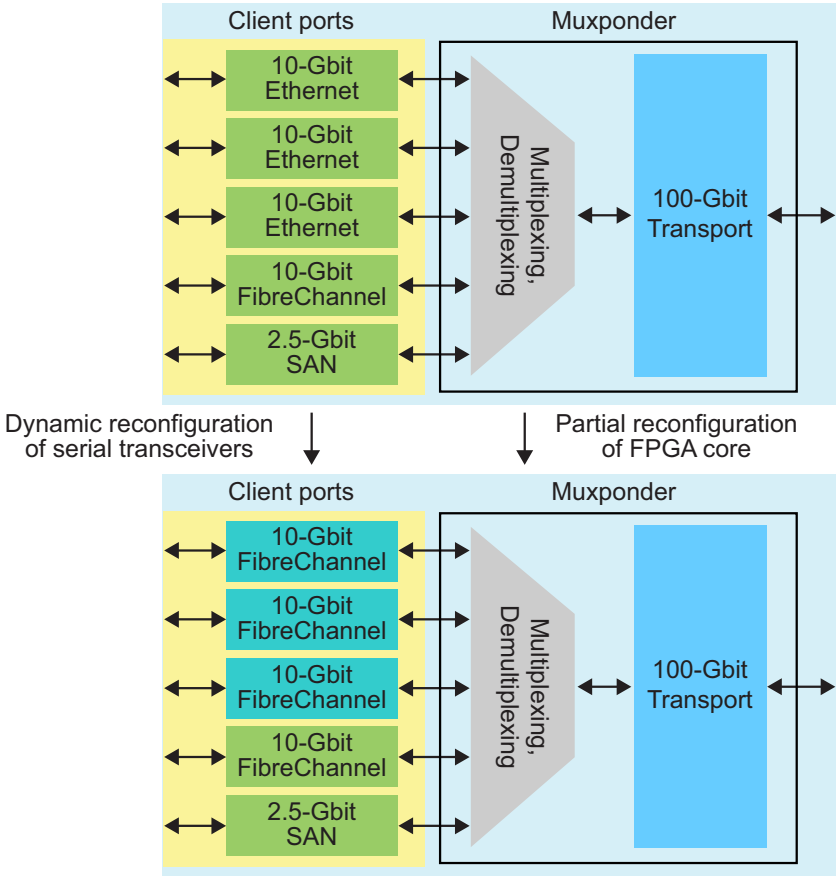


Partial Reconfiguration of Core Logic and Dynamic Reconfiguration of Transceivers

Once the muxponder is running in-system, it is a requirement that the number of clients in use can be increased or decreased on demand, while the rest of the system continues to carry traffic and operate normally. In addition, some scenarios require one or more of the client-side protocols to be changed when cables are rearranged on the front panel. Again, this change must be made while the rest of the system continues to carry traffic and operate normally.

To facilitate these system changes, Stratix V FPGAs offer both partial reconfiguration of the FPGA core and dynamic reconfiguration of the serial transceivers. Both of these techniques (Figure 6) are non-intrusive, so the rest of the FPGA continues to operate normally while the changes are taking place, maximizing the system uptime.

Figure 6. Partial Reconfiguration of FPGA Core and Dynamic Reconfiguration of Transceivers



To add a client interface, the transceiver is enabled and configured using dynamic reconfiguration, while the protocol logic and multiplexing functions are added into the FPGA core using partial reconfiguration of the core. To remove an unused client interface, the transceiver is disabled and the client logic is removed from the FPGA core, reducing the overall power dissipation.

High-Performance, Low-Power FPGA Core Fabric

Implementation of a 100-Gbit OTN muxponder in an FPGA requires a core fabric that can support pipelined, high-frequency parallel buses with low power dissipation. Stratix V FPGAs include a number of key innovations that address these requirements:

- Enhanced adaptive logic module (ALM) doubles the number of registers available, providing easier timing closure for register-rich and heavily pipelined designs
- Enhanced MultiTrack routing architecture, with more connections to neighboring logic elements (LEs), provides increased system performance, higher logic utilization, and reduced compile times for tightly packed designs
- New 20-Kbit internal memory blocks, with high performance and small footprint, includes built-in error correcting code (ECC) protection
- Programmable power technology automatically reduces the static power dissipation in the core for non-critical timing paths
- Clock trees can be turned on and off in sections to minimize the dynamic power dissipation and prevent unnecessary switching noise
- High-performance, high-K metal gate 28-nm process technology delivers state-of-the-art performance and power efficiency with a 0.85-V core power supply

Conclusion

The explosive demand for bandwidth in the metro and long-haul networking space is driving service providers to make efficient use of their optical fiber. One important technique that has emerged is the use of 100-Gbit OTN muxponders.

Recognizing this market need, Altera has included a number of key innovations in Stratix V FPGAs that directly address the needs of 100-Gbit OTN muxponder applications. These innovations allow the system designer to reduce cost, power, and board space, while enjoying the flexibility of an FPGA-based system with partial- and dynamic-reconfiguration capability.

To complete the 100-Gbit OTN muxponder solution, Altera also provides the industry-leading Quartus® II design software, OTN reference designs, partner intellectual-property (IP) solutions, and Stratix V hardware development kits.

Further Information

- Stratix V FPGAs: Built for Bandwidth: www.altera.com/products/devices/stratix-fpgas/stratix-v/stxv-index.jsp
- Literature: Stratix V Devices: www.altera.com/products/devices/stratix-fpgas/stratix-v/literature/stv-literature.jsp

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