



INTEL® ARRIA® 10 PRODUCT TABLE

| PRODUCT LINE | | GX 160 SX 160 | GX 220 SX 220 | GX 270 SX 270 | GX 320 SX 320 | GX 480 SX 480 | GX 570 SX 570 | GX 660 SX 660 | GX 900 | GX 1150 | GT 900 | GT 1150 | |
|--|---|--|------------------|------------------|------------------|------------------|------------------|------------------|-------------|-------------|-------------|-------------|---|
| Resources | LEs (K) | 160 | 220 | 270 | 320 | 480 | 570 | 660 | 900 | 1,150 | 900 | 1,150 | |
| | System logic elements (K) | 210 | 288 | 354 | 419 | 629 | 747 | 865 | 1,180 | 1,506 | 1,180 | 1,506 | |
| | Adaptive logic modules (ALMs) | 61,510 | 83,730 | 101,620 | 118,730 | 181,790 | 217,080 | 250,540 | 339,620 | 427,200 | 339,620 | 427,200 | |
| | Registers | 246,040 | 334,920 | 406,480 | 474,920 | 727,160 | 868,320 | 1,002,160 | 1,358,480 | 1,708,800 | 1,358,480 | 1,708,800 | |
| | M20K memory blocks | 440 | 588 | 750 | 891 | 1,438 | 1,800 | 2,133 | 2,423 | 2,713 | 2,423 | 2,713 | |
| | M20K memory (Mb) | 9 | 11 | 15 | 17 | 28 | 35 | 42 | 47 | 53 | 47 | 53 | |
| | MLAB memory (Mb) | 1.0 | 1.8 | 2.4 | 2.8 | 4.3 | 5.0 | 5.7 | 9.2 | 12.7 | 9.2 | 12.7 | |
| | Hardened single-precision floating-point multipliers/adders | 156/156 | 191/191 | 830/830 | 985/985 | 1,368/1,368 | 1,523/1,523 | 1,688/1,688 | 1,518/1,518 | 1,518/1,518 | 1,518/1,518 | 1,518/1,518 | |
| | 18 x 19 multipliers | 312 | 382 | 1,660 | 1,970 | 2,736 | 3,046 | 3,376 | 3,036 | 3,036 | 3,036 | 3,036 | |
| | Peak fixed-point performance (GMACS) ¹ | 343 | 420 | 1,826 | 2,167 | 3,010 | 3,351 | 3,714 | 3,340 | 3,340 | 3,340 | 3,340 | |
| Peak floating-point performance (GFLOPS) | 140 | 172 | 747 | 887 | 1,231 | 1,371 | 1,519 | 1,366 | 1,366 | 1,366 | 1,366 | | |
| Clocks, Maximum I/O Pins, and Architectural Features | Global clock networks | 32 | 32 | 32 | 32 | 32 | 32 | 32 | 32 | 32 | 32 | 32 | |
| | Regional clocks | 8 | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 16 | 16 | 16 | |
| | Hard processor system (available in SX devices only) | Dual-core Arm® Cortex®-A9 MPCore® processor. See the following page for details. | | | | | | | | - | | | |
| | Maximum LVDS channels (1.6 G) | 120 | 120 | 168 | 168 | 222 | 324 | 270 | 384 | 384 | 312 | 312 | |
| | Maximum user I/O pins | 288 | 288 | 384 | 384 | 492 | 696 | 696 | 768 | 768 | 624 | 624 | |
| | Transceiver count (17.4 Gbps) | 12 | 12 | 24 | 24 | 36 | 48 | 48 | 96 | 96 | 72 | 72 | |
| | Transceiver count (25.78 Gbps) | - | - | - | - | - | - | - | - | - | - | 6 | 6 |
| | PCIe® hardened IP blocks (Gen3 x8) ² | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 4 | 4 | 4 | 4 | |
| | Maximum 3 V I/O pins | 48 | 48 | 48 | 48 | 48 | 96 | 96 | - | - | - | - | |

Package Options³ and I/O Pins⁴: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs⁵, and Transceiver Count

| | | | | | | | | | | | | |
|------|-------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|-----------------|-----------------|-----------------|
| U19 | U484 pin (19 mm) | 192, 48, 72, 6 | 192, 48, 72, 6 | - | - | - | - | - | - | - | - | - |
| F27 | F672 pin (27 mm) | 240, 48, 96, 12 | 240, 48, 96, 12 | 240, 48, 96, 12 | 240, 48, 96, 12 | - | - | - | - | - | - | - |
| F29 | F780 pin (29 mm) | 288, 48, 120, 12 | 288, 48, 120, 12 | 360, 48, 156, 12 | 360, 48, 156, 12 | 360, 48, 156, 12 | - | - | - | - | - | - |
| F34 | F1152 pin (35 mm) | - | - | 384, 48, 168, 24 | 384, 48, 168, 24 | 492, 48, 222, 24 | 492, 48, 222, 24 | 492, 48, 222, 24 | 504, 0, 252, 24 | 504, 0, 252, 24 | - | - |
| F35 | F1152 pin (35 mm) | - | - | 384, 48, 168, 24 | 384, 48, 168, 24 | 396, 48, 174, 36 | 396, 48, 174, 36 | 396, 48, 174, 36 | - | - | - | - |
| KF40 | F1517 pin (40 mm) | - | - | - | - | - | 696, 96, 324, 36 | 696, 96, 324, 36 | - | - | - | - |
| NF40 | F1517 pin (40 mm) | - | - | - | - | - | 588, 48, 270, 48 | 588, 48, 270, 48 | 600, 0, 300, 48 | 600, 0, 300, 48 | - | - |
| RF40 | F1517 pin (40 mm) | - | - | - | - | - | - | - | 342, 0, 154, 66 | 342, 0, 154, 66 | - | - |
| NF45 | F1932 pin (45 mm) | - | - | - | - | - | - | - | 768, 0, 384, 48 | 768, 0, 384, 48 | - | - |
| SF45 | F1932 pin (45 mm) | - | - | - | - | - | - | - | 624, 0, 312, 72 | 624, 0, 312, 72 | 624, 0, 312, 72 | 624, 0, 312, 72 |
| UF45 | F1932 pin (45 mm) | - | - | - | - | - | - | - | 480, 0, 240, 96 | 480, 0, 240, 96 | - | - |

Notes:

1. Fixed-point performance assumes the use of pre-adder.
2. Certain packages might not bond out all PCIe hard IP blocks.
3. All packages are ball grid arrays with 1.0 mm pitch, except for U19 (U484), which is 0.8 mm pitch.
4. A subset of pins for each package are used for 3.3 V and 2.5 V interfaces.
5. Each LVDS pair can be configured as either a differential input or a differential output.
6. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.altera.com.

192, 48, 72, 6 Numbers indicate GPIO count, high-voltage I/O count, LVDS pairs, and transceiver count.

Indicates pin migration.



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| PRODUCT LINE | SX 160 | SX 220 | SX 270 | SX 320 | SX 480 | SX 570 | SX 660 |
|--|---|--------|--------|--------|--------|--------|--------|
| Processor | Dual-core Arm Cortex-A9 MPCore processor | | | | | | |
| Maximum processor frequency | 1.5 GHz ¹ | | | | | | |
| Processor cache and co-processors | <ul style="list-style-type: none"> • L1 instruction cache (32 KB) • L1 data cache (32 KB) • Level 2 cache (512 KB) shared • FPU single and double precision • Arm Neon* media engine • Arm CoreSight* debug and trace technology • Snoop control unit (SCU) • Acceleration coherency port (ACP) | | | | | | |
| Scratch pad RAM | 256 KB | | | | | | |
| HPS DDR memory | DDR4 and DDR3 (Up to 64 bit with error correction code (ECC)) | | | | | | |
| Direct memory access (DMA) controller | 8 channels | | | | | | |
| EMAC | 3X 10/100/1000 EMAC with integrated DMA | | | | | | |
| USB OTG controller | 2X USB OTG with integrated DMA | | | | | | |
| UART controller | 2X UART 16550 compatible | | | | | | |
| Serial peripheral interface (SPI) controller | 4X SPI | | | | | | |
| I ² C controller | 5X I ² C | | | | | | |
| Quad SPI flash controller | 1X SIO, DIO, QIO SPI flash supported | | | | | | |
| SD/SDIO/MMC controller | 1X eMMC 4.5 with DMA and CE-ATA support | | | | | | |
| NAND flash controller | <ul style="list-style-type: none"> • 1X ONFI 1.0 or later • 8 and 16 bit support | | | | | | |
| General-purpose timers | 7X | | | | | | |
| Software-programmable GPIOs | Maximum 54 GPIOs | | | | | | |
| Direct shared I/Os | 48 I/Os to connect HPS peripherals directly to I/O | | | | | | |
| Watchdog timers | 4X | | | | | | |
| Security | Secure boot, Advanced Encryption System (AES), and secure hash algorithm | | | | | | |

Notes:

1. With overdrive feature.