SOLUTION BRIEF

Intel® MAX® 10

How to Design for Increasing Power Constraints

Intel® MAX® 10 FPGAs provide a number of power-saving features to enable small form factor low-power designs in today's power conscious applications and markets. MAX 10 FPGA integration, instant-on capability, sleep mode, and I/O buffer dynamic disable features help system designers achieve their low system power goals.

Industry Challenges

System designers must increasingly focus on designing for a power-constrained environment. Industry and societal trends are contributing to the drive to reduce power consumption and/or add functionality within a fixed power budget. The industry trend of focusing on the operational expense (OpEx) component of total cost of ownership (TCO) is continuing, and accelerating, in markets such as communications and computing. Data centers, service providers, and enterprise customers now routinely evaluate and optimize power efficiency, because power consumption contributes to higher OpEx through direct electricity costs, cooling costs, and facility real estate. At the same time, the societal trend toward greater mobility is driving system designers toward tighter power budgets, as systems that were traditionally stationary are becoming distributed or mobile.

Solving the Power Problem

To address today's power challenges, MAX 10 FPGAs incorporate a number of power-saving capabilities.

Single-Chip Integration

MAX 10 FPGAs incorporate a number of important functions on-die, reducing the need to add additional components to the board. The single-chip integration of MAX 10 FPGAs allows for low-latency, high-bandwidth interfaces using low energy on-die signaling, rather than high-energy inter-device signaling across a printed circuit board (PCB). MAX 10 FPGAs are available with integrated dual-image configuration flash memory, analog-to-digital converters (ADCs), and user flash memory (UFM) for persistent storage of system data.

Low Static Power

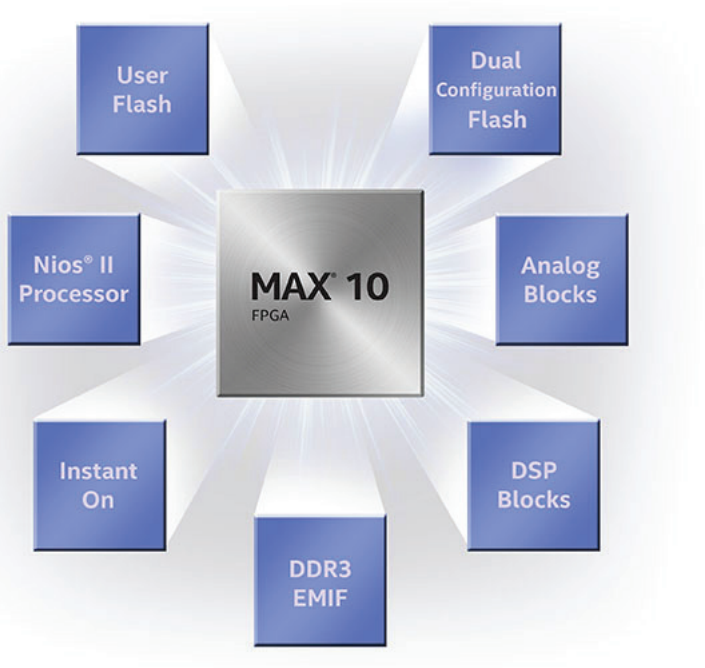
MAX 10 FPGAs begin with a foundation of low static power. Static power is a result of sub-threshold leakage and DC bias current inside an FPGA. MAX 10 FPGAs share a common core fabric architecture with Cyclone® IV E FPGAs, which offer industry leading low static power available in a full featured FPGA product family. By utilizing this low static power 60 nm architecture on a power-optimized 55 nm flashenabled process technology, MAX 10 FPGAs are able to achieve the same low static power levels as Cyclone IV E FPGAs. While MAX 10 FPGAs build on the low power pedigree of Cyclone IV E FPGAs, they also incorporate new power saving features to reduce dynamic power.

I/O Dynamic Power Savings

To provide maximum flexibility to system designers, all FPGA I/O are intrinsically bidirectional. Based on the I/O direction specified in the configuration file, each I/O can be configured as input-only, output-only, or bidirectional. While the output buffer of a bidirectional I/O has always included a dynamic output enable signal, MAX 10 FPGAs also include an input buffer enable/disable capability. When an input buffer is dynamically disabled, the buffer presents its last known state to the FPGA core fabric, so that no inputs inside the FPGA are left floating.

This dynamic input-buffer-disable capability allows power savings on LVDS and voltage-referenced I/O standards, such as SSTL, HSTL, and HSUL. For example, when 1.5 V SSTL bidirectional I/O buffer is used as the data (DQ) and strobe (DQS) signals on a DDR3 SDRAM interface, the input buffer can dynamically power down while the DDR3 SDRAM interface is idle or writing to SDRAM. This capability can save up to 240 mW on a DDR3 SDRAM interface with a low-read duty cycle. The I/O dynamic-buffer-disable capability is available on MAX 10 FPGAs of 16K logic elements (LEs) and higher.

Figure 1. MAX 10 FPGA



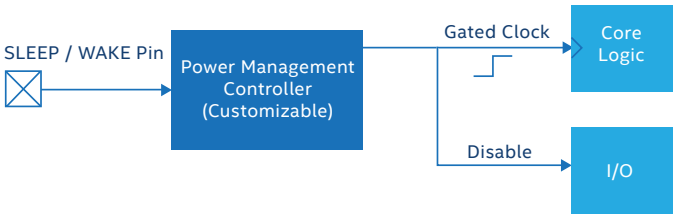
Low-Power Standby Modes

Many applications experience considerable periods of functional inactivity. Even during this inactive period, dynamic switching of global clock networks and logic circuits continues to consume energy. However, system designers are hesitant to shut down the system because of the loss of state information and the time required to restart the system. MAX 10 FPGAs offer two capabilities that allow designers to capture the power savings available during periods of system inactivity: sleep mode and instant-on configuration.

Sleep Mode

Sleep mode allows MAX 10 FPGAs to decrease their standby power, while retaining all needed state information, with the ability to resume full operation in less than 1 millisecond. A sleep-mode-enabled design uses a primary input pin to activate, and resume from, sleep mode. The primary input pin connects to a Power Management Controller (PMC) inside the FPGA fabric, which performs the specific actions to put the FPGA into sleep mode and resume full operation. Intel provides a reference design for the PMC, which the system designer can customize to their specific system requirements. In sleep mode, user-selected global clock networks (GCLKs) of the FPGA are safely gated off one at a time, and supported I/O buffers can be dynamically disabled.

Figure 2. MAX 10 FPGA Sleep Mode



Dynamic power savings in sleep mode varies by the design, according to the active mode power, percentage of logic selected for sleep mode, and system duty cycle, but the power savings can be as high as 90%.

Instant-on Configuration

Instant-on configuration allows MAX 10 FPGAs to power off completely during periods of inactivity, and reconfigure themselves in less than 10 milliseconds. See the MAX 10 FPGA data sheet for exact reconfiguration times of specific FPGA densities. Although state is lost during FPGA reconfiguration, critical data can be written to ondie UFM prior to shutdown, and read back upon restart. Instant-on configuration is great for low duty cycle battery-powered systems, because full FPGA configuration from power-off is too fast to be perceived by human users. Instant-on configuration is available in all MAX 10 FPGAs as a standard feature.

Power Regulation

MAX 10 FPGAs are offered with two power supply variants: a convenient single voltage supply variant (3.0 V or 3.3 V) with an integrated linear regulator, and a native dual voltage supply variant (1.2 V + 2.5 V). By coupling a dual voltage supply MAX 10 FPGA with a high-efficiency Enpirion® PowerSoC switching regulator, designers can achieve low system power, while simultaneously minimizing their PCB footprint. Early Power Estimator (EPE) provides designers with a simple integrated power estimation and regulator selection flow. Because Enpirion is part of Intel, the PowerSoC and FPGAs are designed to work together, and supported by the same team.

Conclusion

MAX 10 FPGAs deliver a number of power saving features to allow systems to reach their full potential in a power-critical world. MAX 10 FPGAs start with the industry leading low static power of Cyclone IV E FPGAs, and extend it with non-volatile integration for instant configuration, sleep mode, and I/O buffer dynamic-disable capability. By pairing MAX 10 FPGAs with high-efficiency Enpirion PowerSoC switching regulators, system designers have an easy way to achieve low system power with a small form factor, integrated solution.

Want to Dig Deeper?

Get more details about our MAX 10 FPGA family by contacting your local Intel sales representative or FAE, or by visiting www.altera.com/max10.

To learn more about achieving low system power, read the following white papers:

- White Paper: Achieving Low Power in 65 nm Cyclone III FPGAs
  www.altera.com/literature/wp/wp-01016.pdf
- White Paper: Adding Hardware Accelerators to Reduce Power in Embedded Systems
  www.altera.com/literature/wp/wp-01112-hw-reduce-power.pdf