intel®

Intel® Cyclone® 10 LP FPGAs

Half the Power at Half the Cost[1]

Intel's Cyclone® 10 LP FPGAs are optimized for low static power and low cost.

Intel Cyclone 10 LP Advantages

- Low power, up to 50% less static power than previous generation[1]
- Cost-optimized solution to bring the lowest cost solution to customers
- High-density sea-of-gates fabric, memory, and I/O architecture
- Automotive, Industrial, and Commercial grade devices
- Only two power supplies required, simplifying power distribution
- Complementary optimized and validated Intel® Enpirion® power solutions

Intel Cyclone 10 LP Target Applications

These capabilities make Intel Cyclone 10 LP FPGAs ideal for next generation designs needing low power and cost. Typical end applications include:

- I/O expansion
- Interfacing
- Bridging
- Sensor fusion
- Industrial motor control

Note:
1. When compared to previous generation Cyclone FPGA early power estimators

Intel Cyclone 10 LP FPGAs Product Table

PRODUCT LINE		10CL006	10CL010	10CL016	10CL025	10CL040	10CL055	10CL080	10CL120
Resources	Logic elements (LEs)[1]	6,000	10,000	16,000	25,000	40,000	55,000	80,000	120,000
	M9K memory blocks	30	46	56	66	126	260	305	432
	M9K memory size (Kb)	270	414	504	594	1,134	2,340	2,745	3,888
	DSP blocks (18 x 18 multipliers)	15	23	56	66	126	156	244	288
	Phase-locked loops (PLL)	2	2	4	4	4	4	4	4
I/O and Architectural Features	Global clock networks	10	10	20	20	20	20	20	20
	Maximum user I/O pins	176	176	340	150	325	321	423	525
	Maximum LVDS channels	65	65	137	52	124	132	178	230

Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, LVDS Pairs[2]

	10CL006	10CL010	10CL016	10CL025	10CL040	10CL055	10CL080	10CL120
M164 pin (8 mm x 8 mm, 0.5 mm pitch)		101,26	87, 22					
U256 pin (14 mm x 14 mm, 0.8 mm pitch)	176, 65	176, 65	162, 53	150, 52				
U484 pin (19 mm x 19 mm, 0.8 mm pitch)			340, 137		325, 124	321, 132	289, 110	
E144 pin (22 mm x 22mm, 0.5 mm pitch)	88, 22	88, 22	78, 19	76, 18				
F484 pin (23 mm x 23 mm, 1.0 mm pitch)			340, 137		325, 124	321, 132	289, 110	277, 103
F780 pin (29 mm x 29 mm, 1.0 mm pitch)							423, 178	525, 230

Notes:
1. LE counts valid in comparing across Intel devices, and are conservative vs. competing FPGAs.
2. This includes both dedicated and emulated LVDS pairs
3. All data is correct at the time of printing and may be subject to change without prior notice. For the latest information, please visit www.altera.com.

71, 22   Numbers indicate GPIO count, LVDS pairs.

Indicates pin migration path.

For more information, visit www.altera.com/cyclone10lp.