Pin Information for the Intel® MAX® 10 10M02DC Device
Version 2017.02.21
Note *(1)*

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	D4
1A	VREFB1N0	IO			DIFFIO_RX_L2n	DIFFOUT_L2n	Low_Speed	F5
1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	E4
1A	VREFB1N0	IO			DIFFIO_RX_L2p	DIFFOUT_L2p	Low_Speed	E5
1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed	G6
1A	VREFB1N0	IO			DIFFIO_RX_L4n	DIFFOUT_L4n	Low_Speed	G3
1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	H6
1A	VREFB1N0	IO			DIFFIO_RX_L4p	DIFFOUT_L4p	Low_Speed	F2
1B	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	G7
1B	VREFB1N0	IO			DIFFIO_RX_L6n	DIFFOUT_L6n	Low_Speed	H2
1B	VREFB1N0	IO		JTAGEN	DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed	H7
1B	VREFB1N0	IO			DIFFIO_RX_L6p	DIFFOUT_L6p	Low_Speed	H1
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	J7
1B	VREFB1N0	IO	VREFB1N0					J3
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	J8
1B	VREFB1N0	IO						J4
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L8n	DIFFOUT_L8n	Low_Speed	H3
1B	VREFB1N0	IO			DIFFIO_RX_L9n	DIFFOUT_L9n	Low_Speed	J2
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L8p	DIFFOUT_L8p	Low_Speed	H4
1B	VREFB1N0	IO			DIFFIO_RX_L9p	DIFFOUT_L9p	Low_Speed	J1
1B	VREFB1N0	IO			DIFFIO_RX_L10n	DIFFOUT_L10n	Low_Speed	J6
1B	VREFB1N0	IO			DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	K2
1B	VREFB1N0	IO			DIFFIO_RX_L10p	DIFFOUT_L10p	Low_Speed	K7
1B	VREFB1N0	IO			DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	K1
1B	VREFB1N0	IO			DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	K4
1B	VREFB1N0	IO			DIFFIO_RX_L13n	DIFFOUT_L13n	Low_Speed	L1
1B	VREFB1N0	IO			DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed	K3
1B	VREFB1N0	IO			DIFFIO_RX_L13p	DIFFOUT_L13p	Low_Speed	L2
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L14n	High_Speed	L3
2	VREFB2N0	IO			DIFFIO_RX_L15n	DIFFOUT_L15n	High_Speed	M1
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L14p	High_Speed	M3
2	VREFB2N0	IO			DIFFIO_RX_L15p	DIFFOUT_L15p	High_Speed	M2
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L16n	DIFFOUT_L16n	High_Speed	K8
2	VREFB2N0	IO			DIFFIO_RX_L17n	DIFFOUT_L17n	High_Speed	N1
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L16p	DIFFOUT_L16p	High_Speed	L8
2	VREFB2N0	IO			DIFFIO_RX_L17p	DIFFOUT_L17p	High_Speed	P1
2	VREFB2N0	IO	DPCLK0		DIFFIO_RX_L18n	DIFFOUT_L18n	High_Speed	M4
2	VREFB2N0	IO	VREFB2N0					R1
2	VREFB2N0	IO	DPCLK1		DIFFIO_RX_L18p	DIFFOUT_L18p	High_Speed	N3
2	VREFB2N0	IO						R2
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L19n	DIFFOUT_L19n	High_Speed	N4
2	VREFB2N0	IO			DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	U1
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L19p	DIFFOUT_L19p	High_Speed	P4
2	VREFB2N0	IO			DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	U2
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	R4
3	VREFB3N0	IO			DIFFIO_RX_B2n	DIFFOUT_B2n	High_Speed	U3
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	T4
3	VREFB3N0	IO			DIFFIO_RX_B2p	DIFFOUT_B2p	High_Speed	V2
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	P6
3	VREFB3N0	IO			DIFFIO_RX_B4n	DIFFOUT_B4n	High_Speed	V3
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	P5
3	VREFB3N0	IO			DIFFIO_RX_B4p	DIFFOUT_B4p	High_Speed	V4
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	R5
3	VREFB3N0	IO			DIFFIO_RX_B6n	DIFFOUT_B6n	High_Speed	U5
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	R6
3	VREFB3N0	IO			DIFFIO_RX_B6p	DIFFOUT_B6p	High_Speed	V5
3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed	T5
3	VREFB3N0	IO			DIFFIO_RX_B8n	DIFFOUT_B8n	High_Speed	T7
3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed	T6
3	VREFB3N0	IO			DIFFIO_RX_B8p	DIFFOUT_B8p	High_Speed	T8
3	VREFB3N0	IO			DIFFIO_TX_RX_B9n	DIFFOUT_B9n	High_Speed	N7
3	VREFB3N0	IO	VREFB3N0					U6
3	VREFB3N0	IO			DIFFIO_TX_RX_B9p	DIFFOUT_B9p	High_Speed	N8
3	VREFB3N0	IO						V6
3	VREFB3N0	IO			DIFFIO_TX_RX_B10n	DIFFOUT_B10n	High_Speed	R8
3	VREFB3N0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	High_Speed	U7
3	VREFB3N0	IO			DIFFIO_TX_RX_B10p	DIFFOUT_B10p	High_Speed	R9
3	VREFB3N0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	High_Speed	V7
3	VREFB3N0	IO			DIFFIO_TX_RX_B12n	DIFFOUT_B12n	High_Speed	V9
3	VREFB3N0	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	High_Speed	U8
3	VREFB3N0	IO			DIFFIO_TX_RX_B12p	DIFFOUT_B12p	High_Speed	U9
3	VREFB3N0	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	High_Speed	V8
3	VREFB3N0	IO			DIFFIO_TX_RX_B14n	DIFFOUT_B14n	High_Speed	M8
3	VREFB3N0	IO			DIFFIO_TX_RX_B14p	DIFFOUT_B14p	High_Speed	M9
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	T9
3	VREFB3N0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	High_Speed	V12
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	T10
3	VREFB3N0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	High_Speed	U11
5	VREFB5N0	IO			DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	N14
5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	T16
5	VREFB5N0	IO			DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	P14
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed	R16
5	VREFB5N0	IO			DIFFIO_RX_R3p	DIFFOUT_R3p	High_Speed	R15
5	VREFB5N0	IO						P16

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
5	VREFB5N0	IO			DIFFIO_RX_R3n	DIFFOUT_R3n	High_Speed	P15
5	VREFB5N0	IO	VREFB5N0					P17
5	VREFB5N0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	High_Speed	L12
5	VREFB5N0	IO			DIFFIO_RX_R5p	DIFFOUT_R5p	High_Speed	T17
5	VREFB5N0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	High_Speed	L11
5	VREFB5N0	IO			DIFFIO_RX_R5n	DIFFOUT_R5n	High_Speed	R17
5	VREFB5N0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	High_Speed	L15
5	VREFB5N0	IO			DIFFIO_RX_R7p	DIFFOUT_R7p	High_Speed	L16
5	VREFB5N0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	High_Speed	K15
5	VREFB5N0	IO			DIFFIO_RX_R7n	DIFFOUT_R7n	High_Speed	K16
5	VREFB5N0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	High_Speed	R18
5	VREFB5N0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	High_Speed	N18
5	VREFB5N0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	High_Speed	P18
5	VREFB5N0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	High_Speed	M18
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	K12
6	VREFB6N0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	High_Speed	M17
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	K11
6	VREFB6N0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	High_Speed	L18
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R12p	DIFFOUT_R12p	High_Speed	L17
6	VREFB6N0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	High_Speed	K18
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R12n	DIFFOUT_R12n	High_Speed	K17
6	VREFB6N0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	High_Speed	J18
6	VREFB6N0	IO			DIFFIO_RX_R14p	DIFFOUT_R14p	High_Speed	H18
6	VREFB6N0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	High_Speed	H17
6	VREFB6N0	IO			DIFFIO_RX_R14n	DIFFOUT_R14n	High_Speed	G18
6	VREFB6N0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	High_Speed	G17
6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	H11
6	VREFB6N0	IO	VREFB6N0					F18
6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed	H12
6	VREFB6N0	IO						E18
6	VREFB6N0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	High_Speed	F15
6	VREFB6N0	IO			DIFFIO_RX_R18p	DIFFOUT_R18p	High_Speed	G16
6	VREFB6N0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	High_Speed	G15
6	VREFB6N0	IO			DIFFIO_RX_R18n	DIFFOUT_R18n	High_Speed	F16
6	VREFB6N0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	High_Speed	E16
6	VREFB6N0	IO			DIFFIO_RX_R20p	DIFFOUT_R20p	High_Speed	D18
6	VREFB6N0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	High_Speed	D16
6	VREFB6N0	IO			DIFFIO_RX_R20n	DIFFOUT_R20n	High_Speed	E17
6	VREFB6N0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	High_Speed	G11
6	VREFB6N0	IO			DIFFIO_RX_R22p	DIFFOUT_R22p	High_Speed	C18
6	VREFB6N0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	High_Speed	G12
6	VREFB6N0	IO			DIFFIO_RX_R22n	DIFFOUT_R22n	High_Speed	B18
6	VREFB6N0	IO	PLL_R_CLKOUTp		DIFFIO_RX_R23p	DIFFOUT_R23p	High_Speed	E15
6	VREFB6N0	IO			DIFFIO_RX_R24p	DIFFOUT_R24p	High_Speed	D17
6	VREFB6N0	IO	PLL_R_CLKOUTn		DIFFIO_RX_R23n	DIFFOUT_R23n	High_Speed	D15
6	VREFB6N0	IO			DIFFIO_RX_R24n	DIFFOUT_R24n	High_Speed	C17
8	VREFB8N0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	Low_Speed	F10
8	VREFB8N0	IO			DIFFIO_RX_T2p	DIFFOUT_T2p	Low_Speed	A9
8	VREFB8N0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	Low_Speed	G10
8	VREFB8N0	IO			DIFFIO_RX_T2n	DIFFOUT_T2n	Low_Speed	A8
8	VREFB8N0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	Low_Speed	B9
8	VREFB8N0	IO			DIFFIO_RX_T4p	DIFFOUT_T4p	Low_Speed	C10
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T3n	DIFFOUT_T3n	Low_Speed	B8
8	VREFB8N0	IO			DIFFIO_RX_T4n	DIFFOUT_T4n	Low_Speed	C9
8	VREFB8N0	IO		DEV_OE	DIFFIO_RX_T5p	DIFFOUT_T5p	Low_Speed	D8
8	VREFB8N0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	Low_Speed	D7
8	VREFB8N0	IO	VREFB8N0					B7
8	VREFB8N0	IO		CONFIG_SEL				G9
8	VREFB8N0	IO			DIFFIO_RX_T6p	DIFFOUT_T6p	Low_Speed	A6
8	VREFB8N0	Input_only		nCONFIG				H9
8	VREFB8N0	IO			DIFFIO_RX_T6n	DIFFOUT_T6n	Low_Speed	A5
8	VREFB8N0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	Low_Speed	C6
8	VREFB8N0	IO			DIFFIO_RX_T8p	DIFFOUT_T8p	Low_Speed	C8
8	VREFB8N0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	Low_Speed	B5
8	VREFB8N0	IO			DIFFIO_RX_T8n	DIFFOUT_T8n	Low_Speed	C7
8	VREFB8N0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	Low_Speed	C5
8	VREFB8N0	IO			DIFFIO_RX_T10p	DIFFOUT_T10p	Low_Speed	A4
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T9n	DIFFOUT_T9n	Low_Speed	C4
8	VREFB8N0	IO			DIFFIO_RX_T10n	DIFFOUT_T10n	Low_Speed	B4
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T11p	DIFFOUT_T11p	Low_Speed	G8
8	VREFB8N0	IO						A3
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T11n	DIFFOUT_T11n	Low_Speed	H8
8	VREFB8N0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	Low_Speed	D6
8	VREFB8N0	IO			DIFFIO_RX_T14p	DIFFOUT_T14p	Low_Speed	A2
8	VREFB8N0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	Low_Speed	D5
8	VREFB8N0	IO			DIFFIO_RX_T14n	DIFFOUT_T14n	Low_Speed	B2
		GND						V18
		GND						V1
		GND						U4
		GND						U14
		GND						U10
		GND						R7
		GND						N5
		GND						N2

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
		GND						N17
		GND						N12
		GND						N10
		GND						M14
		GND						L4
		GND						K9
		GND						K6
		GND						K13
		GND						J17
		GND						J10
		GND						H14
		GND						G4
		GND						G2
		GND						F8
		GND						F17
		GND						E6
		GND						E13
		GND						E10
		GND						D3
		GND						B6
		GND						B15
		GND						B10
		GND						A18
		GND						A1
		VCC						L9
		VCC						K10
		VCC						J9
		VCC						H10
		VCCD_PLL1						N6
		VCCD_PLL2						F13
		VCCIO1						H5
		VCCIO1						G5
		VCCIO1						K5
		VCCIO1						J5
		VCCIO2						M5
		VCCIO2						L6
		VCCIO2						L5
		VCCIO3						P9
		VCCIO3						P8
		VCCIO3						P7
		VCCIO3						N9
		VCCIO5						M13
		VCCIO5						L14
		VCCIO5						L13
		VCCIO5						K14
		VCCIO6						J14
		VCCIO6						J13
		VCCIO6						H13
		VCCIO6						G14
		VCCIO6						G13
		VCCIO8						F9
		VCCIO8						E9
		VCCIO8						E8
		VCCIO8						E7
		NC						V17
		NC						V16
		NC						V15
		NC						V14
		NC						V13
		NC						V11
		NC						V10
		NC						U18
		NC						U17
		NC						U16
		NC						U15
		NC						U13
		NC						U12
		NC						T3
		NC						T2
		NC						T18
		NC						T15
		NC						T14
		NC						T13
		NC						T12
		NC						T11
		NC						T1
		NC						R3
		NC						R14
		NC						R13
		NC						R12
		NC						R11
		NC						R10
		NC						P3
		NC						P2

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	U324
		NC						P12
		NC						P11
		NC						P10
		NC						N16
		NC						N15
		NC						N13
		NC						N11
		NC						M7
		NC						M16
		NC						M15
		NC						M12
		NC						M11
		NC						M10
		NC						L7
		NC						L10
		NC						J16
		NC						J15
		NC						J12
		NC						J11
		NC						H16
		NC						H15
		NC						G1
		NC						F7
		NC						F4
		NC						F3
		NC						F12
		NC						F11
		NC						F1
		NC						E3
		NC						E2
		NC						E14
		NC						E12
		NC						E11
		NC						E1
		NC						D9
		NC						D2
		NC						D14
		NC						D13
		NC						D12
		NC						D11
		NC						D10
		NC						D1
		NC						C3
		NC						C2
		NC						C16
		NC						C15
		NC						C14
		NC						C13
		NC						C12
		NC						C11
		NC						C1
		NC						B3
		NC						B17
		NC						B16
		NC						B14
		NC						B13
		NC						B12
		NC						B11
		NC						B1
		NC						A7
		NC						A17
		NC						A16
		NC						A15
		NC						A14
		NC						A13
		NC						A12
		NC						A11
		NC						A10
		VCCA1						M6
		VCCA2						F14
		VCCA3						F6
		VCCA4						P13

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the MAX 10 FPGA Device Family Pin Connection Guidelines.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	V36
1B	VREFB1N0	IO		JTAGEN				C2
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	C3
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	D3
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L8n	DIFFOUT_L8n	Low_Speed	C1
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L8p	DIFFOUT_L8p	Low_Speed	D2
1B	VREFB1N0	IO						E2
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L14n	High_Speed	D1
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L14p	High_Speed	E1
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	F2
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	F3
3	VREFB3N0	IO			DIFFIO_TX_RX_B7n	DIFFOUT_B7n	High_Speed	E3
3	VREFB3N0	IO			DIFFIO_TX_RX_B7p	DIFFOUT_B7p	High_Speed	F4
3	VREFB3N0	IO			DIFFIO_TX_RX_B16n	DIFFOUT_B16n	High_Speed	E4
3	VREFB3N0	IO			DIFFIO_TX_RX_B16p	DIFFOUT_B16p	High_Speed	E5
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R10p	DIFFOUT_R10p	High_Speed	D6
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R10n	DIFFOUT_R10n	High_Speed	E6
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R12p	DIFFOUT_R12p	High_Speed	D5
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R12n	DIFFOUT_R12n	High_Speed	C6
6	VREFB6N0	IO	PLL_R_CLKOUTp		DIFFIO_RX_R23p	DIFFOUT_R23p	High_Speed	C5
6	VREFB6N0	IO	PLL_R_CLKOUTn		DIFFIO_RX_R23n	DIFFOUT_R23n	High_Speed	B6
8	VREFB8N0	IO		DEV_CLRn				A5
8	VREFB8N0	IO		DEV_OE				B5
8	VREFB8N0	IO		CONFIG_SEL				B4
8	VREFB8N0	Input_only		nCONFIG				A4
8	VREFB8N0	IO		CRC_ERROR				A3
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T11p	DIFFOUT_T11p	Low_Speed	B2
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T11n	DIFFOUT_T11n	Low_Speed	A2
		GND						F6
		GND						F1
		GND						B3
		VCC						F5
		VCC						B1
		VCCIO1_2_8						C4
		VCCIO3_5_6						D4
		VCCA2						A6
		VCCA3						A1

Note:
(1) For more information about pin definition and pin connection guidelines, refer to the MAX 10 FPGA Device Family Pin Connection Guidelines.

Date	Version	Changes Made
December 2014	2014.12.15	Initial release.
December 2016	2016.12.23	Removed I/O performance for single-ended pins.
February 2017	2017.02.21	Rebranded as Intel.