



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated TriX Channel	Emulated LVDS Output Channel	U0F2	DQS for X8	DQS for X16	HMC Pin Assignment for DQS/ADDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
0		REFCLK1n					N8								
0		REFCLK1p					P8								
0		GXB TX 15n					D1								
0		GXB TX 15p					D2								
0		GXB RX 15p GXB REFCLK 15p					F2								
0		GXB RX 15n GXB REFCLK 15n					F1								
0		GXB TX 14n					H1								
0		GXB TX 14p					H2								
0		GXB RX 14p GXB REFCLK 14p					K2								
0		GXB RX 14n GXB REFCLK 14n					K1								
0		GXB TX 13n					M1								
0		GXB TX 13p					M2								
0		GXB RX 13n GXB REFCLK 13n					Q2								
0		GXB RX 13n GXB REFCLK 13n					Q1								
0		GXB TX 12n					T1								
0		GXB RX 12p GXB REFCLK 12p					V2								
0		GXB RX 12n GXB REFCLK 12n					V1								
0		GXB TX 11n					W1								
0		GXB TX 11p					W2								
0		GXB RX 11p GXB REFCLK 11p					AB2								
0		GXB RX 11n GXB REFCLK 11n					AB1								
0		GXB TX 10n					AD1								
0		GXB TX 10p					AD2								
0		GXB RX 10p GXB REFCLK 10p					AF2								
0		GXB RX 10n GXB REFCLK 10n					AF1								
0		REFCLK0n					U5								
0		REFCLK0p					V5								
0		TDO		TDO			Y9								
0		ASD0		DATA4			AA6								
0		TMS		TMS			AC7								
0		AS_DATA3		DATA3			AB6								
0		TC0		TC0			AB5								
0		AS_DATA2		DATA2			AC5								
0		TD1		TD1			W10								
0		AS_DATA1		DATA1			AC6								
0		DCLK		DCLK			AA8								
0		AS_DATA0 ASD0		DATA0			AD7								
0	VREFBIAND	ID		DATA5	DIFFIO_RX_B1n	DIFFIOUT_B1n	V8	DQ1B							
0	VREFBIAND	ID		DATA5	DIFFIO_TX_B2n	DIFFIOUT_B2n	V4								
0	VREFBIAND	ID		DATA7	DIFFIO_RX_B1p	DIFFIOUT_B1p	W8	DQ1B							
0	VREFBIAND	ID		DATA7	DIFFIO_TX_B2p	DIFFIOUT_B2p	V2	DQ1B							
0	VREFBIAND	ID		DATA10	DIFFIO_RX_B3n	DIFFIOUT_B3n	T8	DQS0B							
0	VREFBIAND	ID		DATA9	DIFFIO_TX_B4n	DIFFIOUT_B4n	AB4	DQ1B							
0	VREFBIAND	ID		DATA2	DIFFIO_RX_B3p	DIFFIOUT_B3p	V2	DQS0B							
0	VREFBIAND	ID		DATA11	DIFFIO_TX_B4p	DIFFIOUT_B4p	AA4								
0	VREFBIAND	ID		DATA14	DIFFIO_RX_B5n	DIFFIOUT_B5n	V10	DQ1B							
0	VREFBIAND	ID		DATA11	DIFFIO_TX_B5p	DIFFIOUT_B5p	AD4								
0	VREFBIAND	ID		CLKUSR	DIFFIO_RX_B5p	DIFFIOUT_B5p	U10	DQ1B							
0	VREFBIAND	ID		DATA15	DIFFIO_TX_B5p	DIFFIOUT_B5p	AC4	DQ1B							
0	VREFBIAND	ID		PR_DONE	DIFFIO_RX_B7n	DIFFIOUT_B7n	AA11								
0	VREFBIAND	ID		PR_READY	DIFFIO_TX_B8n	DIFFIOUT_B8n	AE6	DQ1B							
0	VREFBIAND	ID		PR_ERROR	DIFFIO_RX_B7p	DIFFIOUT_B7p	V11								
0	VREFBIAND	ID			DIFFIO_TX_B8p	DIFFIOUT_B8p	AD5	DQ1B							
0	VREFBIAND	ID			DIFFIO_TX_B8n	DIFFIOUT_B8n	AF4			GND					
0	VREFBIAND	ID			DIFFIO_RX_B10n	DIFFIOUT_B10n	AE9	DQ2B		B.A.15					
0	VREFBIAND	ID			DIFFIO_TX_B9p	DIFFIOUT_B9p	AE4	DQ2B		B.VREF					
0	VREFBIAND	ID			DIFFIO_RX_B10p	DIFFIOUT_B10p	AD10	DQ2B		B.A.14					
0	VREFBIAND	ID			DIFFIO_RX_B11n	DIFFIOUT_B11n	U11	DQS0B		B.CSF.1		B.CSF.1			
0	VREFBIAND	ID			DIFFIO_TX_B12n	DIFFIOUT_B12n	AE8	DQ2B		B.A.13					
0	VREFBIAND	ID			DIFFIO_RX_B11p	DIFFIOUT_B11p	T11	DQS0B		B.CSF.0		B.CSF.0			
0	VREFBIAND	ID			DIFFIO_TX_B12p	DIFFIOUT_B12p	AE7			B.A.12					
0	VREFBIAND	ID			DIFFIO_TX_B13n	DIFFIOUT_B13n	AF9	DQ2B		B.A.11					
0	VREFBIAND	ID			DIFFIO_RX_B14n	DIFFIOUT_B14n	AE11	DQ2B		B.A.9					
0	VREFBIAND	ID			DIFFIO_TX_B13p	DIFFIOUT_B13p	AE8	DQ2B		B.A.10					
0	VREFBIAND	ID			DIFFIO_RX_B14p	DIFFIOUT_B14p	AD11	DQ2B		B.A.11					
0	VREFBIAND	ID	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B15n	DIFFIOUT_B15n	W11			B.RAS#					
0	VREFBIAND	ID			DIFFIO_TX_B16n	DIFFIOUT_B16n	AF6	DQ2B							
0	VREFBIAND	ID	CLK0p,FPLL_BL_FBP		DIFFIO_RX_B16p	DIFFIOUT_B16p	V11								
0	VREFBIAND	ID			DIFFIO_TX_B16p	DIFFIOUT_B16p	AF5	DQ2B		B.CAS#					
0	VREFBIAND	ID			DIFFIO_TX_B17n	DIFFIOUT_B17n	AG8			GND					
0	VREFBIAND	ID			DIFFIO_RX_B18n	DIFFIOUT_B18n	AF10	DQ3B		B.BA.2					
0	VREFBIAND	ID			DIFFIO_TX_B17p	DIFFIOUT_B17p	AF7	DQ3B		B.BA.0					
0	VREFBIAND	ID			DIFFIO_RX_B18p	DIFFIOUT_B18p	AF11	DQ3B		B.BA.1					
0	VREFBIAND	ID			DIFFIO_RX_B19n	DIFFIOUT_B19n	T12	DQS0B		B.CKE					
0	VREFBIAND	ID			DIFFIO_TX_B20n	DIFFIOUT_B20n	AH2	DQ3B		B.A.7					
0	VREFBIAND	ID			DIFFIO_RX_B19p	DIFFIOUT_B19p	T13	DQS0B		B.CK					
0	VREFBIAND	ID			DIFFIO_TX_B20p	DIFFIOUT_B20p	AH3			B.A.6					
0	VREFBIAND	ID	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B21n	DIFFIOUT_B21n	AA4	DQ3B		B.A.3					
0	VREFBIAND	ID			DIFFIO_RX_B22n	DIFFIOUT_B22n	AD12	DQ3B		B.A.4					
0	VREFBIAND	ID	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B21p	DIFFIOUT_B21p	AG5	DQ3B		B.A.2					
0	VREFBIAND	ID			DIFFIO_RX_B22p	DIFFIOUT_B22p	AE12	DQ3B		B.A.4					
0	VREFBIAND	ID	CLK1n		DIFFIO_RX_B23n	DIFFIOUT_B23n	W12								
0	VREFBIAND	ID			DIFFIO_TX_B24n	DIFFIOUT_B24n	AH5	DQ3B		B.A.1					
0	VREFBIAND	ID	CLK1p		DIFFIO_RX_B23p	DIFFIOUT_B23p	V12								
0	VREFBIAND	ID			DIFFIO_TX_B24p	DIFFIOUT_B24p	AH6	DQ3B		B.A.0					
0	VREFBIAND	ID	RZ0_0		DIFFIO_TX_B25n	DIFFIOUT_B25n	AH7								
0	VREFBIAND	ID			DIFFIO_RX_B26n	DIFFIOUT_B26n	AF13	DQ4B		B.DQ.0					
0	VREFBIAND	ID			DIFFIO_TX_B26p	DIFFIOUT_B26p	AG8	DQ4B		B.DQ.2					
0	VREFBIAND	ID			DIFFIO_RX_B26p	DIFFIOUT_B26p	AG13	DQ4B		B.DQ.1					
0	VREFBIAND	ID			DIFFIO_RX_B27n	DIFFIOUT_B27n	U13	DQS0B		B.DQS.0					
0	VREFBIAND	ID			DIFFIO_TX_B28n.3	DIFFIOUT_B28n.3	AH8	DQ4B		B.DQ.3					
0	VREFBIAND	ID			DIFFIO_RX_B27p	DIFFIOUT_B27p	U14	DQS0B		B.DQS.0					
0	VREFBIAND	ID			DIFFIO_TX_B28n	DIFFIOUT_B28n	AG9			B.ODT.0					
0	VREFBIAND	ID			DIFFIO_TX_B28n.1	DIFFIOUT_B28n.1	AH9	DQ4B		B.ODT.1					
0	VREFBIAND	ID			DIFFIO_RX_B30n	DIFFIOUT_B30n	AE15	DQ4B		B.DQ.4					
0	VREFBIAND	ID			DIFFIO_TX_B29p	DIFFIOUT_B29p	AG10	DQ4B		B.DQ.6					
0	VREFBIAND	ID			DIFFIO_RX_B30p	DIFFIOUT_B30p	AF15	DQ4B		B.DQ.5					
0	VREFBIAND	ID	CLK2n		DIFFIO_RX_B31n	DIFFIOUT_B31n	AA13								
0	VREFBIAND	ID			DIFFIO_TX_B32n	DIFFIOUT_B32n	AH11	DQ4B		B.DQ.7					
0	VREFBIAND	ID	CLK2p		DIFFIO_RX_B31p	DIFFIOUT_B31p	V13								
0	VREFBIAND	ID			DIFFIO_TX_B32p	DIFFIOUT_B32p	AG11	DQ4B		B.DM.0					
0	VREFBIAND	ID			DIFFIO_RX_B34n	DIFFIOUT_B34n	AG16	DQ5B		B.DQ.8					
0	VREFBIAND	ID			DIFFIO_TX_B33p	DIFFIOUT_B33p	AH12	DQ5B		B.DQ.10					
0	VREFBIAND	ID			DIFFIO_RX_B34p	DIFFIOUT_B34p	AF17	DQ5B		B.DQ.9					
0	VREFBIAND	ID			DIFFIO_RX_B35n	DIFFIOUT_B35n	V13	DQS0B		B.DQS.1					
0	VREFBIAND	ID			DIFFIO_TX_B36n	DIFFIOUT_B36n	AH13	DQ5B		B.DQ.11					
0	VREFBIAND	ID			DIFFIO_RX_B35p	DIFFIOUT_B35p	W14	DQS0B		B.DQS.1					
0	VREFBIAND	ID			DIFFIO_TX_B36p	DIFFIOUT_B36p	AZ14			B.CLK.1					
0	VREFBIAND	ID			DIFFIO_TX_B37n	DIFFIOUT_B37n	AH14	DQ5B		B.CK.0					
0	VREFBIAND	ID			DIFFIO_RX_B38n	DIFFIOUT_B38n	AE17	DQ5B		B.DQ.12					
0	VREFBIAND	ID			DIFFIO_TX_B37p	DIFFIOUT_B37p	AG15	DQ5B		B.DQ.14					
0	VREFBIAND	ID			DIFFIO_RX_B38p	DIFFIOUT_B38p	AD17	DQ5B		B.DQ.13					
0	VREFBIAND	ID	CLK3n		DIFFIO_RX_B39n	DIFFIOUT_B39n	AA15								
0	VREFBIAND	ID			DIFFIO_TX_B40n	DIFFIOUT_B40n	AH16	DQ5B		B.DQ.15					
0	VREFBIAND	ID	CLK3p		DIFFIO_RX_B39p	DIFFIOUT_B39p	V15								
0	VREFBIAND	ID			DIFFIO_TX_B40p	DIFFIOUT_B40p	AH17	DQ5B		B.DM.1					
0	VREFBIAND	ID			DIFFIO_RX_B42n	DIFFIOUT_B42n	AD19	DQ5B		B.DQ.16					
0	VREFBIAND	ID			DIFFIO_TX_B41p	DIFFIOUT_B41p	AF18	DQ5B		B.DQ.18					
0	VREFBIAND	ID			DIFFIO_RX_B42p	DIFFIOUT_B42p	AE19	DQ5B		B.DQ.17					
0	VREFBIAND	ID			DIFFIO_RX_B43n	DIFFIOUT_B43n	AA18	DQS0B		B.DQS.2					
0	VREFBIAND	ID			DIFFIO_TX_B44n	DIFFIOUT_B44n	AH18	DQS0B		B.DQ.19					
0	VREFBIAND	ID			DIFFIO_RX_B43p	DIFFIOUT_B43p	AA19	DQS0B		B.DQS.2					
0	VREFBIAND	ID			DIFFIO_TX_B44p	DIFFIOUT_B44p	AG18	DQS0B		B.DQS.2					
0	VREFBIAND	ID			DIFFIO_TX_B45n	DIFFIOUT_B45n	AH19	DQ5B							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U072	DQS for X8	DQS for X16	HMC Pin Assignment for DDR0/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
4A	VREFBIAND	ID			DFFIO RX B46p	DFFOUT B46p	A020	DQ08	DQ18	B_DQ_20	B_DQ_20				
4A	VREFBIAND	ID			DFFIO TX B45p	DFFOUT B45p	A019	DQ08	DQ18	B_DQ_22	B_DQ_22				
4A	VREFBIAND	ID			DFFIO RX B46p	DFFOUT B46p	A020	DQ08	DQ18	B_DQ_21	B_DQ_21				
4A	VREFBIAND	ID			DFFIO TX B45p	DFFOUT B45p	A019	DQ08	DQ18	B_DQ_23	B_DQ_23				
4A	VREFBIAND	ID			DFFIO TX B46p	DFFOUT B46p	A020	DQ08	DQ18	B_DM_2	B_DM_2				
4A	VREFBIAND	ID			DFFIO RX B50m	DFFOUT B50m	A021	DQ07B	DQ28	B_DQ_24	B_DQ_24				
4A	VREFBIAND	ID			DFFIO TX B49p	DFFOUT B49p	A021	DQ07B	DQ28	B_DQ_26	B_DQ_26				
4A	VREFBIAND	ID			DFFIO RX B50p	DFFOUT B50p	A022	DQ07B	DQ28	B_DQ_25	B_DQ_25				
4A	VREFBIAND	ID			DFFIO TX B51m	DFFOUT B51m	A022	DQ07B	DQ28	B_DQS#_3	B_DQS#_3				
4A	VREFBIAND	ID			DFFIO TX B51p	DFFOUT B51p	A023	DQ07B	DQ28	B_DQ_27	B_DQ_27				
4A	VREFBIAND	ID			DFFIO TX B53m	DFFOUT B53m	A022	DQ07B	DQ28	QND	QND				
4A	VREFBIAND	ID			DFFIO TX B54m	DFFOUT B54m	A023	DQ07B	DQ28	B_DQ_28	B_DQ_28				
4A	VREFBIAND	ID			DFFIO TX B53p	DFFOUT B53p	A023	DQ07B	DQ28	B_DQ_30	B_DQ_30				
4A	VREFBIAND	ID			DFFIO RX B54p	DFFOUT B54p	A023	DQ07B	DQ28	B_DQ_29	B_DQ_29				
4A	VREFBIAND	ID			DFFIO TX B56p	DFFOUT B56p	A024	DQ07B	DQ28	B_DQ_31	B_DQ_31				
4A	VREFBIAND	ID			DFFIO TX B56p	DFFOUT B56p	A024	DQ07B	DQ28	B_DM_3	B_DM_3				
4A	VREFBIAND	ID			DFFIO RX B59m	DFFOUT B59m	A023	DQ08B	DQ28	B_DQ_32	B_DQ_32				
4A	VREFBIAND	ID			DFFIO TX B59p	DFFOUT B59p	A026	DQ08B	DQ28	B_DQ_34	B_DQ_34				
4A	VREFBIAND	ID			DFFIO RX B59p	DFFOUT B59p	A024	DQ08B	DQ28	B_DM_33	B_DM_33				
4A	VREFBIAND	ID			DFFIO RX B59m	DFFOUT B59m	A023	DQ08B	DQ28	B_DQS#_2	B_DQS#_2				
4A	VREFBIAND	ID			DFFIO TX B60m	DFFOUT B60m	A026	DQ08B	DQ28	B_DQ_35	B_DQ_35				
4A	VREFBIAND	ID			DFFIO RX B59p	DFFOUT B59p	A022	DQ08B	DQ28	B_DQS_4	B_DQS_4				
4A	VREFBIAND	ID			DFFIO TX B61m	DFFOUT B61m	A027	DQ08B	DQ28	QND	QND				
4A	VREFBIAND	ID			DFFIO RX B62p	DFFOUT B62p	A025	DQ08B	DQ28	B_DQ_36	B_DQ_36				
4A	VREFBIAND	ID			DFFIO TX B61p	DFFOUT B61p	A028	DQ08B	DQ28	B_DM_38	B_DM_38				
4A	VREFBIAND	ID			DFFIO RX B62p	DFFOUT B62p	A026	DQ08B	DQ28	B_DQ_37	B_DQ_37				
4A	VREFBIAND	ID			DFFIO TX B64m	DFFOUT B64m	A028	DQ08B	DQ28	B_DM_39	B_DM_39				
4A	VREFBIAND	ID			DFFIO TX B64p	DFFOUT B64p	A027	DQ08B	DQ28	B_DM_4	B_DM_4				
5A	VREFBIAND	ID	BDQ_1		DFFIO TX B65m	DFFOUT B65m	A028	DQ08B	DQ28						
5A	VREFBIAND	ID		INT_DONE	DFFIO RX R2p	DFFOUT R2p	A020								
5A	VREFBIAND	ID		PR_REQUEST	DFFIO TX R1m	DFFOUT R1m	A026	DQ1R							
5A	VREFBIAND	ID		CRG_ERROR	DFFIO TX R2m	DFFOUT R2m	A028	DQ1R							
5A	VREFBIAND	ID		MEMO	DFFIO TX R3p	DFFOUT R3p	A025	DQ1R							
5A	VREFBIAND	ID			DFFIO RX R4p	DFFOUT R4p	V17	DQ1R							
5A	VREFBIAND	ID		CIP_CONF_DONE	DFFIO TX R5m	DFFOUT R5m	A026	DQ1R							
5A	VREFBIAND	ID		DEV_OE	DFFIO RX R4m	DFFOUT R4m	A024								
5A	VREFBIAND	ID		HPSRSTL0	DFFIO TX R5p	DFFOUT R5p	V18	DQ1R							
5A	VREFBIAND	ID		DEV_CLRn	DFFIO TX R5m	DFFOUT R5m	A023	DQ1R							
5A	VREFBIAND	ID		HPSRSTL1	DFFIO RX R6m	DFFOUT R6m	V15	DQS#1R							
5A	VREFBIAND	ID			DFFIO TX R7p	DFFOUT R7p	A024	DQ1R							
5A	VREFBIAND	ID			DFFIO RX R6p	DFFOUT R6p	V16	DQ1R							
5A	VREFBIAND	ID			DFFIO TX R7m	DFFOUT R7m	A023								
5A	VREFBIAND	ID			DFFIO RX R6m	DFFOUT R6m	V15	DQ1R							
0B	VREFBIAND_HPS	HPS DDR					A028			HPS_DM_4	HPS_DM_4				
0B	VREFBIAND_HPS	HPS DDR					A028			HPS_DQ_39	HPS_DQ_39				
0B	VREFBIAND_HPS	HPS DDR					V20			HPS_DQ_37	HPS_DQ_37				
0B	VREFBIAND_HPS	HPS DDR					A027			HPS_DQ_38	HPS_DQ_38				
0B	VREFBIAND_HPS	HPS DDR					V19			HPS_DQ_36	HPS_DQ_36				
0B	VREFBIAND_HPS	HPS DDR					V18			HPS_DQ_35	HPS_DQ_35				
0B	VREFBIAND_HPS	HPS GPI3					V24								
0B	VREFBIAND_HPS	HPS DDR					V17			HPS_DQS#_4	HPS_DQS#_4				
0B	VREFBIAND_HPS	HPS DDR					V25			HPS_DQ_35	HPS_DQ_35				
0B	VREFBIAND_HPS	HPS DDR					U25			HPS_DQ_33	HPS_DQ_33				
0B	VREFBIAND_HPS	HPS DDR					A028			HPS_DQ_34	HPS_DQ_34				
0B	VREFBIAND_HPS	HPS DDR					T26			HPS_DQ_32	HPS_DQ_32				
0B	VREFBIAND_HPS	HPS GPI2					A027								
0B	VREFBIAND_HPS	HPS GPI1					U16								
0B	VREFBIAND_HPS	HPS DDR					H028			HPS_DM_3	HPS_DM_3				
0B	VREFBIAND_HPS	HPS GPI0					U15								
0B	VREFBIAND_HPS	HPS DDR					A027			HPS_DQ_31	HPS_DQ_31				
0B	VREFBIAND_HPS	HPS DDR					T24			HPS_DQ_29	HPS_DQ_29				
0B	VREFBIAND_HPS	HPS DDR					V27			HPS_DQ_30	HPS_DQ_30				
0B	VREFBIAND_HPS	HPS DDR					R24			HPS_DQ_28	HPS_DQ_28				
0B	VREFBIAND_HPS	VREFBIAND_HPS					V27								
0B	VREFBIAND_HPS	HPS DDR					U19			HPS_DQS_3	HPS_DQS_3				
0B	VREFBIAND_HPS	HPS DDR					T26								
0B	VREFBIAND_HPS	HPS DDR					T20			HPS_DQS#_3	HPS_DQS#_3				
0B	VREFBIAND_HPS	HPS DDR					W26			HPS_DQ_27	HPS_DQ_27				
0B	VREFBIAND_HPS	HPS DDR					R25			HPS_DQ_25	HPS_DQ_25				
0B	VREFBIAND_HPS	HPS DDR					A028			HPS_DQ_26	HPS_DQ_26				
0B	VREFBIAND_HPS	HPS DDR					R26			HPS_DQ_24	HPS_DQ_24				
0B	VREFBIAND_HPS	VREFBIAND_HPS					V28								
0B	VREFBIAND_HPS	HPS GPI7					V16								
0B	VREFBIAND_HPS	HPS DDR					W28			HPS_DM_2	HPS_DM_2				
0B	VREFBIAND_HPS	HPS GPI6					T17								
0B	VREFBIAND_HPS	HPS DDR					V27			HPS_DQ_23	HPS_DQ_23				
0B	VREFBIAND_HPS	HPS DDR					N27			HPS_DQ_21	HPS_DQ_21				
0B	VREFBIAND_HPS	HPS DDR					R27			HPS_DQ_22	HPS_DQ_22				
0B	VREFBIAND_HPS	HPS DDR					N26			HPS_DQ_20	HPS_DQ_20				
0B	VREFBIAND_HPS	HPS GPI5					P26								
0B	VREFBIAND_HPS	HPS DDR					T19			HPS_DQS_2	HPS_DQS_2				
0B	VREFBIAND_HPS	HPS DDR					V28			HPS_RESET#	HPS_RESET#				
0B	VREFBIAND_HPS	HPS DDR					T18			HPS_DQS#_2	HPS_DQS#_2				
0B	VREFBIAND_HPS	HPS DDR					U28			HPS_DQ_19	HPS_DQ_19				
0B	VREFBIAND_HPS	HPS DDR					N25			HPS_DQ_17	HPS_DQ_17				
0B	VREFBIAND_HPS	HPS DDR					T28			HPS_DQ_18	HPS_DQ_18				
0B	VREFBIAND_HPS	HPS DDR					N24			HPS_DQ_16	HPS_DQ_16				
0B	VREFBIAND_HPS	HPS GPI4					R28								
0A	VREFBIAND_HPS	HPS GPI3					R21								
0A	VREFBIAND_HPS	HPS DDR					P26			HPS_DM_1	HPS_DM_1				
0A	VREFBIAND_HPS	HPS GPI2					R20								
0A	VREFBIAND_HPS	HPS DDR					N28			HPS_DQ_15	HPS_DQ_15				
0A	VREFBIAND_HPS	HPS DDR					M26			HPS_DQ_13	HPS_DQ_13				
0A	VREFBIAND_HPS	HPS DDR					M28			HPS_DQ_14	HPS_DQ_14				
0A	VREFBIAND_HPS	HPS DDR					M27			HPS_DQ_12	HPS_DQ_12				
0A	VREFBIAND_HPS	HPS DDR					L28			HPS_CKE_0	HPS_CKE_0				
0A	VREFBIAND_HPS	HPS DDR					R19			HPS_DQS_1	HPS_DQS_1				
0A	VREFBIAND_HPS	HPS DDR					K28			HPS_CKE_1	HPS_CKE_1				
0A	VREFBIAND_HPS	HPS DDR					R18			HPS_DQS#_1	HPS_DQS#_1				
0A	VREFBIAND_HPS	HPS DDR					J28			HPS_DM_11	HPS_DM_11				
0A	VREFBIAND_HPS	HPS DDR					L25			HPS_DQ_9	HPS_DQ_9				
0A	VREFBIAND_HPS	HPS DDR					A27			HPS_DQ_10	HPS_DQ_10				
0A	VREFBIAND_HPS	HPS DDR					K25			HPS_DQ_8	HPS_DQ_8				
0A	VREFBIAND_HPS	HPS GPI1					K27								
0A	VREFBIAND_HPS	HPS DDR					M25								
0A	VREFBIAND_HPS	HPS DDR					G28			HPS_DM_0	HPS_DM_0				
0A	VREFBIAND_HPS	HPS DDR					T28			HPS_DQ_7	HPS_DQ_7				
0A	VREFBIAND_HPS	HPS DDR					K26			HPS_DQ_5	HPS_DQ_5				
0A	VREFBIAND_HPS	HPS DDR					G27			HPS_DQ_6	HPS_DQ_6				
0A	VREFBIAND_HPS	HPS DDR					J26			HPS_DQ_4	HPS_DQ_4				
0A	VREFBIAND_HPS	HPS DDR					K26			HPS_ODT_1	HPS_ODT_1				
0A	VREFBIAND_HPS	HPS DDR					R17			HPS_DQS_0	HPS_DQS_0				
0A	VREFBIAND_HPS	HPS DDR					D28			HPS_ODT_0	HPS_ODT_0				
0A	VREFBIAND_HPS	HPS DDR					R16			HPS_DQS#_0	HPS_DQS#_0				
0A	VREFBIAND_HPS	HPS DDR					J27			HPS_DQ_3	HPS_DQ_3				
0A	VREFBIAND_HPS	HPS DDR					J25			HPS_DQ_2	HPS_DQ_2				
0A	VREFBIAND_HPS	HPS DDR					E28			HPS_DQ_2	HPS_DQ_2				
0A	VREFBIAND_HPS	HPS DDR					J25			HPS_DQ_0	HPS_DQ_0				
0A	VREFBIAND_HPS	VREFBIAND_HPS					N28								
0A	VREFBIAND_HPS	VREFBIAND_HPS					C28			HPS_CA_					



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U0F2	DQS for X8	DQS for X16	HMC Pin Assignment for DDR0/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
6A	VREFBIAND	HPS DDR					D0			HPS_A.6	HPS_CA.6				
6A	VREFBIAND	HPS DDR					D06			HPS_A.3	HPS_CA.3				
6A	VREFBIAND	HPS DDR					D01			HPS_CK	HPS_CK				
6A	VREFBIAND	HPS DDR					D06			HPS_A.6	HPS_CA.6				
6A	VREFBIAND	HPS DDR					D00			HPS_CK6	HPS_CK6				
6A	VREFBIAND	HPS DDR					D06			HPS_A.7	HPS_CA.7				
6A	VREFBIAND	HPS DDR					D05			HPS_BA.1					
6A	VREFBIAND	HPS DDR					A27			HPS_BA.0					
6A	VREFBIAND	HPS DDR					D26			HPS_BA.2					
6A	VREFBIAND	HPS DDR					A26			HPS_C06					
6A	VREFBIAND	HPS DDR					A25			HPS_RAS0					
6A	VREFBIAND	HPS DDR					F26			HPS_A.8	HPS_CA.8				
6A	VREFBIAND	HPS DDR					A24			HPS_A.10					
6A	VREFBIAND	HPS DDR					F25			HPS_A.9	HPS_CA.9				
6A	VREFBIAND	HPS DDR					B04			HPS_A.11					
6A	VREFBIAND	HPS DDR					D23			HPS_C06.0	HPS_C06.0				
6A	VREFBIAND	HPS DDR					D04			HPS_A.12					
6A	VREFBIAND	HPS DDR					L00			HPS_C06.1	HPS_C06.1				
6A	VREFBIAND	HPS DDR					C04								
6A	VREFBIAND	HPS DDR					G23			HPS_A.14					
6A	VREFBIAND	HPS DDR					C04			HPS_V06					
6A	VREFBIAND	HPS DDR					F24			HPS_A.15					
6A	VREFBIAND	HPS R20_0					D05								
7A		GND					F23								
7A		GND					E23								
7A		HPS_HRST					A23								
7A		HPS_H00R					H18								
7A		HPS_YD0					B03								
7A		VCCRSTCLK_HPS					J19								
7A		HPS_TMS					C23								
7A		HPS_TCK					K19								
7A		HPS_TRST					C22								
7A		HPS_TDI					D22								
7A		GND					D21								
7A		HPS_PORSEL					E18								
7A		HPS_CLK2					F20								
7A		HPS_CLK2					D00								
7A	VREFBIAND	TRACE_CLK					C21					TRACE_CLK			HPS_GPD08
7A	VREFBIAND	TRACE_D0					A20					TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPD09
7A	VREFBIAND	TRACE_D1					B01					TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPD00
7A	VREFBIAND	TRACE_D2					A21					TRACE_D2	SPIS0_MISO	IC21_SDA	HPS_GPD01
7A	VREFBIAND	TRACE_D3					K18					TRACE_D3	SPIS0_SS0	IC21_SCL	HPS_GPD02
7A	VREFBIAND	TRACE_D4					A30					TRACE_D4	SPIS0_CLK	CAN0_RX	HPS_GPD03
7A	VREFBIAND	TRACE_D5					J18					TRACE_D5	SPIS0_MOSI	CAN0_TX	HPS_GPD04
7A	VREFBIAND	TRACE_D6					A19					TRACE_D6	SPIS0_MISO	IC20_SDA	HPS_GPD05
7A	VREFBIAND	TRACE_D7					C18					TRACE_D7	SPIS0_MISO	IC20_SCL	HPS_GPD06
7A	VREFBIAND	SPIM0_CLK					A18					SPIM0_CLK	IC21_SDA	UART0_CTS	HPS_GPD07
7A	VREFBIAND	SPIM0_MOSI					C17					SPIM0_MOSI	IC21_SCL	UART0_RST	HPS_GPD08
7A	VREFBIAND	SPIM0_MISO					B17					SPIM0_MISO	CAN0_RX	UART1_CTS	HPS_GPD09
7A	VREFBIAND	SPIM0_SS0/BOOTSEL0					J17					SPIM0_SS0	CAN0_TX	UART1_BTS	HPS_GPD00
7A	VREFBIAND	UART0_TX_CLKSEL1					A17					UART0_RX	SPIM0_SS1		HPS_GPD01
7A	VREFBIAND	IC20_SDA					H17					UART0_TX	SPIM0_SS1		HPS_GPD02
7A	VREFBIAND	IC20_SCL					C19					IC20_SDA	UART1_RX	SPIM0_CLK	HPS_GPD03
7A	VREFBIAND	CAN0_RX					B16					IC20_SCL	UART1_TX	SPIM0_MOSI	HPS_GPD04
7A	VREFBIAND	CAN0_RX					B19					CAN0_RX	SPIM0_MISO		HPS_GPD05
7A	VREFBIAND	CAN0_TX_CLKSEL0					C16					CAN0_TX	SPIM0_SS0		HPS_GPD06
7B	VREFBIAND	MAN0_ALE					J15					MAN0_ALE	RGMI0_TX_CLK		HPS_GPD14
7B	VREFBIAND	MAN0_CE					A16					RGMI0_TXD0	USB1_D0		HPS_GPD15
7B	VREFBIAND	MAN0_CLE					J14					MAN0_CLE	RGMI0_TXD1	USB1_D1	HPS_GPD16
7B	VREFBIAND	MAN0_RE					A15					MAN0_RE	RGMI0_TXD2	USB1_D2	HPS_GPD17
7B	VREFBIAND	MAN0_RB					D17					MAN0_RB	RGMI0_TXD3	USB1_D3	HPS_GPD18
7B	VREFBIAND	MAN0_D00					A14					MAN0_D00	RGMI0_RXD0		HPS_GPD19
7B	VREFBIAND	MAN0_D01					E16					MAN0_D01	RGMI0_RXD1	IC21_SDA	HPS_GPD20
7B	VREFBIAND	MAN0_D02					A13					MAN0_D02	RGMI0_RXD2	IC21_SCL	HPS_GPD21
7B	VREFBIAND	MAN0_D03					J13					MAN0_D03	RGMI0_RX_CTL	USB1_D4	HPS_GPD22
7B	VREFBIAND	MAN0_D04					A12					MAN0_D04	RGMI0_TX_CTL	USB1_D5	HPS_GPD23
7B	VREFBIAND	MAN0_D05					J12					MAN0_D05	RGMI0_RX_CLK	USB1_D6	HPS_GPD24
7B	VREFBIAND	MAN0_D06					A11					MAN0_D06	RGMI0_RXD1	USB1_D7	HPS_GPD25
7B	VREFBIAND	MAN0_D07					C15					MAN0_D07	RGMI0_RXD0		HPS_GPD26
7B	VREFBIAND	MAN0_WP					A09					MAN0_WP	RGMI0_RXD3	OSPI_SS2	HPS_GPD27
7B	VREFBIAND	MAN0_WP/BOOTSEL2					D16					MAN0_WP	OSPI_SS1		HPS_GPD28
7B	VREFBIAND	OSPI_A00					A08					OSPI_A00	USB1_CLK		HPS_GPD29
7B	VREFBIAND	OSPI_A01					H16					OSPI_A01	USB1_STP		HPS_GPD30
7B	VREFBIAND	OSPI_A02					A07					OSPI_A02	USB1_DM0		HPS_GPD31
7B	VREFBIAND	OSPI_A03					J18					OSPI_A03	USB1_NXT		HPS_GPD32
7B	VREFBIAND	OSPI_SS0/BOOTSEL1					A06					OSPI_SS0			HPS_GPD33
7B	VREFBIAND	OSPI_CLK					C14					OSPI_CLK			HPS_GPD34
7B	VREFBIAND	OSPI_SS1					B14					OSPI_SS1			HPS_GPD35
7C	VREFBIAND	SDMMC_CMD					D14					SDMMC_CMD	USB0_D0		HPS_GPD36
7C	VREFBIAND	SDMMC_A0/RWEN					A6					SDMMC_A0/RWEN	USB0_D1		HPS_GPD37
7C	VREFBIAND	SDMMC_D0					C13					SDMMC_D0	USB0_D2		HPS_GPD38
7C	VREFBIAND	SDMMC_D1					B6					SDMMC_D1	USB0_D3		HPS_GPD39
7C	VREFBIAND	SDMMC_D4					H13					SDMMC_D4	USB0_D4		HPS_GPD40
7C	VREFBIAND	SDMMC_D5					A4					SDMMC_D5	USB0_D5		HPS_GPD41
7C	VREFBIAND	SDMMC_D6					H12					SDMMC_D6	USB0_D6		HPS_GPD42
7C	VREFBIAND	SDMMC_D7					B4					SDMMC_D7	USB0_D7		HPS_GPD43
7C	VREFBIAND	SDMMC_GPI0/4					B12					SDMMC_D8	USB0_CLK		HPS_GPD44
7C	VREFBIAND	SDMMC_CCLK_OUT					B9					SDMMC_CCLK_OUT	USB0_STP		HPS_GPD45
7C	VREFBIAND	SDMMC_D3					B11					SDMMC_D3	USB0_DM		HPS_GPD46
7C	VREFBIAND	SDMMC_D3					B8					SDMMC_D3	USB0_NXT		HPS_GPD47
7D	VREFBIAND	RGMI0_TX_CLK					E4					RGMI0_TX_CLK			HPS_GPD0
7D	VREFBIAND	RGMI0_TXD0					C10					RGMI0_TXD0	USB1_D0		HPS_GPD01
7D	VREFBIAND	RGMI0_TXD1					F5					RGMI0_TXD1	USB1_D1		HPS_GPD02
7D	VREFBIAND	RGMI0_TXD2					C9					RGMI0_TXD2	USB1_D2		HPS_GPD03
7D	VREFBIAND	RGMI0_TXD3					C4					RGMI0_TXD3	USB1_D3		HPS_GPD04
7D	VREFBIAND	RGMI0_RXD0					C8					RGMI0_RXD0	USB1_D4		HPS_GPD05
7D	VREFBIAND	RGMI0_RXD1					D4					RGMI0_RXD1	USB1_D5		HPS_GPD06
7D	VREFBIAND	RGMI0_RXD2					C7					RGMI0_RXD2	IC22_SDA		HPS_GPD07
7D	VREFBIAND	RGMI0_RX_CTL					F4					RGMI0_RX_CTL	IC22_SCL		HPS_GPD08
7D	VREFBIAND	RGMI0_TX_CTL					C6					RGMI0_TX_CTL			HPS_GPD09
7D	VREFBIAND	RGMI0_RX_CLK					F4					RGMI0_RX_CLK	USB1_CLK		HPS_GPD10
7D	VREFBIAND	RGMI0_RXD1					C5					RGMI0_RXD1	USB1_STP		HPS_GPD11
7D	VREFBIAND	RGMI0_RXD2					E5					RGMI0_RXD2	USB1_DM		HPS_GPD12
7D	VREFBIAND	RGMI0_RXD3					D6					RGMI0_RXD3	USB1_NXT		HPS_GPD13
8A	VREFBIAND	ID	CLKp7				D12								
8A	VREFBIAND	ID	CLKn7				C12								
8A	VREFBIAND	ID	FPLL_TL_CLKOUT0/FPLL_TL_CLKOUT1/FPLL_TL_FB				F8								
8A	VREFBIAND	ID	FPLL_TL_CLKOUT0/FPLL_TL_CLKOUT1				D8								
8A	VREFBIAND	ID	CLK0p/FPLL_TL_FB0				E11								
8A	VREFBIAND	ID	CLK0n/FPLL_TL_FB0				D11								
8A	VREFBIAND	ID	CLK1p/FPLL_TL_FB1				L10								
8A	VREFBIAND	ID	CLK1n/FPLL_TL_FB1				H6								
8A	VREFBIAND	ID	CLK2p/FPLL_TL_FB2				L9								
8A	VREFBIAND	ID	CLK2n/FPLL_TL_FB2				H5								
8A	VREFBIAND	ID	CLK3p/FPLL_TL_FB3				L8								
8A	VREFBIAND	ID	CLK3n/FPLL_TL_FB3				H8								
8A	VREFBIAND	ID	CLK4p/FPLL_TL_FB4				H4								
8A	VREFBIAND	ID	CLK4n/FPLL_TL_FB4				J10								
8A	VREFBIAND	ID	CONF_DONE	MSEL0			J8								
8A	VREFBIAND	ID	CONF_DONE	MSEL1			H8								
8A	VREFBIAND	ID	CONF_DONE	MSEL2			E8								
8A	VREFBIAND	ID	CONF_DONE	MSEL3			G8								
8A	VREFBIAND	ID	CONF_DONE	MSEL4			K10								
8A	VREFBIAND	ID	CONF_DONE	MSEL5			F7								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U0F2	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		MSEL4		MSEL4			K3								
		GND					F8								
		GND					A10								
		GND					A3								
		GND					AA1								
		GND					AA7								
		GND					AA2								
		GND					AA3								
		GND					AA9								
		GND					AB4								
		GND					AB27								
		GND					AB3								
		GND					AC1								
		GND					AC2								
		GND					AC3								
		GND					AD14								
		GND					AD22								
		GND					AD35								
		GND					AD3								
		GND					AD6								
		GND					AD8								
		GND					AE1								
		GND					AE16								
		GND					AE16								
		GND					AE2								
		GND					AE3								
		GND					AF34								
		GND					AF3								
		GND					AG1								
		GND					AG17								
		GND					AG2								
		GND					AG27								
		GND					AG3								
		GND					AG7								
		GND					AH10								
		GND					AH20								
		GND					B15								
		GND					B17								
		GND					B20								
		GND					B22								
		GND					B25								
		GND					B27								
		GND					B3								
		GND					B5								
		GND					B7								
		GND					C1								
		GND					C11								
		GND					C2								
		GND					C3								
		GND					D10								
		GND					D13								
		GND					D16								
		GND					D3								
		GND					E1								
		GND					E19								
		GND					E2								
		GND					E22								
		GND					E24								
		GND					E27								
		GND					E3								
		GND					E9								
		GND					F3								
		GND					F51								
		GND					G2								
		GND					G3								
		GND					H11								
		GND					H15								
		GND					H16								
		GND					H20								
		GND					H24								
		GND					H27								
		GND					H5								
		GND					V3								
		GND					V20								
		GND					V20								
		GND					J1								
		GND					J5								
		GND					J5								
		GND					J5								
		GND					J8								
		GND					K11								
		GND					K12								
		GND					K14								
		GND					K16								
		GND					K20								
		GND					K3								
		GND					K4								
		GND					Y14								
		GND					L1								
		GND					Y12								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L2								
		GND					L24								
		GND					L27								
		GND					L3								
		GND					L5								
		GND					U4								
		GND					U5								
		GND					M10								
		GND					M11								
		GND					M14								
		GND					M16								
		GND					M20								
		GND					M3								
		GND					M8								
		GND					N1								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N2								
		GND					N3								
		GND					N6								
		GND					P10								
		GND					P16								
		GND					P18								
		GND					P20								
		GND					P25								
		GND					P3								
		GND					P5								
		GND					P5								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U62	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					R1								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R2								
		GND					R3								
		GND					R8								
		GND					T10								
		GND					T14								
		GND					T3								
		GND					U1								
		GND					U12								
		GND					U17								
		GND					U2								
		GND					U20								
		GND					U25								
		GND					U27								
		GND					U3								
		GND					U5								
		GND					U14								
		GND					U3								
		GND					U5								
		GND					V9								
		GND					W1								
		GND					W16								
		GND					W19								
		GND					W2								
		GND					W25								
		GND					W24								
		GND					Y24								
		GND					AA26								
		GND					W20								
		GND					W26								
		GND					W21								
		GND					U26								
		GND					U21								
		VCC					J11								
		VCC					K13								
		VCC					K15								
		VCC					L11								
		VCC					L12								
		VCC					L14								
		VCC					M12								
		VCC					M13								
		VCC					M15								
		VCC					M8								
		VCC					N10								
		VCC					N11								
		VCC					N12								
		VCC					N14								
		VCC					N8								
		VCC					P11								
		VCC					P13								
		VCC					P14								
		VCC					P15								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					R9								
		VCC					T15								
		VCC					T9								
		VCC					U26								
		DNU					A2								
		DNU					B2								
		DNU					D23								
		DNU					E12								
		DNU					U8								
		DNU					U614								
		VCCP6M					V10								
		VCCP6M					AD24								
		VCCP6M					H19								
		VCC1A1					D7								
		VCC10A					AA5								
		VCC10A					H19								
		VCC10B					AA12								
		VCC10B					AE10								
		VCC10B					AE13								
		VCC10B					AG4								
		VCC10A					AA16								
		VCC10A					AE21								
		VCC10A					AF14								
		VCC10A					AF19								
		VCC10A					AG13								
		VCC10A					AG22								
		VCC10A					AH15								
		VCC10A					AH25								
		VCC10A					W13								
		VCC10A					AC25								
		VCC10A					W17								
		VCC10A_HPS					C25								
		VCC10A_HPS					C27								
		VCC10A_HPS					F27								
		VCC10A_HPS					G24								
		VCC10A_HPS					H21								
		VCC10A_HPS					H26								
		VCC10A_HPS					L26								
		VCC10A_HPS					M21								
		VCC10B_HPS					AD27								
		VCC10B_HPS					P27								
		VCC10B_HPS					T21								
		VCC10B_HPS					T26								
		VCC10B_HPS					U18								
		VCC10B_HPS					U27								
		VCC10A_HPS					C20								
		VCC10A_HPS					D18								
		VCC10B_HPS					B13								
		VCC10B_HPS					H14								
		VCC10C_HPS					B10								
		VCC10D_HPS					D6								
		VCC10D_HPS					G6								
		VCC10A					E7								
		VCCP10A					AA10								
		VCCP10A					AA14								
		VCCP10A					AD13								
		VCCP10A					AD16								
		VCCP10A					AD18								
		VCCP10A					AD21								
		VCCP10A					AD9								
		VCCP10A					V21								
		VCCP10A_HPS					K21								
		VCCP10A_HPS					K24								
		VCCP10A_HPS					M24								
		VCCP10A_HPS					P21								
		VCCP10A_HPS					P24								
		VCCP10A_HPS					E21								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U072	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPDY0_HPS					E17								
		VCCPDY0_HPS					E14								
		VCCPDY0_HPS					E15								
		VCCPDY0_HPS					E19								
3A	VREFB3AND	VREFB3AND					A65								
3B	VREFB3BND	VREFB3BND					AF12								
4A	VREFB4AND	VREFB4AND					AF16								
5A	VREFB5AND	VREFB5AND					AC26								
		VREFB7A/B/C/D/E/G_HPS	VREFB7A/B/C/D/E/G_HPS				D19								
8A	VREFB8AND	VREFB8AND					D9								
		NC					W25								
		NC					AA25								
		NC					W19								
		VCC4_GXB1					M4								
		VCC4_GXB1					R4								
		VCC4_GXB1					L4								
		VCC4_GXB1					T4								
		MCPSSTCLK_HPS					F22								
		RREF_TL					B1								
		VCCA_FP1L					K5								
		VCCA_FP1L					R4								
		VCCA_FP1L					U4								
		VCCA_FP1L					U5								
		VCCA_FP1L					J4								
		VCCA_FP1L					AA21								
		VCC_AUX					AC21								
		VCC_AUX					AC6								
		VCC_AUX					AD15								
		VCC_AUX					E16								
		VCC_AUX					F8								
		VCC_AUX_SHARED					F21								
		VCC4_GXB1					M5								
		VCC4_GXB1					N5								
		VCC4_GXB1					R5								
		VCC4_GXB1					T5								
		VCC4_GXB1					H23								
		VCC_HPS					U21								
		VCC_HPS					K17								
		VCC_HPS					L16								
		VCC_HPS					L18								
		VCC_HPS					M17								
		VCC_HPS					M19								
		VCC_HPS					M19								
		VCC_HPS					N16								
		VCC_HPS					N19								
		VCC_HPS					P17								
		VCC_HPS					P19								

Notes:  
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Cyclone V Device Family Pin Connection Guidelines](#).  
 (2) HPS DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.  
 (3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSXFC4 Device  
Version 1.2

Version Number	Date	Changes Made
1.0	7/8/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.