



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated TriX Channel	Emulated LVDS Output Channel	U0E2	DQS for X8	DQS for X16	HMC Pin Assignment for DQS#ADDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3A		TDO		TDO			Y5								
3A		RCSO		TDO			AM6								
3A		TMS		TMS			AC7								
3A		AS_DATA3		DATA3			AB6								
3A		TCK		TCK			AB6								
3A		AS_DATA2		DATA2			AC5								
3A		TDI		TDI			W10								
3A		AS_DATA1		DATA1			AC6								
3A		CLK		CLK			AA6								
3A		AS_DATA3SS0		DATA3			AD7								
3A	VREFBIAND	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	V8	DQ1B							
3A	VREFBIAND	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	V4								
3A	VREFBIAND	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	V8	DQ1B							
3A	VREFBIAND	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V5	DQ1B							
3A	VREFBIAND	IO		DATA9	DIFFIO_RX_B3n	DIFFOUT_B3n	1B	DQS#1B							
3A	VREFBIAND	IO		DATA8	DIFFIO_TX_B4n	DIFFOUT_B4n	MB4	DQ1B							
3A	VREFBIAND	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	U9	DQS1B							
3A	VREFBIAND	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA5								
3A	VREFBIAND	IO		DATA4	DIFFIO_RX_B5n	DIFFOUT_B5n	V5	DQ1B							
3A	VREFBIAND	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AD4	DQ1B							
3A	VREFBIAND	IO		DATA5	DIFFIO_RX_B5p	DIFFOUT_B5p	U10	DQ1B							
3A	VREFBIAND	IO		DATA5	DIFFIO_TX_B6p	DIFFOUT_B6p	AC4	DQ1B							
3A	VREFBIAND	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AA11								
3A	VREFBIAND	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AE3	DQ1B							
3A	VREFBIAND	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	V11								
3A	VREFBIAND	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AD5	DQ1B							
3A	VREFBIAND	IO			DIFFIO_RX_B9n	DIFFOUT_B9n	AC4		GND						
3B	VREFBIAND	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AE3	DQ2B		B_A_15			GND		
3B	VREFBIAND	IO			DIFFIO_RX_B9p	DIFFOUT_B9p	AE4	DQ2B		B_WE#					
3B	VREFBIAND	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AD6	DQ2B		B_A_14					
3B	VREFBIAND	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	U11	DQS#2B		B_CSA_1			B_CSA#_1		
3B	VREFBIAND	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AF9	DQ2B		B_A_13					
3B	VREFBIAND	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	T11	DQS#2B		B_CSA_0			B_CSA#_0		
3B	VREFBIAND	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AE7	DQ2B		B_A_12					
3B	VREFBIAND	IO			DIFFIO_RX_B13n	DIFFOUT_B13n	AF9	DQ2B		B_A_11					
3B	VREFBIAND	IO			DIFFIO_TX_B14n	DIFFOUT_B14n	AE11	DQ2B		B_A_1				B_CA_3	
3B	VREFBIAND	IO			DIFFIO_RX_B13p	DIFFOUT_B13p	AE8	DQ2B		B_A_10					
3B	VREFBIAND	IO			DIFFIO_TX_B14p	DIFFOUT_B14p	AD11	DQ2B		B_A_9				B_CA_8	
3B	VREFBIAND	IO		CLK0p,FPLL_BL_FBn	DIFFIO_RX_B15n	DIFFOUT_B15n	W11			B_RA#P					
3B	VREFBIAND	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AF5	DQ2B							
3B	VREFBIAND	IO		CLK0p,FPLL_BL_FBn	DIFFIO_RX_B15p	DIFFOUT_B15p	V11								
3B	VREFBIAND	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AF6	DQ2B		B_CAS#					
3B	VREFBIAND	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AG6		GND						
3B	VREFBIAND	IO			DIFFIO_TX_B18n	DIFFOUT_B18n	AF10	DQ3B		B_BA_2					
3B	VREFBIAND	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AF7	DQ3B		B_BA_0					
3B	VREFBIAND	IO			DIFFIO_TX_B18p	DIFFOUT_B18p	AF11	DQ3B		B_BA_1					
3B	VREFBIAND	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	T12	DQS#3B		B_CK#			B_CK#		
3B	VREFBIAND	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AW2	DQ3B		B_A_7			B_CK_7		
3B	VREFBIAND	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	T13	DQS#3B		B_CK			B_CK		
3B	VREFBIAND	IO		FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn	DIFFIO_TX_B20p	DIFFOUT_B20p	AW3			B_A_6			B_CA_6		
3B	VREFBIAND	IO			DIFFIO_RX_B21n	DIFFOUT_B21n	AW4	DQ3B		B_A_5			B_CA_5		
3B	VREFBIAND	IO			DIFFIO_TX_B22n	DIFFOUT_B22n	AD12	DQ3B		B_A_5			B_CA_5		
3B	VREFBIAND	IO		FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTn,FPLL_BL_FB	DIFFIO_RX_B21p	DIFFOUT_B21p	AG5	DQ3B		B_A_2			B_CA_2		
3B	VREFBIAND	IO			DIFFIO_TX_B22p	DIFFOUT_B22p	AE12	DQ3B		B_A_4			B_CA_4		
3B	VREFBIAND	IO		CLK1n	DIFFIO_RX_B23n	DIFFOUT_B23n	W12			B_A_1					
3B	VREFBIAND	IO		CLK1p	DIFFIO_TX_B24n	DIFFOUT_B24n	AW6	DQ3B							
3B	VREFBIAND	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	V12			B_A_1					
3B	VREFBIAND	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AW6	DQ3B		B_A_0					
4A	VREFBIAND	IO	R2Z_0	DIFFIO_RX_B25n	DIFFOUT_B25n	AW7									
4A	VREFBIAND	IO		DIFFIO_TX_B26n	DIFFOUT_B26n	AF13	DQ4B			B_DD_0			B_DD_0		
4A	VREFBIAND	IO		DIFFIO_RX_B25p	DIFFOUT_B25p	AG8	DQ4B			B_DD_2			B_DD_2		
4A	VREFBIAND	IO		DIFFIO_TX_B26p	DIFFOUT_B26p	AG13	DQ4B			B_DD_1			B_DD_1		
4A	VREFBIAND	IO		DIFFIO_RX_B27n	DIFFOUT_B27n	U13	DQS#4B			B_DD_3			B_DD_3		
4A	VREFBIAND	IO		DIFFIO_TX_B28n	DIFFOUT_B28n	AW8	DQ4B			B_DD_3			B_DD_3		
4A	VREFBIAND	IO		DIFFIO_RX_B27p	DIFFOUT_B27p	U14	DQS#4B			B_DD_0			B_DD_0		
4A	VREFBIAND	IO		DIFFIO_TX_B28p	DIFFOUT_B28p	AG9	DQ4B			B_ODT_0			B_ODT_0		
4A	VREFBIAND	IO		DIFFIO_RX_B29n	DIFFOUT_B29n	AW9	DQ4B			B_ODT_1			B_ODT_1		
4A	VREFBIAND	IO		DIFFIO_TX_B30n	DIFFOUT_B30n	AE15	DQ4B			B_DD_4			B_DD_4		
4A	VREFBIAND	IO		DIFFIO_RX_B29p	DIFFOUT_B29p	AG10	DQ4B			B_DD_6			B_DD_6		
4A	VREFBIAND	IO		DIFFIO_TX_B30p	DIFFOUT_B30p	AF15	DQ4B			B_DD_5			B_DD_5		
4A	VREFBIAND	IO	CLK2n	DIFFIO_RX_B31n	DIFFOUT_B31n	AA13									
4A	VREFBIAND	IO		DIFFIO_TX_B32n	DIFFOUT_B32n	AA11	DQ4B			B_DD_7			B_DD_7		
4A	VREFBIAND	IO	CLK2p	DIFFIO_RX_B31p	DIFFOUT_B31p	V13				B_DM_0			B_DM_0		
4A	VREFBIAND	IO		DIFFIO_TX_B32p	DIFFOUT_B32p	AG11	DQ4B			B_DM_8			B_DM_8		
4A	VREFBIAND	IO		DIFFIO_RX_B34n	DIFFOUT_B34n	AG16	DQ5B	DQ1B		B_DD_8			B_DD_8		
4A	VREFBIAND	IO		DIFFIO_TX_B33n	DIFFOUT_B33n	AA12	DQ5B	DQ1B		B_DD_10			B_DD_10		
4A	VREFBIAND	IO		DIFFIO_RX_B34p	DIFFOUT_B34p	AF17	DQ5B	DQ1B		B_DD_9			B_DD_9		
4A	VREFBIAND	IO		DIFFIO_TX_B35n	DIFFOUT_B35n	V13	DQS#5B	DQ1B		B_DQS#_1			B_DQS#_1		
4A	VREFBIAND	IO		DIFFIO_RX_B35p	DIFFOUT_B35p	AA18	DQS#5B	DQ1B		B_DQS#_2			B_DQS#_2		
4A	VREFBIAND	IO		DIFFIO_TX_B36n	DIFFOUT_B36n	AA13	DQ5B	DQ1B		B_DD_11			B_DD_11		
4A	VREFBIAND	IO		DIFFIO_RX_B36p	DIFFOUT_B36p	W14	DQS#5B	DQ1B		B_DQS_1			B_DQS_1		
4A	VREFBIAND	IO		DIFFIO_TX_B37n	DIFFOUT_B37n	AA14	DQ5B	DQ1B		B_CKE_0			B_CKE_0		
4A	VREFBIAND	IO		DIFFIO_RX_B37p	DIFFOUT_B37p	AG15	DQ5B	DQ1B		B_DD_14			B_DD_14		
4A	VREFBIAND	IO		DIFFIO_TX_B38n	DIFFOUT_B38n	AD17	DQ5B	DQ1B		B_DD_13			B_DD_13		
4A	VREFBIAND	IO	CLK3n	DIFFIO_RX_B38p	DIFFOUT_B38p	AA15									
4A	VREFBIAND	IO		DIFFIO_TX_B40n	DIFFOUT_B40n	AW16	DQ5B	DQ1B		B_DD_15			B_DD_15		
4A	VREFBIAND	IO	CLK3p	DIFFIO_RX_B39p	DIFFOUT_B39p	V15									
4A	VREFBIAND	IO		DIFFIO_TX_B40p	DIFFOUT_B40p	AW17	DQ5B	DQ1B		B_DM_1			B_DM_1		
4A	VREFBIAND	IO		DIFFIO_RX_B42n	DIFFOUT_B42n	AD19	DQ6B	DQ1B		B_DD_16			B_DD_16		
4A	VREFBIAND	IO		DIFFIO_TX_B41n	DIFFOUT_B41n	AF18	DQ6B	DQ1B		B_DD_18			B_DD_18		
4A	VREFBIAND	IO		DIFFIO_RX_B42p	DIFFOUT_B42p	AE19	DQ6B	DQ1B		B_DD_17			B_DD_17		
4A	VREFBIAND	IO		DIFFIO_TX_B43n	DIFFOUT_B43n	AA18	DQS#6B	DQS#1B		B_DQS#_2			B_DQS#_2		
4A	VREFBIAND	IO		DIFFIO_RX_B43p	DIFFOUT_B43p	AA18	DQS#6B	DQ1B		B_DD_19			B_DD_19		
4A	VREFBIAND	IO		DIFFIO_TX_B44n	DIFFOUT_B44n	AA19	DQS#6B	DQ1B		B_DQS_2			B_DQS_2		
4A	VREFBIAND	IO		DIFFIO_RX_B44p	DIFFOUT_B44p	AG18	DQ6B	DQ1B		B_RESET#			B_RESET#		
4A	VREFBIAND	IO		DIFFIO_TX_B45n	DIFFOUT_B45n	AA19	DQ6B	DQ1B		GND			GND		
4A	VREFBIAND	IO		DIFFIO_RX_B45p	DIFFOUT_B45p	AD20	DQ6B	DQ1B		B_DD_20			B_DD_20		
4A	VREFBIAND	IO		DIFFIO_TX_B46n	DIFFOUT_B46n	AG19	DQ6B	DQ1B</							



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	UEF2	DQS for X8	DQS for X16	HMC Pin Assignment for DQS1/DQS2 (3)	HMC Pin Assignment for LPDQS1	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
5A	VREFBIAND	ID		DEFIO TX_R0d	DEFIO_TX_R0d	DEFOUT_R0d	AF27	DQ0B	DQ0B	B_DM_4					
5A	VREFBIAND	ID	RZQ_1	DEFIO TX_R1p	DEFIO_TX_R1p	DEFOUT_R1p	AF26	DQ1R							
5A	VREFBIAND	ID		INT_DONE	DEFIO_RX_R3p	DEFOUT_R3p	AA20								
5A	VREFBIAND	ID		PS_REQUEST	DEFIO_TX_R1m	DEFOUT_R1m	AE26	DQ1R							
5A	VREFBIAND	ID		CRC_ERROR	DEFIO_RX_R2m	DEFOUT_R2m	119								
5A	VREFBIAND	ID		ICED	DEFIO_TX_R3p	DEFOUT_R3p	AE25	DQ1R							
5A	VREFBIAND	ID		CpF_CONFIGONE	DEFIO_RX_R4p	DEFOUT_R4p	117	DQ1R							
5A	VREFBIAND	ID			DEFIO_TX_R3m	DEFOUT_R3m	AD26	DQ1R							
5A	VREFBIAND	ID		DEV_OE	DEFIO_RX_R4m	DEFOUT_R4m	118	DQ1R							
5A	VREFBIAND	ID			DEFIO_TX_R5p	DEFOUT_R5p	AC24								
5A	VREFBIAND	ID		DEV_CLRn	DEFIO_RX_R6p	DEFOUT_R6p	116	DQS1R							
5A	VREFBIAND	ID			DEFIO_TX_R5m	DEFOUT_R5m	AA23	DQ1R							
5A	VREFBIAND	ID			DEFIO_RX_R6m	DEFOUT_R6m	W15	DQS1R							
5A	VREFBIAND	ID			DEFIO_TX_R7p	DEFOUT_R7p	AA24	DQ1R							
5A	VREFBIAND	ID			DEFIO_RX_R8p	DEFOUT_R8p	116	DQ1R							
5A	VREFBIAND	ID			DEFIO_TX_R7m	DEFOUT_R7m	AA23								
5A	VREFBIAND	ID			DEFIO_RX_R8m	DEFOUT_R8m	115	DQ1R							
0B	VREFBIAND_HPS	HPS_DDR					AE28			HPS_DM_4		HPS_DM_4			
0B	VREFBIAND_HPS	HPS_DDR					AD28			HPS_DO_39		HPS_DO_39			
0B	VREFBIAND_HPS	HPS_DDR					120			HPS_DO_37		HPS_DO_37			
0B	VREFBIAND_HPS	HPS_DDR					AE37			HPS_DO_38		HPS_DO_38			
0B	VREFBIAND_HPS	HPS_DDR					119			HPS_DO_36		HPS_DO_36			
0B	VREFBIAND_HPS	HPS_DDR					118			HPS_DQS_4		HPS_DQS_4			
0B	VREFBIAND_HPS	HPS_DQS1					124								
0B	VREFBIAND_HPS	HPS_DDR					117			HPS_DQS1_4		HPS_DQS1_4			
0B	VREFBIAND_HPS	HPS_DDR					125			HPS_DO_35		HPS_DO_35			
0B	VREFBIAND_HPS	HPS_DDR					126			HPS_DO_33		HPS_DO_33			
0B	VREFBIAND_HPS	HPS_DDR					AC28			HPS_DO_34		HPS_DO_34			
0B	VREFBIAND_HPS	HPS_DDR					126			HPS_DO_32		HPS_DO_32			
0B	VREFBIAND_HPS	HPS_GPI2					AC27								
0B	VREFBIAND_HPS	HPS_GPI1					116								
0B	VREFBIAND_HPS	HPS_DDR					AB28			HPS_DM_3		HPS_DM_3			
0B	VREFBIAND_HPS	HPS_GPI0					115								
0B	VREFBIAND_HPS	HPS_DDR					AA27			HPS_DO_31		HPS_DO_31			
0B	VREFBIAND_HPS	HPS_DDR					124			HPS_DO_29		HPS_DO_29			
0B	VREFBIAND_HPS	HPS_DDR					127			HPS_DO_30		HPS_DO_30			
0B	VREFBIAND_HPS	HPS_DDR					824			HPS_DO_28		HPS_DO_28			
0B	VREFBIAND_HPS	VREFBIAND_HPS					127								
0B	VREFBIAND_HPS	HPS_DDR					119			HPS_DQS_3		HPS_DQS_3			
0B	VREFBIAND_HPS	HPS_GPI0					126								
0B	VREFBIAND_HPS	HPS_DDR					120			HPS_DQS1_3		HPS_DQS1_3			
0B	VREFBIAND_HPS	HPS_DDR					105			HPS_DO_27		HPS_DO_27			
0B	VREFBIAND_HPS	HPS_DDR					826			HPS_DO_25		HPS_DO_25			
0B	VREFBIAND_HPS	HPS_DDR					AA28			HPS_DO_26		HPS_DO_26			
0B	VREFBIAND_HPS	HPS_DDR					826			HPS_DO_24		HPS_DO_24			
0B	VREFBIAND_HPS	HPS_GPI8					128								
0B	VREFBIAND_HPS	HPS_GPI7					116								
0B	VREFBIAND_HPS	HPS_DDR					123			HPS_DM_2		HPS_DM_2			
0B	VREFBIAND_HPS	HPS_GPI6					117								
0B	VREFBIAND_HPS	HPS_DDR					127			HPS_DO_23		HPS_DO_23			
0B	VREFBIAND_HPS	HPS_DDR					127			HPS_DO_21		HPS_DO_21			
0B	VREFBIAND_HPS	HPS_DDR					827			HPS_DO_22		HPS_DO_22			
0B	VREFBIAND_HPS	HPS_DDR					126			HPS_DO_20		HPS_DO_20			
0B	VREFBIAND_HPS	HPS_GPI5					126								
0B	VREFBIAND_HPS	HPS_DDR					119			HPS_DQS_2		HPS_DQS_2			
0B	VREFBIAND_HPS	HPS_DDR					128			HPS_RESE19		HPS_RESE19			
0B	VREFBIAND_HPS	HPS_DDR					118			HPS_DQS1_2		HPS_DQS1_2			
0B	VREFBIAND_HPS	HPS_DDR					128			HPS_DO_19		HPS_DO_19			
0B	VREFBIAND_HPS	HPS_DDR					126			HPS_DO_17		HPS_DO_17			
0B	VREFBIAND_HPS	HPS_DDR					128			HPS_DO_18		HPS_DO_18			
0B	VREFBIAND_HPS	HPS_DDR					124			HPS_DO_16		HPS_DO_16			
0B	VREFBIAND_HPS	HPS_GPI4					828								
0B	VREFBIAND_HPS	HPS_GPI3					829								
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_DM_1		HPS_DM_1			
0B	VREFBIAND_HPS	HPS_GPI2					828								
0B	VREFBIAND_HPS	HPS_DDR					120			HPS_DO_15		HPS_DO_15			
0B	VREFBIAND_HPS	HPS_DDR					120			HPS_DO_13		HPS_DO_13			
0B	VREFBIAND_HPS	HPS_DDR					120			HPS_DO_14		HPS_DO_14			
0B	VREFBIAND_HPS	HPS_DDR					827			HPS_DO_12		HPS_DO_12			
0B	VREFBIAND_HPS	HPS_DDR					128			HPS_CKE_0		HPS_CKE_0			
0B	VREFBIAND_HPS	HPS_DDR					819			HPS_DQS_1		HPS_DQS_1			
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_CKE_1		HPS_CKE_1			
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_CKE_1		HPS_CKE_1			
0B	VREFBIAND_HPS	HPS_DDR					118			HPS_DQS1_1		HPS_DQS1_1			
0B	VREFBIAND_HPS	HPS_DDR					118			HPS_DO_11		HPS_DO_11			
0B	VREFBIAND_HPS	HPS_DDR					125			HPS_DO_9		HPS_DO_9			
0B	VREFBIAND_HPS	HPS_DDR					827			HPS_DO_10		HPS_DO_10			
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_DO_8		HPS_DO_8			
0B	VREFBIAND_HPS	HPS_GPI1					827								
0B	VREFBIAND_HPS	HPS_GPI0					828								
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_DM_0		HPS_DM_0			
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_DO_7		HPS_DO_7			
0B	VREFBIAND_HPS	HPS_DDR					826			HPS_DO_6		HPS_DO_6			
0B	VREFBIAND_HPS	HPS_DDR					827			HPS_DO_5		HPS_DO_5			
0B	VREFBIAND_HPS	HPS_DDR					826			HPS_DO_4		HPS_DO_4			
0B	VREFBIAND_HPS	HPS_DDR					817			HPS_ODT_0		HPS_ODT_0			
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_ODT_0		HPS_ODT_0			
0B	VREFBIAND_HPS	HPS_DDR					816			HPS_DQS1_0		HPS_DQS1_0			
0B	VREFBIAND_HPS	HPS_DDR					827			HPS_DO_3		HPS_DO_3			
0B	VREFBIAND_HPS	HPS_DDR					824			HPS_DO_1		HPS_DO_1			
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_DO_2		HPS_DO_2			
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_DO_0		HPS_DO_0			
0B	VREFBIAND_HPS	VREFBIAND_HPS					808								
0B	VREFBIAND_HPS	HPS_DDR					828			HPS_A_0		HPS_A_0			
0B	VREFBIAND_HPS	HPS_DDR					808			HPS_A_1		HPS_A_1			
0B	VREFBIAND_HPS	HPS_DDR					801			HPS_A_4		HPS_A_4			
0B	VREFBIAND_HPS	HPS_DDR					826			HPS_A_2		HPS_A_2			
0B	VREFBIAND_HPS	HPS_DDR					820			HPS_A_6		HPS_A_6			
0B	VREFBIAND_HPS	HPS_DDR					806			HPS_A_3		HPS_A_3			
0B	VREFBIAND_HPS	HPS_DDR					821			HPS_CK		HPS_CK			
0B	VREFBIAND_HPS	HPS_DDR					826			HPS_CK_6		HPS_CK_6			
0B	VREFBIAND_HPS	HPS_DDR					820			HPS_CK_4		HPS_CK_4			
0B	VREFBIAND_HPS	HPS_DDR					826			HPS_A_7		HPS_A_7			
0B	VREFBIAND_HPS	HPS_DDR					825			HPS_BA_1		HPS_BA_1			
0B	VREFBIAND_HPS	HPS_DDR					827			HPS_BA_0		HPS_BA_0			
0B	VREFBIAND_HPS	HPS_DDR					825			HPS_BA_2		HPS_BA_2			
0B	VREFBIAND_HPS	HPS_DDR					826			HPS_CAS		HPS_CAS			
0B	VREFBIAND_HPS	HPS_DDR					825			HPS_RAS		HPS_RAS			
0B	VREFBIAND_HPS	HPS_DDR					826			HPS_A_8		HPS_A_8			
0B	VREFBIAND_HPS	HPS_DDR					824			HPS_A_10		HPS_A_10			
0B	VREFBIAND_HPS	HPS_DDR					825			HPS_A_9		HPS_A_9			
0B	VREFBIAND_HPS	HPS_DDR					824			HPS_A_11		HPS_A_11			
0B	VREFBIAND_HPS	HPS_DDR					821			HPS_CSB_0		HPS_CSB_0			
0B	VREFBIAND_HPS	HPS_DDR					824			HPS_A_12		HPS_A_12			
0B	VREFBIAND_HPS	HPS_DDR					820			HPS_CSB_1		HPS_CSB_1			
0B	VREFBIAND_HPS	HPS_DDR					824			HPS_A_13		HPS_A_13			
0B	VREFBIAND_HPS	HPS_DDR					823			HPS_A_14		HPS_A_14			
0B	VREFBIAND_HPS	HPS_DDR					825			HPS_VREF		HPS_VREF			
0B	VREFBIAND_HPS	HPS_DDR					824			HPS_A_15		HPS_A_15			
0B	VREFBIAND_HPS	HPS_RZQ_0					825								
0A	GND						823								
0A	GND						823								
0A	GND						823								
0A	HPS_HRST						823								
0A	HPS_HPOW						819								
0A	HPS_TDO						823								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U02	DQS for X8	DQS for X16	HMC Pin Assignment for DQS/ADDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AC1								
		GND					AC2								
		GND					AC3								
		GND					AD14								
		GND					AD22								
		GND					AD25								
		GND					AD3								
		GND					AD6								
		GND					AD8								
		GND					AE1								
		GND					AE16								
		GND					AE18								
		GND					AE2								
		GND					AE3								
		GND					AF34								
		GND					AF3								
		GND					AG1								
		GND					AG17								
		GND					AG2								
		GND					AG27								
		GND					AG3								
		GND					AG7								
		GND					AH10								
		GND					AH8								
		GND					B15								
		GND					B17								
		GND					B20								
		GND					B22								
		GND					B25								
		GND					B27								
		GND					B3								
		GND					B5								
		GND					BF								
		GND					C1								
		GND					C11								
		GND					C2								
		GND					C3								
		GND					D10								
		GND					D13								
		GND					D16								
		GND					D3								
		GND					E1								
		GND					E19								
		GND					E2								
		GND					E22								
		GND					E24								
		GND					E27								
		GND					E3								
		GND					E9								
		GND					F3								
		GND					G1								
		GND					G2								
		GND					G3								
		GND					H11								
		GND					H15								
		GND					H18								
		GND					H30								
		GND					H24								
		GND					H27								
		GND					I5								
		GND					I3								
		GND					I26								
		GND					I29								
		GND					J1								
		GND					J2								
		GND					J3								
		GND					J5								
		GND					J8								
		GND					K11								
		GND					K12								
		GND					K14								
		GND					K16								
		GND					K20								
		GND					K3								
		GND					K5								
		GND					K6								
		GND					Y14								
		GND					L1								
		GND					L12								
		GND					L13								
		GND					L4								
		GND					L17								
		GND					L19								
		GND					L2								
		GND					L24								
		GND					L27								
		GND					L3								
		GND					L5								
		GND					W4								
		GND					M3								
		GND					M10								
		GND					M11								
		GND					M14								
		GND					M16								
		GND					M20								
		GND					M3								
		GND					M8								
		GND					N1								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N2								
		GND					N3								
		GND					N4								
		GND					P10								
		GND					P12								
		GND					P16								
		GND					P18								
		GND					P20								
		GND					P25								
		GND					P3								
		GND					P5								
		GND					P9								
		GND					R1								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R5								
		GND					R6								
		GND					R8								
		GND					T10								
		GND					T14								
		GND					T3								
		GND					U1								
		GND					U12								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					I17								
		GND					I2								
		GND					U20								
		GND					U24								
		GND					U27								
		GND					U8								
		GND					U9								
		GND					V14								
		GND					V3								
		GND					V8								
		GND					V9								
		GND					W1								
		GND					W16								
		GND					W18								
		GND					W2								
		GND					W25								
		GND					W24								
		GND					V25								
		GND					W26								
		GND					W20								
		GND					W28								
		GND					W21								
		GND					V28								
		GND					K21								
		GCC					J11								
		GCC					K13								
		GCC					K16								
		GCC					L11								
		GCC					L12								
		GCC					L14								
		GCC					M12								
		GCC					M13								
		GCC					M16								
		GCC					N9								
		GCC					N10								
		GCC					N11								
		GCC					N12								
		GCC					N14								
		GCC					N8								
		GCC					P11								
		GCC					P13								
		GCC					P14								
		GCC					P16								
		GCC					R10								
		GCC					R12								
		GCC					R14								
		GCC					R9								
		GCC					T13								
		GCC					T9								
		GCC					L4								
		GCC					T4								
		GCC					M5								
		GCC					N5								
		GCC					R5								
		GCC					T5								
		GCC					U26								
		DNU					A2								
		DNU					B2								
		DNU					D1								
		DNU					D2								
		DNU					H1								
		DNU					H2								
		DNU					M1								
		DNU					M2								
		DNU					T1								
		DNU					T2								
		DNU					Y1								
		DNU					Y2								
		DNU					AD1								
		DNU					AD2								
		DNU					CD3								
		DNU					E12								
		DNU					U8								
		DNU					AE14								
		DNU					Y10								
		VCCP5M					AD24								
		VCCP5M					H10								
		VCCP5M					D7								
		VCCBAT					AA5								
		VCCIO3A					H5								
		VCCIO3A					AA12								
		VCCIO3B					AE10								
		VCCIO3B					AE13								
		VCCIO3B					AG4								
		VCCIO4A					AA16								
		VCCIO4A					AE1								
		VCCIO4A					AF14								
		VCCIO4A					AF19								
		VCCIO4A					AG13								
		VCCIO4A					AG22								
		VCCIO4A					AH15								
		VCCIO4A					AK25								
		VCCIO4A					W13								
		VCCIO5A					AC25								
		VCCIO5A					W17								
		VCCIO6A_HPS					C26								
		VCCIO6A_HPS					C27								
		VCCIO6A_HPS					F27								
		VCCIO6A_HPS					EA4								
		VCCIO6A_HPS					H21								
		VCCIO6A_HPS					H26								
		VCCIO6A_HPS					L26								
		VCCIO6A_HPS					M21								
		VCCIO6B_HPS					AD27								
		VCCIO6B_HPS					P27								
		VCCIO6B_HPS					T21								
		VCCIO6B_HPS					T26								
		VCCIO6B_HPS					U18								
		VCCIO6B_HPS					W27								
		VCCIO7A_HPS					CD3								
		VCCIO7A_HPS					D18								
		VCCIO7B_HPS					B13								
		VCCIO7B_HPS					H14								
		VCCIO7C_HPS					B10								
		VCCIO7D_HPS					D6								
		VCCIO7D_HPS					G8								
		VCCIO8A					E7								
		VCCPD3A					AD10								
		VCCPD3A					AA14								
		VCCPD3BA					AD13								
		VCCPD3BA					AD16								
		VCCPD3BA					AD18								
		VCCPD3BA					AD21								
		VCCPD3BA					AD8								
		VCCPD5A					V21								



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U072	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPD6MB_HPS					K21								
		VCCPD6MB_HPS					K24								
		VCCPD6MB_HPS					U04								
		VCCPD6MB_HPS					P21								
		VCCPD6MB_HPS					P24								
		VCCPD7A_HPS					E21								
		VCCPD7B_HPS					E17								
		VCCPD7C_HPS					E14								
		VCCPD7D_HPS					E18								
		VCCPD8A					E16								
3A	VREFB3AND	VREFB3AND					A65								
3B	VREFB3BND	VREFB3BND					AF12								
4A	VREFB4AND	VREFB4AND					AF16								
5A	VREFB5AND	VREFB5AND					AC26								
		VREFB7A/B/C/D/E/HPS					D19								
8A	VREFB8AND	VREFB8AND					D6								
		NC					W25								
		NC					AK25								
		NC					W35								
		NC					W39								
		VCCRSTCLK_HPS					F29								
		RREF_TL					B1								
		VCCA_FPLL					W5								
		VCCA_FPLL					P4								
		VCCA_FPLL					Q4								
		VCCA_FPLL					W5								
		VCCA_FPLL					J4								
		VCCA_FPLL					AK21								
		VCCA_FPLL					M4								
		VCCA_FPLL					R4								
		VCC_AUX					AK24								
		VCC_AUX					AC8								
		VCC_AUX					AD15								
		VCC_AUX					E15								
		VCC_AUX					F8								
		VCC_AUX_SHARED					F21								
		VCCRLL_HPS					H23								
		VCC_HPS					U21								
		VCC_HPS					K17								
		VCC_HPS					L16								
		VCC_HPS					L18								
		VCC_HPS					M17								
		VCC_HPS					M15								
		VCC_HPS					M19								
		VCC_HPS					N16								
		VCC_HPS					N15								
		VCC_HPS					P17								
		VCC_HPS					P19								

Notes:
 (1) For more information about pin definitions and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
 (2) HPS DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
 (3) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CSEMA4 Device
Version 1.2

Version Number	Date	Changes Made
1.0	7/8/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.