Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
3A		TDO		TDO			Y9								
3A		nCSO		DATA4			AA6								
3A		TMS		TMS			AC7								
3A		AS_DATA3		DATA3			AB6								
3A		TCK		TCK			AB5								
3A		AS_DATA2		DATA2			AC5								
3A		TDI		TDI			W10								
3A		AS_DATA1		DATA1			AC6								
3A		DCLK		DCLK			AA8								
3A		AS_DATA0,ASDO		DATA0			AD7								
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	Y8	DQ1B							
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	Y4								
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	W8	DQ1B							
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	Y5	DQ1B							
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	T8	DQSn1B							
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB4	DQ1B							
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	U9	DQS1B							
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA4								
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	V10	DQ1B							
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AD4	DQ1B							
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	U10	DQ1B							
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AC4	DQ1B							
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AA11								
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AE6	DQ1B							
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	Y11								
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AD5	DQ1B							
3B	VREFB3BN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	AF4			GND	GND				
3B	VREFB3BN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	AE9	DQ2B		B_A_15					
3B	VREFB3BN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	AE4	DQ2B		B_WE#					
3B	VREFB3BN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	AD10	DQ2B		B_A_14					
3B	VREFB3BN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	U11	DQSn2B		B_CS#_1	B_CS#_1				
3B	VREFB3BN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AF8	DQ2B		B_A_13					
3B	VREFB3BN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	T11	DQS2B		B_CS#_0	B_CS#_0				
3B	VREFB3BN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AE7			B_A_12					
3B	VREFB3BN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AF9	DQ2B		B_A_11					
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AE11	DQ2B		B_A_9	B_CA_9				
3B	VREFB3BN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AE8	DQ2B		B_A_10					
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	AD11	DQ2B		B_A_8	B_CA_8				
3B	VREFB3BN0	IO		CLK0n,FPLL_BL_FBn	DIFFIO_RX_B15n	DIFFOUT_B15n	W11								
3B	VREFB3BN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AF6	DQ2B		B_RAS#					
3B	VREFB3BN0	IO		CLK0p,FPLL_BL_FBp	DIFFIO_RX_B15p	DIFFOUT_B15p	V11								
3B	VREFB3BN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AF5	DQ2B		B_CAS#					
3B	VREFB3BN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	AG6			GND	GND				
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AF10	DQ3B		B_BA_2					
3B	VREFB3BN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AF7	DQ3B		B_BA_0					
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AF11	DQ3B		B_BA_1					
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	T12	DQSn3B		B_CK#	B_CK#				
3B	VREFB3BN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AH2	DQ3B		B_A_7	B_CA_7				
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	T13	DQS3B		B_CK	B_CK				
3B	VREFB3BN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AH3			B_A_6	B_CA_6				
3B	VREFB3BN0	IO		FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn	DIFFIO_TX_B21n	DIFFOUT_B21n	AH4	DQ3B		B_A_3	B_CA_3				
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	AD12	DQ3B		B_A_5	B_CA_5				
3B	VREFB3BN0	IO		FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB	DIFFIO_TX_B21p	DIFFOUT_B21p	AG5	DQ3B		B_A_2	B_CA_2				
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	AE12	DQ3B		B_A_4	B_CA_4				
3B	VREFB3BN0	IO		CLK1n	DIFFIO_RX_B23n	DIFFOUT_B23n	W12								
3B	VREFB3BN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AH5	DQ3B		B_A_1	B_CA_1				
3B	VREFB3BN0	IO		CLK1p	DIFFIO_RX_B23p	DIFFOUT_B23p	V12								
3B	VREFB3BN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AH6	DQ3B		B_A_0	B_CA_0				
4A	VREFB4AN0	IO		RZQ_0	DIFFIO_TX_B25n	DIFFOUT_B25n	AH7								
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AF13	DQ4B		B_DQ_0	B_DQ_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AG8	DQ4B		B_DQ_2	B_DQ_2				
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AG13	DQ4B		B_DQ_1	B_DQ_1				
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	U13	DQSn4B		B_DQS#_0	B_DQS#_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AH8	DQ4B		B_DQ_3	B_DQ_3				
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	U14	DQS4B		B_DQS_0	B_DQS_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AG9			B_ODT_0	B_ODT_0				
4A	VREFB4AN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AH9	DQ4B		B_ODT_1	B_ODT_1				
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AE15	DQ4B		B_DQ_4	B_DQ_4				
4A	VREFB4AN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AG10	DQ4B		B_DQ_6	B_DQ_6				
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AF15	DQ4B		B_DQ_5	B_DQ_5				
4A	VREFB4AN0	IO		CLK2n	DIFFIO_RX_B31n	DIFFOUT_B31n	AA13								
4A	VREFB4AN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AH11	DQ4B		B_DQ_7	B_DQ_7				
4A	VREFB4AN0	IO		CLK2p	DIFFIO_RX_B31p	DIFFOUT_B31p	Y13								
4A	VREFB4AN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AG11	DQ4B		B_DM_0	B_DM_0				
4A	VREFB4AN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AG16	DQ5B	DQ1B	B_DQ_8	B_DQ_8				
4A	VREFB4AN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AH12	DQ5B	DQ1B	B_DQ_10	B_DQ_10				
4A	VREFB4AN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AF17	DQ5B	DQ1B	B_DQ_9	B_DQ_9				
4A	VREFB4AN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	V13	DQSn5B	DQ1B	B_DQS#_1	B_DQS#_1				
4A	VREFB4AN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AH13	DQ5B	DQ1B	B_DQ_11	B_DQ_11				
4A	VREFB4AN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	W14	DQS5B	DQ1B	B_DQS_1	B_DQS_1				
4A	VREFB4AN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AG14			B_CKE_1	B_CKE_1				
4A	VREFB4AN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AH14	DQ5B	DQ1B	B_CKE_0	B_CKE_0				
4A	VREFB4AN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AE17	DQ5B	DQ1B	B_DQ_12	B_DQ_12				
4A	VREFB4AN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AG15	DQ5B	DQ1B	B_DQ_14	B_DQ_14				
4A	VREFB4AN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AD17	DQ5B	DQ1B	B_DQ_13	B_DQ_13				
4A	VREFB4AN0	IO		CLK3n	DIFFIO_RX_B39n	DIFFOUT_B39n	AA15								
4A	VREFB4AN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AH16	DQ5B	DQ1B	B_DQ_15	B_DQ_15				
4A	VREFB4AN0	IO		CLK3p	DIFFIO_RX_B39p	DIFFOUT_B39p	Y15								
4A	VREFB4AN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AH17	DQ5B	DQ1B	B_DM_1	B_DM_1				
4A	VREFB4AN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AD19	DQ6B	DQ1B	B_DQ_16	B_DQ_16				
4A	VREFB4AN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AF18	DQ6B	DQ1B	B_DQ_18	B_DQ_18				
4A	VREFB4AN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AE19	DQ6B	DQ1B	B_DQ_17	B_DQ_17				
4A	VREFB4AN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AA18	DQSn6B	DQS1B	B_DQS#_2	B_DQS#_2				
4A	VREFB4AN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AH18	DQ6B	DQ1B	B_DQ_19	B_DQ_19				
4A	VREFB4AN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	AA19	DQS6B	DQS1B	B_DQS_2	B_DQS_2				
4A	VREFB4AN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AG18			B_RESET#	B_RESET#				
4A	VREFB4AN0	IO			DIFFIO_TX_B45n	DIFFOUT_B45n	AH19	DQ6B	DQ1B	GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AD20	DQ6B	DQ1B	B_DQ_20	B_DQ_20				
4A	VREFB4AN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AG19	DQ6B	DQ1B	B_DQ_22	B_DQ_22				
4A	VREFB4AN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AE20	DQ6B	DQ1B	B_DQ_21	B_DQ_21				
4A	VREFB4AN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AG20	DQ6B	DQ1B	B_DQ_23	B_DQ_23				
4A	VREFB4AN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AF20	DQ6B	DQ1B	B_DM_2	B_DM_2				
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AF21	DQ7B	DQ2B	B_DQ_24	B_DQ_24				
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AG21	DQ7B	DQ2B	B_DQ_26	B_DQ_26				
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AF22	DQ7B	DQ2B	B_DQ_25	B_DQ_25				
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	AE22	DQSn7B	DQ2B	B_DQS#_3	B_DQS#_3				
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AH21	DQ7B	DQ2B	B_DQ_27	B_DQ_27				
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	AD23	DQS7B	DQ2B	B_DQS_3	B_DQS_3				
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AH22	DQ7B	DQ2B	GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AF23	DQ7B	DQ2B	B_DQ_28	B_DQ_28				
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AH23	DQ7B	DQ2B	B_DQ_30	B_DQ_30				
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AG23	DQ7B	DQ2B	B_DQ_29	B_DQ_29				
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AH24	DQ7B	DQ2B	B_DQ_31	B_DQ_31				
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AG24	DQ7B	DQ2B	B_DM_3	B_DM_3				
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AE23	DQ8B	DQ2B	B_DQ_32	B_DQ_32				
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AG26	DQ8B	DQ2B	B_DQ_34	B_DQ_34				
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AE24	DQ8B	DQ2B	B_DQ_33	B_DQ_33				
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AC23	DQSn8B	DQSn2B	B_DQS#_4	B_DQS#_4				
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AH26	DQ8B	DQ2B	B_DQ_35	B_DQ_35				
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AC22	DQS8B	DQS2B	B_DQS_4	B_DQS_4				
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AH27	DQ8B	DQ2B	GND	GND				
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AG25	DQ8B	DQ2B	B_DQ_36	B_DQ_36				
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AG28	DQ8B	DQ2B	B_DQ_38	B_DQ_38				
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AF25	DQ8B	DQ2B	B_DQ_37	B_DQ_37				
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AF28	DQ8B	DQ2B	B_DQ_39	B_DQ_39				

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AF27	DQ8B	DQ2B	B_DM 4	B_DM 4				
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AF26	DQ1R							
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	AA20								
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AE26	DQ1R							
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	Y19								
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AE25	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	Y17	DQ1R							
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AD26	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	Y18	DQ1R							
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AC24								
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	Y16	DQS1R							
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AB23	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R6n	W15	DQSn1R							
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	AA24	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	V16	DQ1R							
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	AA23								
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	V15	DQ1R							
6B	VREFB6BN0_HPS	HPS_DDR					AE28			HPS_DM 4	HPS_DM 4				
6B	VREFB6BN0_HPS	HPS_DDR					AD28			HPS_DQ 39	HPS_DQ 39				
6B	VREFB6BN0_HPS	HPS_DDR					V20			HPS_DQ 37	HPS_DQ 37				
6B	VREFB6BN0_HPS	HPS_DDR					AE27			HPS_DQ 38	HPS_DQ 38				
6B	VREFB6BN0_HPS	HPS_DDR					V19			HPS_DQ 36	HPS_DQ 36				
6B	VREFB6BN0_HPS	HPS_DDR					V18			HPS_DQS 4	HPS_DQS 4				
6B	VREFB6BN0_HPS	HPS_GPI13					V24								
6B	VREFB6BN0_HPS	HPS_DDR					V17			HPS_DQS# 4	HPS_DQS# 4				
6B	VREFB6BN0_HPS	HPS_DDR					V25			HPS_DQ 35	HPS_DQ 35				
6B	VREFB6BN0_HPS	HPS_DDR					U25			HPS_DQ 33	HPS_DQ 33				
6B	VREFB6BN0_HPS	HPS_DDR					AC28			HPS_DQ 34	HPS_DQ 34				
6B	VREFB6BN0_HPS	HPS_DDR					T26			HPS_DQ 32	HPS_DQ 32				
6B	VREFB6BN0_HPS	HPS_GPI12					AC27								
6B	VREFB6BN0_HPS	HPS_GPI11					U16								
6B	VREFB6BN0_HPS	HPS_DDR					AB28			HPS_DM 3	HPS_DM 3				
6B	VREFB6BN0_HPS	HPS_GPI10					U15								
6B	VREFB6BN0_HPS	HPS_DDR					AA27			HPS_DQ 31	HPS_DQ 31				
6B	VREFB6BN0_HPS	HPS_DDR					T24			HPS_DQ 29	HPS_DQ 29				
6B	VREFB6BN0_HPS	HPS_DDR					Y27			HPS_DQ 30	HPS_DQ 30				
6B	VREFB6BN0_HPS	HPS_DDR					R24			HPS_DQ 28	HPS_DQ 28				
6B	VREFB6BN0_HPS	VREFB6BN0_HPS					T27								
6B	VREFB6BN0_HPS	HPS_DDR					U19			HPS_DQS 3	HPS_DQS 3				
6B	VREFB6BN0_HPS	HPS_GPI9					Y26								
6B	VREFB6BN0_HPS	HPS_DDR					T20			HPS_DQS# 3	HPS_DQS# 3				
6B	VREFB6BN0_HPS	HPS_DDR					W26			HPS_DQ 27	HPS_DQ 27				
6B	VREFB6BN0_HPS	HPS_DDR					R25			HPS_DQ 25	HPS_DQ 25				
6B	VREFB6BN0_HPS	HPS_DDR					AA28			HPS_DQ 26	HPS_DQ 26				
6B	VREFB6BN0_HPS	HPS_DDR					R26			HPS_DQ 24	HPS_DQ 24				
6B	VREFB6BN0_HPS	HPS_GPI8					Y28								
6B	VREFB6BN0_HPS	HPS_GPI7					T16								
6B	VREFB6BN0_HPS	HPS_DDR					W28			HPS_DM 2	HPS_DM 2				
6B	VREFB6BN0_HPS	HPS_GPI6					T17								
6B	VREFB6BN0_HPS	HPS_DDR					V27			HPS_DQ 23	HPS_DQ 23				
6B	VREFB6BN0_HPS	HPS_DDR					N27			HPS_DQ 21	HPS_DQ 21				
6B	VREFB6BN0_HPS	HPS_DDR					R27			HPS_DQ 22	HPS_DQ 22				
6B	VREFB6BN0_HPS	HPS_DDR					N26			HPS_DQ 20	HPS_DQ 20				
6B	VREFB6BN0_HPS	HPS_GPI5					P26								
6B	VREFB6BN0_HPS	HPS_DDR					T19			HPS_DQS 2	HPS_DQS 2				
6B	VREFB6BN0_HPS	HPS_DDR					V28			HPS_RESET#	HPS_RESET#				
6B	VREFB6BN0_HPS	HPS_DDR					T18			HPS_DQS# 2	HPS_DQS# 2				
6B	VREFB6BN0_HPS	HPS_DDR					U28			HPS_DQ_19	HPS_DQ_19				
6B	VREFB6BN0_HPS	HPS_DDR					N25			HPS_DQ 17	HPS_DQ 17				
6B	VREFB6BN0_HPS	HPS_DDR					T28			HPS_DQ 18	HPS_DQ 18				
6B	VREFB6BN0_HPS	HPS_DDR					N24			HPS_DQ_16	HPS_DQ_16				
6B	VREFB6BN0_HPS	HPS_GPI4					R28								
6A	VREFB6AN0_HPS	HPS_GPI3					R21								
6A	VREFB6AN0_HPS	HPS_DDR					P28			HPS_DM 1	HPS_DM 1				
6A	VREFB6AN0_HPS	HPS_GPI2					R20								
6A	VREFB6AN0_HPS	HPS_DDR					N28			HPS_DQ_15	HPS_DQ_15				
6A	VREFB6AN0_HPS	HPS_DDR					M26			HPS_DQ_13	HPS_DQ_13				
6A	VREFB6AN0_HPS	HPS_DDR					M28			HPS_DQ_14	HPS_DQ_14				
6A	VREFB6AN0_HPS	HPS_DDR					M27			HPS_DQ_12	HPS_DQ_12				
6A	VREFB6AN0_HPS	HPS_DDR					L28			HPS_CKE_0	HPS_CKE_0				
6A	VREFB6AN0_HPS	HPS_DDR					R19			HPS_DQS_1	HPS_DQS_1				
6A	VREFB6AN0_HPS	HPS_DDR					K28			HPS_CKE_1	HPS_CKE_1				
6A	VREFB6AN0_HPS	HPS_DDR					R18			HPS_DQS#_1	HPS_DQS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					J28			HPS_DQ_11	HPS_DQ_11				
6A	VREFB6AN0_HPS	HPS_DDR					L25			HPS_DQ_9	HPS_DQ_9				
6A	VREFB6AN0_HPS	HPS_DDR					J27			HPS_DQ_10	HPS_DQ_10				
6A	VREFB6AN0_HPS	HPS_DDR					K25			HPS_DQ_8	HPS_DQ_8				
6A	VREFB6AN0_HPS	HPS_GPI1					K27								
6A	VREFB6AN0_HPS	HPS_GPI0					M25								
6A	VREFB6AN0_HPS	HPS_DDR					G28			HPS_DM 0	HPS_DM 0				
6A	VREFB6AN0_HPS	HPS_DDR					F28			HPS_DQ_7	HPS_DQ_7				
6A	VREFB6AN0_HPS	HPS_DDR					K26			HPS_DQ_5	HPS_DQ_5				
6A	VREFB6AN0_HPS	HPS_DDR					G27			HPS_DQ_6	HPS_DQ_6				
6A	VREFB6AN0_HPS	HPS_DDR					J26			HPS_DQ_4	HPS_DQ_4				
6A	VREFB6AN0_HPS	HPS_DDR					G26			HPS_ODT_1	HPS_ODT_1				
6A	VREFB6AN0_HPS	HPS_DDR					R17			HPS_DQS_0	HPS_DQS_0				
6A	VREFB6AN0_HPS	HPS_DDR					D28			HPS_ODT_0	HPS_ODT_0				
6A	VREFB6AN0_HPS	HPS_DDR					R16			HPS_DQS#_0	HPS_DQS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					D27			HPS_DQ_3	HPS_DQ_3				
6A	VREFB6AN0_HPS	HPS_DDR					J24			HPS_DQ_1	HPS_DQ_1				
6A	VREFB6AN0_HPS	HPS_DDR					E28			HPS_DQ_2	HPS_DQ_2				
6A	VREFB6AN0_HPS	HPS_DDR					J25			HPS_DQ_0	HPS_DQ_0				
6A	VREFB6AN0_HPS	VREFB6AN0_HPS					H28								
6A	VREFB6AN0_HPS	HPS_DDR					C28			HPS_A_0	HPS_CA_0				
6A	VREFB6AN0_HPS	HPS_DDR					B28			HPS_A_1	HPS_CA_1				
6A	VREFB6AN0_HPS	HPS_DDR					J21			HPS_A_4	HPS_CA_4				
6A	VREFB6AN0_HPS	HPS_DDR					E26			HPS_A_2	HPS_CA_2				
6A	VREFB6AN0_HPS	HPS_DDR					J20			HPS_A_5	HPS_CA_5				
6A	VREFB6AN0_HPS	HPS_DDR					D26			HPS_A_3	HPS_CA_3				
6A	VREFB6AN0_HPS	HPS_DDR					N21			HPS_CK	HPS_CK				
6A	VREFB6AN0_HPS	HPS_DDR					C26			HPS_A_6	HPS_CA_6				
6A	VREFB6AN0_HPS	HPS_DDR					N20			HPS_CK#	HPS_CK#				
6A	VREFB6AN0_HPS	HPS_DDR					B26			HPS_A_7	HPS_CA_7				
6A	VREFB6AN0_HPS	HPS_DDR					H25			HPS_BA_1					
6A	VREFB6AN0_HPS	HPS_DDR					A27			HPS_BA_0					
6A	VREFB6AN0_HPS	HPS_DDR					G25			HPS_BA_2					
6A	VREFB6AN0_HPS	HPS_DDR					A26			HPS_CAS#					
6A	VREFB6AN0_HPS	HPS_DDR					A25			HPS_RAS#					
6A	VREFB6AN0_HPS	HPS_DDR					F26			HPS_A_8	HPS_CA_8				
6A	VREFB6AN0_HPS	HPS_DDR					A24			HPS_A_10					
6A	VREFB6AN0_HPS	HPS_DDR					F25			HPS_A_9	HPS_CA_9				
6A	VREFB6AN0_HPS	HPS_DDR					B24			HPS_A_11					
6A	VREFB6AN0_HPS	HPS_DDR					L21			HPS_CS#_0	HPS_CS#_0				
6A	VREFB6AN0_HPS	HPS_DDR					D24			HPS_A_12					
6A	VREFB6AN0_HPS	HPS_DDR					L20			HPS_CS#_1	HPS_CS#_1				
6A	VREFB6AN0_HPS	HPS_DDR					C24			HPS_A_13					
6A	VREFB6AN0_HPS	HPS_DDR					G23			HPS_A_14					
6A	VREFB6AN0_HPS	HPS_DDR					E25			HPS_WE#					
6A	VREFB6AN0_HPS	HPS_DDR					F24			HPS_A_15					
6A	VREFB6AN0_HPS	HPS_RZQ_0					D25								
7A		GND					F23								
7A		GND					E23								
7A		HPS_nRST					A23								
7A		HPS_nPOR					H19								
7A		HPS_TDO					B23								

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCRSTCLK_HPS					J19								
7A		HPS_TMS					C23								
7A		HPS_TCK					K19								
7A		HPS_TRST					C22								
7A		HPS_TDI					D22								
7A		GND					D21								
7A		HPS_PORSEL					E18								
7A		HPS_CLK1					E20								
7A		HPS_CLK2					D20								
7A	VREFB7A/B7C7/DN0_HPS	TRACE_CLK					C21					TRACE_CLK			HPS_GPIO48
7A	VREFB7A/B7C7/DN0_HPS	TRACE_D0					A22					TRACE_D0	SPIS0_CLK	UART0_RX	HPS_GPIO49
7A	VREFB7A/B7C7/DN0_HPS	TRACE_D1					B21					TRACE_D1	SPIS0_MOSI	UART0_TX	HPS_GPIO50
7A	VREFB7A/B7C7/DN0_HPS	TRACE_D2					A21					TRACE_D2	SPIS0_MISO	I2C1_SDA	HPS_GPIO51
7A	VREFB7A/B7C7/DN0_HPS	TRACE_D3					K18					TRACE_D3	SPIS0_SS0	I2C1_SCL	HPS_GPIO52
7A	VREFB7A/B7C7/DN0_HPS	TRACE_D4					A20					TRACE_D4	SPIS1_CLK	CAN1_RX	HPS_GPIO53
7A	VREFB7A/B7C7/DN0_HPS	TRACE_D5					J18					TRACE_D5	SPIS1_MOSI	CAN1_TX	HPS_GPIO54
7A	VREFB7A/B7C7/DN0_HPS	TRACE_D6					A19					TRACE_D6	SPIS1_SS0	I2C0_SDA	HPS_GPIO55
7A	VREFB7A/B7C7/DN0_HPS	TRACE_D7					C18					TRACE_D7	SPIS1_MISO	I2C0_SCL	HPS_GPIO56
7A	VREFB7A/B7C7/DN0_HPS	SPIM0_CLK					A18					SPIM0_CLK	I2C1_SDA	UART0_CTS	HPS_GPIO57
7A	VREFB7A/B7C7/DN0_HPS	SPIM0_MOSI					C17					SPIM0_MOSI	I2C1_SCL	UART0_RTS	HPS_GPIO58
7A	VREFB7A/B7C7/DN0_HPS	SPIM0_MISO					B18					SPIM0_MISO	CAN1_RX	UART1_CTS	HPS_GPIO59
7A	VREFB7A/B7C7/DN0_HPS	SPIM0_SS0,BOOTSEL0					J17					SPIM0_SS0	CAN1_TX	UART1_RTS	HPS_GPIO60
7A	VREFB7A/B7C7/DN0_HPS	UART0_RX					A17					UART0_RX	CAN0_RX	SPIM0_SS1	HPS_GPIO61
7A	VREFB7A/B7C7/DN0_HPS	UART0_TX,CLKSEL1					H17					UART0_TX	CAN0_TX	SPIM1_SS1	HPS_GPIO62
7A	VREFB7A/B7C7/DN0_HPS	I2C0_SDA					C19					I2C0_SDA	UART1_RX	SPIM1_CLK	HPS_GPIO63
7A	VREFB7A/B7C7/DN0_HPS	I2C0_SCL					B16					I2C0_SCL	UART1_TX	SPIM1_MOSI	HPS_GPIO64
7A	VREFB7A/B7C7/DN0_HPS	CAN0_RX					B19					CAN0_RX	UART0_RX	SPIM1_MISO	HPS_GPIO65
7A	VREFB7A/B7C7/DN0_HPS	CAN0_TX,CLKSEL0					C16					CAN0_TX	UART0_TX	SPIM1_SS0	HPS_GPIO66
7B	VREFB7A/B7C7/DN0_HPS	NAND_ALE					J15					NAND_ALE	RGMII1_TX_CLK	QSPI_SS3	HPS_GPIO14
7B	VREFB7A/B7C7/DN0_HPS	NAND_CE					A16					NAND_CE	RGMII1_TXD0	USB1_D0	HPS_GPIO15
7B	VREFB7A/B7C7/DN0_HPS	NAND_CLE					J14					NAND_CLE	RGMII1_TXD1	USB1_D1	HPS_GPIO16
7B	VREFB7A/B7C7/DN0_HPS	NAND_RE					A15					NAND_RE	RGMII1_TXD2	USB1_D2	HPS_GPIO17
7B	VREFB7A/B7C7/DN0_HPS	NAND_RB					D17					NAND_RB	RGMII1_TXD3	USB1_D3	HPS_GPIO18
7B	VREFB7A/B7C7/DN0_HPS	NAND_DQ0					A14					NAND_DQ0	RGMII1_RXD0		HPS_GPIO19
7B	VREFB7A/B7C7/DN0_HPS	NAND_DQ1					E16					NAND_DQ1	RGMII1_MDIO	I2C3_SDA	HPS_GPIO20
7B	VREFB7A/B7C7/DN0_HPS	NAND_DQ2					A13					NAND_DQ2	RGMII1_MDC	I2C3_SCL	HPS_GPIO21
7B	VREFB7A/B7C7/DN0_HPS	NAND_DQ3					J13					NAND_DQ3	RGMII1_RX_CTL	USB1_D4	HPS_GPIO22
7B	VREFB7A/B7C7/DN0_HPS	NAND_DQ4					A12					NAND_DQ4	RGMII1_TX_CTL	USB1_D5	HPS_GPIO23
7B	VREFB7A/B7C7/DN0_HPS	NAND_DQ5					J12					NAND_DQ5	RGMII1_RX_CLK	USB1_D6	HPS_GPIO24
7B	VREFB7A/B7C7/DN0_HPS	NAND_DQ6					A11					NAND_DQ6	RGMII1_RXD1	USB1_D7	HPS_GPIO25
7B	VREFB7A/B7C7/DN0_HPS	NAND_DQ7					C15					NAND_DQ7	RGMII1_RXD2		HPS_GPIO26
7B	VREFB7A/B7C7/DN0_HPS	NAND_WP					A9					NAND_WP	RGMII1_RXD3	QSPI_SS2	HPS_GPIO27
7B	VREFB7A/B7C7/DN0_HPS	NAND_WE,BOOTSEL2					D15					NAND_WE	QSPI_SS1		HPS_GPIO28
7B	VREFB7A/B7C7/DN0_HPS	QSPI_IO0					A8					QSPI_IO0		USB1_CLK	HPS_GPIO29
7B	VREFB7A/B7C7/DN0_HPS	QSPI_IO1					H16					QSPI_IO1		USB1_STP	HPS_GPIO30
7B	VREFB7A/B7C7/DN0_HPS	QSPI_IO2					A7					QSPI_IO2		USB1_DIR	HPS_GPIO31
7B	VREFB7A/B7C7/DN0_HPS	QSPI_IO3					J16					QSPI_IO3		USB1_NXT	HPS_GPIO32
7B	VREFB7A/B7C7/DN0_HPS	QSPI_SS0,BOOTSEL1					A6					QSPI_SS0			HPS_GPIO33
7B	VREFB7A/B7C7/DN0_HPS	QSPI_CLK					C14					QSPI_CLK			HPS_GPIO34
7B	VREFB7A/B7C7/DN0_HPS	QSPI_SS1					B14					QSPI_SS1			HPS_GPIO35
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_CMD					D14					SDMMC_CMD	USB0_D0		HPS_GPIO36
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_PWREN					A5					SDMMC_PWREN	USB0_D1		HPS_GPIO37
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_D0					C13					SDMMC_D0	USB0_D2		HPS_GPIO38
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_D1					B6					SDMMC_D1	USB0_D3		HPS_GPIO39
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_D4					H13					SDMMC_D4	USB0_D4		HPS_GPIO40
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_D5					A4					SDMMC_D5	USB0_D5		HPS_GPIO41
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_D6					H12					SDMMC_D6	USB0_D6		HPS_GPIO42
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_D7					B4					SDMMC_D7	USB0_D7		HPS_GPIO43
7C	VREFB7A/B7C7/DN0_HPS	HPS_GPIO44					B12						USB0_CLK		HPS_GPIO44
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_CCLK_OUT					B8					SDMMC_CCLK_OUT	USB0_STP		HPS_GPIO45
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_D2					B11					SDMMC_D2	USB0_DIR		HPS_GPIO46
7C	VREFB7A/B7C7/DN0_HPS	SDMMC_D3					B9					SDMMC_D3	USB0_NXT		HPS_GPIO47
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_TX_CLK					E4					RGMII0_TX_CLK			HPS_GPIO0
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_TXD0					C10					RGMII0_TXD0	USB1_D0		HPS_GPIO1
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_TXD1					F5					RGMII0_TXD1	USB1_D1		HPS_GPIO2
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_TXD2					C9					RGMII0_TXD2	USB1_D2		HPS_GPIO3
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_TXD3					C4					RGMII0_TXD3	USB1_D3		HPS_GPIO4
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_RXD0					C8					RGMII0_RXD0	USB1_D4		HPS_GPIO5
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_MDIO					D4					RGMII0_MDIO	USB1_D5	I2C2_SDA	HPS_GPIO6
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_MDC					C7					RGMII0_MDC	USB1_D6	I2C2_SCL	HPS_GPIO7
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_RX_CTL					F4					RGMII0_RX_CTL	USB1_D7		HPS_GPIO8
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_TX_CTL					C6					RGMII0_TX_CTL			HPS_GPIO9
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_RX_CLK					G4					RGMII0_RX_CLK	USB1_CLK		HPS_GPIO10
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_RXD1					C5					RGMII0_RXD1	USB1_STP		HPS_GPIO11
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_RXD2					E5					RGMII0_RXD2	USB1_DIR		HPS_GPIO12
7D	VREFB7A/B7C7/DN0_HPS	RGMII0_RXD3					D5					RGMII0_RXD3	USB1_NXT		HPS_GPIO13
8A	VREFB8AN0	IO	CLK7p		DIFFIO_RX_T1p	DIFFOUT_T1p	D12								
8A	VREFB8AN0	IO	CLK7n		DIFFIO_RX_T1n	DIFFOUT_T1n	C12								
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T4p	DIFFOUT_T4p	E8								
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T4n	DIFFOUT_T4n	D8								
8A	VREFB8AN0	IO	CLK6p,FPLL_TL_FBp		DIFFIO_RX_T9p	DIFFOUT_T9p	E11								
8A	VREFB8AN0	IO	CLK6n,FPLL_TL_FBn		DIFFIO_RX_T9n	DIFFOUT_T9n	D11								
8A	VREFB8AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	L10								
8A	VREFB8AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	H6								
8A	VREFB8AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	L9								
8A	VREFB8AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	H5								
8A	VREFB8AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	L8								
8A	VREFB8AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	K8								
8A	VREFB8AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	H4								
9A		MSEL0		MSEL0			J10								
9A		CONF_DONE		CONF_DONE			J8								
9A		MSEL1		MSEL1			H9								
9A		nSTATUS		nSTATUS			H8								
9A		nCE		nCE			E6								
9A		MSEL2		MSEL2			G6								
9A		MSEL3		MSEL3			K10								
9A		nCONFIG		nCONFIG			F7								
9A		MSEL4		MSEL4			K9								
		GND					F6								
		GND					N8								
		GND					P8								
		GND					F2								
		GND					F1								
		GND					K2								
		GND					K1								
		GND					P2								
		GND					P1								
		GND					V2								
		GND					V1								
		GND					AB2								
		GND					AB1								
		GND					AF2								
		GND					AF1								
		GND					V5								
		GND					V4								
		GND					A10								
		GND					A3								
		GND					AA1								
		GND					AA17								
		GND					AA2								
		GND					AA3								
		GND					AA9								
		GND					AB24								
		GND					AB27								
		GND					AB3								

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AC1								
		GND					AC2								
		GND					AC3								
		GND					AD14								
		GND					AD22								
		GND					AD25								
		GND					AD3								
		GND					AD6								
		GND					AD8								
		GND					AE1								
		GND					AE16								
		GND					AE18								
		GND					AE2								
		GND					AE3								
		GND					AF24								
		GND					AF3								
		GND					AG1								
		GND					AG17								
		GND					AG2								
		GND					AG27								
		GND					AG3								
		GND					AG7								
		GND					AH10								
		GND					AH20								
		GND					B15								
		GND					B17								
		GND					B20								
		GND					B22								
		GND					B25								
		GND					B27								
		GND					B3								
		GND					B5								
		GND					B7								
		GND					C1								
		GND					C11								
		GND					C2								
		GND					C3								
		GND					D10								
		GND					D13								
		GND					D16								
		GND					D3								
		GND					E1								
		GND					E19								
		GND					E2								
		GND					E22								
		GND					E24								
		GND					E27								
		GND					E3								
		GND					E9								
		GND					F3								
		GND					G1								
		GND					G2								
		GND					G3								
		GND					H11								
		GND					H15								
		GND					H18								
		GND					H20								
		GND					H24								
		GND					H27								
		GND					H3								
		GND					Y3								
		GND					Y25								
		GND					Y20								
		GND					J1								
		GND					J2								
		GND					J3								
		GND					J5								
		GND					J9								
		GND					K11								
		GND					K12								
		GND					K14								
		GND					K16								
		GND					K20								
		GND					K3								
		GND					K4								
		GND					Y14								
		GND					L1								
		GND					Y12								
		GND					L13								
		GND					L15								
		GND					L17								
		GND					L19								
		GND					L2								
		GND					L24								
		GND					L27								
		GND					L3								
		GND					L5								
		GND					W4								
		GND					W3								
		GND					M10								
		GND					M11								
		GND					M14								
		GND					M16								
		GND					M20								
		GND					M3								
		GND					M8								
		GND					N1								
		GND					N13								
		GND					N15								
		GND					N17								
		GND					N19								
		GND					N2								
		GND					N3								
		GND					N4								
		GND					P10								
		GND					P12								
		GND					P16								
		GND					P18								
		GND					P20								
		GND					P25								
		GND					P3								
		GND					P5								
		GND					P9								
		GND					R1								
		GND					R11								
		GND					R13								
		GND					R15								
		GND					R2								
		GND					R3								
		GND					R8								
		GND					T10								
		GND					T14								
		GND					T3								
		GND					U1								
		GND					U12								

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					U17								
		GND					U2								
		GND					U20								
		GND					U24								
		GND					U27								
		GND					U3								
		GND					U5								
		GND					V14								
		GND					V3								
		GND					V8								
		GND					V9								
		GND					W1								
		GND					W16								
		GND					W18								
		GND					W2								
		GND					AB25								
		GND					W24								
		GND					Y24								
		GND					AA26								
		GND					W20								
		GND					AB26								
		GND					W21								
		GND					V26								
		GND					V21								
		VCC					J11								
		VCC					K13								
		VCC					K15								
		VCC					L11								
		VCC					L12								
		VCC					L14								
		VCC					M12								
		VCC					M13								
		VCC					M15								
		VCC					M9								
		VCC					N10								
		VCC					N11								
		VCC					N12								
		VCC					N14								
		VCC					N9								
		VCC					P11								
		VCC					P13								
		VCC					P14								
		VCC					P15								
		VCC					R10								
		VCC					R12								
		VCC					R14								
		VCC					R9								
		VCC					T15								
		VCC					T9								
		VCC					L4								
		VCC					T4								
		VCC					M5								
		VCC					N5								
		VCC					R5								
		VCC					T5								
		VCC					U26								
		DNU					A2								
		DNU					B2								
		DNU					D1								
		DNU					D2								
		DNU					H1								
		DNU					H2								
		DNU					M1								
		DNU					M2								
		DNU					T1								
		DNU					T2								
		DNU					Y1								
		DNU					Y2								
		DNU					AD1								
		DNU					AD2								
		DNU					D23								
		DNU					E12								
		DNU					U8								
		DNU					AE14								
		VCCPGM					Y10								
		VCCPGM					AD24								
		VCCPGM					H10								
		VCCBAT					D7								
		VCCIO3A					AA5								
		VCCIO3A					W9								
		VCCIO3B					AA12								
		VCCIO3B					AE10								
		VCCIO3B					AE13								
		VCCIO3B					AG4								
		VCCIO4A					AA16								
		VCCIO4A					AE21								
		VCCIO4A					AF14								
		VCCIO4A					AF19								
		VCCIO4A					AG12								
		VCCIO4A					AG22								
		VCCIO4A					AH15								
		VCCIO4A					AH25								
		VCCIO4A					W13								
		VCCIO5A					AC25								
		VCCIO5A					W17								
		VCCIO6A_HPS					C25								
		VCCIO6A_HPS					C27								
		VCCIO6A_HPS					F27								
		VCCIO6A_HPS					G24								
		VCCIO6A_HPS					H21								
		VCCIO6A_HPS					H26								
		VCCIO6A_HPS					L26								
		VCCIO6A_HPS					M21								
		VCCIO6B_HPS					AD27								
		VCCIO6B_HPS					P27								
		VCCIO6B_HPS					T21								
		VCCIO6B_HPS					T25								
		VCCIO6B_HPS					U18								
		VCCIO6B_HPS					W27								
		VCCIO7A_HPS					C20								
		VCCIO7A_HPS					D18								
		VCCIO7B_HPS					B13								
		VCCIO7B_HPS					H14								
		VCCIO7C_HPS					B10								
		VCCIO7D_HPS					D6								
		VCCIO7D_HPS					G5								
		VCCIO9A					E7								
		VCCPD3A					AA10								
		VCCPD3B4A					AA14								
		VCCPD3B4A					AD13								
		VCCPD3B4A					AD16								
		VCCPD3B4A					AD18								
		VCCPD3B4A					AD21								
		VCCPD3B4A					AD9								
		VCCPD5A					Y21								

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (3)	HMC Pin Assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCPD6A6B_HPS					K21								
		VCCPD6A6B_HPS					K24								
		VCCPD6A6B_HPS					M24								
		VCCPD6A6B_HPS					P21								
		VCCPD6A6B_HPS					P24								
		VCCPD7A_HPS					E21								
		VCCPD7B_HPS					E17								
		VCCPD7C_HPS					E14								
		VCCPD7D_HPS					E13								
		VCCPD8A					E10								
3A	VREFB3AN0	VREFB3AN0					AE5								
3B	VREFB3BN0	VREFB3BN0					AF12								
4A	VREFB4AN0	VREFB4AN0					AF16								
5A	VREFB5AN0	VREFB5AN0					AC26								
	VREFB7A7B7C7DN0_HPS	VREFB7A7B7C7DN0_HPS					D19								
8A	VREFB8AN0	VREFB8AN0					D9								
		NC					W25								
		NC					AA25								
		NC					W19								
		VCCRSTCLK_HPS					F22								
		RREF_TL					B1								
		VCCA_FPLL					K5								
		VCCA_FPLL					P4								
		VCCA_FPLL					U4								
		VCCA_FPLL					W5								
		VCCA_FPLL					J4								
		VCCA_FPLL					AA21								
		VCCA_FPLL					M4								
		VCCA_FPLL					R4								
		VCC_AUX					AC21								
		VCC_AUX					AC8								
		VCC_AUX					AD15								
		VCC_AUX					E15								
		VCC_AUX					F8								
		VCC_AUX_SHARED					F21								
		VCCPLL_HPS					H23								
		VCC_HPS					U21								
		VCC_HPS					K17								
		VCC_HPS					L16								
		VCC_HPS					L18								
		VCC_HPS					M17								
		VCC_HPS					M18								
		VCC_HPS					M19								
		VCC_HPS					N16								
		VCC_HPS					N18								
		VCC_HPS					P17								
		VCC_HPS					P19								

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Cyclone V Device Family Pin Connection Guidelines.
(2) HPS DDR pins are for memory interface only. For the dedicated pin function corresponding with the respective memory interfaces, refer to the HMC columns.
(3) RESET pin is only applicable for DDR3 device.

Version Number	Date	Changes Made
1.0	7/8/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.