Explore, Acquire, Analyze, Decide.
Deliver Sooner, Better.
System Expertise

Military Communications
ISR, Radar, EW
Avionics, Missile Defense
Intelligence / Cyber Security
Space

Productivity & Technology

Unparalleled Productivity
OpenCL™
Full-Throttle Performance
Best-in-Class IP

Design Flow

FPGA Designers
GPU Programmers
Embedded Developers

Altera
Military / Aerospace / Government
Solutions Portfolio
Explore more ideas quickly.

Acquire new concepts easily.

Deliver designs sooner, better.

You win.

- First Floating-Point FPGA
- 10+ TFLOPS at 100 GFLOPS/Watt
- 500 GFLOPS FFT 50 Gsps FFT Generation
- Cholesky and QRD Up to 1,000,000 Matrices/Sec
- Industry’s Longest Product Life Cycle
- OpenCL Conformant
- Only On-Shore, High-End FPGA Fabric
Unparalleled Productivity

- Hardware in the Loop integrated reference designs
- DSP Builder Advanced Blockset is high-level, schematic-entry design:
  - Constraint-driven design (select f_MAX, latency, number of channels, device family, etc.)
  - Single datapath logic system clock
  - Automatic pipelining, register balancing
  - Fast, automatic timing closure
- Best-in-Class IP
  - Finite impulse response (FIR) filters
  - Support multichannel, time-division multiplexed (TDM), and sample rate >> clock rate
  - Fast Fourier transforms (FFTs) fixed and floating point
  - Cascaded Integrator Comb (CIC) filters and waveform generating or mixing blocks
  - Largest, fastest portfolio of floating-point functions

Full-Throttle Performance

- Industry’s first floating-point FPGA
- 10 TFLOPS at 100 GFLOPS/Watt
- Up to 26 TMACs and 1 GHz fabric
- Common environment for system architect and design engineers
- Best-in-Class IP
  - Finite impulse response (FIR) filters
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System Expertise

Avionics, Missile Defense
- Support for DO-254 and DO-178C
- Package and radiation reliability report
- Guidance and control IP with reference designs

Intelligence / Cyber Security
- OpenCL accelerator FPGA cards
- High-performance IP for Cyber
- Enable software developers to program FPGAs
- Open Source Security and extensive ecosystem
- Expedite time to mission

Space
- Latch-up immunity
- Radiation test report and analysis
- LEO application-capable
- Custom screening and bare die

Design Flow

- FPGA Designers
- HDL automatically optimized
- Design-visible COTS boards
- Conformant to Open Systems
- C-Tools direct to ARM
- Real-time verification with System-in-the-Loop
- OpenCL

ISR, Radar, EW
- Solution for digitization of phased-array antennas
- Fastest digital signal processing (DSP) blocks
- Comprehensive floating point and linear algebra library
- Modular Open Systems Architecture — commercial off-the-shelf (COTS) solutions
- System Integration Framework for rapid system development

Military Communications
- 28 Gbps serializer/deserializer (SERDES) transceivers
- Densest logic count in small-form-factor (SFF) packages
- Cryptographic partner IP cores
- Government-approved design methodologies
- Assured design for information assurance

Military / Aerospace / Government

Productivity & Technology

OpenCL
- Productivity: heterogeneous design platform including FPGA
- Performance: optimum throughput and latency for data and task-parallel algorithms
- Efficiency: industry-leading performance per watt

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Design Flow
Solutions & Benefits

Digital Beamforming with System-in-the-Loop

- FPGA
  - Target Emulation
  - Rx Noise Emulation
  - TxB Time Delay Beamforming
  - Waveform Generator
  - Pulse Compression

Matlab API

Beamformed and Pulse Compressed Output — Top View

Beamformed and Pulse Compressed Output — 3D

Pulse Doppler Processing

- Data Snapshot Angle Doppler Response

Normalized Doppler Frequency vs. Angle (degrees)

- Normalized Frequency
- Power (dB)

Space Time Adaptive Processing (STAP)

- SMI Weights Angle Doppler Response

Normalized Doppler Frequency vs. Angle (degrees)

- Normalized Frequency
- Power (dB)

Ultra-Wideband Channelizer

- Input Signal
- Input Signal 2
- Target Input Signal

Delay Techniques

Perfect Reconstruction

Altera Product Leadership

- 18x18 Mults
- SP FP Mults
- SP TFLOPs

Military Security
- NIST AES-256 bitstream encryption
- NIST HMAC SHA-256 bitstream authentication
- Hard configuration error detection and correction
- On-chip voltage and temperature sensors
- 64 bit unique device ID
- Type-I and CSfC compliant solutions
- Security Supervisor IP (SSIP)
- Robust cryptographic partner IP

Commitment to Defense Industry
- Domestic fabrication — 14 nm Intel partnership
- Dedicated engineering support
- Pin-compatible migration (device migration)

Reliability and Longevity
- Industry’s longest product life cycle
- Test above industry standard for package quality
- Leadless packages
- Broad selection of military temperature devices
- Latch-up immune

Integration

Baseboard Digital Processing

- Altera FPGA
- Logic Elements
  - ARM
  - Ethernet (GigE, 10GE)
  - DDR2/3/4 Memory
  - General Purpose Processor
  - HyperLink
  - MultiCore DSP

- AXI4
- ML Multiplier
- MatLab API

- Network Interface
  - Packet-switch Interconnect (chip, board, backplane)
  - Point-to-Point Link Layer (chip, board, backplane)

- PCIe
- DDR2/3/4 Memory
- Board-level Interconnect
- FPGAs (or other Chip)

- Software-defined (SDM)
- FPGA (or other)
- HDL

- Analog (SPI, etc.)
- ARM Processor
- User Memory
- JESD 204B Tx
- JESD 204B Rx
- JESD 204B Rx

- SMI Weights Angle Doppler Response

- Distance (Range Bin)
- Azimuth
- Normalized Doppler Frequency

- Power (dB)

- Angle (degrees)

- Frequency (Hz)

- Power (dB)

- Angle (degrees)

- Frequency (Hz)

- Power (dB)
Test Drive Altera Today!

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