Creating Testbench using ModelSim-Altera Wave Editor

You can use ModelSim-Altera Wave Editor to draw your test input waveforms and generate a Verilog HDL or VHDL testbench. You can then perform an RTL or gate-level simulation to verify the correctness of your design.

1. **Invoke ModelSim-Altera and compile design files:**
   a. You can invoke ModelSim-Altera and compile your design files through NativeLink. To learn how to do this, please go through the tutorial, "How to simulate your design through NativeLink" at http://www.altera.com/support/kdb/solutions/rd10312011_847.html. Please note that you cannot specify the testbench as you have not yet created one.

      Once you compile the design you will see the modules in the designs in the work library as shown in the figure below.

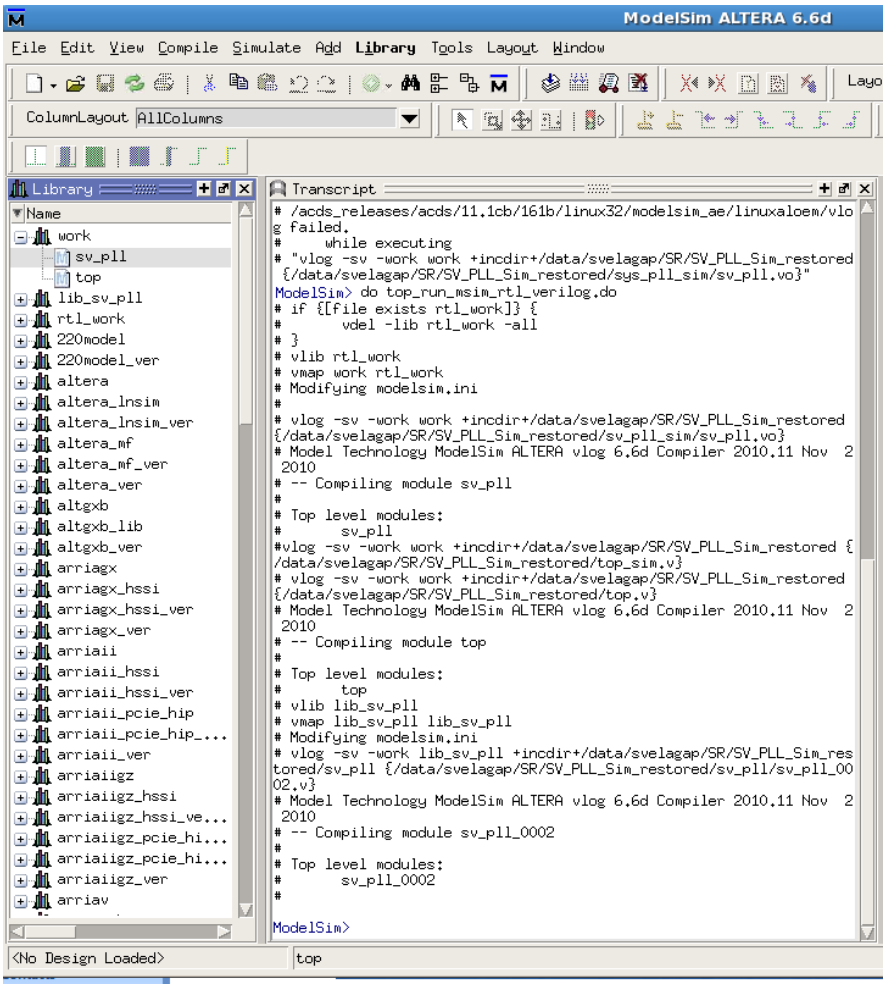

Figure 1

2. **Adding signals to Wave Editor**
    a. Right-click on the entity you are interested in and click on “Create Wave” to get all the signals in the entity to be added to the wave editor.

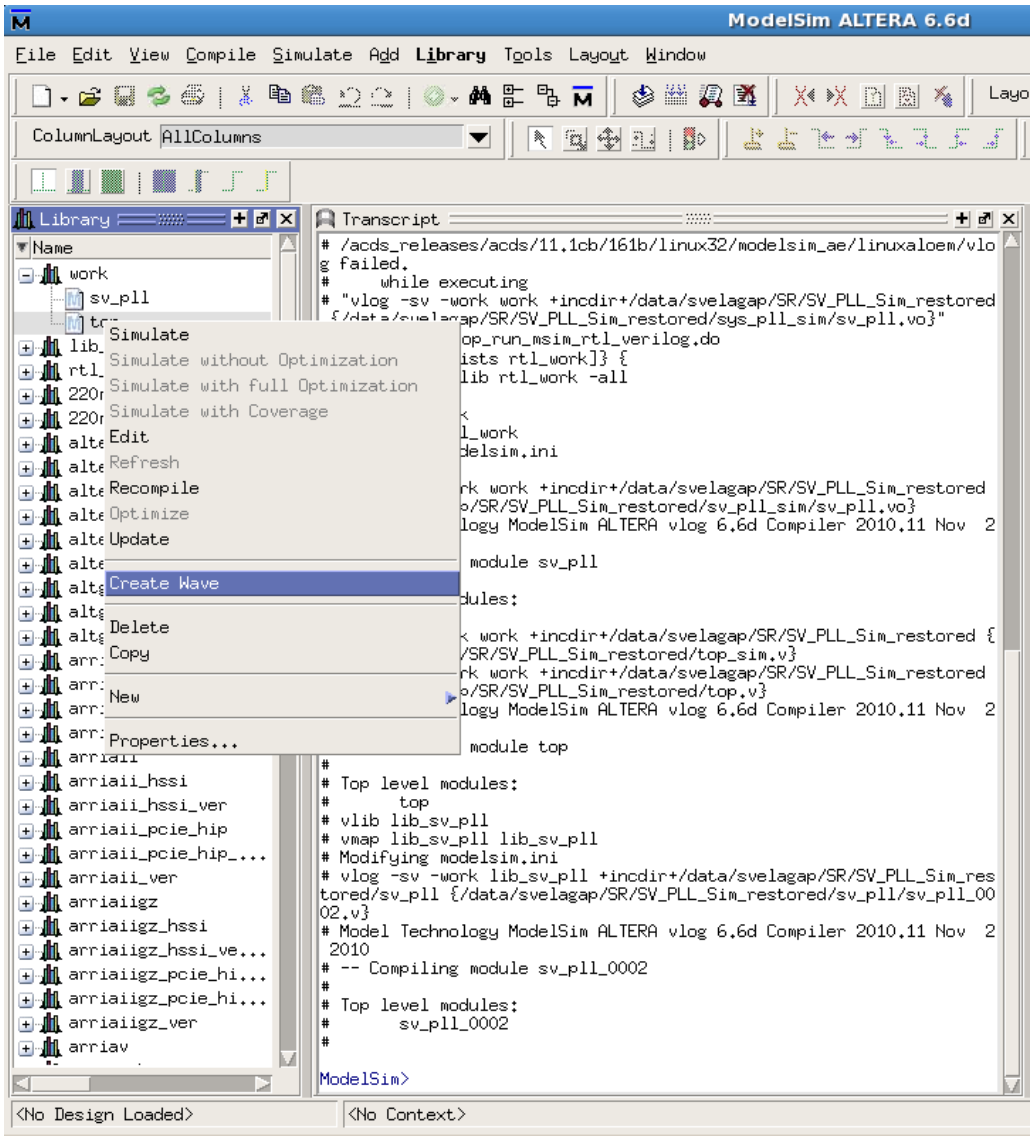

Figure 2

1. **Specifying Input Test Vectors**
    a. Specify the input test vectors for the module. For example in the design module “top” as shown in Figure 3, `ref_clk` and `rst` are the inputs. We need to specify the input vectors for these signals.

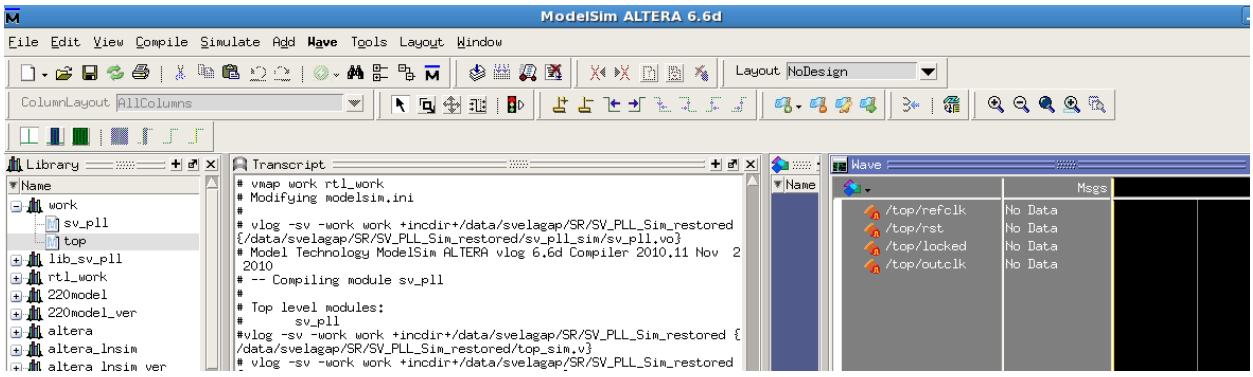

Figure 3

b. To specify the input vector for `ref_clk`, right click on `ref_clk` and select Edit -> Create/Modify Waveform as shown in the Figure 4.

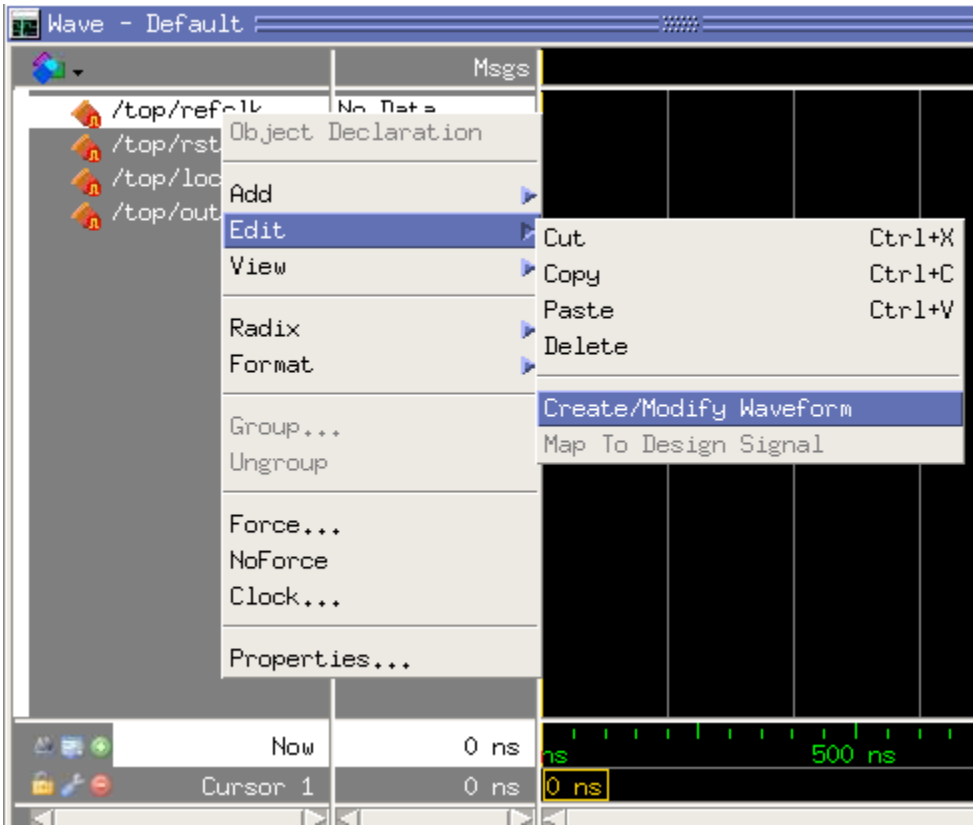

Figure 4

c. Create a clock by giving the start time and end time and click next as see in Figure 5 and click Next.

Figure 5

d. Give the initial value and clock period as shown in Figure 6 and click Finish.

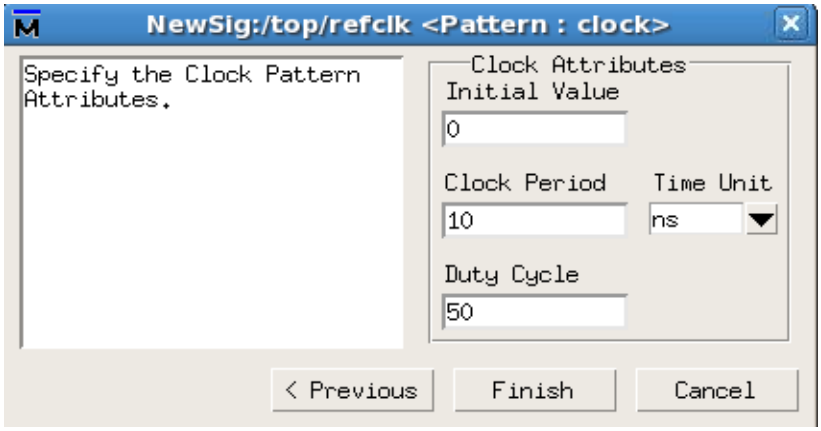

Figure 6

e. To create a reset signal, right-click the `rst` signal.
f. Click on “Create/Modify Waveform” and click on constant.
g. Pick the start time as 0 and end time as 100 ns and give value of “0” and press Finish.
h. Right-click `rst` again.
i. Click on “Create/Modify Waveform” and click on constant
j. Pick the start time as 100 and end time as 1000 as shown below in Figure 7.

Figure 7

k. Give the value for `rst` as 1 and press Finish.

The table below shows the five available patterns and their descriptions:

Pattern	Description
Clock	Specify an initial value, duty cycle, and clock period for the waveform.
Constant	Specify a value.
Random	Generates different patterns depending upon the seed value. Specify the type (normal or uniform), an initial value, and a seed value. If you don't specify a seed value, ModelSim uses a default value of 5.
Repeater	Specify an initial value and pattern that repeats. You can also specify how many times the pattern repeats.
Counter	Specify start and end values, time period, type (Range, Binary, Gray, One Hot, Zero Hot, Johnson), counter direction, step count, and repeat number.

2. <u>Converting from Wave form to Verilog/VHDL</u>

a. Once you are done with creating the input test vectors, click on File -> Export -> Waveform as shown in Figure 8.

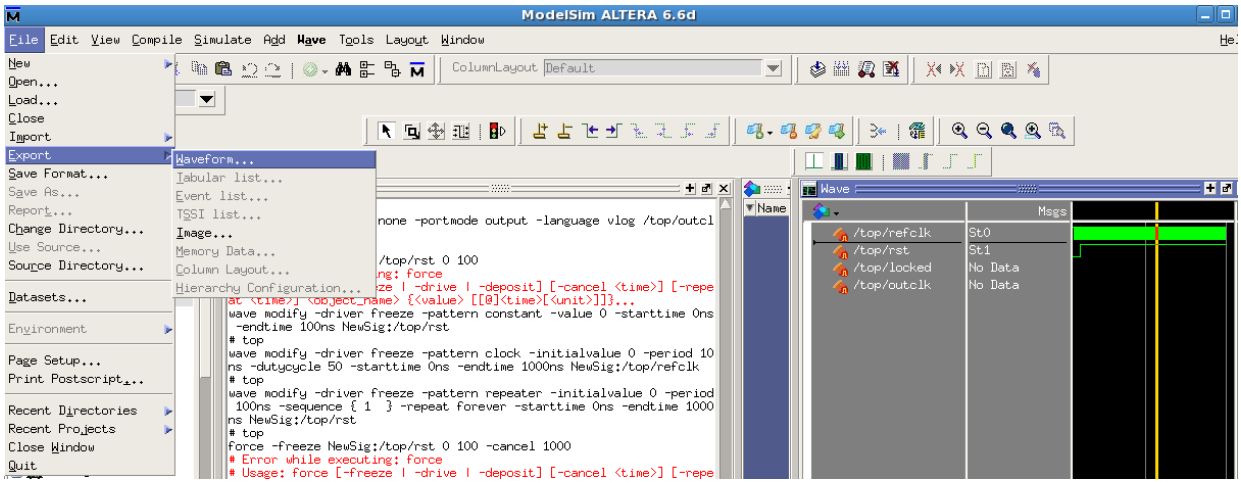

Figure 8

b. Select VHDL or Verilog testbench and give the filename as shown is Figure 9 below.

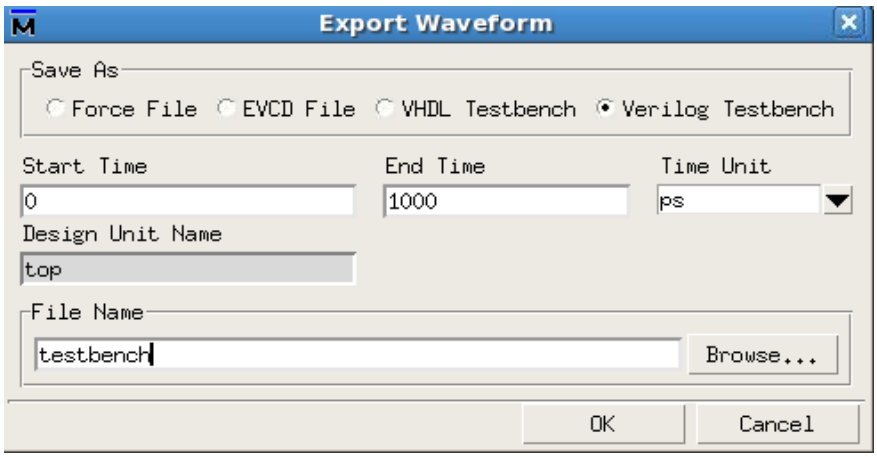

Figure 9

3. Simulating with the testbench

a. Once the testbench is created, input the testbench information in the EDA Simulation tab as described in the NativeLink simulation doc and simulate your design.

Revision	Changes Made	Date
V1.0	Initial release.	DEC 2011