**How to reduce the percentage of crosstalk and SSN towards differential pins in Cyclone V devices**

**Introduction**

This document will describe how to reduce the percentage (%) of crosstalk and percentage (%) of SSN towards differential pins in the Quartus® II software when targeting Cyclone® V devices.

1. **Setup**

The guidelines in this document are applicable to Cyclone V devices and Quartus II software version 13.1 or later.

1. **How to reduce the % of crosstalk that affects differential pins**

When a design containing both differential and single ended (SE) I/O pins is compiled in the Quartus II software versions 13.1 or later, you may see a Critical Warning message such as the example shown below:

Critical Warning (12881): Too many 2.5-V SE IO in bank 8A with LVDS TX pin out\_bus[0]. Reduce the number of 2.5-V I/Os used and re-run the analysis again. Please refer to the guideline from the Knowledge Base solution ID: rd10102013\_979 and ensure the total % of crosstalk for the following SE I/O pins does not exceed 100%.

 Info (12900): SE I/O out\_bus[11] contributed to 263% of crosstalk

 Info (12900): SE I/O out\_bus[7] contributed to 20% of crosstalk

 Info (12900): SE I/O out\_bus[3] contributed to 71% of crosstalk

To reduce the % of crosstalk to a value within the safe threshold of < 100%, follow the steps below :

* Download the [*Cyclone V differential pad placement rule and pad mapping files* (.zip)](http://www.altera.com/literature/dp/cyclone-v/differential_pad_placement_mapping_files.zip)  and locate the pad mapping spreadsheet which matches the Cyclone V device you are targeting.
* Open up the spreadsheet and identify the violating SE I/O pins and the respective differential pin pair locations.
* Start with the violating SE I/O pin which contributes the most % of crosstalk. Reassign or move the violating SE I/O pin away from the differential pins as shown in Figure 2-1 below. It is recommended to move the violating SE I/O pin at least three to four pads away from the differential I/O pins.

For example:

The D6 and C6 pins are differential pins and D7 is the violating SE I/O pin. You can reassign the D7 SE I/O pin location to another location away from differential pin location. For example, move the D7 SE I/O pin location to G6.



**Figure 2-1.** Example of relocating a single ended I/O to reduce % of crosstalk on a differential pin pair

* Recompile the design after reassigning or moving the violating SE I/O pins. You will get no further warnings if the summed % of the aggressors for a given victim is less than 100%.
* For further details of the physics based rules please refer to the [*Cyclone V Device Family Pin Connection Guidelines* (PDF)](http://www/literature/dp/cyclone-v/PCG-01014.pdf) (notes 11, 12, and 13).
1. **How to reduce the % of SSN towards differential pins**

When a design containing differential and single ended IO is compiled in Quartus II software versions 13.1 or later, you may see a Critical Warning message such as the example shown below:

Critical Warning (12887): Too many 2.5-V SE IO in bank 8A with LVDS RX pin in\_bus[0]. Reduce the number of 2.5-V I/Os used and re-run the analysis again. Please refer to the guideline from the Knowledge Base solution ID: rd10102013\_979 and ensure the total % of SSN for the following SE I/O pins does not exceed 100%.

 Info (12899): SE I/O out\_bus[12] contributed to 8% of the SSN

 Info (12899): SE I/O out\_bus[11] contributed to 8% of the SSN

 Info (12899): SE I/O out\_bus[10] contributed to 8% of the SSN

 Info (12899): SE I/O out\_bus[9] contributed to 8% of the SSN

 Info (12899): SE I/O out\_bus[8] contributed to 8% of the SSN

<TRUNCATED>

To reduce the % of SSN to a value within the safe threshold of < 100%, follow the steps below :

* Reduce the drive strength and slew rate of the violating SE I/O pins. Start with the violating SE I/O which contributes the most % of SSN.
* If you know that the SE I/O pins toggle rate are less than 100 MHz, you can use the IO\_MAXIMUM\_TOGGLE\_RATE assignment (e.g. 99 MHz) on the violating SE I/O pins to make the physics based rules calculation less restrictive.
* Recompile the design after making the appropriate changes to the SE I/O pins. You will get no further warnings if the summed % of the aggressors for a given victim is less than 100%.
1. **Conclusion**

This document provides guidelines on how to reduce the % of crosstalk and % of SSN in designs that target Cyclone V devices and use a mixture of differential and single ended I/O, when using Quartus II software versions 13.1 or later.

1. **Revision History**

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| --- | --- | --- |
| **Revision** | **Changes Made** | **Date** |
| V1.0 | Initial release. | Nov 2013 |

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