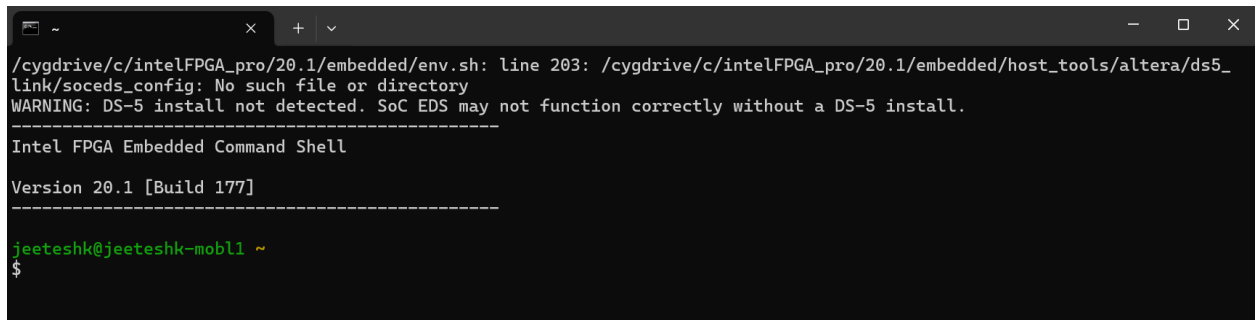


Step by Step Procedure to run the Intel® Arria® 10 SoCFPGA-HardwareLib-Ethernet-A10-ARMCC example in Intel® SoC FPGA Embedded Development Suite (SoC EDS) Professional Edition Software Version 2020.1

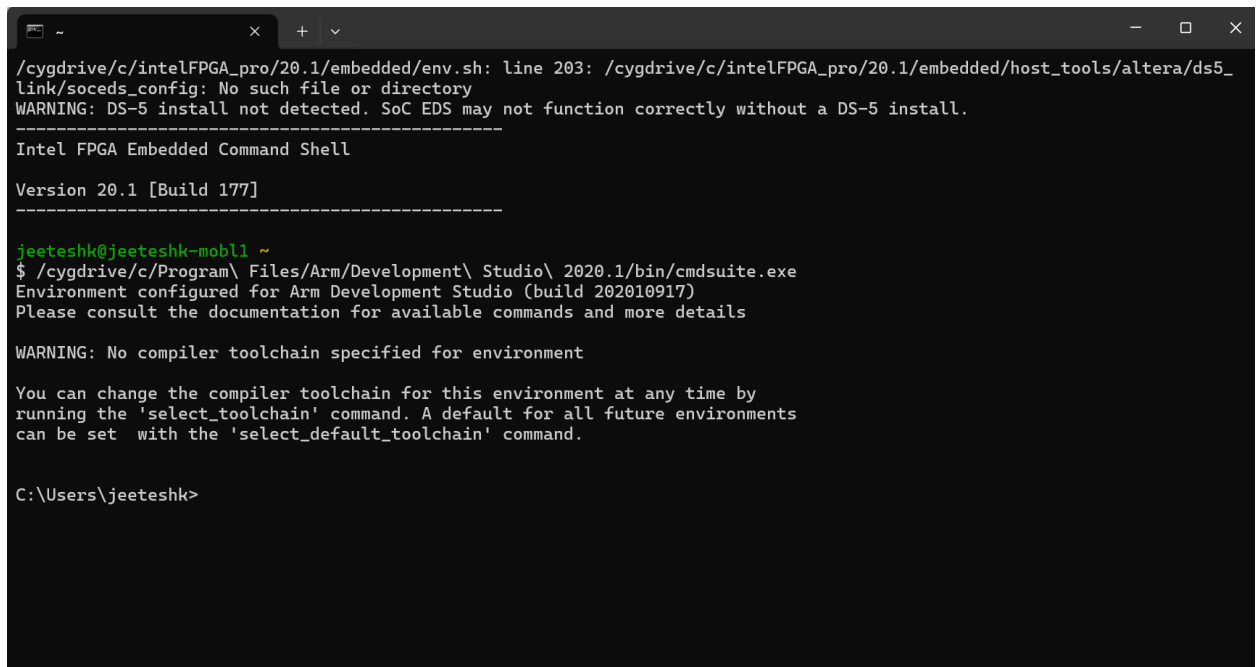
1. Open SoC EDS Command Shell using the below command-
For 20.1 Pro: **Start menu > Intel FPGA 20.1 Pro Edition > SoC EDS Command Shell.**



```
/cygdrive/c/intelFPGA_pro/20.1/embedded/env.sh: line 203: /cygdrive/c/intelFPGA_pro/20.1/embedded/host_tools/altera/ds5_
link/soceds_config: No such file or directory
WARNING: DS-5 install not detected. SoC EDS may not function correctly without a DS-5 install.
-----
Intel FPGA Embedded Command Shell

Version 20.1 [Build 177]
-----
jeeteshk@jeeteshk-mobl1 ~
$
```

2. Run the cmdsuite program
`/cygdrive/c/Program\ Files/Arm/Development\ Studio\ 2020.1/bin/cmdsuite.exe`



```
/cygdrive/c/intelFPGA_pro/20.1/embedded/env.sh: line 203: /cygdrive/c/intelFPGA_pro/20.1/embedded/host_tools/altera/ds5_
link/soceds_config: No such file or directory
WARNING: DS-5 install not detected. SoC EDS may not function correctly without a DS-5 install.
-----
Intel FPGA Embedded Command Shell

Version 20.1 [Build 177]
-----
jeeteshk@jeeteshk-mobl1 ~
$ /cygdrive/c/Program\ Files/Arm/Development\ Studio\ 2020.1/bin/cmdsuite.exe
Environment configured for Arm Development Studio (build 202010917)
Please consult the documentation for available commands and more details

WARNING: No compiler toolchain specified for environment

You can change the compiler toolchain for this environment at any time by
running the 'select_toolchain' command. A default for all future environments
can be set with the 'select_default_toolchain' command.

C:\Users\jeeteshk>
```

3. If needed, run the **select_toolchain** command to select between Arm Compiler 5 and Arm Compiler 6
4. Run the **armds_ide** command.

```
/cygdrive/c/intelFPGA_pro/20.1/embedded/env.sh: line 203: /cygdrive/c/intelFPGA_pro/20.1/embedded/host_tools/altera/ds5_
link/soceds_config: No such file or directory
WARNING: DS-5 install not detected. SoC EDS may not function correctly without a DS-5 install.
-----
Intel FPGA Embedded Command Shell
Version 20.1 [Build 177]
-----

jeeteshk@jeeteshk-mobl1 ~
$ /cygdrive/c/Program Files/Arm/Development Studio/2020.1/bin/cmdsuite.exe
Environment configured for Arm Development Studio
Please consult the documentation for available commands

WARNING: No compiler toolchain specified for e

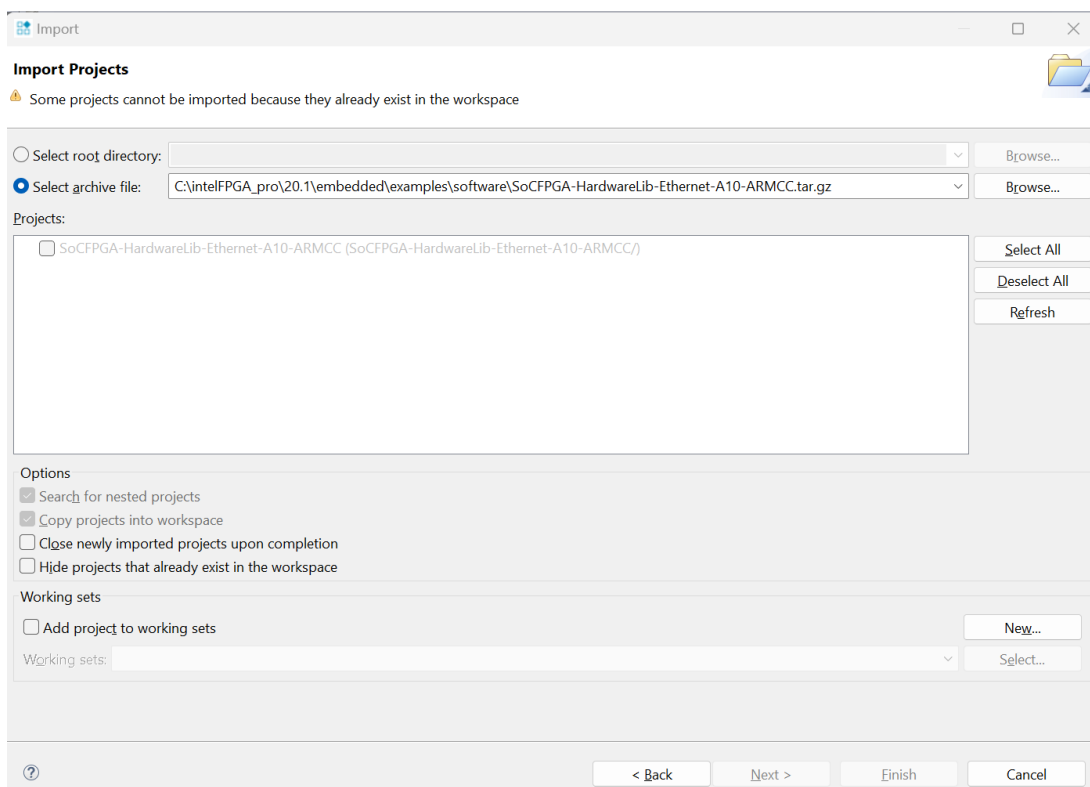
You can change the compiler toolchain for this
running the 'select_toolchain' command. A defa
can be set with the 'select_default_toolchain

C:\Users\jeeteshk>armds_ide

C:\Users\jeeteshk>
```



5. Click on File→Import Projects
6. Select Archive file and browse the SoCFPGA-HardwareLib-Ethernet-A10-ARMCC, select all and Finish.



7. Boot the Intel® Arria® 10 SX SoC Development Kit from the SD Card.
8. Press any key to stop at u-boot.

```
U-Boot SPL 2023.04 (Oct 03 2023 - 08:37:14 +0000)
FPGA: Checking FPGA configuration setting ...
FPGA: Start to program peripheral/full bitstream ...
FPGA: Early Release Succeeded.
FPGA: Checking FPGA configuration setting ...
FPGA: Start to program peripheral/full bitstream ...
FPGA: Early Release Succeeded.

U-Boot SPL 2023.04 (Oct 03 2023 - 08:37:14 +0000)
DDRCAL: Success
DDRCAL: Scrubbing ECC RAM (1024 MiB).
DDRCAL: SDRAM-ECC initialized success with 332 ms
FPGA: Checking FPGA configuration setting ...
FPGA: Skipping configuration ...
WDT: Started watchdog@ff800300 with servicing every 1000ms (10s timeout)
Trying to boot from MMC1

U-Boot 2023.04 (Oct 03 2023 - 08:37:14 +0000)socfpga_arria10

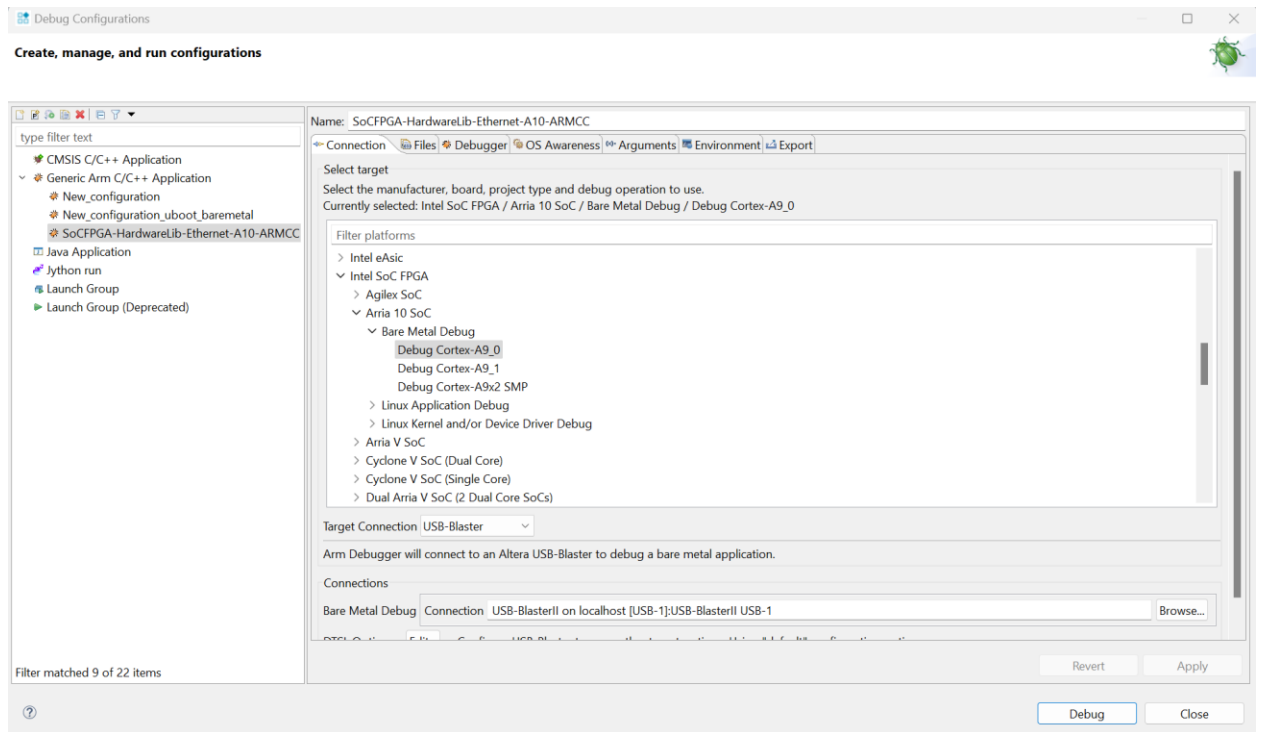
CPU: Altera SoCFPGA Arria 10
BOOT: SD/MMC External Transceiver (1.8V)
Model: Altera SOCFPGA Arria 10
DRAM: 1 GiB
Core: 77 devices, 20 uclasses, devicetree: separate
WDT: Started watchdog@ff800300 with servicing every 1000ms (10s timeout)
MMC: dwmmc0@ff808000: 0
Loading Environment from MMC... *** Warning - bad CRC, using default environment

In: serial
Out: serial
Err: serial
Model: Altera SOCFPGA Arria 10
Net:
Warning: ethernet@ff800000 (eth0) using random MAC address - 3a:fc:65:32:f3:4e
eth0: ethernet@ff800000
Hit any key to stop autoboot: 0
=>
=>
```

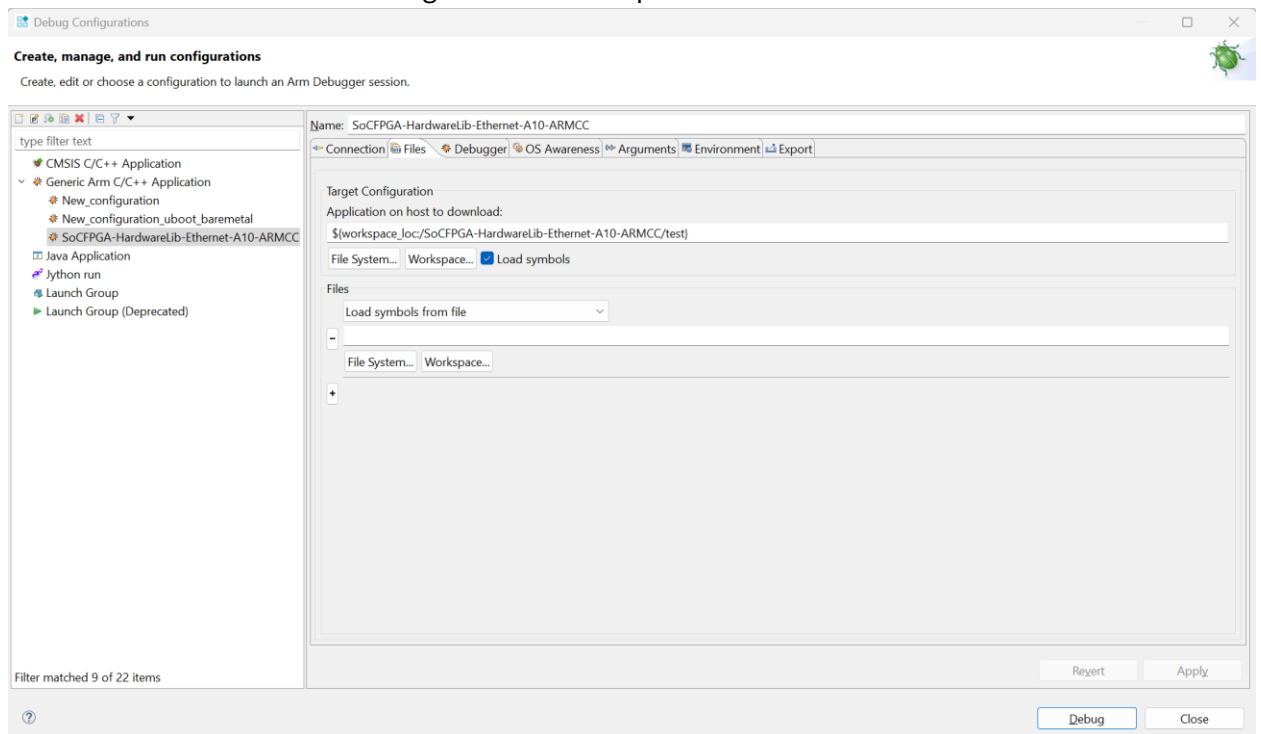
9. Run these below commands at uboot.

```
=> setenv autoload no
=> dhcp
Speed: 1000, full duplex
BOOTP broadcast 1
DHCP client bound to address 10.227.90.150 (9 ms)
=> dcache off
=> icache off
```

10. Right click on SoCFPGA-HardwareLib-Ethernet-A10-ARMCC in Project Explorer and select the Debug As→Debug Configurations and make changes to Connection tab as below snapshot.



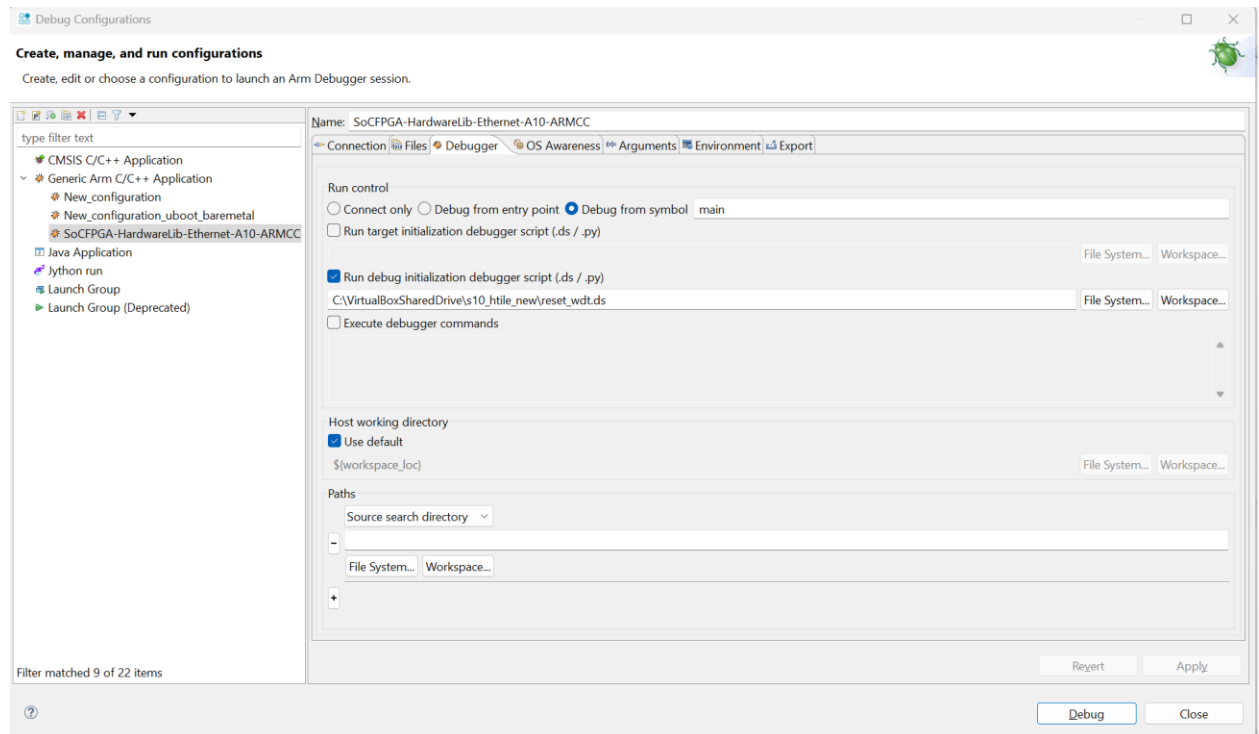
11. Click on Files tab and make changes as below snapshot.



12. Create a file naming with reset_wdt.ds and copy the below lines in reset_wdt.ds file.

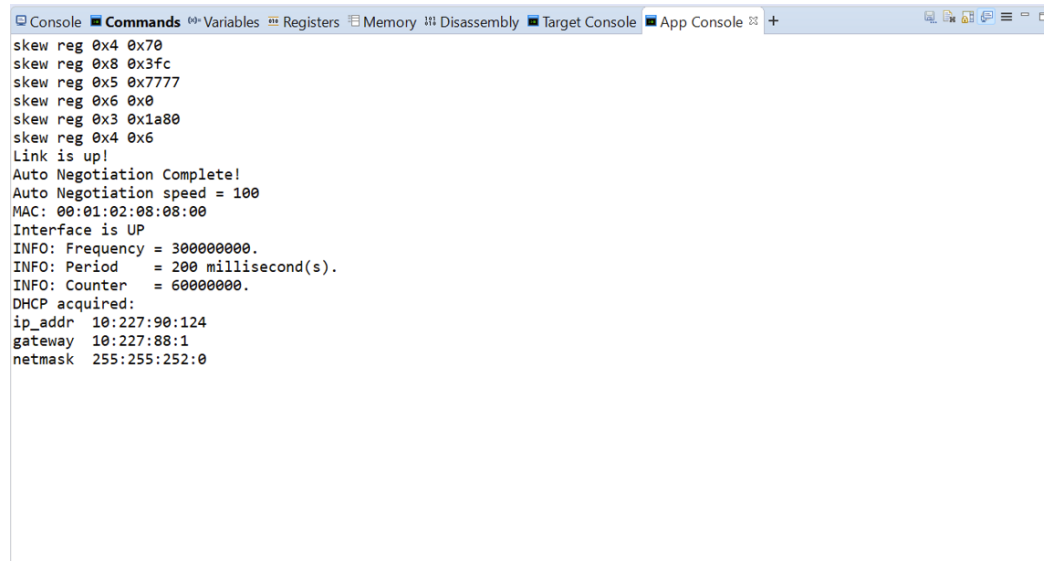
```
set var $Peripherals::$i_rst_mgr::$i_rst_mgr_per1modrst.watchdog0 = 0x1
set var $Peripherals::$i_rst_mgr::$i_rst_mgr_per1modrst.watchdog1 = 0x1
```

13. Click on Debugger tab and make changes as below snapshot.



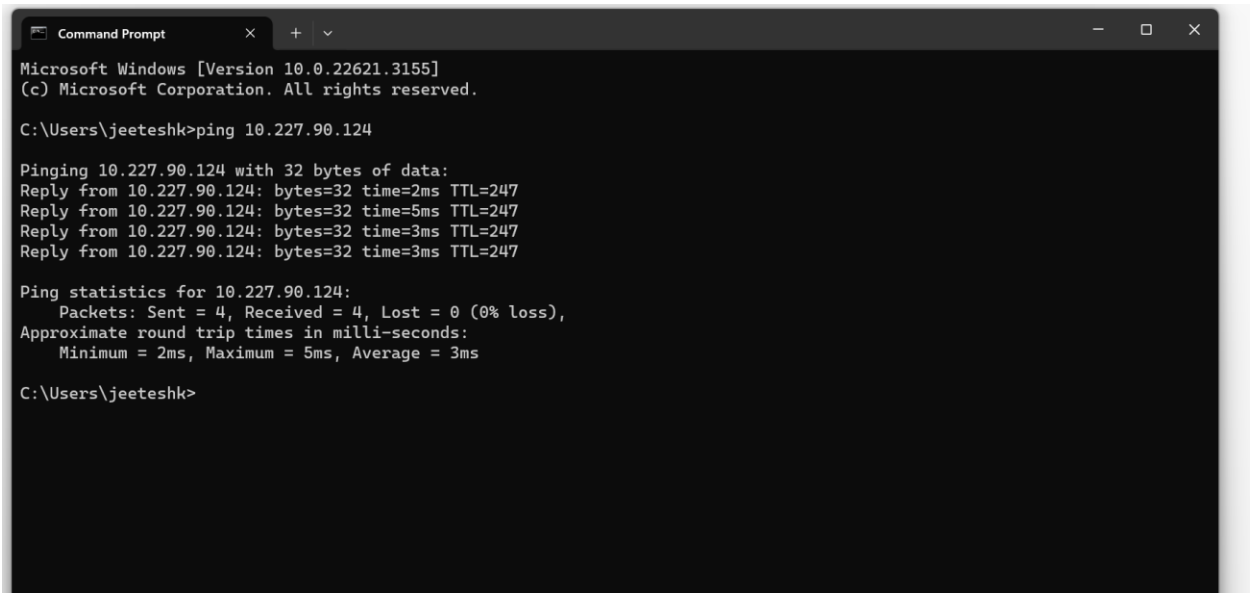
14. Click on Apply and Debug.

15. You will see that ethernet application starts printing on App Console



16. From the above snapshot, you will see that board received the IP address from the server i.e. 10.227.90.124

From PC you can ping the board IP address 10.227.90.124



```
Command Prompt
Microsoft Windows [Version 10.0.22621.3155]
(c) Microsoft Corporation. All rights reserved.

C:\Users\jeeteshk>ping 10.227.90.124

Pinging 10.227.90.124 with 32 bytes of data:
Reply from 10.227.90.124: bytes=32 time=2ms TTL=247
Reply from 10.227.90.124: bytes=32 time=5ms TTL=247
Reply from 10.227.90.124: bytes=32 time=3ms TTL=247
Reply from 10.227.90.124: bytes=32 time=3ms TTL=247

Ping statistics for 10.227.90.124:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
    Approximate round trip times in milli-seconds:
        Minimum = 2ms, Maximum = 5ms, Average = 3ms

C:\Users\jeeteshk>
```