Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process and Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology¹

Datasheet

2 GHz – 3.40 GHz Frequencies Supporting Hyper-Threading Technology¹ at 3.06 GHz with 533 MHz System Bus and All Frequencies with 800 MHz System Bus

- Available at 2 GHz, 2.20 GHz, 2.26 GHz, 2.40 GHz, 2.50 GHz, 2.53 GHz, 2.60 GHz, 2.66 GHz, 2.80 GHz, 3 GHz, 3.06 GHz, 3.20 GHz, and 3.40 GHz
- Supports Hyper-Threading Technology (HT Technology) at 3.06 GHz with 533 MHz system bus and all frequencies with 800 MHz system bus
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel NetBurst® microarchitecture
- System bus frequency at 400 MHz, 533 MHz, and 800 MHz
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper-Pipelined Technology
  — Advance Dynamic Execution
  — Very deep out-of-order execution
- Enhanced branch prediction
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- 8-KB Level 1 data cache
- Level 1 Execution Trace Cache stores 12-K micro-ops and removes decoder latency from main execution loops
- 512-KB Advanced Transfer Cache (on-die, full-speed Level 2 (L2) cache) with 8-way associativity and Error Correcting Code (ECC)
- 2-MB Integrated Level 3 (L3) cache with 8-way associativity that is supported by Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology
- 144 Streaming SIMD Extensions 2 (SSE2) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  — System Management mode
  — Multiple low-power states
- 8-way cache associativity provides improved cache hit rate on load/store operations
- 478-Pin Package

The Intel® Pentium® 4 processor family supporting Hyper-Threading Technology¹ (HT Technology) delivers Intel's most advanced, most powerful processors for desktop PCs and entry-level workstations, which are based on the Intel NetBurst® microarchitecture. The Pentium 4 processor is designed to deliver performance across applications and usages where end-users can truly appreciate and experience the performance. These applications include Internet audio and streaming video, image processing, video content creation, speech, 3D, CAD, games, multimedia, and multitasking user environments. The Intel® Pentium® 4 processor Extreme Edition supporting HT Technology features 2 MB of L3 cache and offers high levels of performance targeted specifically for high-end gamers and computing power users.
Contents

1 Introduction ..................................................................................................................9
  1.1 Terminology ...........................................................................................................11
  1.1.1 Processor Packaging Terminology .................................................................11
  1.2 References ...........................................................................................................12

2 Electrical Specifications ..............................................................................................15
  2.1 System Bus and GTLREF .....................................................................................15
  2.2 Power and Ground Pins .......................................................................................15
  2.3 Decoupling Guidelines .........................................................................................16
      2.3.1 VCC Decoupling .....................................................................................16
      2.3.2 System Bus AGTL+ Decoupling .............................................................16
  2.4 Voltage Identification ...........................................................................................16
      2.4.1 Phase Lock Loop (PLL) Power and Filter ...............................................18
  2.5 Reserved, Unused Pins, and TESTHI[12:0] ...........................................................20
  2.6 System Bus Signal Groups .................................................................................21
  2.7 Asynchronous GTL+ Signals ...............................................................................22
  2.8 Test Access Port (TAP) Connection .....................................................................22
  2.9 System Bus Frequency Select Signals (BSEL[1:0]) .............................................22
  2.10 Maximum Ratings ............................................................................................23
  2.11 Processor DC Specifications .............................................................................23
  2.12 AGTL+ System Bus Specifications ....................................................................35

3 Package Mechanical Specifications ..........................................................................37
  3.1 Package Load Specifications ..............................................................................40
  3.2 Processor Insertion Specifications .....................................................................41
  3.3 Processor Mass Specifications ...........................................................................41
  3.4 Processor Materials ............................................................................................41
  3.5 Processor Markings ............................................................................................42

4 Pin Lists and Signal Descriptions .............................................................................45
  4.1 Processor Pin Assignments .................................................................................45
  4.2 Signal Descriptions .............................................................................................58

5 Thermal Specifications and Design Considerations .................................................67
  5.1 Processor Thermal Specifications .......................................................................68
      5.1.1 Thermal Specifications ...........................................................................68
      5.1.2 Thermal Metrology .................................................................................70
          5.1.2.1 Processor Case Temperature Measurement .....................................70

6 Features .....................................................................................................................71
  6.1 Power-On Configuration Options ........................................................................71
  6.2 Clock Control and Low Power States .................................................................71
      6.2.1 Normal State—State 1 ...........................................................................71
      6.2.2 AutoHALT Powerdown State—State 2 .................................................72
      6.2.3 Stop-Grant State—State 3 .....................................................................73
      6.2.4 HALT/Grant Snoop State—State 4 .........................................................73
      6.2.5 Sleep State—State 5 ..............................................................................74
6.3 Thermal Monitor .................................................................................................. 74
6.3.1 Thermal Diode ............................................................................................ 76

7 Boxed Processor Specifications ......................................................................... 77
7.1 Introduction ....................................................................................................... 77
7.2 Mechanical Specifications ............................................................................... 78
  7.2.1 Boxed Processor Cooling Solution Dimensions ........................................ 78
  7.2.2 Boxed Processor Fan Heatsink Weight ..................................................... 79
  7.2.3 Boxed Processor Retention Mechanism and Heatsink Assembly ................ 79
7.3 Electrical Requirements .................................................................................. 80
  7.3.1 Fan Heatsink Power Supply ...................................................................... 80
7.4 Thermal Specifications ...................................................................................... 82
  7.4.1 Boxed Processor Cooling Requirements ................................................... 82
  7.4.2 Variable Speed Fan .................................................................................. 83

8 Debug Tools Specifications ............................................................................... 85
8.1 Logic Analyzer Interface (LAI) ........................................................................ 85
  8.1.1 Mechanical Considerations ...................................................................... 85
  8.1.2 Electrical Considerations .......................................................................... 85
Figures

2-1  $V_{CCVID}$ Pin Voltage and Current Requirements .................................................. 17
2-2  Typical VCCIOPLL, VCCA and VSSA Power Distribution .................................. 19
2-3  Phase Lock Loop (PLL) Filter Requirements ...................................................... 19
2-4  $V_{CC}$ Static and Transient Tolerance (For Intel® Pentium® 4 Processor With 512-KB L2 Cache on 0.13 Micron Process)............................... 29
2-5  $V_{CC}$ Static and Transient Tolerance (For Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology)............... 31
2-6  ITPCLKOUT[1:0] Output Buffer Diagram ............................................................... 34
2-7  Test Circuit ............................................................................................................ 35
3-1  Exploded View of Processor Components on a System Board ......................... 37
3-2  Processor Package ............................................................................................... 38
3-3  Processor Cross-Section and Keep-In .................................................................... 39
3-4  Processor Pin Detail ............................................................................................. 39
3-5  IHS Flatness Specification .................................................................................... 40
3-6  Processor Markings (Processors with Fixed VID) ................................................ 42
3-7  Processor Markings (Processors with Multiple VID) .......................................... 42
3-8  The Coordinates of the Processor Pins As Viewed from the Top of the Package ................................................................................................. 43
5-1  Example Thermal Solution (Not to Scale) ............................................................ 67
5-2  Guideline Locations for Case Temperature (TC) Thermocouple Placement .... 70
6-1  Stop Clock State Machine ................................................................................... 72
7-1  Mechanical Representation of the Boxed Processor ............................................ 77
7-2  Side View Space Requirements for the Boxed Processor ................................... 78
7-3  Top View Space Requirements for the Boxed Processor ................................... 79
7-4  Boxed Processor Fan Heatsink Power Cable Connector Description ............... 80
7-5  MotherBoard Power Header Placement Relative to Processor Socket ............ 81
7-6  Boxed Processor Fan Heatsink Airspace Keep-Out Requirements (Side 1 View) ................................................................................................. 82
7-7  Boxed Processor Fan Heatsink Airspace Keep-Out Requirements (Side 2 View) ................................................................................................. 83
7-8  Boxed Processor Fan Heatsink Set Points .............................................................. 83
Tables

1-1 References ................................................................................................................. 12
2-1 $V_{CCVID}$ Pin Voltage Requirements ................................................................. 17
2-2 Voltage Identification Definition ........................................................................ 18
2-3 System Bus Pin Groups ....................................................................................... 21
2-4 BSEL[1:0] Frequency Table for BCLK[1:0] ...................................................... 22
2-5 Processor DC Absolute Maximum Ratings ....................................................... 23
2-6 Voltage and Current Specifications ................................................................... 24
2-7 $V_{CC}$ Static and Transient Tolerance (For Intel® Pentium® 4
Processor With 512-KB L2 Cache on 0.13 Micron Process) ............................. 28
2-8 VCC Static and Transient Tolerance (For Intel® Pentium® 4
Processor Extreme Edition Supporting Hyper-Threading Technology) .......... 30
2-9 AGTL+ Signal Group DC Specifications ........................................................... 32
2-10 Asynchronous GTL+ Signal Group DC Specifications .................................... 32
2-11 PWRGOOD and TAP Signal Group DC Specifications .................................. 33
2-12 ITPCLKOUT[1:0] DC Specifications ................................................................. 33
2-13 BSEL [1:0] and VID[4:0] DC Specifications ..................................................... 34
2-14 AGTL+ Bus Voltage Definitions ........................................................................ 35
3-1 Description Table for Processor Dimensions .................................................... 38
3-2 Package Dynamic and Static Load Specifications .............................................. 40
3-3 Processor Mass .................................................................................................. 41
3-4 Processor Material Properties ............................................................................ 41
4-1 Pin Listing by Pin Name ...................................................................................... 46
4-2 Pin Listing by Pin Number ................................................................................... 52
4-3 Signal Descriptions ............................................................................................. 58
5-1 Processor Thermal Design Power ...................................................................... 69
6-1 Power-On Configuration Option Pins ............................................................... 71
6-2 Thermal Diode Parameters ............................................................................... 76
6-3 Thermal Diode Interface .................................................................................... 76
7-1 Fan Heatsink Power and Signal Specifications ................................................. 81
7-2 Boxed Processor Fan Heatsink Set Points ....................................................... 84
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>-005</td>
<td>Added Thermal and Electrical Specifications for frequencies through 3.06 GHz and included multiple VID specifications. Updated the THERMTRIP# and DBI# signal descriptions. Removed Deep Sleep State section. Updated Boxed Processor Fan Heatsink Set Points table and figure. Update Power-on Configuration Option pins table.</td>
<td>November 2002</td>
</tr>
<tr>
<td>-006</td>
<td>Minor update to DC specifications</td>
<td>December 2002</td>
</tr>
<tr>
<td>-007</td>
<td>Corrected Table 4-3, Signal Description. Item TRST#, last sentence. Measurement changed from 680 W pull-down resistor to 680 Ω pull-down resistor.</td>
<td>January 2003</td>
</tr>
<tr>
<td>-008</td>
<td>Added 800 MHz system bus specifications. Added IMPSEL definition. Updated Stop-Grant, HALT, and AutoHALT states</td>
<td>April 2003</td>
</tr>
<tr>
<td>-009</td>
<td>Added thermal and electrical specifications for 2.40C GHz, 2.60C GHz, and 2.80C GHz with 800 MHz system bus. Updated thermal specifications and thermal monitor chapter. Updated PROCHOT# pin definition.</td>
<td>May 2003</td>
</tr>
<tr>
<td>-010</td>
<td>Added thermal and electrical specifications for 3.20C GHz. Updated processor markings.</td>
<td>June 2003</td>
</tr>
<tr>
<td>-012</td>
<td>Added 3.40 GHz thermal and electrical specifications for the Intel Pentium 4 Processor Extreme Edition and Intel Pentium 4 Processor with 512-KB L2 Cache on 0.13 Micron Process</td>
<td>February 2004</td>
</tr>
</tbody>
</table>
This page is intentionally left blank.
The Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process and the Intel® Pentium® 4 processor Extreme Edition supporting Hyper-Threading Technology are follow-on processors to the Intel® Pentium® 4 processor in the 478-pin package with Intel NetBurst® microarchitecture. These processors use Flip-Chip Pin Grid Array (FC-PGA2) package technology, and plug into a 478-pin surface mount, Zero Insertion Force (ZIF) socket, referred to as the mPGA478B socket. The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology, like the Pentium 4 processor in the 478-pin package, are based on the same Intel 32-bit microarchitecture and maintain the tradition of compatibility with IA-32 software. The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process contains an on-die 512-KB advanced transfer L2 cache. The Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology contains an on-die 512-KB level 2 (L2) advanced transfer cache and an on-die 2-MB integrated level 3 (L3) cache. Both processors are on a 0.13 micron process.

This document covers the Pentium 4 processors with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology.

**Note:** Unless otherwise specified in this document, the term “Pentium 4 processor on 0.13 micron process” (or simply processor) refers to both the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology.

Hyper-Threading Technology\(^1\) is a new feature in the Pentium 4 processor on 0.13 micron process at 800 MHz system bus. It is also on the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process at 3.06 GHz/533 MHz system bus. HT Technology allows a single, physical Pentium 4 processor on 0.13 micron process to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architecture state with its own set of general-purpose registers, control registers to provide increased system responsiveness in multitasking environments, and headroom for next generation multi-threaded applications. Intel recommends enabling HT Technology with Microsoft Windows® XP Professional or Windows® XP Home, and disabling HT Technology via the BIOS for all previous versions of Windows operating systems. For more information on Hyper-Threading Technology, see [www.intel.com/info/hyperthreading](http://www.intel.com/info/hyperthreading). Refer to [Section 6.1](#) for HT Technology configuration details.

The Intel NetBurst microarchitecture features include hyper-pipelined technology, a rapid execution engine, a 400 MHz, 533 MHz, or 800 MHz system bus, and an execution trace cache. The hyper-pipelined technology doubles the pipeline depth in the Pentium 4 processor on 0.13 micron process, allowing the processor to reach much higher core frequencies. The rapid execution engine allows the two integer ALUs in the processor to run at twice the core frequency; this allows many integer instructions to execute in 1/2 clock cycle. The 400 MHz, 533 MHz, or 800 MHz system bus is a quad-pumped bus running off a 100 MHz or a 133 MHz system clock, making 3.2 Gbytes/sec, 4.3 Gbytes/sec, or 6.4 Gbytes/sec data transfer rates possible. The execution trace cache is a first-level cache that stores approximately 12-K decoded micro-operations that removes the instruction decoding logic from the main execution path, thereby increasing performance.
Additional features within the Intel NetBurst microarchitecture include advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 512-KB, on-die level 2 (L2) cache. A new floating point and multi-media unit has been implemented that provides superior performance for multi-media and mathematically intensive applications. Finally, SSE2 adds 144 new instructions for double-precision floating point, SIMD integer, and memory management. Power management capabilities (such as AutoHALT, Stop-Grant, and Sleep) have been retained.

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multi-media applications including 3-D graphics, video decoding/encoding, and speech recognition. The new packed double-precision floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3-D geometry techniques (such as ray tracing).

The 2-MB L3 cache is available with only the Pentium 4 processor Extreme Edition. The additional third level of cache is located on the processor die and is designed specifically to meet the compute needs of high-end gamers and other power users. The integrated level 3 cache is available in 2-MB and is coupled with the 800 MHz system bus to provide a high bandwidth path to memory. The efficient design of the integrated Level 3 cache provides a faster path to large data sets stored in cache on the processor. This results in reduced average memory latency and increased throughput for larger workloads.

The Intel NetBurst microarchitecture system bus on the Pentium 4 processor on 0.13 micron process uses a split-transaction, deferred reply protocol like the Pentium 4 processor in the 478-pin package. This system bus is not compatible with the P6 processor family bus. The Intel NetBurst microarchitecture system bus uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a “double-clocked” or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 6.4 Gbytes/second.

Intel will enable support components for the Pentium 4 processor on 0.13 micron process including heatsinks, heatsink retention mechanisms, and sockets. Manufacturability is a high priority; hence, mechanical assembly can be completed from the top of the motherboard, and should not require any special tooling.

The processor system bus uses a variant of GTL+ signalling technology called Assisted Gunning Transceiver Logic (AGTL+) signal technology.
1.1 Terminology

A ‘#’ symbol after a signal name refers to an active low signal, indicating that the signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as address or data), the ‘#’ symbol indicates that the signal is inverted. For example, \( D[3:0] = 'HLHL' \) refers to a hex ‘A’, and \( D[3:0]# = 'LHLH' \) also refers to a hex ‘A’ (H= High logic level, L= Low logic level).

The term “System Bus” refers to the interface between the processor and system core logic (also known as the chipset components). The system bus is a multiprocessing interface to processors, memory, and I/O.

1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- **Intel Pentium 4 processor in the 478-pin package** — 0.18-micron Pentium 4 processor core in the FC-PGA2 package.
- **Intel Pentium 4 processor in the 423-pin package** — 0.18-micron Pentium 4 processor core in the PGA package.
- **Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process** — 0.13 micron version of Pentium 4 processor in the 478-pin package core in the FC-PGA2 package with a 512-KB L2 cache.
- **Intel Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology** — 0.13 micron version of Pentium 4 processor in the 478-pin package core in the FC-PGA2 package with a 512-KB L2 cache and a 2-MB L3 cache.
- **Processor** — For this document, the term processor shall mean Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology.
- **Keep-out zone** — The area on or near the processor that system design can not utilize. This area must be kept free of all components to make room for the processor package, retention mechanism, heatsink, and heatsink clips.
- **Hyper-Threading Technology** — Hyper-Threading Technology allows a single, physical Pentium 4 processor to function as two logical processors when the necessary system ingredients are present. For more information, see: www.intel.com/info/hyperthreading.
- **Intel® 875P chipset** — Chipset that supports DDR memory technology for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process. This chipset also supports the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology in platforms that meet the thermal design guidelines for this processor.
- **Intel® 865G/865GV/865PE chipset** — Chipset that supports DDR memory technology for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
- **Intel® 865P chipset** — Chipset that supports DDR memory technology for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.
- **Intel® 850 chipset** — Chipset that supports Rambus RDRAM* memory technology for Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and Pentium 4 processor in the 478-pin package.
- **Intel® 845 chipset** — Chipset that supports PC133 and DDR memory technologies for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and Pentium 4 processor in the 478-pin package.
Introduction

- **Processor core** — Pentium 4 processor with 512-KB L2 cache on 0.13 micron process core die with integrated L2 cache and the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology core die with integrated L2 and L3 caches.
- **FC-PGA2 package** — Flip-Chip Pin Grid Array package with 50-mil pin pitch and integrated heat spreader.
- **mPGA478B socket** — Surface mount, 478 pin, Zero Insertion Force (ZIF) socket with 50-mil pin pitch. The socket mates the processor to the system board.
- **Integrated heat spreader** — The surface used to make contact between a heatsink or other thermal solution and the processor. Integrated heat spreader is abbreviated IHS.
- **Retention mechanism** — The structure mounted on the system board that provides support and retention of the processor heatsink.

### 1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

**Table 1-1. References (Sheet 1 of 2)**

<table>
<thead>
<tr>
<th>Document</th>
<th>Location</th>
</tr>
</thead>
</table>
## Table 1-1. References (Sheet 2 of 2)

<table>
<thead>
<tr>
<th>Document</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Architecture</td>
<td></td>
</tr>
<tr>
<td>Instruction Set Reference</td>
<td></td>
</tr>
<tr>
<td>System Programming Guide</td>
<td></td>
</tr>
</tbody>
</table>
This page is intentionally left blank.
2.1 System Bus and GTLREF

Most Pentium 4 processor on 0.13 micron process system bus signals use Assisted Gunning Transceiver Logic (AGTL+) signalling technology. As with the P6 family of microprocessors, this signalling technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. Like the Pentium 4 processor in the 478-pin package, the termination voltage level for the Pentium 4 processor on 0.13 micron process AGTL+ signals is $V_{CC}$, which is the operating voltage of the processor core. The use of a termination voltage that is determined by the processor core allows better voltage scaling on the system bus for the Pentium 4 processor on 0.13 micron process. Because of the speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families. Design guidelines for the Pentium 4 processor on 0.13 micron process system bus are detailed in the appropriate platform design guide (refer to Table 1-1).

The AGTL+ inputs require a reference voltage (GTLREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board.

Termination resistors are provided on the processor silicon and are terminated to its core voltage ($V_{CC}$). The Intel® 875P chipset, Intel® 865G/865GV/865PE/865P chipsets, Intel® 850 chipset, and the Intel® 845 chipset also provide on-die termination. This eliminates the need to terminate the bus on the system board for most AGTL+ signals. However, some AGTL+ signals do not include on-die termination and must be terminated on the system board. For more information, refer to the appropriate platform design guide.

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus, including trace lengths, is highly recommended when designing a system. For more information, refer to the appropriate platform design guide.

2.2 Power and Ground Pins

For clean on-chip power distribution, the Pentium 4 processor on 0.13 micron process has 85 VCC (power) and 180 VSS (ground) inputs. All power pins must be connected to $V_{CC}$, while all $V_{SS}$ pins must be connected to a system ground plane. The processor VCC pins must be supplied with the voltage defined by the VID (Voltage ID) pins and the loadline specifications (see Figure 2-4).
2.3 Decoupling Guidelines

Because of the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 2-6. Failure to do so can result in timing violations and/or affect the long term reliability of the processor. For further information and design guidelines, refer to the appropriate platform design guide and the Intel® Pentium® 4 Processor VR-Down Design Guidelines.

2.3.1 VCC Decoupling

VCC regulator solutions need to provide sufficient decoupling capacitance to satisfy processor voltage specifications. This includes bulk capacitance with low effective series resistance (ESR) to keep the voltage rail within specifications during large swings in load current. In addition, ceramic decoupling capacitors are required to filter high frequency content generated by bus and processor activity. Consult the Voltage Regulator Down design guide and appropriate platform design guide for further information.

2.3.2 System Bus AGTL+ Decoupling

Pentium 4 processors on 0.13 micron process integrate signal termination on the die and incorporate high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system motherboard for proper AGTL+ bus operation. For more information, refer to the appropriate platform design guide.

2.4 Voltage Identification

The VID specification for Pentium 4 processors on 0.13 micron process is supported by the Intel® Pentium® 4 Processor VR-Down Design Guidelines, Voltage Regulator-Down (VRD) 10.0 Design Guide, and Voltage Regulator-Down (VRD) 10.0 Design Guide Addendum. The voltage set by the VID pins is the maximum voltage allowed by the processor. A minimum voltage is provided in Table 2-6 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can work with all supported frequencies.

Pentium 4 processors on 0.13 micron process use five voltage identification pins, VID[4:0], to support automatic selection of power supply voltages. The VID pins for the Pentium 4 processor on 0.13 micron process are open drain outputs driven by the processor VID circuitry. The VID signals rely on pull-up resistors tied to a 3.3 V (maximum) supply to set the signal to a logic high level. These pull-up resistors may be either external logic on the motherboard, or internal to the Voltage Regulator. Table 2-2 specifies the voltage level corresponding to the state of VID[4:0]. A ‘1’ in this table refers to a high voltage level, and a ‘0’ refers to low voltage level. The definition provided in Table 2-2 is not related in any way to previous P6 processors or VRs, but is compatible with the Pentium 4 processor in the 478-pin package. If the processor socket is empty (VID[4:0] = 11111) or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself. See the Intel® Pentium® 4 Processor VR-Down Design Guidelines, Voltage Regulator-Down (VRD) 10.0 Design Guide, or Voltage Regulator-Down (VRD) 10.0 Design Guide Addendum for more details.
Power source characteristics must be stable when the supply to the voltage regulator is stable. Refer to the appropriate platform design guide for timing details of the power up sequence. Refer to the appropriate platform design guide for implementation details.

The Voltage Identification circuit requires an independent 1.2 V supply. This voltage must be routed to the processor V\textsubscript{CCVID} pin. Figure 2-1 and Table 2-1 show the voltage and current requirements of the V\textsubscript{CCVID} pin.

### Table 2-1. V\textsubscript{CCVID} Pin Voltage Requirements

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{CCVID}</td>
<td>V\textsubscript{CC} for Voltage Identification circuit</td>
<td>–5%</td>
<td>1.2</td>
<td>+10%</td>
<td>V</td>
<td>1</td>
</tr>
</tbody>
</table>

**NOTE:**
1. This specification applies to both static and transient components. The rising edge of V\textsubscript{CCVID} must be monotonic from 0 to 1.1 V. See Figure 2-1 for current requirements. In this case, monotonic is defined as continuously increasing with less than 50 mV of peak to peak noise for any width greater than 2 ns superimposed on the rising edge.

**Figure 2-1. V\textsubscript{CCVID} Pin Voltage and Current Requirements**

![V\textsubscript{CCVID} Pin Voltage and Current Requirements Diagram]
2.4.1 Phase Lock Loop (PLL) Power and Filter

$V_{CCA}$ and $V_{CCIPLL}$ are power sources required by the PLL clock generators on the Pentium 4 processor on 0.13 micron process. Since these PLLs are analog, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system; it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from $V_{CC}$. A typical filter topology is shown in Figure 2-2.

The AC low-pass requirements, with input at $V_{CC}$ and output measured across the capacitor ($C_A$ or $C_{IO}$ in Figure 2-2), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

Refer to the appropriate platform design guide for recommendations on implementing the filter.
NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond fcore (core frequency).
3. fpeak, if existent, should be less than 0.05 MHz.
2.5 Reserved, Unused Pins, and TESTHI[12:0]

All RESERVED pins must remain unconnected. Connection of these pins to $V_{CC}$, $V_{SS}$, or to any other signal (including each other) can result in component malfunction or incompatibility with future Pentium 4 processors on 0.13 micron process. See Chapter 4 for a pin listing of the processor and the location of all RESERVED pins.

For reliable operation, always connect unused inputs or bidirectional signals that are not terminated on the die to an appropriate signal level. Note that on-die termination has been included on the Pentium 4 processor on 0.13 micron process to allow signals to be terminated within the processor silicon. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Table 2-3 lists details on AGTL+ signals that do not include on-die termination. Unused active high inputs should be connected through a resistor to ground ($V_{SS}$). Refer to the appropriate platform design guide for the appropriate resistor values.

Unused outputs can be left unconnected. However, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused AGTL+ input or I/O signals that don’t have on-die termination, use pull-up resistors of the same value in place of the on-die termination resistors (RTT). See Table 2-14.

The TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and used outputs must be terminated on the system board. Unused outputs may be terminated on the system board or left unconnected. Note that leaving unused output unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the appropriate platform design guide listed in Table 1-1.

The TESTHI pins should be tied to the processor $V_{CC}$ using a matched resistor, where a matched resistor has a resistance value within $\pm$ 20% of the impedance of the board transmission line traces. For example, if the trace impedance is 50 $\Omega$, then a value between 40 $\Omega$ and 60 $\Omega$ is required.

The TESTHI pins may use individual pull-up resistors or may be grouped together as follows:

1. TESTHI[1:0]
2. TESTHI[5:2]
3. TESTHI[10:8]
4. TESTHI[12:11]

A matched resistor should be used for each group.

Additionally, if the ITPCLKOUT[1:0] pins are not used, they may be connected individually to $V_{CC}$ using matched resistors or may be grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1 k$\Omega$ resistors is required. Tying ITPCLKOUT[1:0] directly to $V_{CC}$ or sharing a pull-up resistor to $V_{CC}$ will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an inboard debug port.

As an alternative, group2 (TESTHI[5:2]) and the ITPCLKOUT[1:0] pins may be tied directly to the processor $V_{CC}$. This has no impact on system functionality. TESTHI0 and TESTHI12 may also be tied directly to the processor $V_{CC}$ if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0] pins, direct tie to $V_{CC}$ is strongly discouraged for system boards that do not implement an inboard debug port.

Tying any of the TESTHI pins together will prevent the ability to perform boundary scan testing.
2.6 System Bus Signal Groups

To simplify the following discussion, the system bus signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers that use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals that are dependent on the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.), and the second set is for the source synchronous signals that are relative to their respective strobe lines (data and address), as well as the rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 2-3 identifies which signals are common clock, source synchronous, and asynchronous signals.

### Table 2-3. System Bus Pin Groups

<table>
<thead>
<tr>
<th>Signal Group</th>
<th>Type</th>
<th>Associated Strobe</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGTL+ Common Clock Input</td>
<td>Common Clock</td>
<td>BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#</td>
</tr>
<tr>
<td>AGTL+ Common Clock I/O</td>
<td>Synchronous</td>
<td>AP[1:0]#, ADS#, BINIT#, BRN#, BPM[5:0]#, BR0#, DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#</td>
</tr>
<tr>
<td>AGTL+ Strobes</td>
<td>Common Clock</td>
<td>ADSTB0#, ADSTB1#</td>
</tr>
<tr>
<td>Asynchronous GTL+ Input4,5</td>
<td>Asynchronous</td>
<td>A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, STPCLK#</td>
</tr>
<tr>
<td>Asynchronous GTL+ Output4</td>
<td>Asynchronous</td>
<td>FERR#, IERR#², THERMTRIP#</td>
</tr>
<tr>
<td>Asynchronous GTL+ Input/ Output4</td>
<td>Asynchronous</td>
<td>PROCHOT#</td>
</tr>
<tr>
<td>TAP Input4</td>
<td>Synchronous to TCK</td>
<td>TCK, TDI, TMS, TRST#</td>
</tr>
<tr>
<td>TAP Output4</td>
<td>Synchronous to TCK</td>
<td>TDO</td>
</tr>
<tr>
<td>System Bus Clock</td>
<td>N/A</td>
<td>BCLK[1:0], ITP_CLK[1:0]²</td>
</tr>
<tr>
<td>Power/Other</td>
<td>N/A</td>
<td>VCC, VCCA, VCCIOPLL, VCCVID, VID[4:0], VSS, VSSA, GTLREF[3:0], COMP[1:0], RESERVED, TESTH[5:0, 12:8], ITPCLKOUT[1:0], THERMDA, THERMDC, IMPSEL, DBR#, PWRGOOD, SKTOCC#, VCCSense, VSSSense, BSEL[1:0],</td>
</tr>
</tbody>
</table>

NOTES:
1. Refer to Section 5.2 for signal descriptions.
2. These AGTL+ signals do not have on-die termination. Refer to Section 2.5 and the ITP700 Debug Port Design Guide for termination requirements.
3. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
4. These signal groups are not terminated by the processor. Refer to Section 2.5, the ITP700 Debug Port Design Guide, and the appropriate Platform Design Guide for termination requirements and further details.
5. The value of these pins during the active-to-inactive edge of RESET# defines the processor configuration options. See Section 6.1 for details.
2.7 Asynchronous GTL+ Signals

The Pentium 4 processor on 0.13 micron process does not use CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals (such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK#) use GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP#) use GTL+ output buffers. PROCHOT# uses GTL+ input/output buffer. All of these signals follow the same DC requirements as AGTL+ signals; however, the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs for the processor to recognize them. See Section 2.11 for the DC specifications for the Asynchronous GTL+ signal groups. See Section 6.2 for additional timing requirements for entering and leaving the low power states.

2.8 Test Access Port (TAP) Connection

Because of the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Pentium 4 processor on 0.13 micron process be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage level. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required, with each driving a different voltage level.

2.9 System Bus Frequency Select Signals (BSEL[1:0])

The BSEL[1:0] are output signals used to select the frequency of the processor input clock (BCLK[1:0]). Table 2-4 defines the possible combinations of the signals, and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency.

The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process currently operates at a 400 MHz, 533 MHz, or 800 MHz system bus frequency. The Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology currently operates at 800 MHz system bus frequency. Individual processors will operate only at their specified system bus frequency.

For more information about these pins, refer to Section 4.2 and the appropriate platform design guidelines.

Table 2-4. BSEL[1:0] Frequency Table for BCLK[1:0]

<table>
<thead>
<tr>
<th>BSEL1</th>
<th>BSEL0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>100 MHz</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>133 MHz</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>200 MHz</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>RESERVED</td>
</tr>
</tbody>
</table>
2.10 Maximum Ratings

Table 2-5 lists the processor’s maximum environmental stress ratings. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from Electro Static Discharge (ESD), one should always take precautions to avoid high static voltages or electric fields.

Table 2-5. Processor DC Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSTORAGE</td>
<td>Processor storage temperature</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
<td>2</td>
</tr>
<tr>
<td>VCC</td>
<td>Any processor supply voltage with respect to VSS</td>
<td>–0.3</td>
<td>1.75</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>VinAGTL+</td>
<td>AGTL+ buffer DC input voltage with respect to VSS</td>
<td>–0.1</td>
<td>1.75</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VinAsynch_GTL+</td>
<td>Asynch GTL+ buffer DC input voltage with respect to VSS</td>
<td>–0.1</td>
<td>1.75</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IVID</td>
<td>Max VID pin current</td>
<td>5</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. This rating applies to any processor pin.
2. Contact Intel for storage requirements in excess of one year.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core silicon unless noted otherwise. See Chapter 4 for the pin signal definitions and signal pin assignments. Most of the signals on the processor system bus are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 2-9.

Previously, legacy signals and Test Access Port (TAP) signals to the processor used low-voltage CMOS buffer types. However, these interfaces now follow DC specifications similar to GTL+. The DC specifications for these signal groups are listed in Table 2-10.

Table 2-6 through Table 2-10 list the DC specifications for the Pentium 4 processor on 0.13 micron process, and are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Processors with multiple VID have I_{CC_MAX} of the highest VID for the specified frequency. For example, for processors through 2.80 GHz, the I_{CC_MAX} would be the one at VID=1.525 V.
## Electrical Specifications

### Table 2-6. Voltage and Current Specifications (Sheet 1 of 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Notes^10</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{CC}</td>
<td>V\text{CC} for Processor at V\text{ID}=1.475 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2A GHz</td>
<td>1.315</td>
<td></td>
<td></td>
<td>1.390</td>
<td>V</td>
<td>1, 2, 3, 4</td>
</tr>
<tr>
<td>2.20 GHz</td>
<td>1.310</td>
<td></td>
<td></td>
<td>1.385</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.40 GHz</td>
<td>1.300</td>
<td></td>
<td></td>
<td>1.380</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.50 GHz</td>
<td>1.300</td>
<td></td>
<td></td>
<td>1.375</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.60 GHz</td>
<td>1.295</td>
<td></td>
<td></td>
<td>1.375</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V\text{CC} for Processor at V\text{ID}=1.500 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2A GHz</td>
<td>1.340</td>
<td></td>
<td></td>
<td>1.415</td>
<td>V</td>
<td>Refer to Table 2-7 and Figure 2-4</td>
</tr>
<tr>
<td>2.20 GHz</td>
<td>1.335</td>
<td></td>
<td></td>
<td>1.410</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.40 GHz</td>
<td>1.330</td>
<td></td>
<td></td>
<td>1.405</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.50 GHz</td>
<td>1.325</td>
<td></td>
<td></td>
<td>1.400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.60 GHz</td>
<td>1.320</td>
<td></td>
<td></td>
<td>1.400</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V\text{CC} for Processor at V\text{ID}=1.525 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2A GHz</td>
<td>1.365</td>
<td></td>
<td></td>
<td>1.440</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>2.20 GHz</td>
<td>1.360</td>
<td></td>
<td></td>
<td>1.435</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.40 GHz</td>
<td>1.350</td>
<td></td>
<td></td>
<td>1.430</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.50 GHz</td>
<td>1.350</td>
<td></td>
<td></td>
<td>1.430</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.60 GHz</td>
<td>1.345</td>
<td></td>
<td></td>
<td>1.425</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V\text{CC} for Processor at V\text{ID}=1.475 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.26 GHz</td>
<td>1.305</td>
<td></td>
<td></td>
<td>1.380</td>
<td>V</td>
<td>1, 2, 3, 4</td>
</tr>
<tr>
<td>2.408 GHz</td>
<td>1.300</td>
<td></td>
<td></td>
<td>1.380</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.53 GHz</td>
<td>1.295</td>
<td></td>
<td></td>
<td>1.375</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.66 GHz</td>
<td>1.295</td>
<td></td>
<td></td>
<td>1.370</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.80 GHz</td>
<td>1.290</td>
<td></td>
<td></td>
<td>1.370</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.06 GHz</td>
<td>1.265</td>
<td></td>
<td></td>
<td>1.345</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V\text{CC} for Processor at V\text{ID}=1.500 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.26 GHz</td>
<td>1.330</td>
<td></td>
<td></td>
<td>1.405</td>
<td>V</td>
<td>Refer to Table 2-7 and Figure 2-4</td>
</tr>
<tr>
<td>2.408 GHz</td>
<td>1.330</td>
<td></td>
<td></td>
<td>1.405</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.53 GHz</td>
<td>1.325</td>
<td></td>
<td></td>
<td>1.400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.66 GHz</td>
<td>1.320</td>
<td></td>
<td></td>
<td>1.395</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.80 GHz</td>
<td>1.315</td>
<td></td>
<td></td>
<td>1.395</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.06 GHz</td>
<td>1.290</td>
<td></td>
<td></td>
<td>1.370</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V\text{CC} for Processor at V\text{ID}=1.525 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.26 GHz</td>
<td>1.355</td>
<td></td>
<td></td>
<td>1.435</td>
<td>V</td>
<td>1, 2, 3, 4</td>
</tr>
<tr>
<td>2.408 GHz</td>
<td>1.350</td>
<td></td>
<td></td>
<td>1.430</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.53 GHz</td>
<td>1.345</td>
<td></td>
<td></td>
<td>1.430</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.66 GHz</td>
<td>1.345</td>
<td></td>
<td></td>
<td>1.420</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.80 GHz</td>
<td>1.340</td>
<td></td>
<td></td>
<td>1.420</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.06 GHz</td>
<td>1.315</td>
<td></td>
<td></td>
<td>1.395</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V\text{CC} for Processor at V\text{ID}=1.550 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.06 GHz</td>
<td>1.340</td>
<td></td>
<td></td>
<td>1.425</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Electrical Specifications**

### Table 2-6. Voltage and Current Specifications (Sheet 2 of 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc for Processor at VID=1.475 V</td>
<td>2.40 GHz</td>
<td>1.295</td>
<td>1.375</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.60 GHz</td>
<td>1.290</td>
<td>1.370</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.80 GHz</td>
<td>1.288</td>
<td>1.369</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 GHz</td>
<td>1.265</td>
<td>1.350</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.20 GHz</td>
<td>1.260</td>
<td>1.345</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.40 GHz</td>
<td>1.280</td>
<td>1.350</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vcc for Processor at VID=1.500 V</td>
<td>2.40 GHz</td>
<td>1.320</td>
<td>1.400</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.60 GHz</td>
<td>1.315</td>
<td>1.395</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.80 GHz</td>
<td>1.313</td>
<td>1.394</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 GHz</td>
<td>1.290</td>
<td>1.375</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.20 GHz</td>
<td>1.285</td>
<td>1.370</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.40 GHz</td>
<td>1.305</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vcc for Processor at VID=1.525 V</td>
<td>2.40 GHz</td>
<td>1.345</td>
<td>1.425</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.60 GHz</td>
<td>1.340</td>
<td>1.420</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.80 GHz</td>
<td>1.338</td>
<td>1.419</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 GHz</td>
<td>1.315</td>
<td>1.400</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.20 GHz</td>
<td>1.310</td>
<td>1.395</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.40 GHz</td>
<td>1.330</td>
<td>1.400</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vcc for Processor at VID=1.550 V</td>
<td>3 GHz</td>
<td>1.340</td>
<td>1.425</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.20 GHz</td>
<td>1.335</td>
<td>1.420</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.40 GHz</td>
<td>1.355</td>
<td>1.425</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vcc for Processor at VID=1.575 V</td>
<td>3.40 GHz</td>
<td>1.375</td>
<td>1.430</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.40 GHz</td>
<td>1.400</td>
<td>1.455</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vcc for Processor at VID=1.600 V</td>
<td>3.40 GHz</td>
<td>1.400</td>
<td>1.455</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.40 GHz</td>
<td>1.375</td>
<td>1.430</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VccVID</td>
<td>VCC for voltage identification circuit</td>
<td>–5%</td>
<td>1.2</td>
<td>+10%</td>
<td>V</td>
<td>9</td>
</tr>
</tbody>
</table>

Refer to Table 2-7, Figure 2-4, and Table 2-8, Figure 2-5.

V 1, 2, 3, 4, 13
### Table 2-6. Voltage and Current Specifications (Sheet 3 of 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Notes&lt;sup&gt;10&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>for Processor at VID=1.500 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2A GHz</td>
<td>44.3</td>
<td>47.1</td>
<td>49.8</td>
<td>51.3</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>for Processor at VID=1.525 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2A GHz</td>
<td>45.1</td>
<td>47.9</td>
<td>50.7</td>
<td>52.0</td>
<td>53.5</td>
</tr>
<tr>
<td>ICC</td>
<td>for Processor with multiple VIDs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2A GHz</td>
<td>45.1</td>
<td>47.9</td>
<td>50.7</td>
<td>52.0</td>
<td>53.5</td>
</tr>
<tr>
<td>ICC</td>
<td>for Processor at VID=1.500 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.26 GHz</td>
<td>48</td>
<td>49.8</td>
<td>51.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>for Processor at VID=1.525 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.26 GHz</td>
<td>48.6</td>
<td>50.7</td>
<td>52.5</td>
<td>53.9</td>
<td>55.9</td>
</tr>
<tr>
<td>ICC</td>
<td>for Processor with multiple VIDs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.26 GHz</td>
<td>48.6</td>
<td>50.7</td>
<td>52.5</td>
<td>53.9</td>
<td>55.9</td>
</tr>
<tr>
<td>ICC</td>
<td>for Processor with multiple VIDs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.40C GHz</td>
<td>52.4</td>
<td>55.0</td>
<td>55.9</td>
<td></td>
<td>3,4,6,10</td>
</tr>
<tr>
<td>ICC</td>
<td>(800 MHz FSB with 512-KB L2 Cache Only)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.20 GHz</td>
<td>71.5</td>
<td>77.7</td>
<td>A</td>
<td>4,6,10,13</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>for Processor with multiple VIDs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.40 GHz</td>
<td>71.5</td>
<td>77.7</td>
<td>A</td>
<td>4,6,10,13</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>(800 MHz FSB with 2-MB L3 Cache)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<sup>10</sup> Note: Additional notes may be provided in the datasheet.
NOTES:
1. These voltages are targets only. A variable voltage source should exist on systems in the event that a
different voltage is required. See Table 2-2 for more information. The VID bits will set the maximum V CC with
the minimum being defined according to current consumption at that voltage.
2. The voltage specification requirements are measured across V CC_SENSE and V SS_SENSE pins at the socket
with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum
impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external
noise from the system is not coupled in the scope probe.
3. Refer to Table 2-7 and Figure 2-4 for the minimum, typical, and maximum V CC allowed for a given current.
The processor should not be subjected to any V CC and I CC combination wherein V CC exceeds V CC_MAX for a
given current. Failure to adhere to this specification can affect the long term reliability of the processor.
4. V CC_MIN is defined at I CC_MAX.
5. The current specified is also for AutoHALT State.
6. The maximum instantaneous current that the processor will draw while the thermal control circuit is active as
indicated by the assertion of PROCHOT# is the same as the maximum I CC for the processor.
7. I CC Stop-Grant and I CC Sleep are specified at V CC_MAX.
8. These specifications apply to the processor with maximum VID setting of 1.525 V for the Pentium 4
processor with 512-KB L2 cache on 0.13 micron process.
9. This specification applies to processors with maximum VID setting of 1.550 V for the Pentium 4 processor
Extreme Edition supporting Hyper-Threading Technology.
10. Refer to Table 2-8 and Figure 2-5 for the minimum, typical, and maximum V CC allowed for a given current.
The processor should not be subjected to any V CC and I CC combination wherein V CC exceeds V CC_MAX for a
given current. Failure to adhere to this specification can affect the long term reliability of the processor.
11. These specifications apply to processors with maximum VID setting of 1.550 V for the Pentium 4 processor
Extreme Edition supporting Hyper-Threading Technology.
## Electrical Specifications

### Table 2-7. $V_{CC}$ Static and Transient Tolerance (For Intel® Pentium® 4 Processor With 512-KB L2 Cache on 0.13 Micron Process at Frequencies up to and Including 3.2 GHz)

<table>
<thead>
<tr>
<th>Icc (A)</th>
<th>Maximum</th>
<th>Typical</th>
<th>Minimum</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.000</td>
<td>−0.025</td>
<td>−0.050</td>
</tr>
<tr>
<td>5</td>
<td>−0.010</td>
<td>−0.036</td>
<td>−0.062</td>
</tr>
<tr>
<td>10</td>
<td>−0.019</td>
<td>−0.047</td>
<td>−0.075</td>
</tr>
<tr>
<td>15</td>
<td>−0.029</td>
<td>−0.058</td>
<td>−0.087</td>
</tr>
<tr>
<td>20</td>
<td>−0.038</td>
<td>−0.069</td>
<td>−0.099</td>
</tr>
<tr>
<td>25</td>
<td>−0.048</td>
<td>−0.079</td>
<td>−0.111</td>
</tr>
<tr>
<td>30</td>
<td>−0.057</td>
<td>−0.090</td>
<td>−0.124</td>
</tr>
<tr>
<td>35</td>
<td>−0.067</td>
<td>−0.101</td>
<td>−0.136</td>
</tr>
<tr>
<td>40</td>
<td>−0.076</td>
<td>−0.112</td>
<td>−0.148</td>
</tr>
<tr>
<td>45</td>
<td>−0.085</td>
<td>−0.123</td>
<td>−0.160</td>
</tr>
<tr>
<td>50</td>
<td>−0.095</td>
<td>−0.134</td>
<td>−0.173</td>
</tr>
<tr>
<td>55</td>
<td>−0.105</td>
<td>−0.145</td>
<td>−0.185</td>
</tr>
<tr>
<td>60</td>
<td>−0.114</td>
<td>−0.156</td>
<td>−0.197</td>
</tr>
<tr>
<td>65</td>
<td>−0.124</td>
<td>−0.166</td>
<td>−0.209</td>
</tr>
<tr>
<td>70</td>
<td>−0.133</td>
<td>−0.177</td>
<td>−0.222</td>
</tr>
</tbody>
</table>

**NOTES:**
1. The loadline specifications include both static and transient limits.
2. This table is intended to aid in reading discrete points on the following loadline figure.
3. The loadlines specify voltage limits at the die measured at $V_{CC\_SENSE}$ and $V_{SS\_SENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor $V_{CC}$ and $V_{SS}$ pins. Refer to the Intel® Pentium® 4 Processor VR-Down Design Guidelines for $V_{CC}$ and $V_{SS}$ socket loadline specifications and VR implementation details.
4. Adherence to this loadline specification for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is required to ensure reliable processor operation.
Figure 2-4. $V_{CC}$ Static and Transient Tolerance (For Intel® Pentium® 4 Processor With 512-KB L2 Cache on 0.13 Micron Process at Frequencies up to and Including 3.2 GHz)

NOTES:
1. The loadline specification includes both static and transient limits.
2. Refer to Table 2-7 for specific offsets from VID voltage which apply to all VID settings.
3. The loadlines specify voltage limits at the die measured at $V_{CC\_SENSE}$ and $V_{SS\_SENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor $V_{CC}$ and $V_{SS}$ pins. Refer to the Intel® Pentium® 4 Processor VR-Down Design Guidelines $V_{CC}$ and $V_{SS}$ socket loadline specifications and VR implementation details.
4. Adherence to this loadline specification for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is required to ensure reliable processor operation.
### Table 2-8. Vcc Static and Transient Tolerance (For Intel® Pentium® 4 Processor Extreme Edition Supporting Hyper-Threading Technology, and Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process at 3.4 GHz)

<table>
<thead>
<tr>
<th>Icc (A)</th>
<th>Voltage Deviation from VID Setting (V)(^{1,2,3})</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Maximum</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>-0.009</td>
</tr>
<tr>
<td>10</td>
<td>-0.019</td>
</tr>
<tr>
<td>15</td>
<td>-0.028</td>
</tr>
<tr>
<td>20</td>
<td>-0.037</td>
</tr>
<tr>
<td>25</td>
<td>-0.046</td>
</tr>
<tr>
<td>30</td>
<td>-0.056</td>
</tr>
<tr>
<td>35</td>
<td>-0.065</td>
</tr>
<tr>
<td>40</td>
<td>-0.074</td>
</tr>
<tr>
<td>45</td>
<td>-0.083</td>
</tr>
<tr>
<td>50</td>
<td>-0.093</td>
</tr>
<tr>
<td>55</td>
<td>-0.102</td>
</tr>
<tr>
<td>60</td>
<td>-0.111</td>
</tr>
<tr>
<td>65</td>
<td>-0.120</td>
</tr>
<tr>
<td>70</td>
<td>-0.130</td>
</tr>
<tr>
<td>75</td>
<td>-0.139</td>
</tr>
<tr>
<td>80</td>
<td>-0.148</td>
</tr>
<tr>
<td>85</td>
<td>-0.157</td>
</tr>
<tr>
<td>90</td>
<td>-0.167</td>
</tr>
</tbody>
</table>

**NOTES:**
1. The loadline specifications include both static and transient limits.
2. This table is intended to aid in reading discrete points on the following loadline figure.
3. The loadlines specify voltage limits at the die measured at V\(_{CC\_SENSE}\) and V\(_{SS\_SENSE}\) pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V\(_{CC}\) and V\(_{SS}\) pins. Refer to the Voltage Regulator-Down (VRD) 10.0 Design Guide Addendum for V\(_{CC}\) and V\(_{SS}\) socket loadline specifications and VR implementation details.
4. Adherence to this loadline specification for the processor is required to ensure reliable processor operation.
NOTES:
1. The loadline specification includes both static and transient limits.
2. Refer to Table 2-8 for specific offsets from VID voltage which apply to all VID settings.
3. The loadlines specify voltage limits at the die measured at VCC_SENSE and VSS_SENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS pins. Refer to the Voltage Regulator-Down (VRD) 10.0 Design Guide Addendum VCC and VSS socket loadline specifications and VR implementation details.
4. Adherence to this loadline specification for the processor is required to ensure reliable processor operation.
Table 2-9. AGTL+ Signal Group DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTLREF</td>
<td>Reference Voltage</td>
<td>2/3 (V_{CC}) – 2%</td>
<td>2/3 (V_{CC} + 2)%</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>GTLREF Compatible</td>
<td>Reference Voltage</td>
<td>0.63 (V_{CC}) – 2%</td>
<td>0.63 (V_{CC} + 2)%</td>
<td>V</td>
<td>10</td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>Input High Voltage</td>
<td>1.10*GTREF (V_{CC})</td>
<td>(V_{CC})</td>
<td>V</td>
<td>2,5</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Input Low Voltage</td>
<td>0.0</td>
<td>0.9*GTREF V</td>
<td></td>
<td>3,5</td>
</tr>
<tr>
<td>(V_{OH})</td>
<td>Output High Voltage</td>
<td>N/A</td>
<td>(V_{CC})</td>
<td>V</td>
<td>6</td>
</tr>
<tr>
<td>(I_{OL})</td>
<td>Output Low Current</td>
<td>N/A</td>
<td>50 mA</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>(I_{IH})</td>
<td>Pin Leakage High</td>
<td>N/A</td>
<td>100 µA</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>(I_{LO})</td>
<td>Pin Leakage Low</td>
<td>N/A</td>
<td>500 µA</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>(R_{ON})</td>
<td>Buffer On Resistance</td>
<td>7</td>
<td>11 Ω</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>(R_{ON})</td>
<td>Buffer On Resistance</td>
<td>8.4</td>
<td>13.2 Ω</td>
<td></td>
<td>4, 9</td>
</tr>
</tbody>
</table>

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. \(V_{IL}\) is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. \(V_{IH}\) is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. Refer to processor I/O Buffer Models for I/V characteristics.
5. The \(V_{CC}\) referred to in these specifications is the instantaneous \(V_{CC}\).
6. Vol max of 0.450 V is guaranteed when driving into a test load of 50 Ω as indicated in Figure 2-7.
7. Leakage to \(V_{SS}\) with pin held at \(V_{CC}\).
8. Leakage to \(V_{CC}\) with Pin held at 300 mV.
9. \(R_{ON}\) value is defined for a platform that is forward compatible with future processors.

Table 2-10. Asynchronous GTL+ Signal Group DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IH})</td>
<td>Input High Voltage</td>
<td>Asynch GTL+</td>
<td>1.10*GTREF (V_{CC})</td>
<td>V</td>
<td>3, 4</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Input Low Voltage</td>
<td>Asynch GTL+</td>
<td>0</td>
<td>0.9*GTREF V</td>
<td>4</td>
</tr>
<tr>
<td>(V_{OH})</td>
<td>Output High Voltage</td>
<td>Asynch GTL+</td>
<td>(V_{CC})</td>
<td>V</td>
<td>2, 3</td>
</tr>
<tr>
<td>(I_{OL})</td>
<td>Output Low Current</td>
<td>N/A</td>
<td>50 mA</td>
<td></td>
<td>5, 7</td>
</tr>
<tr>
<td>(I_{IH})</td>
<td>Pin Leakage High</td>
<td>N/A</td>
<td>100 µA</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>(I_{LO})</td>
<td>Pin Leakage Low</td>
<td>N/A</td>
<td>500 µA</td>
<td></td>
<td>9</td>
</tr>
<tr>
<td>(R_{ON})</td>
<td>Buffer On Resistance</td>
<td>Asynch GTL+</td>
<td>7</td>
<td>11 Ω</td>
<td>4, 6</td>
</tr>
<tr>
<td>(R_{ON})</td>
<td>Buffer On Resistance</td>
<td>Asynch GTL+</td>
<td>8.4</td>
<td>13.2 Ω</td>
<td>4, 6,10</td>
</tr>
</tbody>
</table>

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open-drain.
3. The \(V_{CC}\) referred to in these specifications refers to instantaneous \(V_{CC}\).
4. This specification applies to the asynchronous GTL+ signal group.
5. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load shown in Figure 2-7.
6. Vol max of 0.270 Volts is guaranteed when driving into a test load of 50 Ω as indicated in Figure 2-7 for the Asynchronous GTL+ signals.
7. Leakage to \(V_{SS}\) with pin held at \(V_{CC}\).
8. Leakage to \(V_{CC}\) with Pin held at 300 mV.
9. \(R_{ON}\) value is defined for a platform that is forward compatible with future processors.
Electrical Specifications

Table 2-11. PWRGOOD and TAP Signal Group DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_HYS</td>
<td>Input Hysteresis</td>
<td>200</td>
<td>300</td>
<td>mV</td>
<td>6</td>
</tr>
<tr>
<td>VT+</td>
<td>Input Low to High Threshold Voltage</td>
<td>1/2*(V_CC+V_HYS_MIN)</td>
<td>1/2*(V_CC+V_HYS_MAX)</td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>VT-</td>
<td>Input High to Low Threshold Voltage</td>
<td>1/2*(V_CC-V_HYS_MAX)</td>
<td>1/2*(V_CC-V_HYS_MIN)</td>
<td>V</td>
<td>5</td>
</tr>
<tr>
<td>V_OH</td>
<td>Output High Voltage</td>
<td>N/A</td>
<td>V_CC</td>
<td>V</td>
<td>2,3,4</td>
</tr>
<tr>
<td>I_OL</td>
<td>Output Low Current</td>
<td>N/A</td>
<td>40</td>
<td>mA</td>
<td>5,6</td>
</tr>
<tr>
<td>I_HI</td>
<td>Pin Leakage High</td>
<td>N/A</td>
<td>100</td>
<td>µA</td>
<td>8</td>
</tr>
<tr>
<td>I_LO</td>
<td>Pin Leakage Low</td>
<td>N/A</td>
<td>500</td>
<td>µA</td>
<td>9</td>
</tr>
<tr>
<td>R_ON</td>
<td>Buffer On Resistance</td>
<td>8.75</td>
<td>13.75</td>
<td>Ω</td>
<td>3</td>
</tr>
</tbody>
</table>

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open-drain.
3. Refer to I/O Buffer Models for I/V characteristics.
4. The V_CC referred to in these specifications refers to instantaneous V_CC.
5. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load shown in Figure 2-7.
6. Vol max of 0.320 V is guaranteed when driving into a test load of 50 Ω as indicated in Figure 2-7 for the TAP Signals.
7. V_HYS represents the amount of hysteresis, nominally centered about 1/2 V_CC for all TAP inputs.
8. Leakage to V_CC with pin held at V_CC.
9. Leakage to V_CC with Pin held at 300 mV.

Table 2-12. ITPCLKOUT[1:0] DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_on</td>
<td>Buffer On Resistance</td>
<td>27</td>
<td>46</td>
<td>Ω</td>
<td>2,3</td>
</tr>
</tbody>
</table>

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are not tested and are based on design simulations.
3. See Figure 2-6 for ITPCLKOUT[1:0] output buffer diagram.
Electrical Specifications

Figure 2-6. ITPCLKOUT[1:0] Output Buffer Diagram

NOTES:
1. See Table 2-12 for range of Ron.
2. The VCC referred to in this figure is the instantaneous Vcc.
3. Refer to the *ITP 700 Debug Port Design Guide* and the appropriate platform design guidelines for the value of Rext.

Table 2-13. BSEL [1:0] and VID[4:0] DC Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ron</td>
<td>Buffer On Resistance</td>
<td>9.2</td>
<td>14.3</td>
<td>Ω</td>
<td>2</td>
</tr>
<tr>
<td>Ron</td>
<td>Buffer On Resistance</td>
<td>7.8</td>
<td>12.8</td>
<td>Ω</td>
<td>2</td>
</tr>
<tr>
<td>$I_{HI}$</td>
<td>Pin Leakage High</td>
<td>N/A</td>
<td>100</td>
<td>µA</td>
<td>3</td>
</tr>
</tbody>
</table>

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are not tested and are based on design simulations.
3. Leakage to Vss with pin held at 2.50 V.
2.12 AGTL+ System Bus Specifications

Routing topology recommendations may be found in the appropriate platform design guide listed in Table 1-1. Termination resistors are not required for most AGTL+ signals because they are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers which compare a signal’s voltage with a reference voltage called GTLREF (known as VREF in previous documentation).

Table 2-14 lists the GTLREF specifications. The AGTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits. It is important that the system board impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and is well-controlled. For more details on platform design, see the appropriate platform design guide.

Table 2-14. AGTL+ Bus Voltage Definitions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTLREF</td>
<td>Bus Reference Voltage</td>
<td>2/3 VCC−2%</td>
<td>2/3 VCC</td>
<td>2/3 VCC+2%</td>
<td>V</td>
<td>2, 3, 6</td>
</tr>
<tr>
<td>GTLREF Compatible</td>
<td>Bus Reference Voltage</td>
<td>0.63 VCC−2%</td>
<td>0.63 VCC</td>
<td>0.63 VCC+2%</td>
<td>V</td>
<td>2, 3, 6, 7</td>
</tr>
<tr>
<td>R_TT</td>
<td>Termination Resistance</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>Ω</td>
<td>4</td>
</tr>
<tr>
<td>R_TT Compatible</td>
<td>Termination Resistance</td>
<td>54</td>
<td>60</td>
<td>66</td>
<td>Ω</td>
<td>4, 7</td>
</tr>
<tr>
<td>COMP[1:0]</td>
<td>COMP Resistance</td>
<td>50.49</td>
<td>51</td>
<td>51.51</td>
<td>Ω</td>
<td>5</td>
</tr>
<tr>
<td>COMP[1:0] Compatible</td>
<td>COMP Resistance</td>
<td>61.3</td>
<td>61.9</td>
<td>62.5</td>
<td>Ω</td>
<td>5, 7</td>
</tr>
</tbody>
</table>

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The tolerances for this specification have been stated generically to enable the system designer to calculate the minimum and maximum values across the range of VCC.
3. GTLREF should be generated from VCC by a voltage divider of 1% tolerance resistors or 1% tolerance, matched resistors. Refer to the appropriate Platform Design Guide for implementation details.
4. R_TT is the on-die termination resistance measured at VOL of the AGTL+ output driver. Refer to processor I/O buffer models for I/V characteristics.
5. COMP resistance must be provided on the system board with 1% tolerance resistors. See the appropriate Platform Design Guide for implementation details.
6. The VCC referred to in these specifications is the instantaneous VCC.
7. The specifications are for a platform to be forward compatible with future processors. A compatible platform is one that is designed for some level of compatibility with future processors.

Figure 2-7. Test Circuit
This page is intentionally left blank.
The Pentium 4 processor on 0.13 micron process is packaged in a Flip-Chip Pin Grid Array (FC-PGA2) package. Components of the package include an integrated heat spreader (IHS), processor die, and the substrate which is the pin carrier. Mechanical specifications for the processor are given in this section. See Section 1.1. for a terminology listing. The processor socket that accepts the Pentium 4 processor on 0.13 micron process is referred to as a 478-Pin micro PGA (mPGA478B) socket. See the Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478B) Socket Design Guidelines for complete details on the mPGA478B socket.

**Note:** For Figure 3-1 through Figure 3-8, the following notes apply:

1. Unless otherwise specified, the following drawings are dimensioned in millimeters.
2. Figures and drawings labelled as “Reference Dimensions” are provided for informational purposes only. Reference dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference dimensions are not checked as part of the processor manufacturing process. Unless noted as such, dimensions in parentheses without tolerances are reference dimensions.
3. Drawings are not to scale.

**Note:** Figure 3-1 is not to scale and is for reference only. The socket and system board are supplied as a reference only.

**Figure 3-1. Exploded View of Processor Components on a System Board**
Table 3-1. Description Table for Processor Dimensions

<table>
<thead>
<tr>
<th>Code Letter</th>
<th>Dimension (mm)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Nominal</td>
</tr>
<tr>
<td>A1</td>
<td>2.266</td>
<td>2.378</td>
</tr>
<tr>
<td>A2</td>
<td>0.980</td>
<td>1.080</td>
</tr>
<tr>
<td>A1</td>
<td>2.42</td>
<td>2.55</td>
</tr>
<tr>
<td>A2</td>
<td>1.13</td>
<td>1.20</td>
</tr>
<tr>
<td>B1</td>
<td>30.800</td>
<td>31.000</td>
</tr>
<tr>
<td>B2</td>
<td>30.800</td>
<td>31.000</td>
</tr>
<tr>
<td>C1</td>
<td>33.000</td>
<td>Includes placement tolerance</td>
</tr>
<tr>
<td>C2</td>
<td>33.000</td>
<td>Includes placement tolerance</td>
</tr>
<tr>
<td>D</td>
<td>34.900</td>
<td>35.000</td>
</tr>
<tr>
<td>D1</td>
<td>31.500</td>
<td>31.750</td>
</tr>
<tr>
<td>G1</td>
<td>13.970</td>
<td>13.970</td>
</tr>
<tr>
<td>G2</td>
<td>13.970</td>
<td>13.970</td>
</tr>
<tr>
<td>G3</td>
<td>1.250</td>
<td>1.250</td>
</tr>
<tr>
<td>H</td>
<td>1.270</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>1.950</td>
<td>2.030</td>
</tr>
<tr>
<td>øP</td>
<td>0.280</td>
<td>0.305</td>
</tr>
<tr>
<td>PIN TP</td>
<td></td>
<td>0.254</td>
</tr>
<tr>
<td>IHS Flatness</td>
<td></td>
<td>0.05</td>
</tr>
</tbody>
</table>
Figure 3-3 details the keep-in specification for pin-side components. The Pentium 4 processor on 0.13 micron process may contain pin-side capacitors mounted to the processor package.

Figure 3-5 details the flatness and tilt specifications for the IHS. Tilt is measured with the reference datum set to the bottom of the processor substrate.

Figure 3-3. Processor Cross-Section and Keep-In

Figure 3-4. Processor Pin Detail

NOTES:
1. Pin plating consists of 0.2 micrometers Au over 2.0 micrometer Ni.
2. 0.254 mm diametric true position, pin-to-pin.
Figure 3-5. IHS Flatness Specification

NOTES:
1. Flatness is specific as overall, not per unit of length.
2. All Dimensions are in millimeters.

3.1 Package Load Specifications

Table 3-2 provides dynamic and static load specifications for the processor IHS. These mechanical load limits should not be exceeded during heatsink assembly, mechanical stress testing, or standard drop and shipping conditions. The heatsink attach solutions must not induce continuous stress onto the processor with the exception of a uniform load to maintain the heatsink-to-processor thermal interface contact. It is not recommended to use any portion of the processor substrate as a mechanical reference or load bearing surface for thermal solutions.

Table 3-2. Package Dynamic and Static Load Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static</td>
<td>100</td>
<td>lbf</td>
<td>1, 2</td>
</tr>
<tr>
<td>Dynamic</td>
<td>200</td>
<td>lbf</td>
<td>1, 3</td>
</tr>
</tbody>
</table>

NOTES:
1. This specification applies to a uniform compressive load.
2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.
3. Dynamic loading specifications are defined assuming a maximum duration of 11 ms and 200 lbf is achieved by superimposing a 100 lbf dynamic load (1 lbm at 50 g) on the static compressive load.
3.2 Processor Insertion Specifications

The Pentium 4 processor on 0.13 micron process can be inserted and removed 15 times from a mPGA478B socket meeting the Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478B) Socket Design Guidelines document.

3.3 Processor Mass Specifications

Table 3-3 specifies the processor’s mass. This includes all components which make up the entire processor product.

Table 3-3. Processor Mass

<table>
<thead>
<tr>
<th>Processor</th>
<th>Mass (grams)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel® Pentium® 4 processor on 0.13 micron process</td>
<td>19</td>
</tr>
</tbody>
</table>

3.4 Processor Materials

The Pentium 4 processor on 0.13 micron process is assembled from several components. The basic material properties are described in Table 3-4.

Table 3-4. Processor Material Properties

<table>
<thead>
<tr>
<th>Component</th>
<th>Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrated Heat Spreader</td>
<td>Nickel over copper</td>
</tr>
<tr>
<td>Substrate</td>
<td>Fiber-reinforced resin</td>
</tr>
<tr>
<td>Substrate pins</td>
<td>Gold over nickel</td>
</tr>
</tbody>
</table>
3.5 Processor Markings

Figure 3-6 and Figure 3-7 detail the processor top-side markings and is provided to aid in the identification of the Pentium 4 processors on 0.13 micron process.

**Figure 3-6. Processor Markings (Processors with Fixed VID)**

![Figure 3-6: Processor Markings (Processors with Fixed VID)](image)

**Figure 3-7. Processor Markings (Processors with Multiple VID)**

![Figure 3-7: Processor Markings (Processors with Multiple VID)](image)

**NOTE:** Intel will continue to ship old and new marked parts until old mark inventory has been depleted.
Figure 3-8. The Coordinates of the Processor Pins As Viewed from the Top of the Package
This page is intentionally left blank.
4.1 Processor Pin Assignments

This section contains pin lists for the Pentium 4 processor on 0.13 micron process. Table 4-1 is ordered alphabetically by pin name; Table 4-2 is ordered alphabetically by pin number.
### Table 4-1. Pin Listing by Pin Name

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>A3#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A4#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A5#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A6#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A7#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A8#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A9#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A10#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A11#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A12#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A13#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A14#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A15#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A16#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A17#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A18#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A19#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A20#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A21#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A22#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A23#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A24#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A25#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A26#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A27#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A28#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A29#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A30#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A31#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A32#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A33#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A34#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A35#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A20M#</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>ADS#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>ADSTB0#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>ADSTB1#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>APO#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AP1#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BCLK0</td>
<td>Bus Clock</td>
<td>Input</td>
</tr>
<tr>
<td>BCLK1</td>
<td>Bus Clock</td>
<td>Input</td>
</tr>
<tr>
<td>BINT1#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BNR#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BPM0#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BPM1#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BPM2#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BPM3#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BPM4#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BPM5#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BPR1#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>BR0#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>BSEL0</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>BSEL1</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>COMP0</td>
<td>Power/Other</td>
<td>Input/Output</td>
</tr>
<tr>
<td>COMP1</td>
<td>Power/Other</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D0#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D1#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D2#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D3#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D4#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D5#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D6#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D7#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D8#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D9#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D10#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D11#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D12#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D13#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D14#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D15#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D16#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D17#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D18#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D19#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D20#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D21#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D22#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D23#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D24#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D25#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D26#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D27#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D28#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D29#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D30#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D31#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D32#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
</tbody>
</table>
### Table 4-1. Pin Listing by Pin Name

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>D33#</td>
<td>N22</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D34#</td>
<td>P21</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D35#</td>
<td>M24</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D36#</td>
<td>N23</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D37#</td>
<td>M26</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D38#</td>
<td>N26</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D39#</td>
<td>N25</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D40#</td>
<td>R21</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D41#</td>
<td>P24</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D42#</td>
<td>R25</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D43#</td>
<td>R24</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D44#</td>
<td>T26</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D45#</td>
<td>T25</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D46#</td>
<td>T22</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D47#</td>
<td>T23</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D48#</td>
<td>U26</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D49#</td>
<td>U24</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D50#</td>
<td>U23</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D51#</td>
<td>V25</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D52#</td>
<td>U21</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D53#</td>
<td>V22</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D54#</td>
<td>V24</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D55#</td>
<td>W26</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D56#</td>
<td>Y26</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D57#</td>
<td>W25</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D58#</td>
<td>Y23</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D59#</td>
<td>Y24</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D60#</td>
<td>Y21</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D61#</td>
<td>AA25</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D62#</td>
<td>AA22</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D63#</td>
<td>AA24</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DB10#</td>
<td>E21</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DB11#</td>
<td>G25</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DB12#</td>
<td>P26</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DB13#</td>
<td>V21</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DB14#</td>
<td>AE25</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>DBS1Y#</td>
<td>H5</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DEFER#</td>
<td>E2</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>DP0#</td>
<td>J26</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DP1#</td>
<td>K25</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DP2#</td>
<td>K26</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DP3#</td>
<td>L25</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DRDY#</td>
<td>H2</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DSTBNO#</td>
<td>E22</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
</tbody>
</table>

### Table 4-1. Pin Listing by Pin Name (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSTBN1#</td>
<td>K22</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DSTBN2#</td>
<td>R22</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DSTBN3#</td>
<td>W22</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DSTBP0#</td>
<td>F21</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DSTBP1#</td>
<td>J23</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DSTBP2#</td>
<td>P23</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>DSTBP3#</td>
<td>W23</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>FERR#</td>
<td>B6</td>
<td>Asynch AGL+</td>
<td>Output</td>
</tr>
<tr>
<td>GTLREF</td>
<td>AA21</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>GTLREF</td>
<td>AA6</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>GTLREF</td>
<td>F20</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>GTLREF</td>
<td>F6</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>HIT#</td>
<td>F3</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>HITM#</td>
<td>E3</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>IERR#</td>
<td>AC3</td>
<td>Common Clock</td>
<td>Output</td>
</tr>
<tr>
<td>IGNNE#</td>
<td>B2</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>IMPSEL</td>
<td>AE26</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>INIT#</td>
<td>W5</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>ITPCLKOUT0</td>
<td>AA20</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>ITPCLKOUT1</td>
<td>AB22</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>ITP_CLK0</td>
<td>AC26</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>LINT0</td>
<td>D1</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>LINT1</td>
<td>E5</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>LOCK#</td>
<td>G4</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>MCERR#</td>
<td>V6</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>PROCHOT#</td>
<td>C3</td>
<td>Asynch GTL+</td>
<td>Input/Output</td>
</tr>
<tr>
<td>PWRGOOD</td>
<td>AB23</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>REQ0#</td>
<td>J1</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>REQ1#</td>
<td>K5</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>REQ2#</td>
<td>J4</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>REQ3#</td>
<td>J3</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>REQ4#</td>
<td>H3</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>RESERVED</td>
<td>A22</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESERVED</td>
<td>A7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESERVED</td>
<td>AD2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESERVED</td>
<td>AD3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESERVED</td>
<td>AE21</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESERVED</td>
<td>AF3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESERVED</td>
<td>AF24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESERVED</td>
<td>AF25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESET#</td>
<td>AB25</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>RS0#</td>
<td>F1</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>RS1#</td>
<td>G5</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>Pin Name</td>
<td>Pin Number</td>
<td>Signal Buffer Type</td>
<td>Direction</td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
<td>--------------------</td>
<td>-----------</td>
</tr>
<tr>
<td>RS2#</td>
<td>F4</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>RSP#</td>
<td>AB2</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>SKTOCC#</td>
<td>AF26</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>SLP#</td>
<td>AB26</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>SM#</td>
<td>B5</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>STPCLK#</td>
<td>Y4</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>TCK#</td>
<td>D4</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>TDI</td>
<td>C1</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>TDO</td>
<td>D5</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH10</td>
<td>AD24</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH11</td>
<td>AA2</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH12</td>
<td>AC21</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH13</td>
<td>AC20</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH14</td>
<td>AC24</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH15</td>
<td>AC23</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH18</td>
<td>U6</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH9</td>
<td>W4</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH110</td>
<td>Y3</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH111</td>
<td>A6</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>TESTH12</td>
<td>AD25</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>THERMDA</td>
<td>B3</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>THERMDC</td>
<td>C4</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>THERMTRIP#</td>
<td>A2</td>
<td>Asynch GTL+</td>
<td>Output</td>
</tr>
<tr>
<td>TMS</td>
<td>F7</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>TRDY#</td>
<td>J6</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>TRST#</td>
<td>E6</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>VCC</td>
<td>A10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>A12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>A14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>A16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>A18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>A20</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>A8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AA10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AA12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AA14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AA16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AA18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AA8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AB11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AB13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AB15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AB17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AB19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AB7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AB9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AC10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AC12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AC14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AC16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AC18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AC8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AD11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AD13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AD15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AD17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AD19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AD7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AD9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AE10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AE12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AE14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AE16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AE18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AE20</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AE6</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AE8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF2</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF5</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AF9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>B11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>B13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>B15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>B17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>B19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>B7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>B9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>C10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>C12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>C14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>C16</td>
<td>Power/Other</td>
<td></td>
</tr>
</tbody>
</table>
### Table 4-1. Pin Listing by Pin Name

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>C18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>C20</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>C8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>D11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>D13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>D15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>D17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>D19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>D7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>D9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>E10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>E12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>E14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>E16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>E18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>E20</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>E8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>F11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>F13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>F15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>F17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>F19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>F9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AD20</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>AE23</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>A5</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>VCCVID</td>
<td>AF4</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>VID0</td>
<td>AE5</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>VID1</td>
<td>AE4</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>VID2</td>
<td>AE3</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>VID3</td>
<td>AE2</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>VID4</td>
<td>AE1</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>VSS</td>
<td>D10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A24</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A26</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A3</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>A9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA1</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA23</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA26</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA4</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AA9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB20</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB24</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB3</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB6</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AB8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC2</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC25</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC5</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AC9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD1</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD23</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD4</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AD8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AE11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AE13</td>
<td>Power/Other</td>
<td></td>
</tr>
</tbody>
</table>
### Table 4-1. Pin Listing by Pin Name

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>AE15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AE17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AE19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AE22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AE24</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AE7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AE9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AF1</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AF10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AF12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AF14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AF16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AF18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AF20</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AF6</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>AF8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B20</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B23</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B26</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B4</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>B8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C2</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C25</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C5</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>C9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>D12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>D14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>D16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>D18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>D20</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>D21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>D24</td>
<td>Power/Other</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>D3</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>D6</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>D8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E1</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E11</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E13</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E15</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E17</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E19</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E23</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E26</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E4</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E7</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>E9</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F10</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F12</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F14</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F16</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F18</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F2</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F25</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F5</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>F8</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>G21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>G24</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>G3</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>G6</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>H1</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>H23</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>H26</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>H4</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>J2</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>J22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>J25</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>J5</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>K21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>K24</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>K3</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>K6</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>L1</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>L23</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>L26</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>L4</td>
<td>Power/Other</td>
<td></td>
</tr>
</tbody>
</table>
### Table 4-1. Pin Listing by Pin Name

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>M2</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>M22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>M25</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>M5</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>N21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>N24</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>N3</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>N6</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>P2</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>P22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>P25</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>P5</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>R1</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>R23</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>R26</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>R4</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>T21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>T24</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>T3</td>
<td>Power/Other</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>T6</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>U2</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>U22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>U25</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>U5</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>V1</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>V23</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>V26</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>V4</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>W21</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>W24</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>W3</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>W6</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>Y2</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>Y22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>Y25</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>Y5</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSSA</td>
<td>AD22</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>VSS_SENSE</td>
<td>A4</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
</tbody>
</table>
### Table 4-2. Pin Listing by Pin Number

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2</td>
<td>THERMTRIP#</td>
<td>Asynch GTL+</td>
<td>Output</td>
</tr>
<tr>
<td>A3</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A4</td>
<td>VSS_SENSE</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A5</td>
<td>VCC_SENSE</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A6</td>
<td>TESTHI11</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>A7</td>
<td>RESERVED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A8</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A9</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A10</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A11</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A12</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A13</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A14</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A15</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A16</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A17</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A18</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A19</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A20</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A21</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A22</td>
<td>RESERVED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A23</td>
<td>D2#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A24</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A25</td>
<td>D3#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A26</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A27</td>
<td>TESTHI1</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>A28</td>
<td>BINIT#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A29</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A30</td>
<td>BPM4#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A31</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A32</td>
<td>BPM1#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A33</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A34</td>
<td>BPM2#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A35</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A36</td>
<td>BPM3#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A37</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A38</td>
<td>BPM4#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A39</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A40</td>
<td>BPM5#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>A41</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>A42</td>
<td>BPM6#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
</tbody>
</table>

### Table 4-2. Pin Listing by Pin Number

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>AA20</td>
<td>ITPCLK[0]</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>AA21</td>
<td>GTLREF</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AA22</td>
<td>D62#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AA23</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AA24</td>
<td>D63#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AA25</td>
<td>D61#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AA26</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB1</td>
<td>A35#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AB2</td>
<td>RSP#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>AB3</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB4</td>
<td>BPM5#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AB5</td>
<td>BPM1#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AB6</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB7</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB8</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB9</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB10</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB11</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB12</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB13</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB14</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB15</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB16</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB17</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB18</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB19</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB20</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB21</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB22</td>
<td>ITPCLK[1]</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>AB23</td>
<td>PWRCGOOD</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AB24</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AB25</td>
<td>RESET#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>AB26</td>
<td>SLP#</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>AC1</td>
<td>AP#[0]</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AC2</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC3</td>
<td>IERR#</td>
<td>Common Clock</td>
<td>Output</td>
</tr>
<tr>
<td>AC4</td>
<td>BPM2#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AC5</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC6</td>
<td>BPM0#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>AC7</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC8</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC9</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC10</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC11</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
</tbody>
</table>
### Table 4-2. Pin Listing by Pin Number

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC12</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC13</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC14</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC15</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC16</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC17</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC18</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC19</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC20</td>
<td>TESTHI3</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AC21</td>
<td>TESTHI2</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AC22</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC23</td>
<td>TESTHI5</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AC24</td>
<td>TESTHI4</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AC25</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AC26</td>
<td>ITP_CLK0</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>AD1</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD2</td>
<td>RESERVED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD3</td>
<td>RESERVED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD4</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD5</td>
<td>BSEL1</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>AD6</td>
<td>BSEL0</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>AD7</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD8</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD9</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD10</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD11</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD12</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD13</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD14</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD15</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD16</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD17</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD18</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD19</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD20</td>
<td>VCCA</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD21</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD22</td>
<td>VSSA</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD23</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AD24</td>
<td>TESTHI0</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AD25</td>
<td>TESTHI2</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AD26</td>
<td>ITP_CLK1</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>AE1</td>
<td>VID4</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>AE2</td>
<td>VID3</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>AE3</td>
<td>VID2</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>AE4</td>
<td>VID1</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>AE5</td>
<td>VID0</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>AE6</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE7</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE8</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE9</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE10</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE11</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE12</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE13</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE14</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE15</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE16</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE17</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE18</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE19</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE20</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE21</td>
<td>RESERVED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AE22</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE23</td>
<td>VCCIOPLL</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE24</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AE25</td>
<td>DBR#</td>
<td>Asynch GTL+</td>
<td>Output</td>
</tr>
<tr>
<td>AE26</td>
<td>IMPSEL</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AF1</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF2</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF3</td>
<td>RESERVED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AF4</td>
<td>VCCVID</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>AF5</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF6</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF7</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF8</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF9</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF10</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF11</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF12</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF13</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF14</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF15</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF16</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF17</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF18</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF19</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF20</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>AF21</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
</tbody>
</table>
### Table 4-2. Pin Listing by Pin Number

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>AF22</td>
<td>BCLK[0]</td>
<td>Bus Clock</td>
<td>Input</td>
</tr>
<tr>
<td>AF23</td>
<td>BCLK[1]</td>
<td>Bus Clock</td>
<td>Input</td>
</tr>
<tr>
<td>AF24</td>
<td>RESERVED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AF25</td>
<td>RESERVED</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AF26</td>
<td>SKTOCC#</td>
<td>Power/Other</td>
<td>Output</td>
</tr>
<tr>
<td>B2</td>
<td>IGNNE#</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>B3</td>
<td>THERMDA</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B4</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B5</td>
<td>SM#</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>B6</td>
<td>FERR#</td>
<td>Asynch AGL+</td>
<td>Output</td>
</tr>
<tr>
<td>B7</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B8</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B9</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B10</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B11</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B12</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B13</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B14</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B15</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B16</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B17</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B18</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B19</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B20</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B21</td>
<td>D0#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>B22</td>
<td>D01#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>B23</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>B24</td>
<td>D6#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>B25</td>
<td>D9#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>B26</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>TDI</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>C2</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>PROCHOT#</td>
<td>Asynch GTL+</td>
<td>Input/Output</td>
</tr>
<tr>
<td>C4</td>
<td>THERMDC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C5</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C6</td>
<td>A20M#</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>C7</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C8</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C9</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C10</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C11</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C12</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C13</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C14</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C15</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C16</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C17</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C18</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C19</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C20</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C21</td>
<td>D4#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>C22</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C23</td>
<td>D7#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>C24</td>
<td>D8#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>C25</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>C26</td>
<td>D12#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D1</td>
<td>LINT0</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>D2</td>
<td>BPRI#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>D3</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>TCK</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>D5</td>
<td>TDO</td>
<td>TAP</td>
<td>Output</td>
</tr>
<tr>
<td>D6</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D7</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D8</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D9</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D10</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D11</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D12</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D13</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D14</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D15</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D16</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D17</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D18</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D19</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D20</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D21</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D22</td>
<td>D5#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D23</td>
<td>D13#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D24</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>D25</td>
<td>D15#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>D26</td>
<td>D23#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>E1</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E2</td>
<td>DEFER#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>E3</td>
<td>HITM#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>E4</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E5</td>
<td>LINT1</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>E6</td>
<td>TRST#</td>
<td>TAP</td>
<td>Input</td>
</tr>
</tbody>
</table>
### Table 4-2. Pin Listing by Pin Number

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>E7</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E8</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E9</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E10</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E11</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E12</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E13</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E14</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E15</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E16</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E17</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E18</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E19</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E20</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E21</td>
<td>DBi0#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>E22</td>
<td>DSBn0#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>E23</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>E24</td>
<td>D17#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>E25</td>
<td>D21#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>E26</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F1</td>
<td>RS0#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>F2</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F3</td>
<td>HIT#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>F4</td>
<td>RS2#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>F5</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F6</td>
<td>GTLREF</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>F7</td>
<td>TMS</td>
<td>TAP</td>
<td>Input</td>
</tr>
<tr>
<td>F8</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F9</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F10</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F11</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F12</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F13</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F14</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F15</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F16</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F17</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F18</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F19</td>
<td>VCC</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F20</td>
<td>GTLREF</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>F21</td>
<td>DSBn0#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>F22</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F23</td>
<td>D19#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>F24</td>
<td>D20#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>F25</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>F26</td>
<td>D22#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>G1</td>
<td>ADS#</td>
<td>Common Clock</td>
<td>Input/Out</td>
</tr>
<tr>
<td>G2</td>
<td>BNR#</td>
<td>Common Clock</td>
<td>Input/Out</td>
</tr>
<tr>
<td>G3</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>G4</td>
<td>LOCK#</td>
<td>Common Clock</td>
<td>Input/Out</td>
</tr>
<tr>
<td>G5</td>
<td>RS1#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>G6</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>G7</td>
<td>DSTBP0#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>G19</td>
<td>D10#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>G20</td>
<td>D18#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>G21</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>G22</td>
<td>D19#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>G23</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>G24</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>G25</td>
<td>DBi1#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>G26</td>
<td>D25#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>H1</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>H2</td>
<td>DRDY#</td>
<td>Common Clock</td>
<td>Input/Out</td>
</tr>
<tr>
<td>H3</td>
<td>REQ4#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>H4</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>H5</td>
<td>DBSY#</td>
<td>Common Clock</td>
<td>Input/Out</td>
</tr>
<tr>
<td>H6</td>
<td>BR0#</td>
<td>Common Clock</td>
<td>Input/Out</td>
</tr>
<tr>
<td>H21</td>
<td>D11#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>H22</td>
<td>D16#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>H23</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>H24</td>
<td>D26#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>H25</td>
<td>D31#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>H26</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>J1</td>
<td>REQ0#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>J2</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>J3</td>
<td>REQ3#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>J4</td>
<td>REQ2#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>J5</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>J6</td>
<td>TRDY#</td>
<td>Common Clock</td>
<td>Input</td>
</tr>
<tr>
<td>J21</td>
<td>D14#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>J22</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>J23</td>
<td>DSBP1#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>J24</td>
<td>D29#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>J25</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>J26</td>
<td>DPO#</td>
<td>Common Clock</td>
<td>Input/Out</td>
</tr>
<tr>
<td>K1</td>
<td>A6#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>K2</td>
<td>A3#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>K3</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>K4</td>
<td>A4#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>K5</td>
<td>REQ1#</td>
<td>Source Synch</td>
<td>Input/Out</td>
</tr>
<tr>
<td>K6</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
</tbody>
</table>
## Table 4-2. Pin Listing by Pin Number

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3</td>
<td>A19#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>P4</td>
<td>A20#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>P5</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>P6</td>
<td>A24#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>P21</td>
<td>D34#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>P22</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>P23</td>
<td>DSTBP2#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>P24</td>
<td>D41#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>P25</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>P26</td>
<td>DBI2#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>R1</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>A18#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>R3</td>
<td>A21#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>R4</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>R5</td>
<td>ADSTB1#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>R6</td>
<td>A28#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>R21</td>
<td>D40#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>R22</td>
<td>DSTBN2#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>R23</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>R24</td>
<td>D43#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>R25</td>
<td>D42#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>R26</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>T1</td>
<td>A17#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>T2</td>
<td>A22#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>T3</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>T4</td>
<td>A26#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>T5</td>
<td>A30#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>T6</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>T21</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>T22</td>
<td>D46#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>T23</td>
<td>D47#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>T24</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>T25</td>
<td>D45#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>T26</td>
<td>D44#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>U1</td>
<td>A23#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>U2</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>U3</td>
<td>A25#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>U4</td>
<td>A31#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>U5</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>U6</td>
<td>TESTHI8</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>U21</td>
<td>D52#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>U22</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>U23</td>
<td>D50#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>U24</td>
<td>D49#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
</tbody>
</table>
### Table 4-2. Pin Listing by Pin Number

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>U25</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>U26</td>
<td>D48#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>V1</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>V2</td>
<td>A27#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>V3</td>
<td>A32#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>V4</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>V5</td>
<td>AP1#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>V6</td>
<td>MCERR#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>V21</td>
<td>DBI3#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>V22</td>
<td>D53#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>V23</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>V24</td>
<td>D54#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>V25</td>
<td>D51#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>V26</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>W1</td>
<td>A29#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>W2</td>
<td>A33#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>W3</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>W4</td>
<td>TESTHI9</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>W5</td>
<td>INIT#</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Signal Buffer Type</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>W6</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>W21</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>W22</td>
<td>DSTBN3#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>W23</td>
<td>DSTBP3#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>W24</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>W25</td>
<td>D57#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>W26</td>
<td>D55#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>Y1</td>
<td>A34#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>Y2</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>Y3</td>
<td>TESTHI10</td>
<td>Power/Other</td>
<td>Input</td>
</tr>
<tr>
<td>Y4</td>
<td>STPCLK#</td>
<td>Asynch GTL+</td>
<td>Input</td>
</tr>
<tr>
<td>Y5</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>Y6</td>
<td>BPM3#</td>
<td>Common Clock</td>
<td>Input/Output</td>
</tr>
<tr>
<td>Y21</td>
<td>D60#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>Y22</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>Y23</td>
<td>D58#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>Y24</td>
<td>D59#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
<tr>
<td>Y25</td>
<td>VSS</td>
<td>Power/Other</td>
<td></td>
</tr>
<tr>
<td>Y26</td>
<td>D56#</td>
<td>Source Synch</td>
<td>Input/Output</td>
</tr>
</tbody>
</table>
### 4.2 Signal Descriptions

Table 4-3. Signal Descriptions  (Sheet 1 of 8)

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A[35:3]#</td>
<td>Input/Output</td>
<td>A[35:3]# (Address) define a $2^{36}$-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel® Pentium® 4 processor on 0.13 micron process system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 6.1 for more details.</td>
</tr>
<tr>
<td>A20M#</td>
<td>Input</td>
<td>If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td>
</tr>
<tr>
<td>ADS#</td>
<td>Input/Output</td>
<td>ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.</td>
</tr>
<tr>
<td>ADSTB[1:0]#</td>
<td>Input/Output</td>
<td>Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Signals</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>REQ[4:0]#, A[16:3]#</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A[35:17]#</td>
</tr>
<tr>
<td>AP[1:0]#</td>
<td>Input/Output</td>
<td>AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium 4 processors on 0.13 micron process system bus agents. The following table defines the coverage model of these signals.</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Request Signals</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>A[35:24]#</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A[23:3]#</td>
</tr>
<tr>
<td></td>
<td></td>
<td>REQ[4:0]#</td>
</tr>
<tr>
<td>BCLK[1:0]</td>
<td>Input</td>
<td>The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing $V_{CROSS}$.</td>
</tr>
</tbody>
</table>
Table 4-3. Signal Descriptions  (Sheet 2 of 8)

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BINIT#</td>
<td>Input/Output</td>
<td>BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IQQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IQQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.</td>
</tr>
<tr>
<td>BNR#</td>
<td>Input/Output</td>
<td>BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.</td>
</tr>
<tr>
<td>BPM[5:0]#</td>
<td>Input/Output</td>
<td>BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Pentium 4 processors on 0.13 micron process system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Refer to the appropriate Platform Design Guide for more detailed information. These signals do not have on-die termination and must be terminated on the system board.</td>
</tr>
<tr>
<td>BPR#</td>
<td>Input</td>
<td>BPR# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPR# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPR# asserted until all of its requests are completed, then releases the bus by deasserting BPR#.</td>
</tr>
<tr>
<td>BR0#</td>
<td>Input/Output</td>
<td>BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. This signal does not have on-die termination and must be terminated.</td>
</tr>
<tr>
<td>BSEL[1:0]</td>
<td>Input/Output</td>
<td>BSEL[1:0] (Bus Select) are used to select the processor input clock frequency. Table 2-4 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. For more information about these pins, including termination recommendations refer to Section 2.9 and the appropriate platform design guidelines.</td>
</tr>
</tbody>
</table>
**Quad-Pumped Signal Groups**

<table>
<thead>
<tr>
<th>Data Group</th>
<th>DSTBN#/ DSBTP#</th>
<th>DBI#</th>
</tr>
</thead>
<tbody>
<tr>
<td>D[15:0]#</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>D[31:16]#</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>D[47:32]#</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>D[63:48]#</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.

**DBI[3:0]# Assignment To Data Bus**

<table>
<thead>
<tr>
<th>Bus Signal</th>
<th>Data Bus Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBI3#</td>
<td>D[63:48]#</td>
</tr>
<tr>
<td>DBI2#</td>
<td>D[47:32]#</td>
</tr>
<tr>
<td>DBI1#</td>
<td>D[31:16]#</td>
</tr>
<tr>
<td>DBI0#</td>
<td>D[15:0]#</td>
</tr>
</tbody>
</table>

**DBR# (Data Bus Reset)** is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.

**DBSY# (Data Bus Busy)** is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.

**DEFER#** is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.

**DP[3:0]# (Data parity)** provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium 4 processor on 0.13 micron process system bus agents.
### Table 4-3. Signal Descriptions (Sheet 4 of 8)

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRDY#</td>
<td>Input/Output</td>
<td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.</td>
</tr>
<tr>
<td>DSTBN[3:0]#</td>
<td>Input/Output</td>
<td>Data strobe used to latch in D[63:0]#:</td>
</tr>
<tr>
<td>DSTBP[3:0]#</td>
<td>Input/Output</td>
<td>Data strobe used to latch in D[63:0]#:</td>
</tr>
<tr>
<td>FERR#/PBE#</td>
<td>Output</td>
<td>FERR#/PBE# (floating point error/pending break event) is a multiplexed signal which is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using Microsoft MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. For addition information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to the IA-32 Intel® Architecture Software Developer’s Manual (Vol. 1 - Vol. 3) and the Intel® Processor Identification and the CPUID Instruction application note.</td>
</tr>
<tr>
<td>GTLREF</td>
<td>Input</td>
<td>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 Vcc. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the appropriate Platform Design Guide for more information.</td>
</tr>
<tr>
<td>HIT#</td>
<td>Input/Output</td>
<td>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</td>
</tr>
<tr>
<td>HITM#</td>
<td>Input/Output</td>
<td></td>
</tr>
<tr>
<td>IERR#</td>
<td>Output</td>
<td>IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#. This signal does not have on-die termination and must be terminated on the system board.</td>
</tr>
</tbody>
</table>

*Note: The table continues on the following pages.*

---

**Pin Lists and Signal Descriptions**

Intel® Pentium® 4 Processor on 0.13 Micron Process Datasheet 61
### Table 4-3. Signal Descriptions  (Sheet 5 of 8)

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGNNE#</td>
<td>Input</td>
<td>IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td>
</tr>
<tr>
<td>IMPSEL</td>
<td>Input</td>
<td>IMPSEL input will determine whether the processor uses a 50 Ω or 60 Ω buffer. This pin must be tied to GND on 50 Ω platforms and left as NC on 60 Ω platforms.</td>
</tr>
<tr>
<td>INIT#</td>
<td>Input</td>
<td>INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).</td>
</tr>
<tr>
<td>ITPCLKOUT[1:0]</td>
<td>Output</td>
<td>ITPCLKOUT[1:0] is an uncompensated differential clock output that is a delayed copy of BCLK[1:0], which is an input to the processor. This clock output can be used as the differential clock into the ITP port that is designed onto the motherboard. If ITPCLKOUT[1:0] outputs are not used, they must be terminated properly. Refer to Section 2.5 for additional details and termination requirements. Refer to the ITP 700 Debug Port Design Guide for details on implementing a debug port.</td>
</tr>
<tr>
<td>ITP_CLK[1:0]</td>
<td>Input</td>
<td>ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.</td>
</tr>
<tr>
<td>LINT[1:0]</td>
<td>Input</td>
<td>LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.</td>
</tr>
<tr>
<td>LOCK#</td>
<td>Input/Output</td>
<td>LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.</td>
</tr>
</tbody>
</table>
Table 4-3. Signal Descriptions  (Sheet 6 of 8)

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
</table>
| MCERR#    | Input/Output | MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents.  
MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options:  
- Enabled or disabled.  
- Asserted, if configured, for internal errors along with IERR#.  
- Asserted, if configured, by the request initiator of a bus transaction after it observes an error.  
- Asserted by any bus agent when it observes an error in a bus transaction.  
| PROCHOT#  | Input/Output | As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system deasserts PROCHOT#. See Section 6.3 for more details.  
**NOTE:** The PROCHOT# signal functionality has changed from output to input/output on CPUID 0xF27 and beyond. |
| PWRGOOD   | Input      | PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. ‘Clean’ implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state.  
The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. |
| REQ[4:0]# | Input/Output | REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for details on parity checking of these signals. |
| RESET#    | Input      | Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted.  
A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 6.1.  
This signal does not have on-die termination and must be terminated on the system board. |
| RS[2:0]#  | Input      | RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents. |
RSP# Input
RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents.
A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.

SKTOCC# Output
SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.

SLP# Input
SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will only recognize the assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units.

SMI# Input
SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.

STPCLK# Input
Assertion of STPCLK# (Stop Clock) causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.

TCK Input
TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).

TDI Input
TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.

TDO Output
TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.

TESTHI[12:8] TESTHI[5:0] Input
TESTHI[12:8] and TESTHI[5:0] must be connected to a VCC power source through a resistor for proper processor operation. See Section 2.5 for more details.

THERMDA Other
Thermal Diode Anode. See Section 6.3.1.

THERMDC Other
Thermal Diode Cathode. See Section 6.3.1.
### Table 4-3. Signal Descriptions (Sheet 8 of 8)

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
</table>
| THERMTRIP# | Output | Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level where permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage ($V_{CC}$) must be removed within 0.5 seconds of the assertion of THERMTRIP#. For processors with CPUID of 0xF24:  
  - Once activated, THERMTRIP# remains latched until RESET# is asserted.  
  - While the assertion of the RESET# signal will de-assert THERMTRIP#, if the processor’s junction temperature remains at or above the trip level, THERMTRIP# will again be asserted. For processors with CPUID of 0xF27 and beyond:  
  - Driving of the THERMTRIP# signal is enabled within 10 µs of the assertion of PWRGOOD and is disabled on de-assertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the de-assertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor’s junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 µs of the assertion of PWRGOOD. |
| TMS        | Input  | TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.                                                         |
| TRDY#      | Input  | TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents. |
| TRST#      | Input  | TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 Ω pull-down resistor. |
| VCCA       | Input  | $V_{CCA}$ provides isolated power for the internal processor core PLLs. Refer to the appropriate Platform Design Guide for complete implementation details. |
| VCCIOPPLL  | Input  | $V_{CCIOPPLL}$ provides isolated power for internal processor system bus PLLs. Follow the guidelines for $V_{CCA}$, and refer to the appropriate Platform Design Guide for complete implementation details. |
| VCC_SENSE  | Output | $V_{CC\_SENSE}$ is an isolated low impedance connection to processor core power ($V_{CC}$). It can be used to sense or measure power near the silicon with little noise. |
| VCCVID     | Input  | Independent 1.2 V supply must be routed to VCCVID pin for the Pentium 4 processor on 0.13 micron process’s Voltage Identification circuit. |
| VID[4:0]   | Output | VID[4:0] (Voltage ID) pins are used to support automatic selection of power supply voltages ($V_{CC}$). Unlike previous generations of processors, these are open drain signals that are driven by the Pentium 4 processor on 0.13 micron process and must be pulled up to 3.3 V (max.) with 1 kΩ resistors. The voltage supply for these pins must be valid before the VR can supply $V_{CC}$ to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2-2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself. |
| VSSA       | Input  | $V_{SSA}$ is the isolated ground for internal PLLs.                                                                                       |
| VSS_SENSE  | Output | $V_{SS\_SENSE}$ is an isolated low impedance connection to processor core $V_{SS}$. It can be used to sense or measure ground near the silicon with little noise. |
This page is intentionally left blank.
The Pentium 4 processor on 0.13 micron process uses an Integrated Heat Spreader (IHS) for heatsink attachment that is intended to provide for multiple types of thermal solutions. This chapter provides data necessary for development of a thermal solution. See Figure 5-1 for an enlarged view of an example of the Pentium 4 processor on 0.13 micron process thermal solution. This is for illustration purposes only. For further thermal solution design details, refer to the Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines.

Note: The processor is shipped either by itself or with a heatsink for boxed processors. See Chapter 7 for details on boxed processors.

Figure 5-1. Example Thermal Solution (Not to Scale)
5.1 Processor Thermal Specifications

The Pentium 4 processor on 0.13 micron process requires a thermal solution to maintain temperatures within the operating limits as set forth in Section 5.1.1. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component-level thermal solutions can include active or passive heatsinks attached to the processor IHS. Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines.

5.1.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum case temperature ($T_C$) specifications when operating at or below the Thermal Design Power (TDP) value listed per frequency in Table 5-1. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the appropriate processor thermal design guidelines.

The case temperature is defined at the geometric top center of the processor IHS. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained periods of time. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 5-1 instead of the maximum processor power consumption. The Thermal Monitor feature is intended to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 6.3. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with a lower thermal dissipation is currently planned. In all cases, the Thermal Monitor feature must be enabled for the processor to remain within specification.
<table>
<thead>
<tr>
<th>Front Side Bus Frequency</th>
<th>Processor and Core Frequency</th>
<th>Thermal Design Power</th>
<th>Minimum $T_C$ ($°C$)</th>
<th>Maximum $T_C$ ($°C$)</th>
<th>Notes $^3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>400 MHz</td>
<td>Processors with VID=1.500 V</td>
<td>2A GHz</td>
<td>52.4</td>
<td>5</td>
<td>68</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.20 GHz</td>
<td>55.1</td>
<td>5</td>
<td>69</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.40 GHz</td>
<td>57.8</td>
<td>5</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.50 GHz</td>
<td>59.3</td>
<td>5</td>
<td>71</td>
</tr>
<tr>
<td></td>
<td>Processors with VID=1.525 V</td>
<td>2A GHz</td>
<td>54.3</td>
<td>5</td>
<td>69</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.20 GHz</td>
<td>57.1</td>
<td>5</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.40 GHz</td>
<td>59.8</td>
<td>5</td>
<td>71</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.50 GHz</td>
<td>61.0</td>
<td>5</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.60 GHz</td>
<td>62.6</td>
<td>5</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>Processors with multiple VIDs</td>
<td>2A GHz</td>
<td>54.3</td>
<td>5</td>
<td>69</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.20 GHz</td>
<td>57.1</td>
<td>5</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.40 GHz</td>
<td>59.8</td>
<td>5</td>
<td>71</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.50 GHz</td>
<td>61.0</td>
<td>5</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.60 GHz</td>
<td>62.6</td>
<td>5</td>
<td>72</td>
</tr>
<tr>
<td>533 MHz</td>
<td>Processors with VID=1.500 V</td>
<td>2.26 GHz</td>
<td>56.0</td>
<td>5</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.40B GHz</td>
<td>57.8</td>
<td>5</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.53 GHz</td>
<td>59.3</td>
<td>5</td>
<td>71</td>
</tr>
<tr>
<td></td>
<td>Processors with VID=1.525 V</td>
<td>2.26 GHz</td>
<td>58.0</td>
<td>5</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.40B GHz</td>
<td>59.8</td>
<td>5</td>
<td>71</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.53 GHz</td>
<td>61.5</td>
<td>5</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.66 GHz</td>
<td>66.1</td>
<td>5</td>
<td>74</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.80 GHz</td>
<td>68.4</td>
<td>5</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td>Processors with multiple VIDs</td>
<td>2.26 GHz</td>
<td>58.0</td>
<td>5</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.40B GHz</td>
<td>59.8</td>
<td>5</td>
<td>71</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.53 GHz</td>
<td>61.5</td>
<td>5</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.66 GHz</td>
<td>66.1</td>
<td>5</td>
<td>74</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.80 GHz</td>
<td>68.4</td>
<td>5</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.06 GHz</td>
<td>81.8</td>
<td>5</td>
<td>68</td>
</tr>
<tr>
<td>800 MHz FSB with 512-KB L2 Cache Only</td>
<td>Processors with multiple VIDs</td>
<td>2.40C GHz</td>
<td>66.2</td>
<td>5</td>
<td>74</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.60C GHz</td>
<td>69.0</td>
<td>5</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.80C GHz</td>
<td>69.7</td>
<td>5</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.0 GHz</td>
<td>81.9</td>
<td>5</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.20C GHz</td>
<td>82.0</td>
<td>5</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.40 GHz</td>
<td>89.0</td>
<td>5</td>
<td>68</td>
</tr>
<tr>
<td>800 MHz FSB with 2-MB L3 Cache</td>
<td>Processors with multiple VIDs</td>
<td>3.20 GHz</td>
<td>92.1</td>
<td>5</td>
<td>64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.40 GHz</td>
<td>102.9</td>
<td>5</td>
<td>67</td>
</tr>
</tbody>
</table>
NOTES:
1. These values are specified at \( V_{CC_{\text{MAX}}} \) for the processor. Systems must be designed to ensure that the processor is not subjected to any static \( V_{CC} \) and \( I_{CC} \) combination wherein \( V_{CC} \) exceeds \( V_{CC_{\text{MAX}}} \) at specified \( I_{CC} \). Refer to loadline specifications in Chapter 2.
2. The numbers in this column reflect Intel’s recommended design point and are not indicative of the maximum power the processor can dissipate under worst case conditions. For more details, refer to the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines*.
3. TDP and \( T_{C} \) are specified for highest VID only. Processors will be shipped under multiple VIDs for each frequency; however, the TDP and \( T_{C} \) specifications will be the same as highest VID specified in the table.

### 5.1.2 Thermal Metrology

#### 5.1.2.1 Processor Case Temperature Measurement

The maximum and minimum case temperature \( (T_{C}) \) for the Pentium 4 processor on 0.13 micron process is specified in Table 5-1. This temperature specification is meant to help ensure proper operation of the processor. Figure 5-2 illustrates where Intel recommends \( T_{C} \) thermal measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the *Intel® Pentium® Processor 4 with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines*.

*Figure 5-2. Guideline Locations for Case Temperature (\( T_{C} \)) Thermocouple Placement*
6.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Pentium 4 processor on 0.13 micron process samples hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, refer to Table 6-1.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor; for reset purposes, the processor does not distinguish between a “warm” reset and a “power-on” reset.

Table 6-1. Power-On Configuration Option Pins

<table>
<thead>
<tr>
<th>Configuration Option</th>
<th>Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output tristate</td>
<td>SMI#</td>
</tr>
<tr>
<td>Execute BIST</td>
<td>INIT#</td>
</tr>
<tr>
<td>In Order Queue pipelining (set IOQ depth to 1)</td>
<td>A7#</td>
</tr>
<tr>
<td>Disable MCERR# observation</td>
<td>A9#</td>
</tr>
<tr>
<td>Disable BINIT# observation</td>
<td>A10#</td>
</tr>
<tr>
<td>APIC Cluster ID (0-3)</td>
<td>A[12:11]#</td>
</tr>
<tr>
<td>Disable bus parking</td>
<td>A15#</td>
</tr>
<tr>
<td>Disable Hyper-Threading Technology</td>
<td>A31#</td>
</tr>
<tr>
<td>Symmetric agent arbitration ID</td>
<td>BR0#</td>
</tr>
</tbody>
</table>

NOTE:
1. Asserting this signal during RESET# will select the corresponding option.

6.2 Clock Control and Low Power States

The use of AutoHALT, Stop-Grant, and Sleep states is allowed in Pentium 4 processor on 0.13 micron process-based systems to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 6-1 for a visual representation of the processor low power states.

6.2.1 Normal State—State 1

This is the normal operating state for the processor.
6.2.2 AutoHALT Powerdown State—State 2

AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel® Architecture Software Developer’s Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power Down state, the processor will process bus snoops and interrupts.

**Figure 6-1. Stop Clock State Machine**

- **1. Normal State**
  - Normal execution.
  - BCLK running.
  - STPCLK# asserted.

- **2. Auto HALT Power Down State**
  - BCLK running.
  - Snoop and interrupts allowed.
  - Snoop Event Occurs
  - STPCLK# asserted

- **3. Stop Grant State**
  - BCLK running.
  - Snoop service snoops to caches.

- **4. HALT/Grant Snoop State**
  - BCLK running.
  - Service snoops to caches.

- **5. Sleep State**
  - BCLK running.
  - No snoops and interrupts allowed.

**Table:**

<table>
<thead>
<tr>
<th>Snoop Event</th>
<th>Occurs</th>
<th>serviced</th>
</tr>
</thead>
<tbody>
<tr>
<td>HALT Instruction and HALT Bus Cycle generated</td>
<td>INIT#, BINIT#, INTR, NMI, SM#, RESET#</td>
<td></td>
</tr>
<tr>
<td>STPCLK# Asserted</td>
<td>STPCLK# De-asserted</td>
<td></td>
</tr>
<tr>
<td>Snoop Event</td>
<td>Snoop Event serviced</td>
<td></td>
</tr>
<tr>
<td>Snoop event occurs</td>
<td>Snoop event serviced</td>
<td></td>
</tr>
<tr>
<td>SLP# Asserted</td>
<td>SLP# De-asserted</td>
<td></td>
</tr>
</tbody>
</table>
6.2.3 Stop-Grant State—State 3

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to VCC) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should only be de-asserted one or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 6.2.4). A transition to the Sleep state (see Section 6.2.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process snoops on the system bus and it will latch interrupts delivered on the system bus.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

6.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop or interrupt transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the system bus has been serviced (whether by the processor or other agent on the system bus) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.
6.2.5 **Sleep State—State 5**

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can be entered only from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should be asserted only when the processor is in the Stop-Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification, and may result in unapproved operation.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state and is held active as specified in the RESET# pin specification, the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure that the processor correctly executes the Reset sequence.

Once in the Sleep state, the SLP# pin must be de-asserted if another asynchronous system bus event needs to occur. The SLP# pin has a minimum assertion of one BCLK period.

When the processor is in Sleep state, it will not respond to interrupts or snoop transactions.

6.3 **Thermal Monitor**

The Thermal Monitor feature helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption by modulating (starting and stopping) the internal processor core clocks. The Thermal Monitor feature must be enabled for the processor to be operating within specifications. The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor feature is enabled, and a high temperature situation exists (i.e., TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30–50%). Clocks often will not be off for more than 3.0 µs when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may
cause a noticeable performance loss, and in some cases may result in a $T_C$ that exceeds the
specified maximum temperature and may affect the long-term reliability of the processor. In
addition, a thermal solution that is significantly under-designed may not be capable of cooling the
processor even when the TCC is active continuously. Refer to the *Intel® Pentium® 4 Processor
with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines* for information on
designing a thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and
cannot be modified. The Thermal Monitor does not require any additional hardware, software
drivers, or interrupt handling routines.

The TCC may also be activated via On-Demand mode. If bit 4 of the ACPI Thermal Monitor
Control Register is written to a 1, the TCC will be activated immediately independent of the
processor temperature. When using On-Demand mode to activate the TCC, the duty cycle of the
clock modulation is programmable via bits 3:1 of the same ACPI Thermal Monitor Control
Register. In automatic mode, the duty cycle is fixed. However, in On-Demand mode, the duty cycle
can be programmed from 12.5% on/87.5% off, to 87.5% on/12.5% off in 12.5% increments.
On-Demand mode may be used at the same time Automatic mode is enabled. However, if the
system tries to enable the TCC via On-Demand mode at the same time automatic mode is enabled
AND a high temperature condition exists, the duty cycle of the automatic mode will override the
duty cycle selected by the On-Demand mode.

An external signal, PROCHOT# (processor hot), is asserted when the processor detects that its
temperature is at the thermal trip point. Bus snooping and interrupt latching are also active while
the TCC is active. The temperature at which the thermal control circuit activates is not user
configurable and is not software visible.

Besides the thermal sensor and TCC, the Thermal Monitor feature also includes one ACPI register,
performance monitoring logic, bits in three model specific registers (MSR), and one I/O pin
(PROCHOT#). All are available to monitor and control the state of the Thermal Monitor feature.
Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of
PROCHOT#.

If automatic mode is disabled, the processor will be operating out of specification. Regardless of
enabling of the automatic or On-Demand modes, in the event of a catastrophic cooling failure the
processor automatically shuts down when the silicon has reached a temperature of approximately
135 °C. At this point the system bus signal THERMTRIP# goes active and stays active until
RESET# has been initiated. THERMTRIP# activation is independent of processor activity and
does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage ($V_{CC}$) must
be removed within 0.5 seconds.
6.3.1 Thermal Diode

The Pentium 4 processor on 0.13 micron process incorporates an on-die thermal diode. A thermal sensor located on the system board may monitor the die temperature of the processor for thermal management/long term die temperature change purposes. Table 6-2 and Table 6-3 provide the diode parameter and interface specifications. This thermal diode is separate from the Thermal Monitor’s thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 6-2. Thermal Diode Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>IFW</td>
<td>Forward Bias Current</td>
<td>5</td>
<td>300</td>
<td></td>
<td>µA</td>
<td>1</td>
</tr>
<tr>
<td>n</td>
<td>Diode Ideality Factor</td>
<td>1.0011</td>
<td>1.0021</td>
<td>1.0030</td>
<td></td>
<td>2,3,4</td>
</tr>
<tr>
<td>RT</td>
<td>Series Resistance</td>
<td>3.64</td>
<td></td>
<td></td>
<td>Ω</td>
<td>2,3,4,5</td>
</tr>
</tbody>
</table>

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized at 75 °C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
   \[ I_{FW} = I_S (e^{q(V_D/kT)} - 1) \]
   Where \( I_S \) = saturation current, \( q \) = electronic charge, \( V_D \) = voltage across the diode, \( k \) = Boltzmann Constant, and \( T \) = absolute temperature (Kelvin).
5. The series resistance, \( R_T \), is provided to allow for a more accurate measurement of the diode junction temperature. \( R_T \) as defined includes the pins of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. \( R_T \) can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:
   \[ T_{error} = \frac{R_T(N-1)I_{FWmin}}{(nk/q)*ln N} \]
   Where \( T_{error} \) = sensor temperature error, \( N \) = sensor current ratio, \( k \) = Boltzmann Constant, \( q \) = electronic charge.

Table 6-3. Thermal Diode Interface

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>THERMDA</td>
<td>B3</td>
<td>diode anode</td>
</tr>
<tr>
<td>THERMDC</td>
<td>C4</td>
<td>diode cathode</td>
</tr>
</tbody>
</table>
7.1 Introduction

The Pentium 4 processor on 0.13 micron process will also be offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Pentium 4 processor on 0.13 micron process will be supplied with a cooling solution. This chapter documents motherboard and system requirements for the cooling solution that will be supplied with the boxed Pentium 4 processor on 0.13 micron process. This chapter is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and inches [in brackets]. Figure 7-1 shows a mechanical representation of a boxed Pentium 4 processor on 0.13 micron process.

Note: Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designer's responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platform and chassis. Refer to the Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines for further guidance.

Figure 7-1. Mechanical Representation of the Boxed Processor

NOTE: The airflow is into the center and out of the sides of the fan heatsink.
7.2 Mechanical Specifications

7.2.1 Boxed Processor Cooling Solution Dimensions

This section describes the mechanical specifications of the boxed Pentium 4 processor on 0.13 micron process. The boxed processor will be shipped with an unattached fan heatsink. Figure 7-1 shows a mechanical representation of the boxed Pentium 4 processor on 0.13 micron process.

Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor with assembled fan heatsink are shown in Figure 7-2 (Side Views), and Figure 7-3 (Top View). The airspace requirements for the boxed processor fan heatsink must also be incorporated into new motherboard and system designs. Airspace requirements are shown in Figure 7-6 and Figure 7-7. Note that some figures have centerlines shown (marked with alphabetic designations) to clarify relative dimensioning.

Figure 7-2. Side View Space Requirements for the Boxed Processor
7.2.2 Boxed Processor Fan Heatsink Weight

The boxed processor fan heatsink will not weigh more than 450 grams. See Chapter 5 and the Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines for details on the processor weight and heatsink requirements.

7.2.3 Boxed Processor Retention Mechanism and Heatsink Assembly

The boxed processor thermal solution requires a processor retention mechanism and a heatsink attach clip assembly to secure the processor and fan heatsink in the baseboard socket. The boxed processor will not ship with retention mechanisms but will ship with the heatsink attach clip assembly. Motherboards designed for use by system integrators should include the retention mechanism that supports the boxed Pentium 4 processor on 0.13 micron process. Motherboard documentation should include appropriate retention mechanism installation instructions.

**Note:** The processor retention mechanism based on the Intel reference design should be used to ensure compatibility with the heatsink attach clip assembly and the boxed processor thermal solution. The heatsink attach clip assembly is latched to the retention tab features at each corner of the retention mechanism.
The target load applied by the clips to the processor heat spreader for Intel’s reference design is $75 \pm 15$ lbf (maximum load is constrained by the package load capability). It is normal to observe a bow or bend in the board due to this compressive load on the processor package and the socket. The level of bow or bend depends on the motherboard material properties and component layout. Any additional board stiffening devices such as plates are not necessary and should not be used along with the reference mechanical components and boxed processor. Using such devices increase the compressive load on the processor package and socket, likely beyond the maximum load that is specified for those components. Refer to the Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines for details on the Intel reference design.

7.3 Electrical Requirements

7.3.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable will be shipped with the boxed processor to draw power from a power header on the motherboard. The power cable connector and pinout are shown in Figure 7-4. Motherboards must provide a matched power header to support the boxed processor. Table 7-1 contains specifications for the input and output signals at the fan heatsink connector. The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides $V_{OH}$ to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

**Note:** The motherboard must supply a constant +12 V to the processor’s power header to ensure proper operation of the variable speed fan for the boxed processor.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 7-5 shows the location of the fan power connector relative to the processor socket. The motherboard power header should be positioned within 4.33 inches from the center of the processor socket.

**Figure 7-4. Boxed Processor Fan Heatsink Power Cable Connector Description**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>+12V</td>
</tr>
<tr>
<td>3</td>
<td>SENSE</td>
</tr>
</tbody>
</table>

Straight square pin, 3-pin terminal housing with polarizing ribs and friction locking ramp.

0.100" pin pitch, 0.025" square pin width.

Waldom/Molex P/N 22-01-3037 or equivalent.

Match with straight pin, friction lock header on motherboard Waldom/Molex P/N 22-23-2031, AMP P/N 640465-3, or equivalent.
Table 7-1. Fan Heatsink Power and Signal Specifications

<table>
<thead>
<tr>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>+12 V: 12 Volt fan power supply</td>
<td>10.2</td>
<td>12</td>
<td>13.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IC: Fan current draw</td>
<td></td>
<td></td>
<td>740</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>SENSE: SENSE frequency</td>
<td>2</td>
<td></td>
<td></td>
<td>pulses per fan revolution</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTE:
1. Motherboard should pull this pin up to V_{CC} with a resistor.

Figure 7-5. MotherBoard Power Header Placement Relative to Processor Socket
7.4 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processor.

7.4.1 Boxed Processor Cooling Requirements

The boxed processor may be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and is ultimately the responsibility of the system integrator. The processor temperature specification is found in Chapter 5. The boxed processor fan heatsink is able to keep the processor temperature within the specifications (see Table 5-1) in chassis that provide good thermal management. For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink be unimpeded. Airflow is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 7-6 and Figure 7-7 illustrate an acceptable airspace clearance for the fan heatsink. The air temperature entering the fan should be kept below 40 °C. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

Figure 7-6. Boxed Processor Fan Heatsink Airspace Keep-Out Requirements (Side 1 View)
7.4.2 Variable Speed Fan

The boxed processor fan will operate at different speeds over a short range of internal chassis temperatures. This allows the processor fan to operate at a lower speed and noise level, while internal chassis temperatures are low. If internal chassis temperature increases beyond a lower set point, the fan speed will rise linearly with the internal temperature until the higher set point is reached. At that point, the fan speed is at its maximum. As fan speed increases, so does fan noise levels. Systems should be designed to provide adequate air around the boxed processor fan heatsink that remains below the lower set point. These set points, represented in Figure 7-8 and Table 7-2, can vary by a few degrees from fan heatsink to fan heatsink. The internal chassis temperature should be kept below 38 °C. Meeting the processor’s temperature specification (see Chapter 5) is the responsibility of the system integrator.
Table 7-2. Boxed Processor Fan Heatsink Set Points

<table>
<thead>
<tr>
<th>Boxed Processor Fan Heatsink Set Point (°C)</th>
<th>Boxed Processor Fan Speed</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boxed Intel® Pentium® 4 Processors 2.80 GHz (and below)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X ≤ 33</td>
<td>When the internal chassis temperature is below or equal to this set point, the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment.</td>
<td>1</td>
</tr>
<tr>
<td>Y = 40</td>
<td>When the internal chassis temperature is at this point, the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst-case operating environment.</td>
<td></td>
</tr>
<tr>
<td>Z ≥ 43</td>
<td>When the internal chassis temperature is above or equal to this set point, the fan operates at its highest speed.</td>
<td>1</td>
</tr>
<tr>
<td>Boxed Intel® Pentium® 4 Processors 3 GHz (and above)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X ≤ 32</td>
<td>When the internal chassis temperature is below or equal to this set point, the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment.</td>
<td>1</td>
</tr>
<tr>
<td>Y = 38</td>
<td>When the internal chassis temperature is at this point, the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst-case operating environment.</td>
<td></td>
</tr>
<tr>
<td>Z ≥ 40</td>
<td>When the internal chassis temperature is above or equal to this set point, the fan operates at its highest speed.</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTE:

1. Set point variance is approximately ± 1 °C from fan heatsink to fan heatsink.
Refer to the ITP 700 Debug Port Design Guide and the appropriate platform design guidelines for more detailed information regarding debug tools specifications (such as integration details).

8.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Pentium 4 processors on 0.13 micron process systems. Tektronix and Agilent should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of the Pentium 4 processor on 0.13 micron process systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a Pentium 4 processor on 0.13 micron process system that can make use of an LAI: mechanical and electrical.

8.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the Pentium 4 processor on 0.13 micron process heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

8.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.