Intel® Pentium® 4 Processor in the 478-pin Package / Intel® 850 Chipset Family Platform

Design Guide

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Revision History

Rev	Description	Date
-001	• Initial revision.	August 2001
-002	• Added ICH2 RTC Section 9.8.8 Power-well Isolation Control • Added ICH2 RTC Section 9.8.9 Power Supply PS_ON Considerations • Replaced ICH2 LAN Figure 121 Trace Routing • Added ICH2 LAN Section 9.9.5 82562ET/EM Disable Guidelines • Added ICH2 LAN Section 9.9.6 82562ET/82562EH Dual Footprint Guidelines • Added ICH2 Section 9.10 FWH Guidelines • Updated ICH2 Section 12.6 ICH2 5VREF and Vcc3.3 Sequencing Requirement • Updated ICH2 Schematic Checklist Section 15.7.12 RTC • Updated processor VCCVID recommendations – includes design guide and schematic update. • Updated processor TESTHI pin recommendations. • Updated BCLK[1:0] frequency strapping recommendations. • Clarified requirements for pull-ups on VID[4:0]. • Updated processor system bus topologies for RESET# and BR0#.	January 2002
-003	• Revised paragraph 3 in Section 12.6 ICH2 V5REF and VCC3_3 Sequencing Requirement • Revised APIC in Section 15.7.6 Interrupt Interface in the Schematics Checklist • Revised V5REF_SUS in Section 15.7.15 Power in the Schematics Checklist • Revised 'Other Recommendations' in Section 11.4, Filter Specifications for VCCA, VCCIOPLL, and VSSA	February 2002
-004	• Editing/formatting throughout for clarity • Combined Chapters 1, 2, 3, and 4 into the Introduction Chapter.	March 2002
-005	• Renamed to 850 chipset family • Added 82850E / 533MHz system bus design guidelines • Added 4 Layer guidelines	May 2002
-006	• Added 82850E 533MHz (PC1066) RDRAM guidelines: • Revised Table 22 in Rambus Signaling Levels in Section 6.1.1 • Added Differential Clock Guidelines for Stripline and Microstrip in Section 6.1.2.3 • Added Direct RDRAM Reference Voltage in Section 6.1.4 • Added Section 6.1.8, RDRAM Channel Margin Improvement • Added Section 6.1.9, 533 MHz (PC1066) RIMM Thermal Consideration • Revised Section 15.6, Rambus RIMM* Connector Checklist	Oct 2002
-007	• Added FMB2 design guidelines into Section 11	Jan 2003
-008	• Separated FMB1 and FMB2 design guidelines	Jan 2003

1 Introduction

In this document when a reference is made to the processor and/or the Intel® Pentium® 4 processor in the 478-pin package, it is intended that this includes the Intel® Pentium® 4 processor in the 478-pin package, and the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process. Where a reference is intended to refer to a specific processor, the specific processors will be listed separately.

This design guide supports the following processors:

- Intel® Pentium® 4 processor in the 478-pin package
- Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process

This design guide documents Intel's design recommendations for systems based on the Pentium 4 processor in the 478-pin package with the Intel® 850 chipset family, which consists of the Intel® 82850 (MCH) and the Intel® 82801BA (ICH2), or the Intel® 82850E (MCH) and the Intel® 82801BA (ICH2). Unless otherwise specified, references to the 850 chipset, 850 MCH, 850 system, or 850 platform refer to both the 82850 and the 82850E chipset. Specific design considerations for 300 MHz /400 MHz Rambus RDRAM* technology versus 533 MHz RDRAM technology are documented separately as required. Design issues such as thermal considerations should be addressed using specific design guides or applications notes for the processor and 850 chipset.

Carefully follow the design information, board schematics, and debug recommendations presented in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two categories below.

- *Design Recommendations* are items based on Intel's simulations and lab experience to date and are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- *Design Considerations* are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as an example, but may not be applicable to particular designs.

Note: The guidelines recommended in this document are based on experience and simulation work done at Intel while developing the processor and 850 chipset based systems.

Platform schematics are shown in Appendix A, and are intended as a reference for board designers. While the schematics may cover a specific design, the core schematics will remain the same for most platforms. The schematic set provides a reference schematic for each platform component as well as common system board options. Additional flexibility is possible through other permutations of these options and components.

1.1 Related Documentation

Refer to the following documents or models for more information. All Intel issued documentation revision numbers are subject to change, and the latest revision should be used. The specific revision numbers referenced should be used for all documents not released by Intel.

- *ITP700 Debug Port Design Guide*
- *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines*
- *Intel® Pentium® 4 Processor 478 Pin Socket (mPGA478) Design Guidelines*
- *Intel® Pentium® 4 Processor in the 478-pin Package* datasheet
- *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process* datasheet
- *Intel® Pentium® 4 Processor in the 478-pin Package I/O Buffer[1] Models*
- *Intel® Pentium® 4 Processor VR Down Design Guidelines*
- *Intel® 850 Chipset Family82850/82850E Memory Controller Hub (MCH) Datasheet*
- *Intel® 850 Chipset Family: 82850/82850E Memory Controller Hub (MCH) Specification Update*
- *Intel® 850 Chipset: Thermal Considerations Application Note (AP-720)*
- *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet*
- *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Specification Update*
- *Communication and Network Riser (CNR) Specification, Revision 1.0*
- *AC '97 Component Specification, Revision 2.1*
- *Accelerated Graphics Port Interface Specification, Revision 2.0*
- *Low Pin Count Interface Specification, Revision 1.0*
- *PCI Local Bus Specification, Revision 2.2*
- *PCI-PCI Bridge Specification, Revision 1.0*
- *PCI Bus Power Management Interface Specification, Revision 1.0*
- *Universal Serial Bus Specification, Revision 1.1*
- *Rambus RDRAM* technology documentation*
- *Advanced Configuration and Power Interface Specification (ACPI), Revision 1.0b*
- *PC '01 Specification*
- *CK00 Clock Synthesizer/Driver Design Guidelines Specification, Revision 1.0*
- *CK00-E Clock Synthesizer/Driver Design Guidelines Specification, Revision 1.0*

Note: [1]The I/O Buffer Models are in IBIS format.

1.2 Conventions and Terminology

This section defines conventions and terminology that will be used throughout this document.

Table 1. Platform Conventions and Terminology

Term	Definition
Aggressor	A network that transmits a coupled signal to another network is the aggressor network.
AGTL+	The processor System Bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors that provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted simultaneously to have the best or worst impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. Performance of an electronic component may change as a result of (including, but not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. The “slow” corner is defined as a component operating at its slowest, weakest drive strength performance. The “fast” corner is defined as a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk – coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. • Forward Crosstalk – coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal. • Even Mode Crosstalk – coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk – coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be: • Time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer’s conditions required for AC timing specifications; e.g., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver’s AC timings. • Maximum and Minimum Flight Time – Flight time variations can be caused by many different variables. The causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some other causes include effects of Simultaneous Switching Output (SSO) and packaging effects. • Maximum flight time is the largest acceptable flight time a network will experience under all variations of conditions. • Minimum flight time is the smallest acceptable flight time a network will experience under all variations of conditions.

Term	Definition
GTL+	GTL+ is the bus technology used by the Intel Pentium Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) bus technology.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between one agent pin and the corresponding agent pin at the far end of the bus.
Overshoot	Maximum voltage observed for a signal at the device pad.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
Pin	The contact point of a component package to the traces on the system board. Signal quality and timings can be measured at the pin.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the microprocessor bus of the Intel Pentium 4 processor. The System Bus is not compatible with the P6 bus protocol.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or “push-out”), or a decrease in propagation delay (or “pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below VSS at the device pad.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
V_{REF} Guardband	A guardband defined above and below V_{REF} to provide a more realistic model accounting for noise such as V_{TT} and V_{REF} variation.

1.3 System Overview

The Pentium 4 processor in the 478-pin package with the Intel 850 chipset family delivers Intel's highest performance desktop platform to date. The processor, chipset, and memory are balanced to provide the best possible performing systems.

1.3.1 Intel® Pentium® 4 Processor in the 478-pin Package

This processor has a number of features that significantly increase its performance from previous generation IA-32 processors. The Intel® NetBurst™ microarchitecture includes a number of new features as well as some improvements on existing features.

Intel NetBurst microarchitecture features include hyper-pipelined technology, rapid execution engine, 400 MHz system bus, and execution trace cache. The hyper pipelined technology doubles the pipeline depth over the previous generation of processors allowing the processor to reach much higher core frequencies. The rapid execution engine allows the 2 integer ALUs in the processor to run at twice the core frequency that allows many integer instructions to execute in 1/2 clock tick. The 400 MHz system bus is a quad-pumped bus running off a 100 MHz system clock making 3.2 GB/sec data transfer rates possible. The execution trace cache is a level 1 cache that stores approximately 12k decoded micro-operations, which removes the decoder from the main execution path, thereby increasing performance.

Improved features within the Intel NetBurst microarchitecture include the advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 256 KB (512 KB for the Intel Pentium 4 processor with 512-KB L2 cache on 0.13 micron process), on-die level 2 cache with an increased bandwidth over previous micro-architectures. The floating point and multi-media units have been improved by making the registers 128 bits wide and adding a separate register for data movement. Finally, SSE2 adds 144 new instructions for double precision floating point, SIMD integer, and memory management.

This processor supports uni-processor configurations only. The same manageability features, which are included in Intel Pentium III processors, are included on the Pentium 4 processor in the 478-pin package with the addition of thermal monitor. Thermal monitor allows systems to be designed for anticipated processor thermals as opposed to worst case with no performance degradation expected.

1.3.2 Intel® 850 Chipset

The Intel 850 chipset consists of two main components: The Memory Controller Hub (MCH), and the IO Controller Hub (ICH2). These components are interconnected via an Intel proprietary interface called hub interface. The hub interface is designed into the Intel 850 chipset to provide efficient communication between components.

Additional hardware platform features include AGP 4X mode, RDRAM technology, Ultra ATA/100, Low Pin Count interface (LPC), integrated LAN and Universal Serial Bus 1.1 (USB). The platform is also ACPI compliant and supports *Full-on, Stop Grant, Suspend to RAM, Suspend to Disk,* and *Soft-off* power management states. Through the use of an appropriate LAN connection, the platform supports *Wake-on-LAN** for remote administration and troubleshooting.

1.3.2.1 Intel® 82850/82850E Memory Controller Hub (MCH)

The MCH component provides the processor interface, Direct RDRAM device interface, AGP interface and hub interfaces in an Intel 850 chipset platform.

The MCH is in a 615-ball OLGA package and has the following functionality:

- Supports a single processor with a data transfer rate of 400 MHz (82850)
- Supports a single processor with a data transfer rate of 533 MHz (82850E)
- Dual Rambus channels support 300 MHz and 400 MHz RDRAM technology (82850)
- Dual Rambus channels support 400 MHz and 533 MHz RDRAM technology (82850E)
- AGTL+ host bus with integrated termination supporting 32-bit host addressing
- 1.5 V AGP interface with 4x SBA/data transfer and 2x/4x fast write capability
- 8-bit, 66 MHz 4x hub interface to ICH2

1.3.2.2 Intel® ICH2

The ICH2 provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many widely utilized I/O functions.

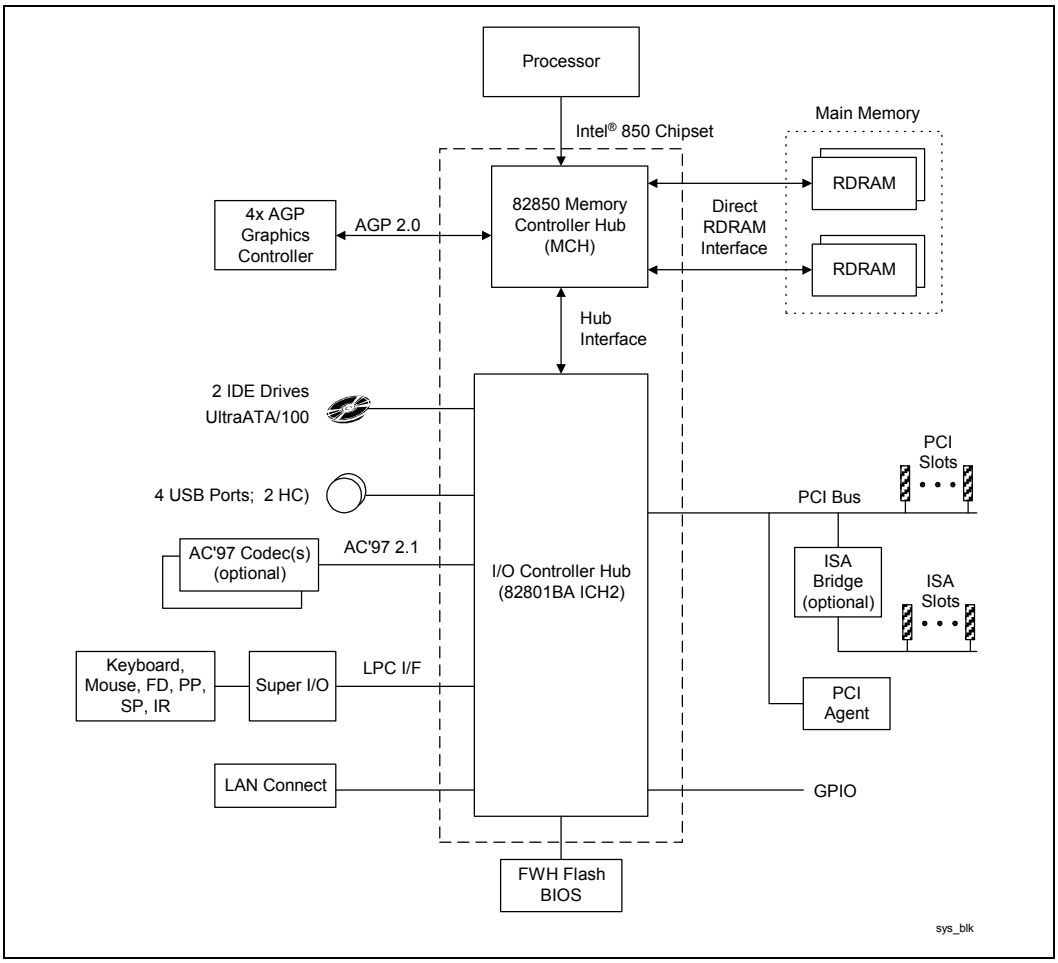
The ICH2 is in a 360 ball EBGA package and contains the following functionality:

- PCI 2.2 bus interface at 33 MHz, 133 MB/s maximum throughput
- Supports up to 6 PCI master devices
- LAN controller with 10/100 Mbit/s Ethernet and 1 Mbit/s HomePDA* support
- Low pin count (LPC) interface
- Firmware Hub (FWH) interface
- 82C54 based timer
- IDE controller with support for Ultra ATA 100/66/33
- Two USB controllers for a total of four ports
- Enhanced DMA controller with support for REQ#/GNT# pairs, LPC DMA, Type F DMA
- SMBus interface
- AC-link for external audio and telephony CODECs

1.3.3 System Configurations

Figure 1 illustrates a typical processor and Intel 850 chipset-based system configuration for professional and high performance desktops using the Pentium 4 processor in the 478-pin package.

Figure 1.Typical System Configuration



1.4 Platform Initiatives

1.4.1 Intel® 850 Chipset

1.4.1.1 Rambus Direct RDRAM* Device Interface

The Direct RDRAM device interface provides the necessary memory bandwidth to obtain optimal performance from the processor as well as a high-performance AGP graphics controller. The MCH Direct RDRAM device interface supports 300 MHz, 400 MHz and 533 MHz operation, delivering up to 3.2 GB/s of theoretical memory bandwidth using two Direct Rambus channels operating in lock step. Coupled with the greater bandwidth, the heavily pipelined RDRAM technology protocol, a substantially more efficient data transfer is achieved.

In addition to the RDRAM device performance features, this new memory architecture provides enhanced power management capabilities. The *powerdown* mode of operation will enable Intel 850 chipset based systems to cost effectively support the *suspend-to-RAM* sleep state.

Industry leading DRAM vendors have agreed to develop RDRAM devices and module vendors will be developing RDRAM Inline Memory Modules. Rambus RIMM* modules are approximately the same form factor as SDRAM DIMMs.

The 64-Mb, 128-Mb and 256-Mb/288-Mb RDRAM technologies will be supported by Intel 850 chipset-based platforms.

1.4.1.2 Accelerated Graphics Port (AGP)

AGP is a high performance, component level interconnect targeted at 3D graphical display applications. AGP is based on a set of performance extensions or enhancements to the PCI bus. The Intel 850 chipset employs an AGP interface that is optimized for a point-to-point topology using 1.5 V signaling in 4x mode. The 4x mode provides a peak bandwidth of 1066 MB/s.

For additional information, refer to the *Accelerated Graphics Port Interface Specification*, Revision *2.0*, which is located at the following URL: http://www.agpforum.org/specs_specs.htm.

1.4.2 Intel® ICH2

1.4.2.1 Integrated LAN Controller

The ICH2 incorporates an integrated LAN Controller. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers processor utilization by off-loading communication tasks from the processor.

The ICH2 functions with several options of LAN connect components to target the desired market segment. The *82562EH* component provides a *HomePNA* 1Mbit/sec connection. The *82562ET* component provides a basic Ethernet 10/100 connection. The *82562EM* component provides an Ethernet 10/100 connection with the added flexibility of *Alert on LAN**. More advanced LAN solutions can be implemented with the 82550 or other PCI based product offerings.

1.4.2.2 Intel® AC'97 6-Channel Support

The *Audio Codec '97* (AC'97) Specification defines a digital link that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC), or both an AC and an MC. The AC'97 Specification defines the interface between the system logic and the audio or modem codec known as the *AC-link*.

The ICH2 AC'97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC-link. Using the ICH2 integrated AC-link reduces cost and eases migration from ISA.

By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio on the Intel 850 chipset platform. In addition, an AC'97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC'97. The ICH2 integrated digital link allows two external codecs to be connected to the ICH2 in several configurations. Refer to Table 2 for the various Intel AC'97 codec implementations.

Table 2. Intel® ICH2 Codec Options

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio/Modem (AMC)	None
Audio (AC)	Modem (MC)
Audio (AC)	Audio (AC)
Audio (AC)	Audio/Modem (AMC)

Modem implementation for different countries must be considered as telephone systems vary. By using a split design, the audio codec can be on-board and the modem codec can be placed on a riser. Intel is developing an AC-link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

The digital link in the ICH2 is AC'97 Revision 2.1 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec. The Intel 850 chipset-based platform expands audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six channel audio consists of Front Left, Front Right, Back Left, Back Right, Center and Woofer for a complete surround sound effect.

Refer to the *AC'97 Specification, Revision 2.1* at http://developer.intel.com/pc-supp/platform/ac97/ for complete details.

1.4.2.3 Low Pin Count (LPC) Interface

In the platform, the super I/O component uses the Low Pin Count (LPC) interface. The LPC super I/O component requires the same feature set as traditional super I/O components. It should include a keyboard and mouse controller, floppy disk controller and serial and parallel ports. In addition to the standard super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In a system with ISA audio, the game port typically existed on the audio card. The fifteen-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface.

For further information, refer to the *Low Pin Count Interface Specification, Revision 1.0*, that is located at the following URL: http://developer.intel.com/design/pcisets/lpc/INDEX.HTM. Consult your super I/O vendor for a comprehensive list of devices offered and features supported.

1.4.2.4 Ultra ATA

Ultra ATA "widens" the path to the hard drive by transferring twice as much data per clock cycle. The net effect is that the maximum burst data transfer rate from the disk drive increases from 16.6 MB/s to 100 MB/s. Hard disk drive manufacturers can now bring higher performance products to market that scale with the rest of the PC platform (faster hard drives to feed faster processors, memory and graphics).

The Ultra ATA protocol allows Intel 850 chipset-based systems to send and retrieve data faster, removing bottlenecks associated with data transfers — especially during sequential operations. Users of new Intel 850 chipset-based systems will need less time to boot their systems and open applications, a direct result of the improved throughput provided by Ultra ATA. Current disk drive technology has been optimized to perform within the limits of the legacy protocol (16.6 MB/s). Raising the data transfer headroom results in moderate performance gains with today's drive technology. Even greater performance improvements will emerge as drive manufacturers introduce products that generate a faster data stream.

The ICH2 supports the IDE controller with two sets of interface signals (Primary and Secondary) that can be independently enabled, tri-stated or driven low. It supports the Ultra ATA/33, Ultra ATA/66 and Ultra ATA/100 protocol transfer rates. Ultra ATA/66 and ATA/100 are similar to the Ultra ATA/33 scheme and are intended to be device driver compatible. The Ultra ATA/66 logic is clocked at 66 MHz and can move 16 bits of data every two clocks (for a maximum of 66 MB/s transfers), and the Ultra ATA/100 logic is clocked at 100 MHz and can move 16 bits of data every two clocks (for a maximum of 100 MB/s transfers).

1.4.2.5 Universal Serial Bus (USB)

Universal Serial Bus (USB) simplifies the peripheral attaching and accessing process to the computer. It also eases the system configuration process from an end-user's perspective. The USB specification outlines a single connector-type for all PC peripherals, automatic detection/configuration of the USB devices and transfer types allowed on the bus.

In the Intel 850 chipset based platform, the ICH2 integrates two USB Host Controllers. The Host Controllers include the root hub with two separate USB ports, resulting in a total of four USB ports. The ICH2 Host Controller supports the standard *Universal Host Controller Interface (UHCI), Revision 1.0*.

Refer to the *USB Specification, Revision 1.1* at http://www.usb.org for further information.

1.4.3 Platform Manageability

The Intel 850 chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system and recover from system lockups without the aid of an external micro-controller.

Interrupt Controller: The interrupt capabilities of the ICH2 in an Intel 850 chipset-based platform expands support for up to 8 PCI interrupt pins and PCI 2.2 Message-Based Interrupts. In addition, the ICH2 supports system bus interrupt delivery.

TCO Timer: The ICH2 integrates a programmable TCO timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# which the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

Processor Present Indicator: The ICH2 looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction the ICH2 has the ability to blink a GPIO and reboot the system at the lowest frequency multiplier.

ECC Error Reporting: The MCH has the ability to send one of several messages to the ICH2 when an ECC error is detected. The MCH can tell the ICH2 to generate either an SMI#, SCI, or SERR# interrupt.

Function Disable: The ICH2 provides the ability to disable the following functions: AC'97 Modem, AC'97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.

Intruder Detect: The ICH2 provides an input signal, INTRUDER#, that can be attached to a switch that is activated by the system case being opened. The ICH2 can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

SMBus: The ICH2 integrates a SMBus controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RIMM modules and thermal probes. A slave interface is also provided to enable additional platform manageability. This interface allows and external microcontroller to access system resources, as well as external system devices the ability to check the system power state, watchdog timer, and system status bits and generate a system reset and other platform messages.

Alert-On-LAN*: The ICH2 supports *Alert-On-LAN**. In response to a TCO event (intruder detect, thermal event, processor not booting) the ICH2 will send a hard-coded message over the SMLink. Refer to the Wired for Management (WfM) Design Guide at http://www.intel.com/ial/wfm/design/ for additional information.

1.5 PC ’99/’01 Platform Compliance

PC ‘99 and PC ’01 are intended to provide guidelines for hardware design that will result in optimal user experience, particularly when the hardware is used with the Windows* family of operating systems. The PC ’99 and PC ’01 design guides include PC ‘99 and PC ’01 requirements and recommendations for basic consumer and office implementations, such as desktop, mobile, and workstation systems, and entertainment PC’s. These documents include guidelines to address the following design issues:

- Design requirements for specific types of system that will run either Windows* 98, Windows* 2000 or Windows Me* operating systems.
- Design requirements related to OnNow design initiative, including requirements related to ACPI, Plug and Play device configuration, and power management in PC systems.
- Manageability requirements that focus on improving Windows 98, Windows 2000 and Windows Me, with the end goal of reducing TCO.
- Clarification and additional design requirements for devices supported under Windows 98, Windows 2000 and Windows Me, including new graphics and video device capabilities, DVD, scanners and digital cameras, and other devices.

Refer to the *PC ‘99 System Design Guide* and *PC ’01 System Design Guide* at http://www.pcdesguide.org for additional information.

2 Component Quadrant Layout

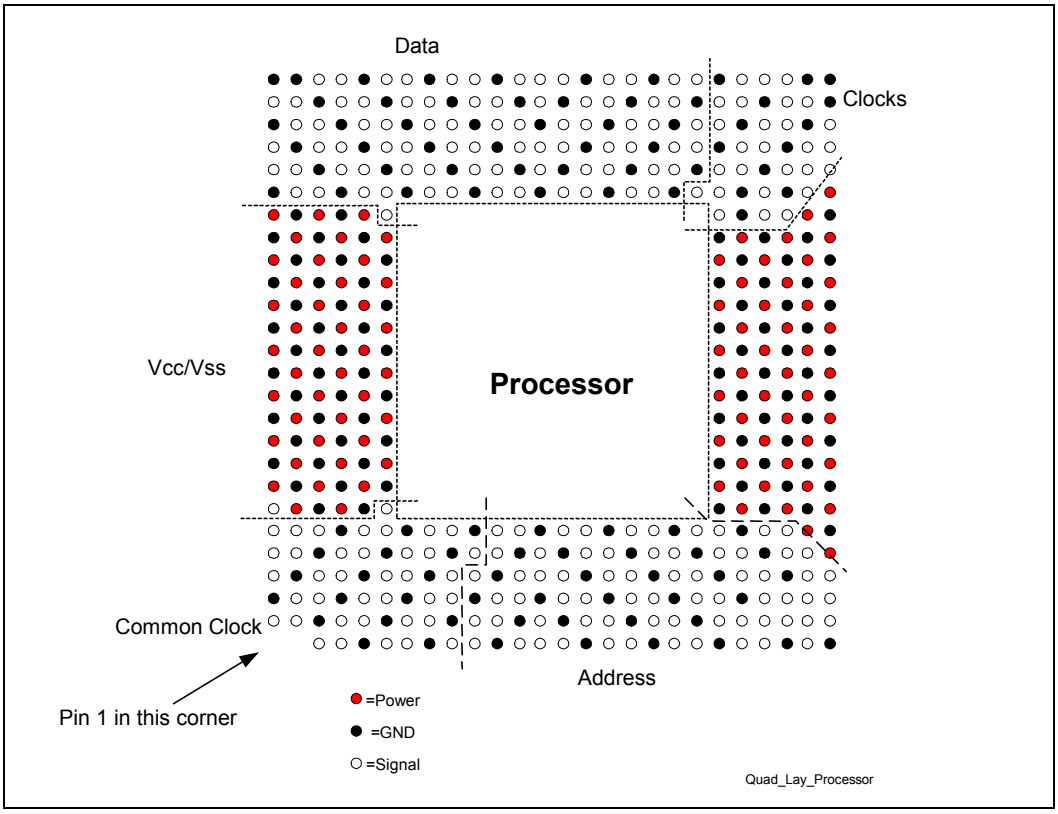
The quadrant layouts shown are approximations. The quadrant layout figures do not show the exact component ball count; only general quadrant information is presented and is intended for reference while using this document. Only the exact pin or ball assignment should be used to conduct routing analysis. Refer to the following documents for pin or ball assignment information.

- Processor datasheet
- *Intel® 850 Chipset: 82850 Memory Controller Hub (MCH) Datasheet*

2.1 Processor Component Quadrant Layout

Figure 2 illustrates the quadrant layout of the processor. In the event that this information conflicts with the processor datasheet, the datasheet data should be considered correct. All figures in this section are from the topside perspective.

Figure 2. Processor Socket Quadrant Layout



2.2 Intel® 850/850E Chipset Component Quadrant Layout

Figure 3 and Figure 4 show the quadrant layouts for the Intel 850 chipset components.

Figure 3. Intel® 850/850E Chipset Quadrant Layout

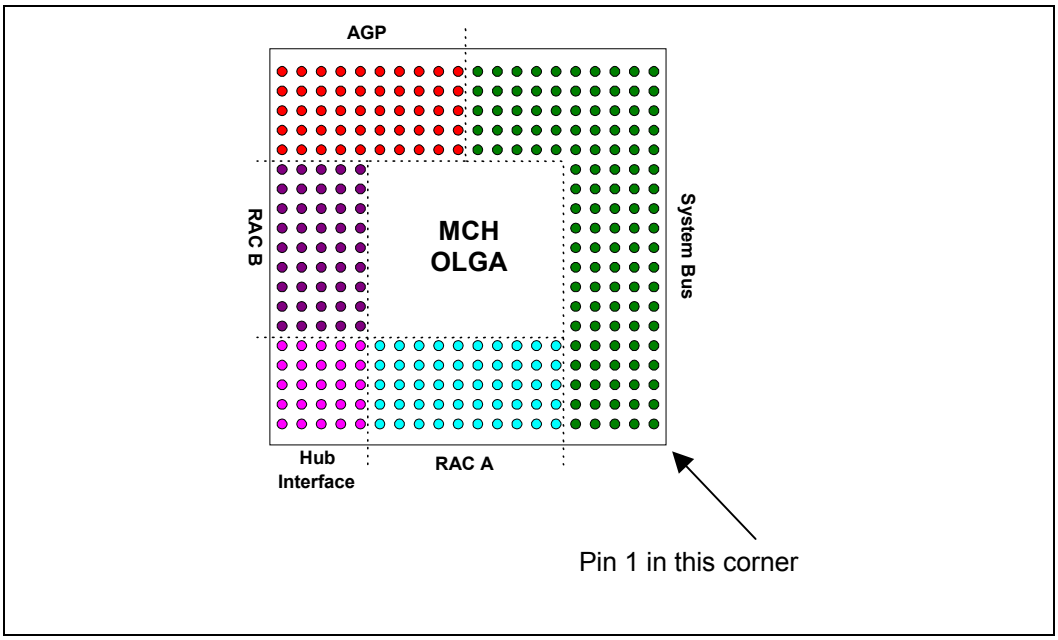
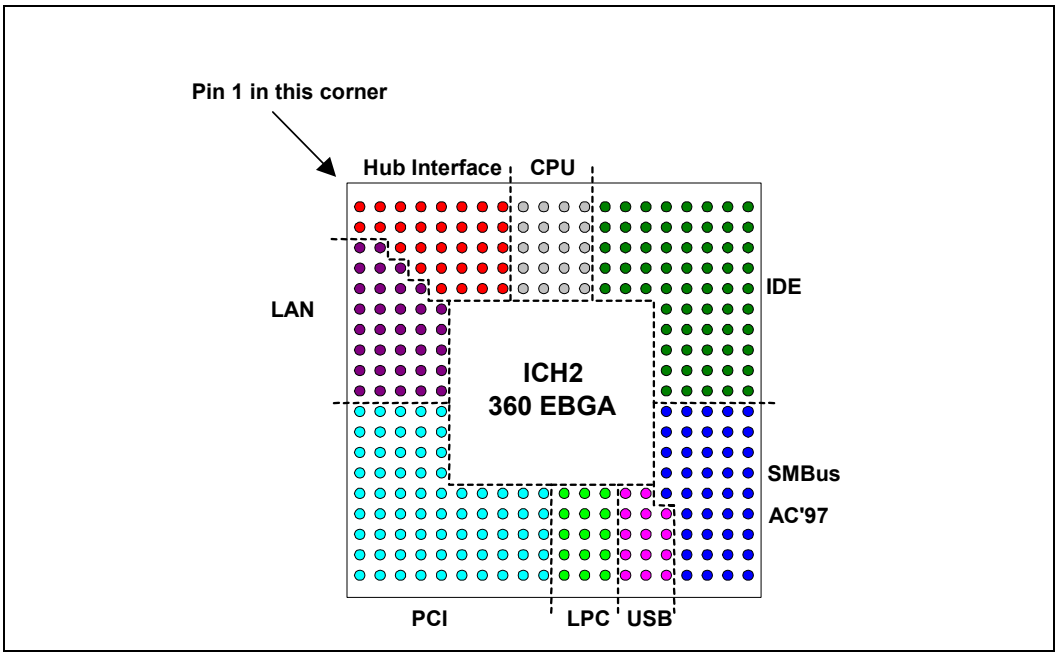


Figure 4. Intel® ICH2 Quadrant Layout



3 Platform Placement and Stack-Up Overview

In this section, examples of Intel 850 chipset platform component placement and stack-up are described for desktop systems in 6-layer ATX and 4-layer µATX motherboard form factors.

3.1 Platform Component Placement

3.1.1 Six-Layer Motherboard

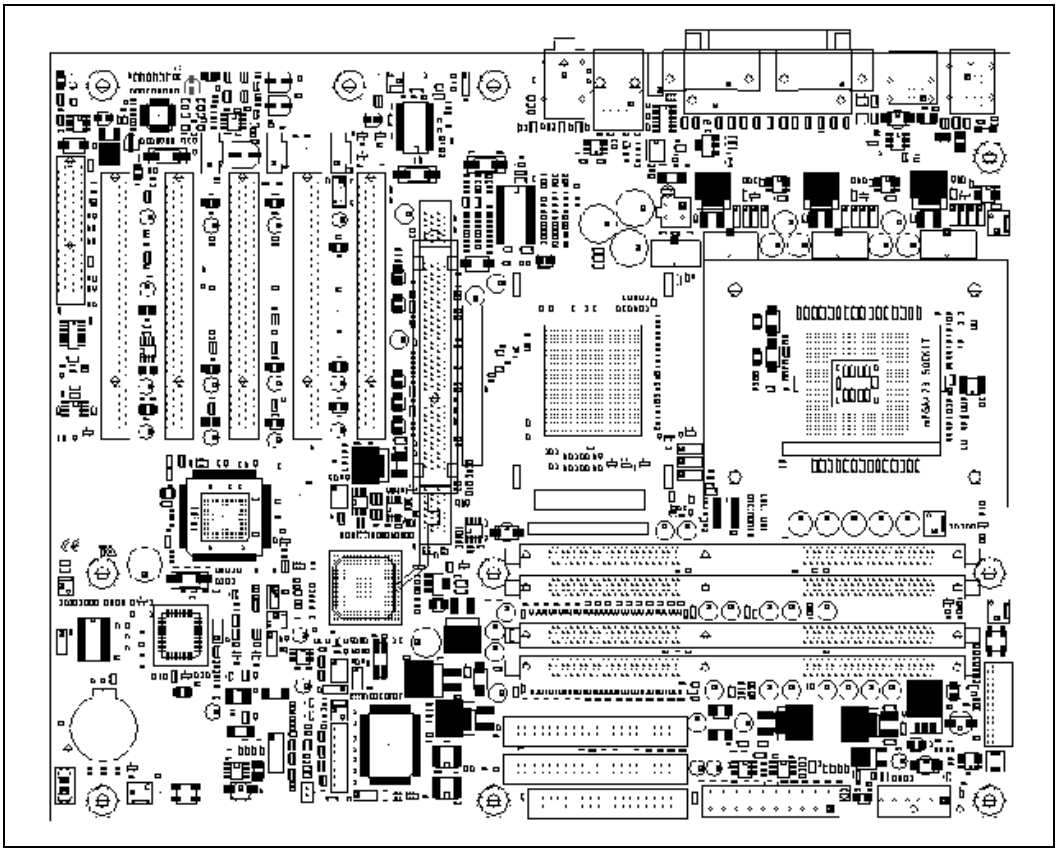
Figure 5 shows general component placement for a Pentium 4 processor in the 478-pin package and Intel 850 chipset-based desktop 6-layer motherboard system. The assumptions used for the component placement are described in Table 3 and are consistent with the 6-layer customer reference board (CRB) schematics.

Note: The processor supports uni-processor configurations only.

Table 3. Placement Assumptions for the Desktop Configuration (6-Layer Motherboard)

System Configuration	Assumptions		
	Form Factor	Number of Layers for Routing	Assembly
Uni-processor	ATX	6 layers	Single sided

Figure 5. Desktop Component Placement Example (6-Layer Motherboard)



3.1.2 Four-Layer Motherboard

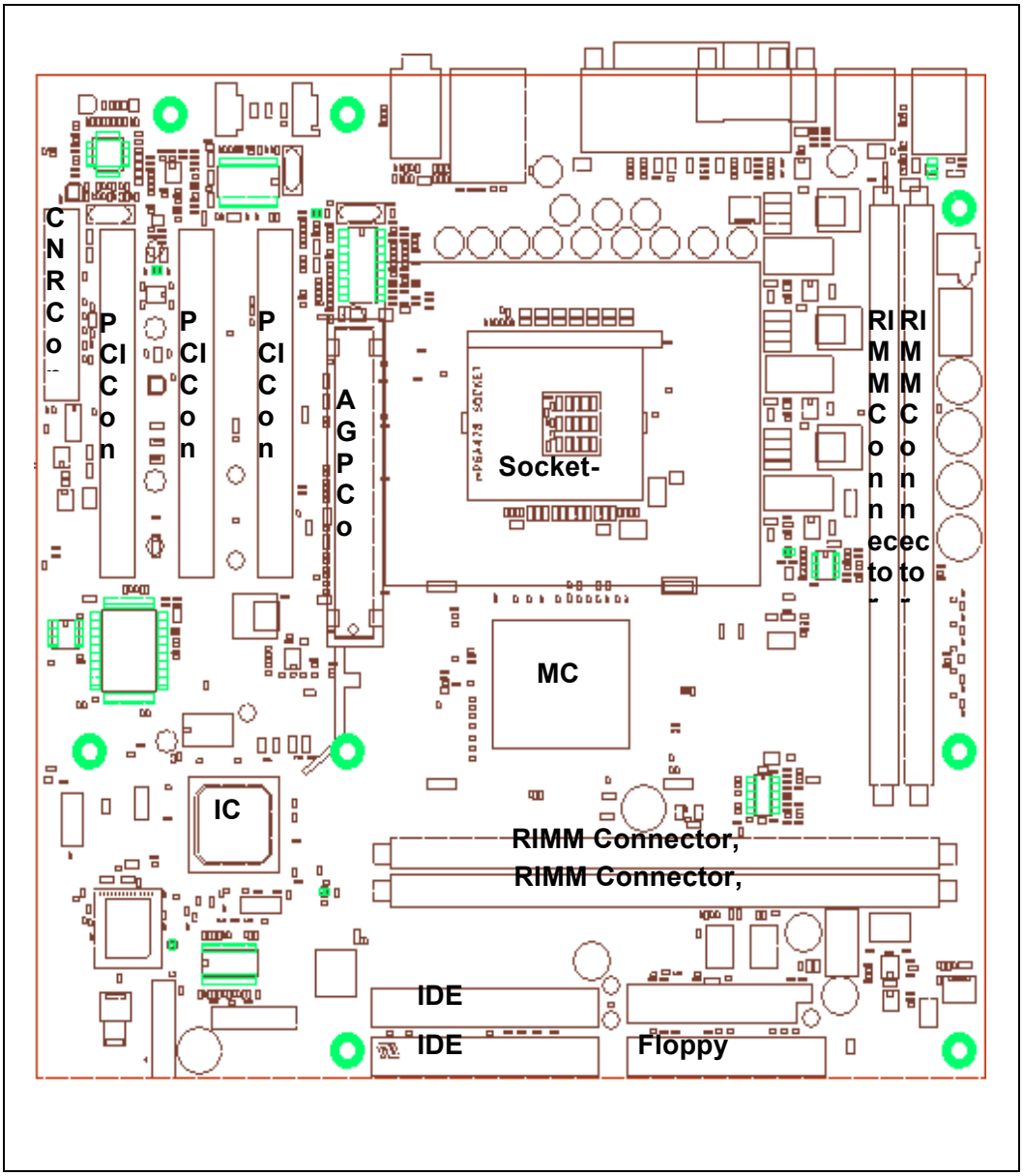
Figure 6 shows general component placement for a Pentium 4 processor in the 478-pin package and Intel 850 chipset-based desktop 4-layer motherboard system. The assumptions used for the component placement are described in Table 3 and are consistent with the 4-layer customer reference board (CRB) schematics.

Table 4. Placement Assumptions for the Desktop Configuration (4-Layer Motherboard)

System Configuration	Assumptions		
	Form Factor		Form Factor
Uni-processor	µATX (1)	Uni-processor	µATX (1)

NOTE: Information from the µATX design can be applied to an ATX form factor.

Figure 6. Desktop Component Placement Example (4-Layer Motherboard)



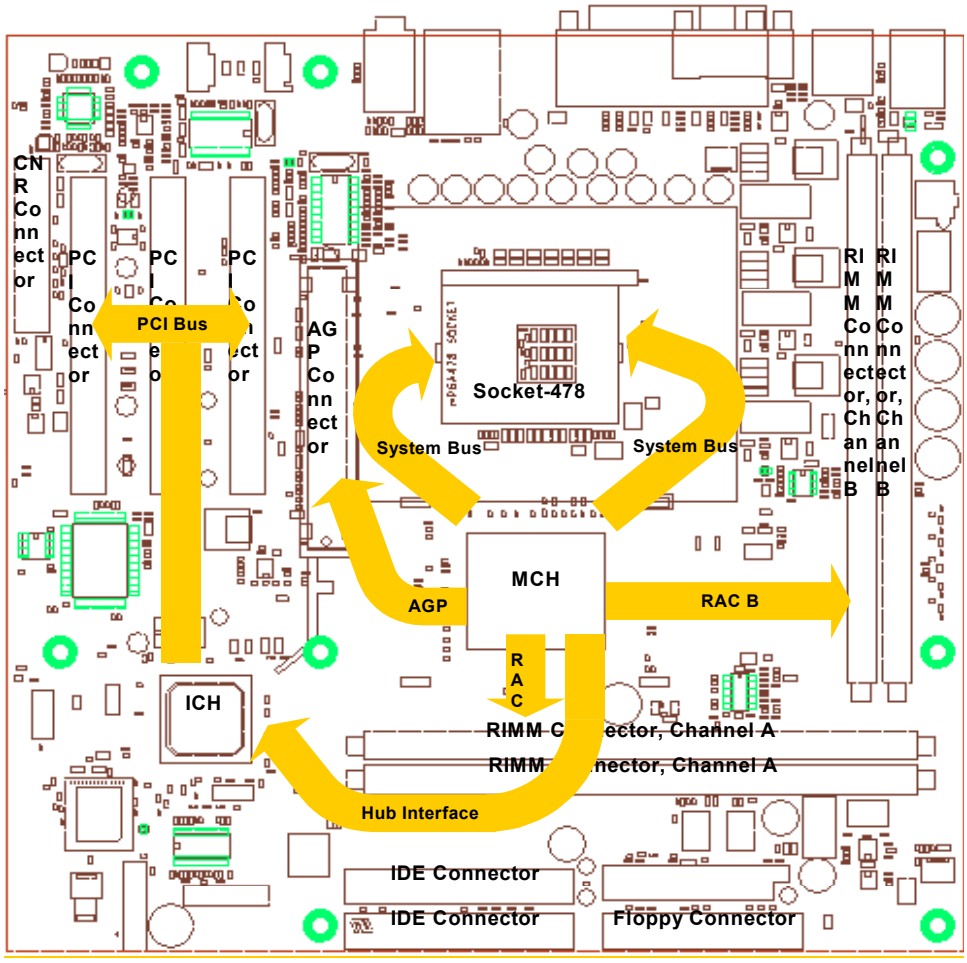
3.1.2.1 Four-Layer Motherboard Routing Strategy

The routing strategy used on the 4-layer CRB is as follows:

- Hub interface routing
  - Route hub interface signals across the middle of the two RIMM connectors on channel A and then across to the ICH2.
  - Breakout hub interface signals on top layer to allow 1.8V core and RAC MCH power to be supplied to the MCH in the hub interface pin field on the bottom layer and power plane.
- AGP routing
  - Half of the signals are routed on the top layer referenced to V_{DDQ} and the other half is routed on the bottom referenced to GND.
- PCI routing
  - PCI signals are routed in a T-topology. Signals are routed on the bottom of the board from the ICH2 towards PCI connectors. When the traces reach the PCI connector, they transition to the top layer and are routed horizontally, freeing up vertical routing channel for clock, LAN, AC'97 and legacy IO routing from the SIO.
- System bus routing
  - The MCH is placed below the processor socket for optimal power delivery to the processor and MCH. System bus signals are routed around the processor. A ground flood on the top layer and a V_{CCP} flood on the bottom layer connect the OSCON and high frequency capacitors together. The floods reduce power/GND plane inductance and maximize capacitor efficiency.
  - Half of the system bus signals are routed on the top layer referenced to V_{CCP} and the other half of the signals are routed on the bottom layer referenced to GND.

Figure 7 shows the general routing strategy for the 4-layer CRB.

Figure 7. Four-Layer Routing Strategy

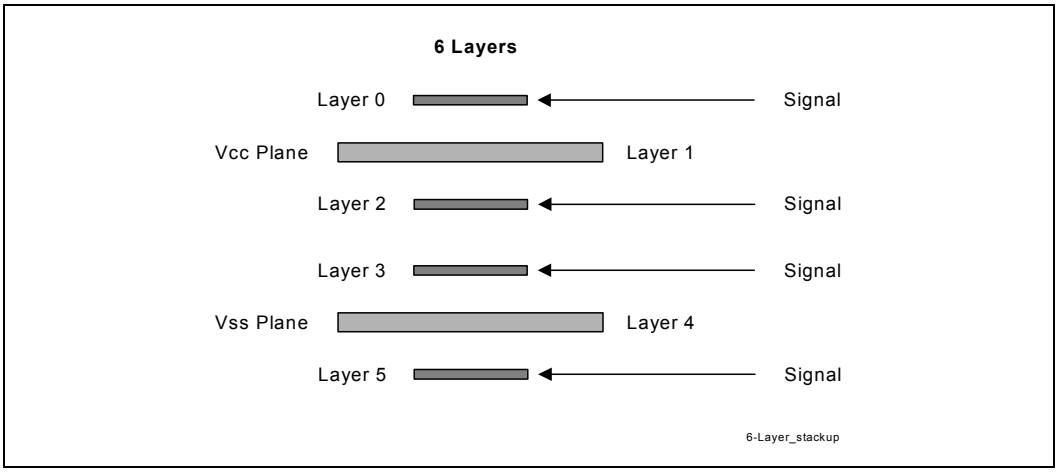


3.2 Motherboard Layer Stack-Up

3.2.1 Six-Layer Motherboard Stack-Up

Figure 8 shows a six-layer stack-up for the system. It is for reference only and the actual board stack-up may vary depending upon the following considerations. The separation between layers 2 and 3 should be kept as large as possible. A distance greater than 2x should be kept between signals on layers 2 and signals on layer 3. Additionally, traces on layer 2 should be routed orthogonally to traces on layer 3. If traces on layer 2 are unable to be routed orthogonally to traces on layer 3, then the distance between layer 2 and layer 3 should be greater than 4x.

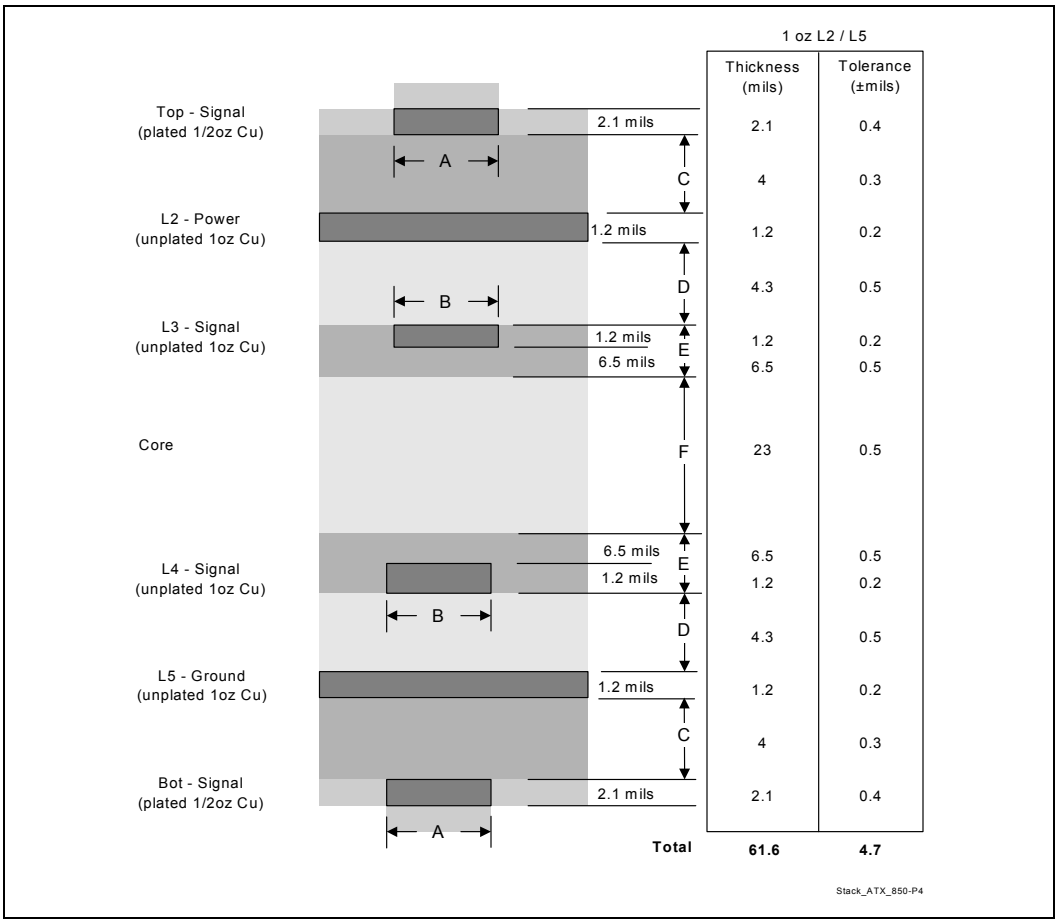
Figure 8. Six Layer Stack-Up



3.2.2 Design Considerations

- Standard vias should be 14 mil hole with a 26 mil pad.

Figure 9. Example Stack-Up for 6-Layer ATX Form Factor

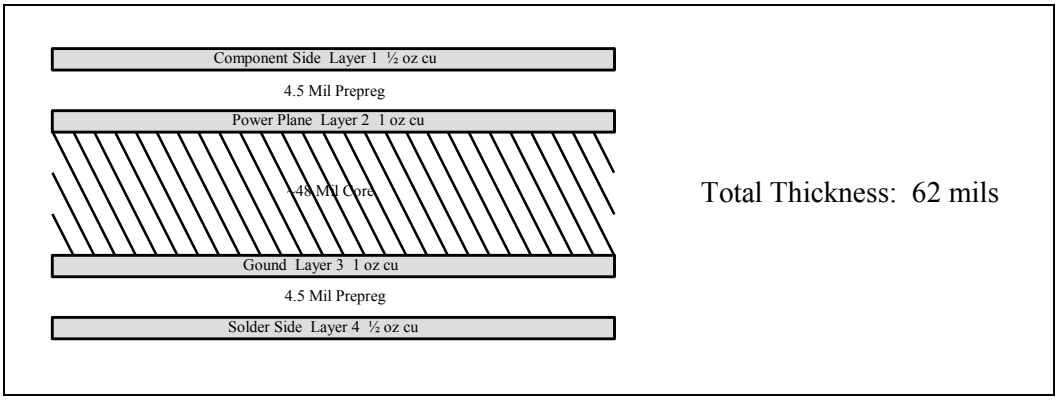


3.2.3 Four-Layer Motherboard Stack-Up

The following figure shows a 4-layer stack-up.

- If possible, signals should be referenced to a V_{SS} plane.

Figure 10. 4-Layer Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Example Stack-Up for µATX Form Factor



Design Considerations

Intel has found that the following recommendations aid in the design of an Intel Pentium 4 processor-based platform.

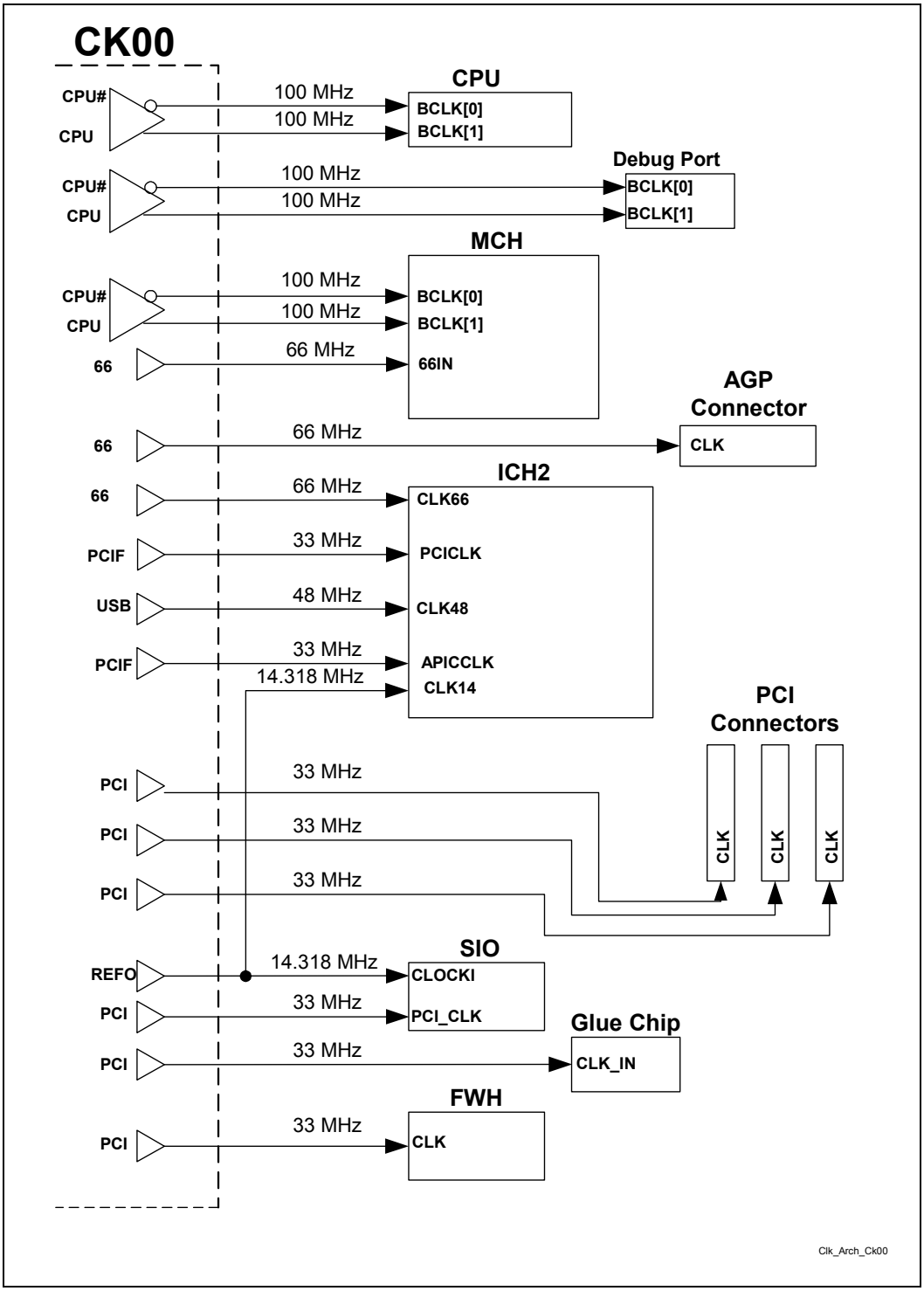
- Impedance requirements
  - 60-ohm impedance ± 15% for AGP at 5mil trace width
  - 50-ohm impedance ± 15% for the system bus at 7 mil trace width
  - 28-ohm impedance ± 10% for the memory interface at 18 mil trace width
- Minimum via size is 12 mil finished in a 26 mil land with 35 mil antipad

4 Platform Clock Routing Guidelines

Intel recommends CK00 compliant clocking for this platform. For more information on CK00 compliance, *for the 82850 chipset with 400 MHz processor system bus* refer to the *CK00 Clock Synthesizer/Driver Design Guidelines. , For the 82850E chipset with 533 MHz processor system bus*, refer to *the CK00-E Clock Synthesizer/Driver Design Guidelines, for Intel® Pentium® 4 Processor in the 478 pin Package / Intel® 850-E Chipset Platform with 533 MHz Processor System Bus*. The *CK00 Clock Synthesizer/Driver Design Guidelines* and *CK00-E Clock Synthesizer/Driver Design Guidelines* specify the platform clocking solution that can be used in the processor and Intel 850 chipset-based design - the CK00 or CK00-E clock synthesizer.

Note: While this design guideline refers to the CK00 clock driver, the CK408 clock driver can also be used. Use of the reference “CK00” also refers to both the CK00 and the CK00-E clock requirements, unless otherwise specified.

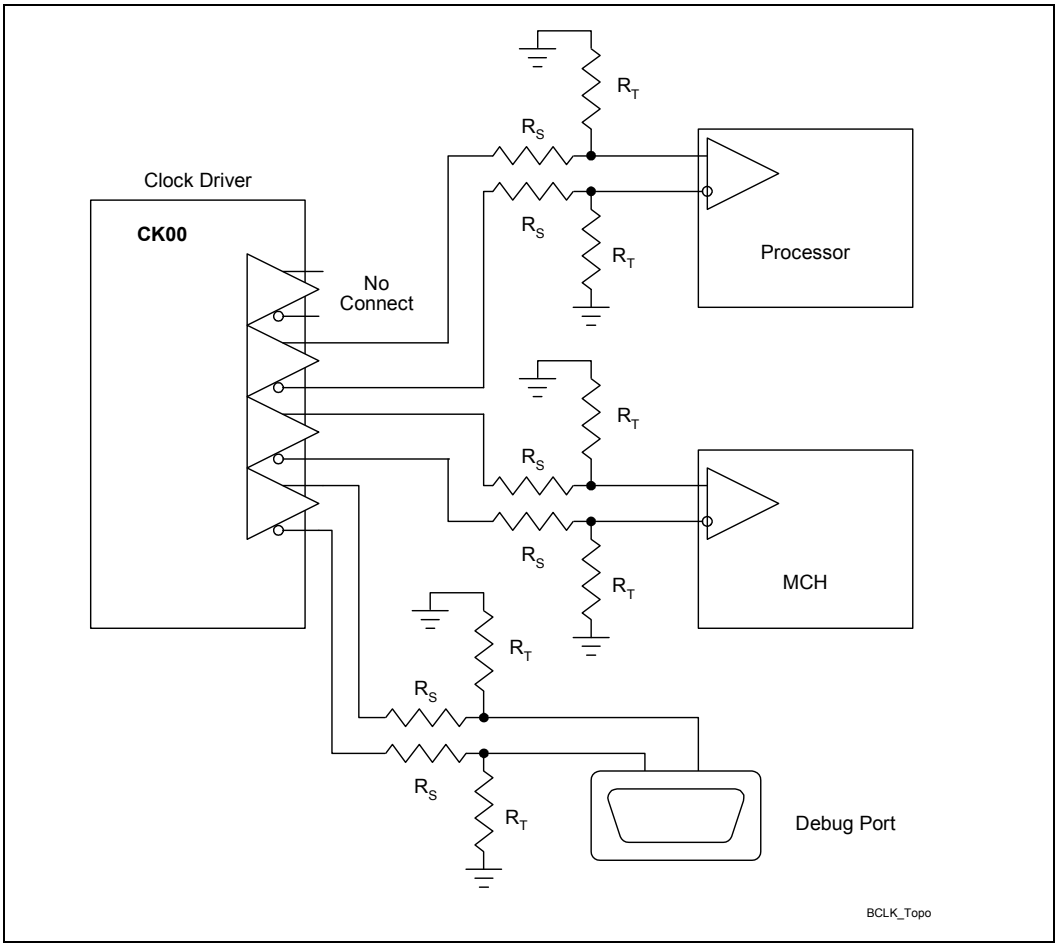
Figure 11. Clocking Architecture Using the CK00



4.1 Routing Guidelines for System Bus Clocks

The CK00 clock synthesizer provides four sets of 100 MHz differential clock outputs. The 100 MHz differential clocks are driven to the processor and MCH as shown in Figure 12.

Figure 12. Processor BCLK Topology



NOTE: *Connect the CK00* component's HOST pin to the BCLK0 pins on the processor and MCH. Additionally, connect the CK00 *HOST_BAR pin to the BCLK1 pins.*

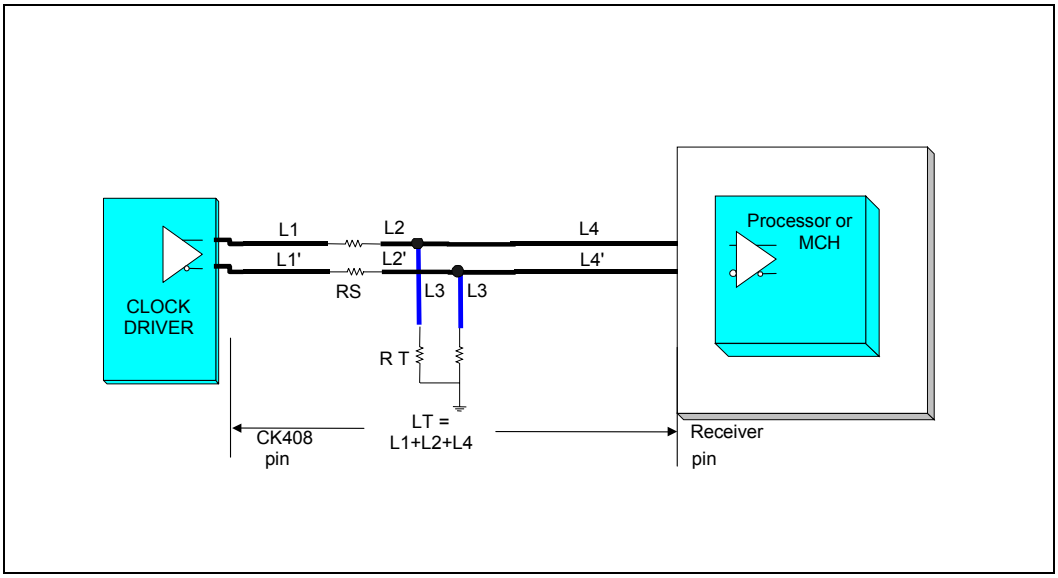
The CK00 clock driver differential bus output structure is a "Current Mode Current Steering" output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying I_{OUT} by the value of Rt. The current I_{OUT} is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

The recommended termination for the CK00 differential bus clock is a "Shunt Source termination." Refer to Figure 13 for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the CK00 to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the

clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the system board and Rs should be 33 Ω.

Figure 13. Source Shunt Termination



The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew. Skew results from variations in dielectric constant and impedance due to physical tolerances of the circuit board material. Routing on internal layers provides the least amount of this variation.

- **Requirement:** Do not split up the two halves of a differential clock pair between layers
- **Goal:** Route clocks to all agents on same physical routing layer

General Routing Guidelines

- If a layer transition is required, make sure that skew induced by the vias used to transition between routing layers is compensated in the traces to other agents
- Layer transitions should only be made between routing layers of the same configuration (i.e., stripline layer to stripline layer)
- Keep routes to all agents as short as possible to minimize the cumulative effects of dielectric constant variations on clock skew
- Do not place vias between adjacent complementary clock traces.
- Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and RS, if needed to shorten length L1.

EMI constraints

Clocks are a significant contributor to EMI and should be treated with care. Following these recommendations can aid in EMI reduction:

- Route clocks on inner layers.
- On internal signals layers maintain a minimum of 100 mils from the edge of the clock traces to the edge of the system board.
- Maintain uniform spacing between the two halves of differential clocks
- Route clocks on a physical layer adjacent to the VSS reference plane only
- Spread spectrum clocking (SSC) should be enabled to reduce the magnitude of EMI.

Table 5 describes the routing guidelines for the bus clock signals.

Table 5. BCLK [1:0] Routing Guidelines

Layout Guideline	Value	Illustration	Notes
BCLK Skew between agents	400 ps total Budget: 150 ps for Clock driver 250 ps for interconnect	Figure 12	1, 2, 3, 4
Differential pair spacing	7.0 mils	Figure 15	5, 6
Spacing to other traces	20 mils	Figure 15	—
Line width	7.0 mils	Figure 15	7
System board Impedance – Differential	100 Ω	—	8
System board Impedance – single ended	50 Ω ±15%	—	9
Processor routing length – L1, L1': Clock driver to Rs	0.5 inches max	Figure 13	12
Processor routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2 inches	Figure 13	12
Processor routing length – L3: RS-RT node to Rt	0 – 0.2 inches	Figure 13	12
Processor routing length – L4, L4': RS-RT Node to Load	0 – 12 inches	Figure 13	
MCH routing length – L1: Clock Driver to RS	0.5 inches max	Figure 13	12
MCH routing length – L2, L2': Rs to Rs-Rt node	0 – 0.2 inches	Figure 13	12
MCH routing length – L3: RS-RT node to Rt	0 – 0.2 inches	Figure 13	12
MCH routing length – L4, L4': RS-RT Node to Load	0 – 12 inches	Figure 13	

Layout Guideline	Value	Illustration	Notes
Clock driver to processor and clock driver to Chipset length matching (LT)	0.600 inches ±0.010 inches (Add to MCH trace length)	Figure 12	10
BCLK0 – BCLK1 length matching	±10 mils	Figure 12	—
Rs Series termination value	33 Ω ±5%	Figure 12	—
Rt Shunt termination value	49.9 Ω ±1% (for 50 Ω MB impedance)	Figure 12	11

NOTES:

1. The skew budget includes clock driver output pair to output pair jitter (differential jitter), and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers and routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
7. Set line width to meet correct system board impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack-up.
8. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1-2*Kb) where Kb is the backwards cross-talk coefficient. For the recommended trace spacing, Kb is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the BCLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the system board trace length for the chipset will be longer than that for the processor. Details of this additional length will be included in a future revision of the processor package files.
11. Rt shunt termination value should match the system board impedance.
12. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ring back.

Figure 14. Clock Skew as Measured from Agent to Agent

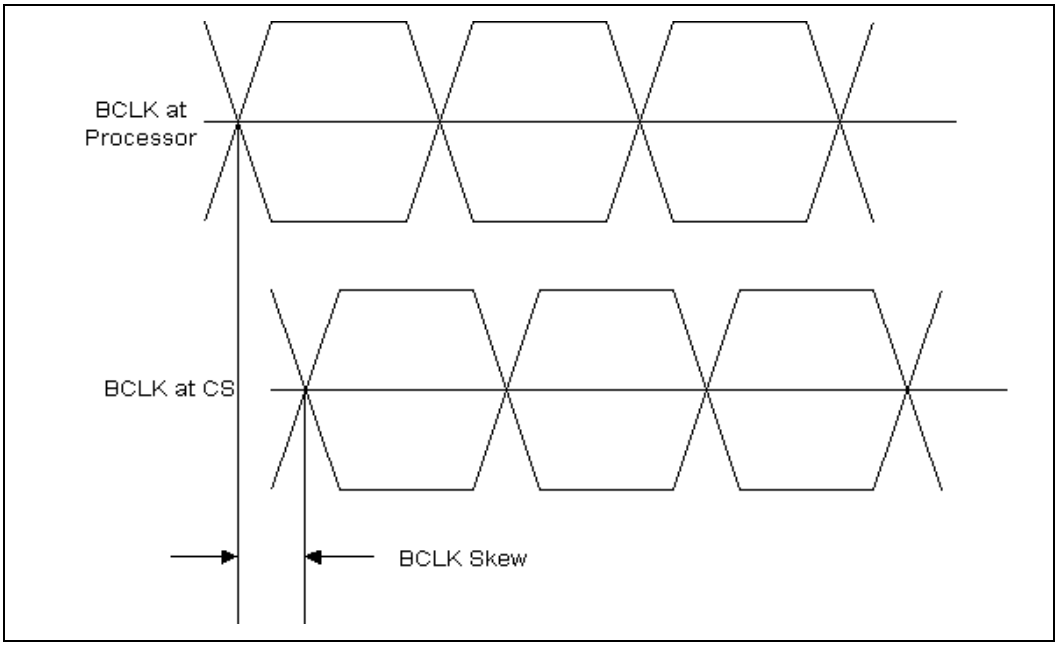
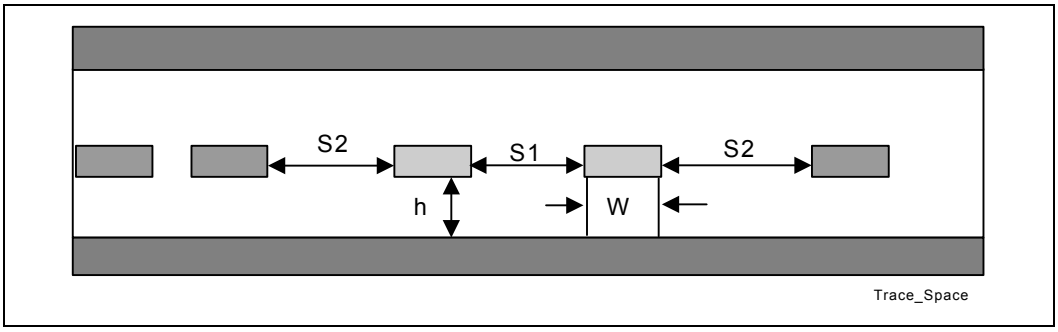


Figure 15. Trace Spacing

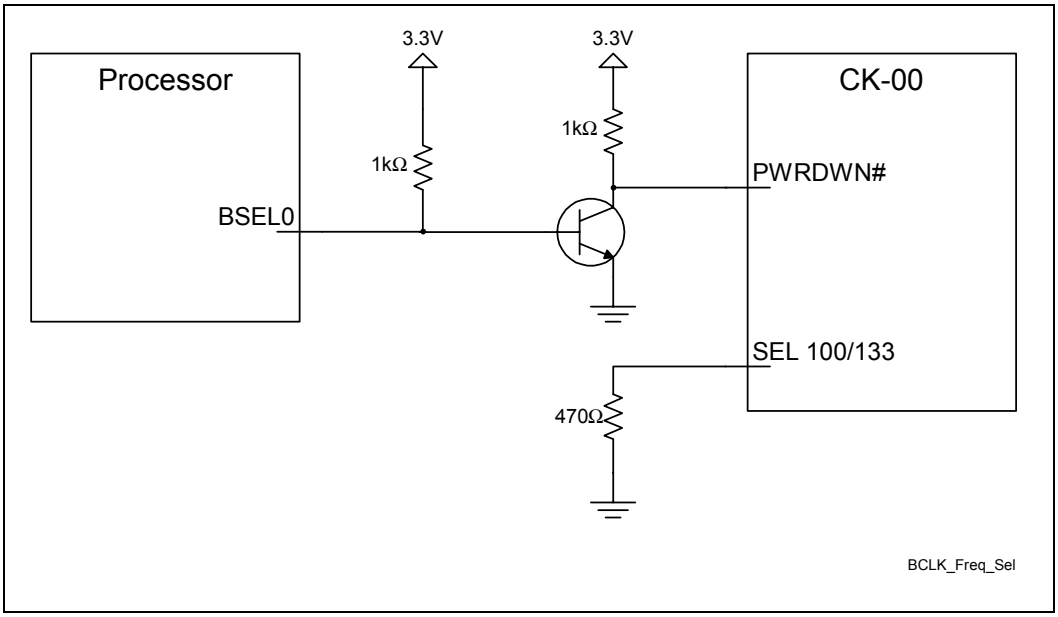


4.2 BCLK[1:0] Frequency Select

4.2.1 100 MHz Operation – Intel® 82850 Chipset

The BCLK[1:0] frequency should be set for 100 MHz operation for the 82850 chipset. This is accomplished with a 470 Ω pull-down on the CK-00 SEL100/133 input. In addition, the platform should be prevented from operating with a processor that requires a BCLK[1:0] frequency other than 100 MHz. The correct frequency select circuitry is show in Figure 16.

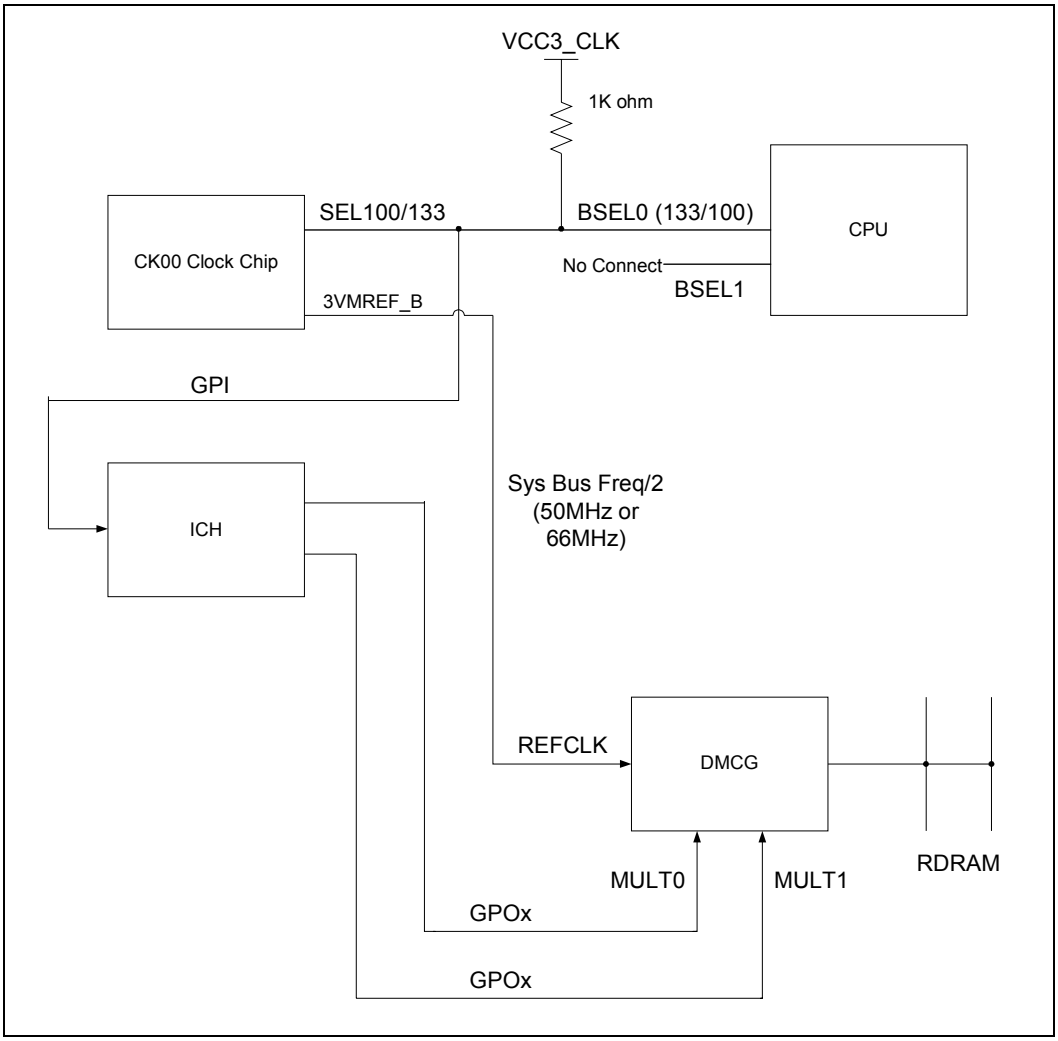
Figure 16. BCLK[1:0] Frequency Select for 100 MHz System Bus Operation



4.2.2 133 MHz Operation – Intel® 82850E Chipset

The BCLK[1:0] frequency should be set for 133 MHz operation for the 82850E chipset. This is accomplished with a 1 kΩ pull-up to VCC3_CLK on the CK-00 SEL100/133 input. The correct frequency select circuitry is show in the Figure below.

Figure 17. BCLK [1:0] Frequency Select for 133 MHz System Bus Operation



4.3 Routing Guidelines for Rambus RDRAM* Device Clocks

The CK00 clock synthesizer provides two 3.3 V clock reference outputs [3Vmref and 3Vmref#] for the Direct Rambus* Clock Generator (DRCG* device). Two DRCG devices are required in an 850 chipset dual-Direct RDRAM channel interface. Some clock vendors may also have a DMCG (Direct Multiple Clock Generator) component that combines the function of two DRCG devices into one part. These DMCG components may be used as a cost-reduction opportunity with appropriate validation.

The DRCG device reference clock operates at one-half the processor clock frequency. The reference clocks are inputs into the DRCG devices and are used to generate the RDRAM device "Clock to Master" differential pair (CTM, CTM#) clocks on each Direct RDRAM channel.

In addition, the DRCG uses phase information provided by the MCH via the RCLKOUT and HCLKOUT phase aligning signals.

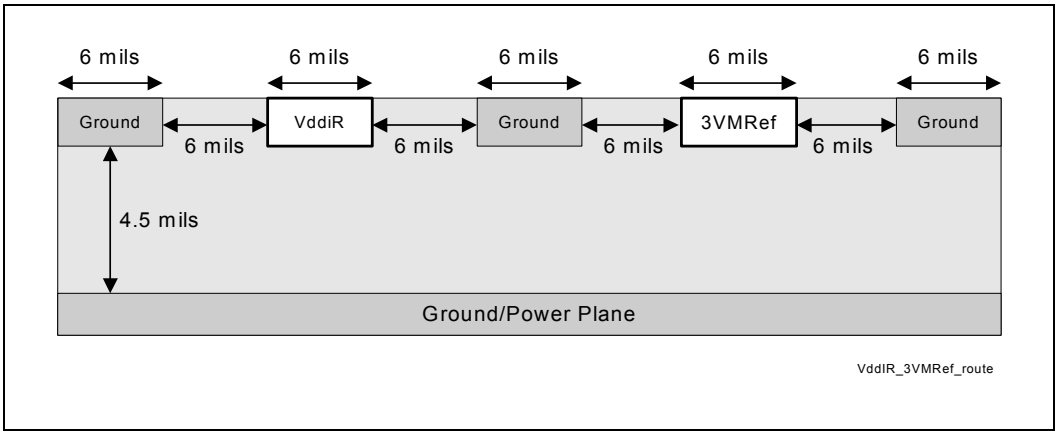
For an 82850E/PC1066 RDRAM technology platform, the DRCG devices should be 533 MHz capable.

4.3.1 CK00 to Rambus DRCG* (Reference Clocks)

The 3VMRef clock output must be routed as shown in Figure 18. Note that the VddIR power pin on the DRCG can be connected directly to 3.3 V near the DRCG if the 3.3 V plane extends near the DRCG. However, if a 3.3 V trace must be used, it should originate at the clock synthesizer and be routed as shown in Figure 18. The maximum routing length for the 3VMRef and 3VMRef# signals is 8 inches.

Note: The following recommendations assume routing of the reference clocks as microstrip traces.

Figure 18. VddIR and 3VMRef Routing



NOTE: 3VMRef# should be routed in a similar manner as 3VMRef.

4.3.2 Intel® MCH to Rambus DRCG* (Phase Aligning Clocks)

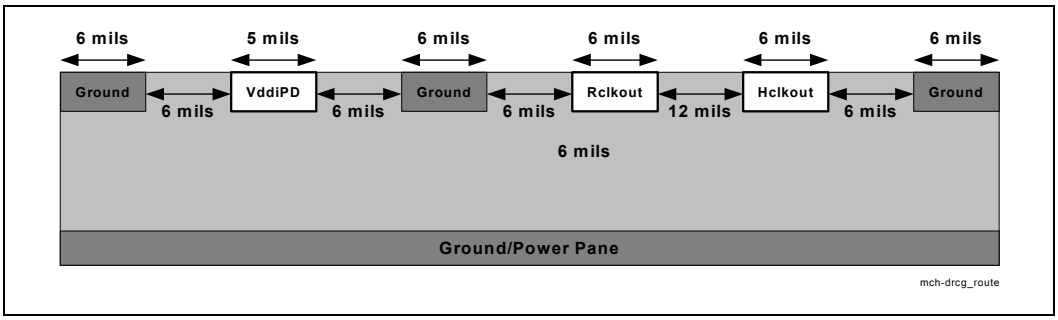
The RCLKOUT and HCLKOUT signals from the MCH should be routed to the SYNCLKN and PCLKM signals on the DRCG, respectively, as shown in Figure 19. Note that the VddiPD power pin on the DRCG can be connected directly to 1.8 V near the DRCG if the 1.8 V plane extends near the DRCG. However, if a 1.8 V trace must be used, it should originate at the CK00 clock synthesizer and be routed as shown with respect to RCLKOUT and HCLKOUT.

The maximum length for RCLKOUT and HCLKOUT is 6 inches. Additionally, these signals must be length matched within 50 mils. These signals should be routed on the same layer. If these signals must switch layers, then BOTH signals should change layers together.

If the VddIPD pin is connected to the 1.8 V plane using a via (i.e., trace is not run from the CK00 clock synthesizers), then HCLKOUT and RCLKOUT must still be routed as shown below and ground isolated.

Note: The following recommendations assume routing of the phase alignment clocks on microstrip.

Figure 19. Intel® MCH to Rambus DRCG* Routing



NOTE: The signals Rclkout and Pclkout are channel specific, and their exact names are CHx_RCLKOUT and CHx_PCLKOUT, where x is the channel, either A or B. Consult the *Intel® 850 Chipset Family: 82850/82850E Memory Controller Hub (MCH) Datasheet* t for more information.

4.3.3 Rambus DRCG* to Direct Rambus Channels (400 MHz Clocks)

The 400 MHz RDRAM device clock signals (CTM/CTM# and CFM/CFM#) are high-speed, impedance matched transmission lines that require strict routing recommendations to insure that the memory timings are met. The following RDRAM device clock recommendations should be strictly followed. Any deviations from the recommendations should be properly simulated.

4.3.3.1 Trace Lengths

Figure 20 shows the critical RDRAM device clock routing sections, with the routing lengths for each section defined in Table 6.

Figure 20. Rambus RDRAM* Device Clock Routing Dimension

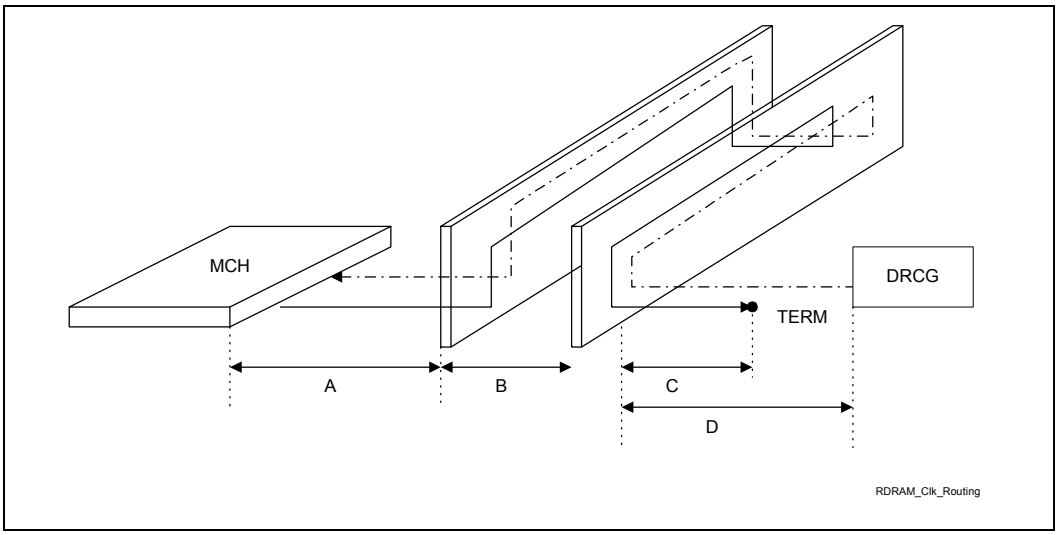


Table 6. Rambus RDRAM* Device Clock Routing Guidelines

Clock	From	To	Length (inches) 300/400 MHz RDRAM Technology	Length (inches) 533 MHz RDRAM Technology	Figure 20 Trace
CTM/CTM# [1]	Rambus DRCG*	Second RIMM* connector	0.0 – 6.0	0.0 – 6.0	D
	RIMM connector	RIMM connector	0.4 – 1.0	0.4 – 1.0	B
	First RIMM connector	Chipset	1.0 – 6.0	1.0 – 4.0	A
CFM/CFM# [2]	Chipset	First RIMM connector	1.0 – 6.0	1.0 – 4.0	A
	RIMM connector	RIMM connector	0.4 – 1.0	0.4 – 1.0	B
	Second RIMM connector	Termination	0.0 – 2.0	0.0 – 2.0	C

NOTES:
1. First RIMM connector to chipset:
   Trace length needs to be compensated to match the RSL signals from chipset to first RIMM connector.
2. Chipset to first RIMM connector:
   Trace length needs to be compensated to match the RSL signals from first RIMM connector to chipset.

In clock routing sections ‘A’ and ‘D’, it is recommended that the clock signals (CTM/CTM# and CFM/CFM#) be routed differentially. An example recommended topology for microstrip differential clock routing is shown in Figure 21.

Note: Clock trace widths and spacing may change with different prepreg thicknesses.

For 300/400 MHz RDRAM technology:

In clock routing sections ‘A’ and ‘D’, it is recommended that the clock signals (CTM/CTM# and CFM/CFM#) be routed differentially.

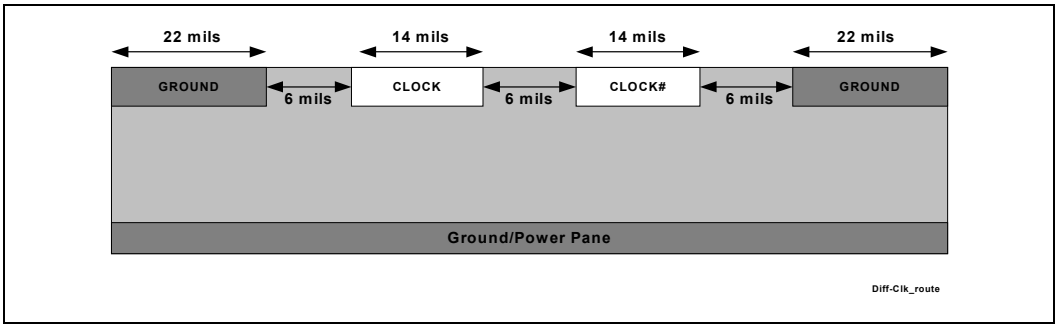
For 533MHz RDRAM technology:

See Section 6.1.2.3 for CTM/CTM#, CFM/CFM# differential clock compensation requirements.

If the clock signals CTM/CTM# and CFM/CFM# are not routed differentially, then an additional 10pS per inch should be added to CTM/CTM# - MCH to first RIMM connector guideline only.

The clock signals shown in the example topology are 14 mils wide and routed differentially. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. The 22 mil ground isolation traces must be connected to ground with a via per every 1 inch. A 6-mil gap is required between the clock signals and the ground isolation traces.

Figure 21. Differential Clock Routing



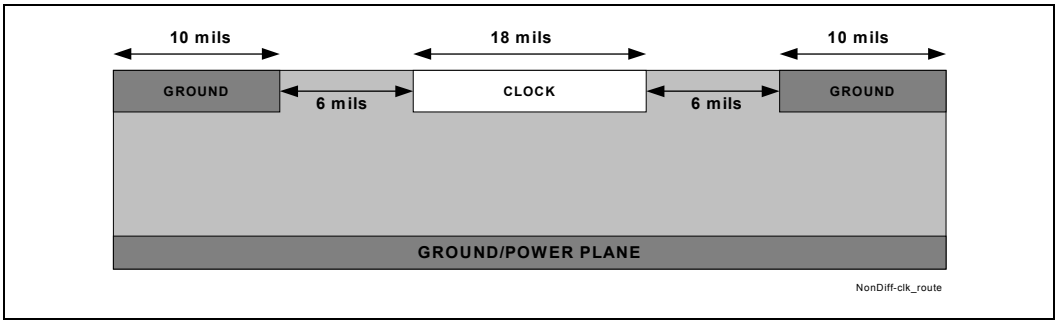
NOTE: “CLOCK” stands for the signals CTM and CFM and “CLOCK#” stands for the signals CTM# and CFM#.

In clock routing section ‘B’, the clock signals (CTM/CTM# and CFM/CFM#) are recommended to be routed non-differentially due to the short routing lengths between RIMM connectors. An example recommended topology for microstip non-differential clock routing is shown in Figure 22.

Note: Clock trace widths and spacing may change for different prepreg thicknesses.

The clock signals shown in the example topology are routed with 18 mil wide traces. When routing the clocks non- differentially, there must be a 10 mil ground isolation trace routed around the single ended clock signals. The 10 mil ground isolation traces must be connected to ground with a via per every 1 inch. A 6 mil gap is required between the clock signals and the ground isolation traces.

Figure 22. Non-Differential Clock Routing



NOTE: "CLOCK" stands for the signals CTM, CTM#, CFM and CFM#.

Note: The CTM/CTM# and CFM/CFM# clock signals must be ground referenced (with continuous ground island/plane) at all times.

4.3.3.2 Topology Considerations

Package trace compensation, via compensation and RSL signal layer alteration must also be considered when routing the RDRAM device clocks. Additionally, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clock's faster trace velocity when routing on microstrip layers.

- For clock routing section 'A', the CTM/CTM# and CFM/CFM# clocks must be length matched within ±2 mils to the RSL channel trace length. Exact matching is preferred.
- For clock routing section 'B', the CTM/CTM# and CFM/CFM# clocks must be length matched within ±2 mils to the RSL channel trace length. Exact matching is preferred.
- For trace section 'C', the CFM/CFM# clocks must be length matched within ±2 mils to the RSL channel trace length. Exact matching is preferred.
- For trace section 'D', the CTM/CTM# clocks must be length matched within ±2 mils to the RSL channel trace length. Exact matching is preferred.

4.3.3.3 Rambus RDRAM* Device ClockTermination

300/400 MHz RDRAM technology:

The CFM/CFM# differential pair signals require termination using either 27 Ω 1% or 28 Ω 2% resistors and a 0.1 µF capacitor as shown in Figure 23.

533 MHz RDRAM technology:

The CFM/CFM# differential pair signals require termination using 27 Ω 1% resistors and a 0.1 µF capacitor as shown in Figure 24.

Figure 23. CFM/CFM# Termination – 300/400 MHz Rambus RDRAM* Technology

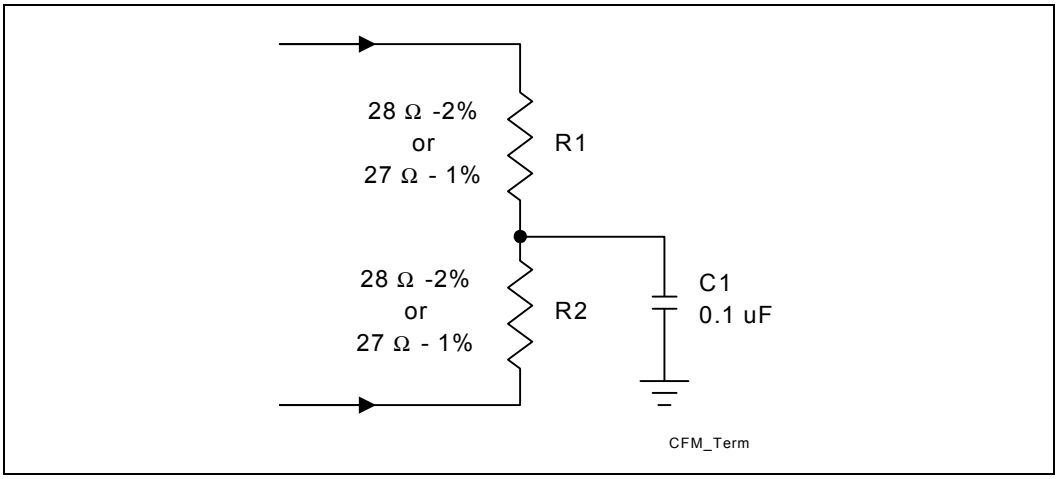
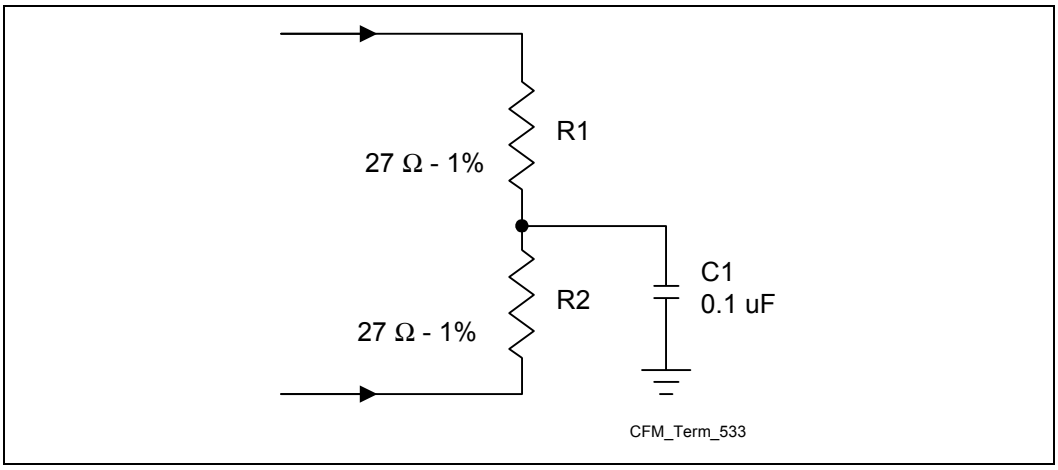


Figure 24. CFM/CFM# Termination – 533 MHz Rambus RDRAM* Technology



4.3.4 Rambus DRCG* Impedance Matching Circuit

The external DRCG impedance matching circuit is shown in Figure 25.

Figure 25. Rambus DRCG* Impedance Matching Network

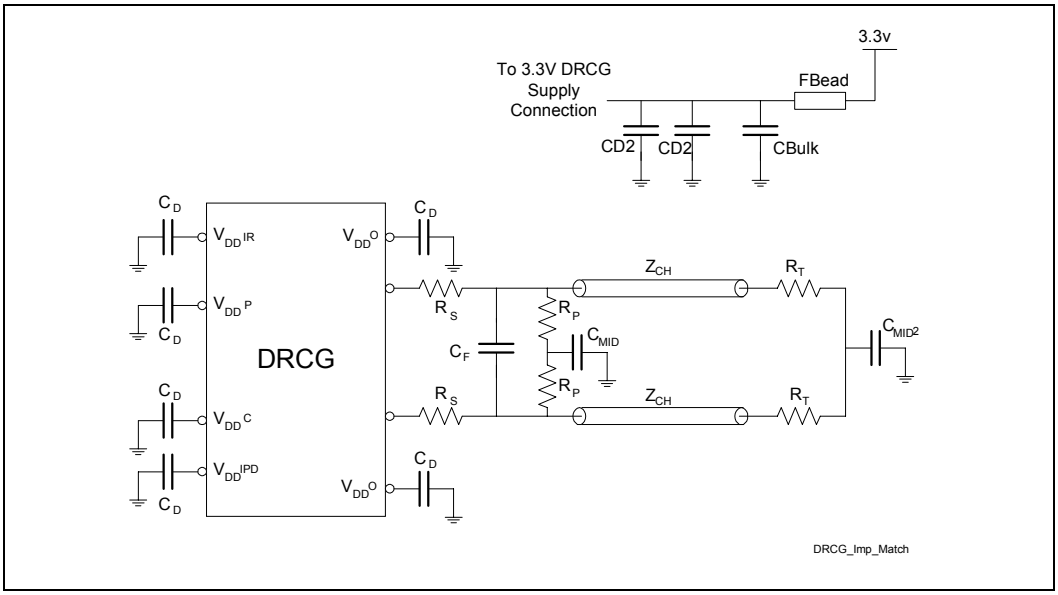


Table 7. Rambus DRCG* Impedance Matching Network Values

Component	Nominal Value	Notes
C_D	0.1 µF	Decoupling capacitors to GND
R_S	39 Ω	Series termination resistor
R_P	51 Ω	Parallel termination resistor
C_{MID1}, C_{MID2}	0.1 µF	Virtual GND caps
R_T	27 Ω	End of channel termination
C_F	4–15 pF	Do Not Stuff, leave pads for future use
FBead	50 Ω @ 100 MHz	Ferrite bead
CD2	0.1 µF	Additional 3.3 V decoupling caps
CBulk	10 µF	Bulk capacitor on device side of ferrite bead

NOTES:

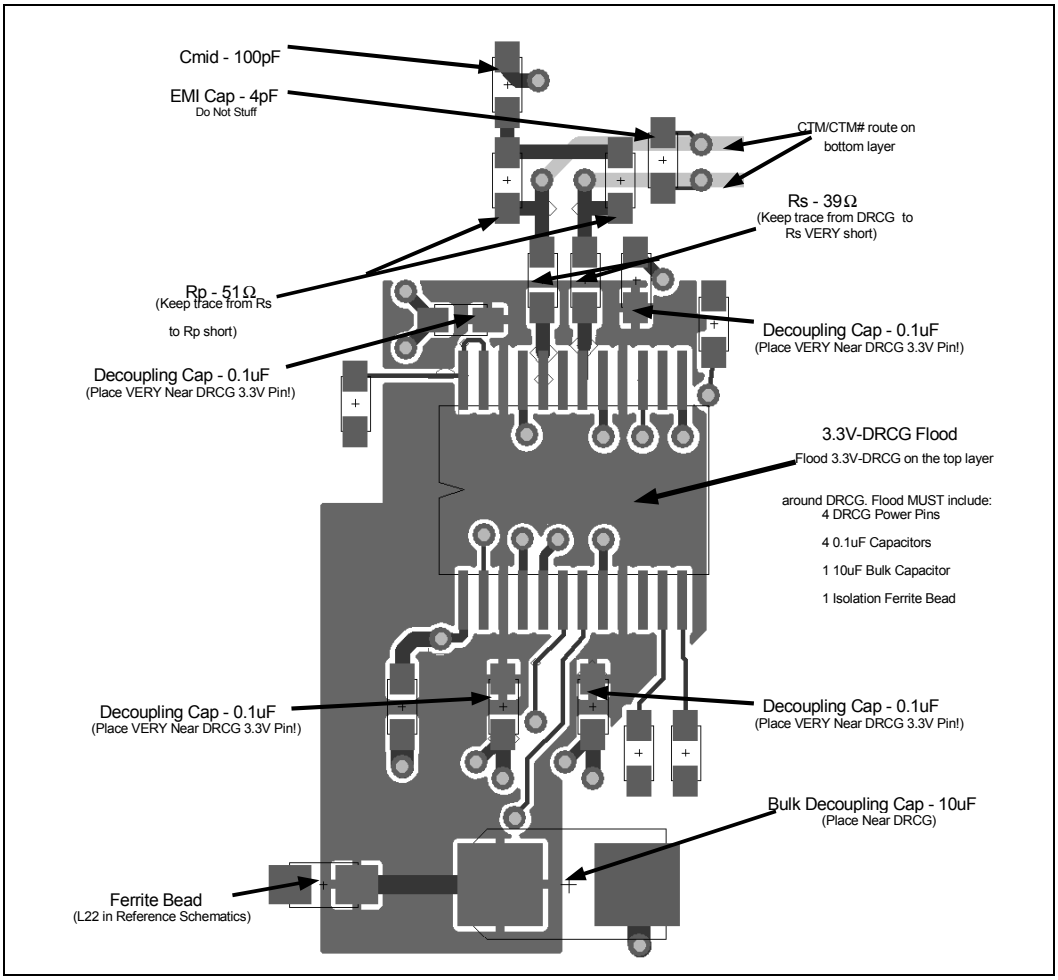
1. Note the removal of the original EMI capacitors between the junctions of RS, RP and ground. These capacitors had minimal impact on EMI and increased DRCG output jitter by approximately 2X.
2. The intent of component CF is to decouple CLK and CLKB outputs to each other, but data shows this actually increases device jitter. CF should not be stuffed at this time.
3. The ferrite bead and 10 µF bulk capacitor combination improves jitter and helps to keep the clock noise away from the rest of the system.
4. 0.1 µF capacitors are better than 0.01 µF or 0.001 µF capacitors for DRCG decoupling.
5. Cmid at 0.1 µF has improved jitter versus Cmid at 100 pF. However, this will increase the latency coming out of a stop clock or tri-state mode.
6. RS, RP, RT were modified to improve channel signal integrity through increasing CTM/CTMN swing.

The circuit shown is required to match the impedance of the DRCG to the 28 Ω channel impedance. More detailed information can be found in the Direct Rambus Clock Generator Specification.

The previously recommended 15 pF capacitors on CTM/CTM# should be removed. The 4 pF capacitor shown in the figure should not be assembled ("no-stuff").

4.3.5 Rambus DRCG* Layout Example

Figure 26. Rambus DRCG* Layout Example



4.4 Routing Guidelines for 66 MHz and 33 MHz Clocks

4.4.1 66 MHz / 33 MHz Clock Relationships

Figure 27 below shows the clock routing relationships between the 66 MHz clocks and the 33 MHz clocks. The routing guidelines and the topologies for these clocks are also documented.

Figure 27. 66 MHz / 33 MHz Clock Relationships

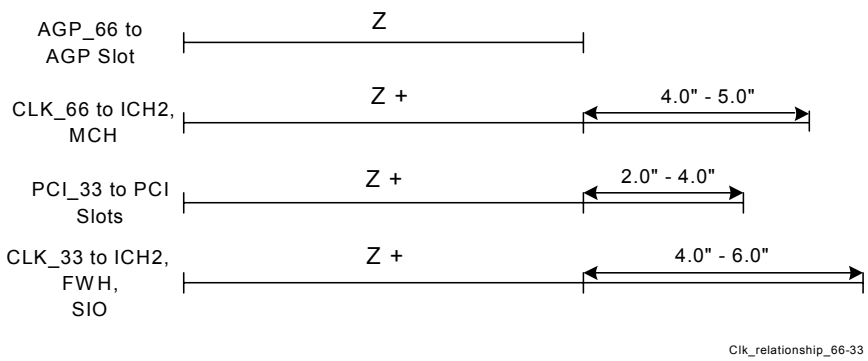


Table 8 summarizes the layout recommendations between the CK00 clock synthesizer and the AGP connector, MCH and ICH2 components, which require a 66 MHz clock.

4.4.2 66 MHz Clock Routing Length Guidelines

Table 8. 66 MHz Clock Routing Length Guidelines

Clock Group	Length of Trace A (in)	Length of Trace B (in)	R1 (Ω)
AGP_66	0” to 0.5”	Z	33
CLK_66	0” to 0.5”	Z + (4” – 5”)	33

NOTE: The routing length value of Z is 5 to 9 inches.

Figure 28 and Figure 29 show the recommended clock routing topologies for the 66 MHz clocks.

Figure 28. AGP_66 Clock Routing Topology

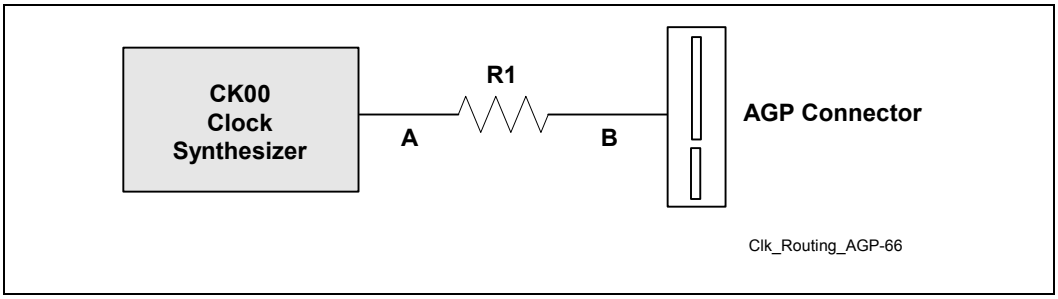
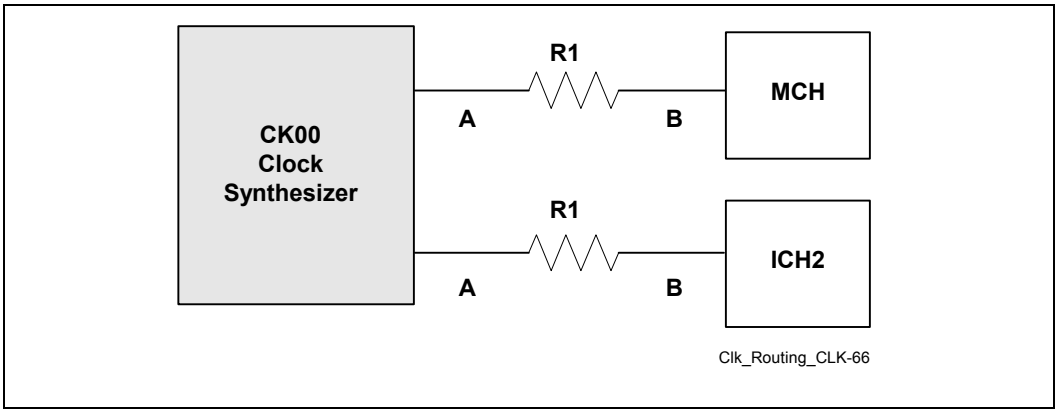


Figure 29. CLK_66 Clock Routing Topology



4.4.2.1 3V66 Clock Routing Requirement for Intel® 82850E Platforms

The 3V66 trace (CK_G_66M_MCH) from the Clock Chip to MCH cannot be shorter than the CPU Clock trace (CK_H_100M_MCH, CK_H_100M_MCH).

4.4.3 33 MHz Clock Routing Length Guidelines

Table 9 summarizes the layout recommendations between the CK00 clock synthesizer and PCI connectors, ICH2, FWH and SIO components that require a 33 MHz clock.

Table 9. 33 MHz Clock Routing Guidelines

Clock Group	Length of Trace A (inches)	Length of Trace B (inches)	R1 (Ω)
PCI_33	0 to 0.5	Z + (2 – 4)	33
CLK_33	0 to 0.5	Z + (4 – 6)	33

NOTE: The routing length value of Z is 5 to 9 inches.

Figure 30 and Figure 31 show the recommended clock routing topologies for the 33 MHz clocks.

Figure 30. PCI_33 Clock Routing Topology

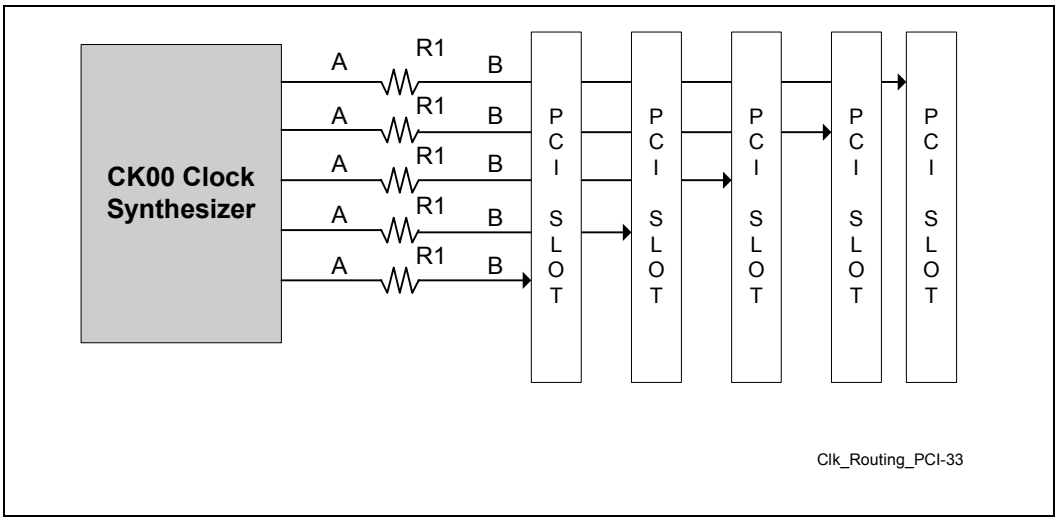
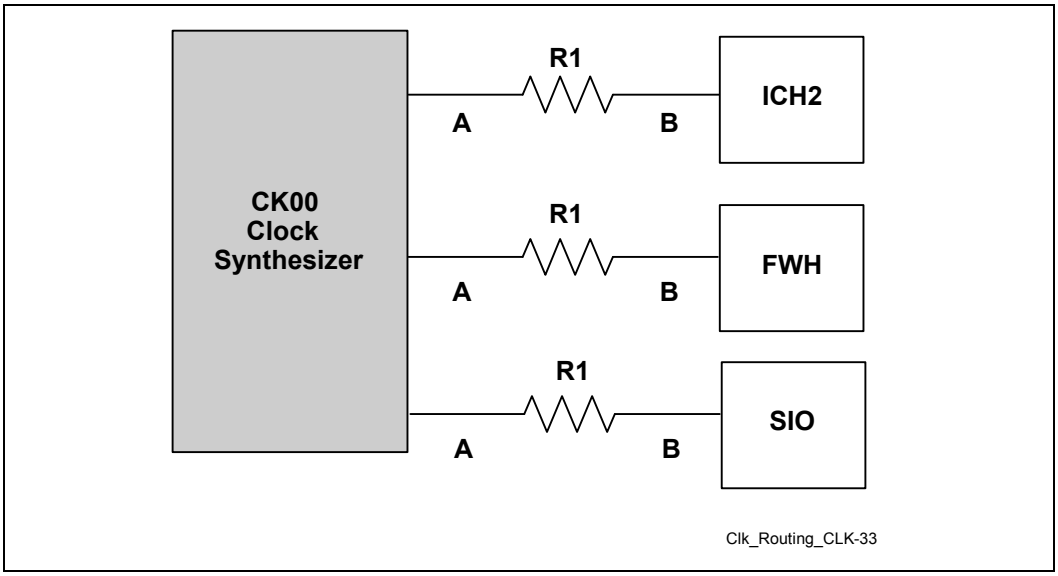


Figure 31. CLK_33 Clock Routing Topology



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5 System Bus Routing

Table 10 summarizes the layout recommendations the processor configurations and expands on specific design issues and their recommendations.

Table 10. System Bus Routing Summary for the Processor

Parameter	Processor Routing Guidelines
Line to line spacing	Data groups, address groups and control signals should be routed with 7 mil traces and 13 mil spacing between traces.
Data Line lengths (a) (agent to agent spacing) for 82850 chipset platforms	2 – 10 inches from pin to pin Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ±100 mils of the median of the associated strobes. Tighter tolerances for length matching will result in greater timing margin for the system bus. The pad is defined as the attach point of the silicon die to the package substrate. Signals in each source synchronous group should be referenced to VSS. Signals within the same group may be routed on different layers provided they are referenced to VSS and the layers are of the same configuration (all stripline or all microstrip).
Data Line lengths (b) (agent to agent spacing) for 82850E chipset platforms	2 – 8 inches from pin to pin Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ±100 mils of the median of the associated strobes. Tighter tolerances for length matching will result in greater timing margin for the system bus. The pad is defined as the attach point of the silicon die to the package substrate. Signals in each source synchronous group should be referenced to VSS. Signals within the same group may be routed on different layers provided they are referenced to VSS and the layers are of the same configuration (all stripline or all microstrip).
DSTBn/p[3:0]#	A data strobe and its complement should be routed within ±25 mils of the same pad-to-pad length. The pad is defined as the attach point of the silicon die to the package substrate. DSTBn/p# should be referenced to VSS.
Address line lengths (agent to agent spacing)	2 – 10 inches from pin to pin Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ±200 mils of the associated strobe. Tighter tolerances for length matching will result in greater timing margin for the system bus. The pad is defined as the attach point of the silicon die to the package substrate. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip).
ADSTBn/p[1:0]#	2 – 10 inches from pin to pin Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ±200 mils of the associated strobe. Tighter tolerances for length matching will result in greater timing margin for the system bus. The pad is defined as the attach point of the silicon die to the package substrate. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip).

Parameter	Processor Routing Guidelines
Common Clock line lengths	6 – 10 inches pin to pin No length compensation is necessary.
Topology	Point to point (chipset to processor).
Routing priorities	All signals should be referenced to VSS. Ideally, layer changes should not occur for any signals. If a layer change must occur, reference plane must be VSS and the layers must all be of the same configuration (all stripline or all microstrip for example). Refer to Section 5.3 for specific details.
Clock Keepout Zones	Clocks pairs should have 20 mils spacing from other signals.
Trace Impedance	50 ohms ± 15% for 7 mil traces

5.1 Return Path

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, vias, VRMs etc. It is useful to think of the return path as following a path of least resistance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths need to be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance will be.

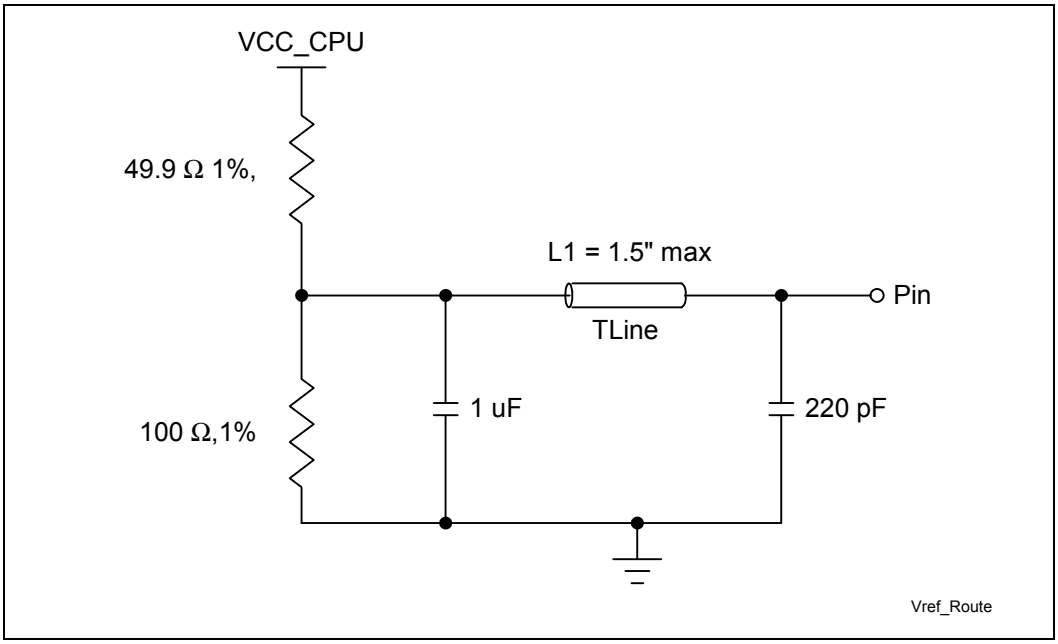
The following sets of return path rules apply:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near system bus signals.
- Maintain VSS as a reference plane for all system bus signals.
- Do not route over via anti-pads or socket anti-pads.

5.2 GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage only needs to be supplied to one of the four pins. The other three pins can be left unconnected.

Figure 32. GTLREF Routing



- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a 1 µF capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin
- Decouple the pin with a high frequency capacitor (such as a 220 pF 603) as close to the pin as possible
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use a minimum of a 7 mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the system bus signals.)

5.3 Processor Configuration

Both recommendations and considerations are described in this section.

For proper operation of the processor and the Intel 850 chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions that may be different than an OEM's system design. The most accurate way to understand the signal integrity and timing of the system bus in your platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stack-up and other parameters can be made that improve system performance.

A schematic of the processor topology is shown in Figure 33. The trace impedance should be 50 Ω ±15%. The traces should maintain a greater than three to one edge-to-edge spacing versus trace to reference plane height ratio. Simulations performed at Intel have assumed, for nominal conditions, a 7 mil wide trace and 13 mil edge-to-edge spacing. As the traces pass through the pin fields this requirement may not be achievable. In these areas where the 7 mil width and 13 mil spacing is not possible, 7 mil traces with 5 mil spacing is acceptable.

Refer to the processor datasheet for a system bus signal list, signal types and definitions.

5.3.1 Topology and Routing

Table 11. Source Synchronous Signal Groups and the Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	ADSTB0#
A[32:17]#	ADSTB1#
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#

Design recommendations will be presented first followed by design considerations.

5.3.1.1 Design Recommendations

Below are the design recommendations for the data, address, strobes, and common clock signals. For the following discussion, the pad is defined as the attach point of the silicon pad to the package substrate.

Data

The pin to pin distance from the processor to the chipset should be between 2.0 to 10 inches (i.e., 2.0 inches < L1 < 10 inches). Data signals of the same source synchronous group should be routed to the same pad to pad length within ±100 mils of the associated strobes. As a result, additional trace will be added to some data nets on the system board in order for all trace lengths within the same data group to be the same length (±100 mils) from the pad of the processor to the pad of the chipset. This length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without the length compensation the flight times between a data signal and its strobe will be different, which results in an inequity between the setup and hold times.

Equation 1. Calculations to determine the package delta addition to motherboard length for UP systems

$$\text{delta}_{\text{net,strobe}} = (\text{cpu\_pkglen}_{\text{net}} - \text{cpu\_pkglen}_{\text{strobe*}}) + (\text{cs\_pkglen}_{\text{net}} - \text{cs\_pkglen}_{\text{strobe}})$$

NOTE: Strobe package length is the average of the strobe pair.

Address

Address signals follow the same rules as data signals except they should be routed to the same pad to pad length within ±200mils of the associated strobes. Address signals may change layers if the reference plane remains VSS and as long as the layers for a given group are all of the same configuration (all stripline or all microstrip).

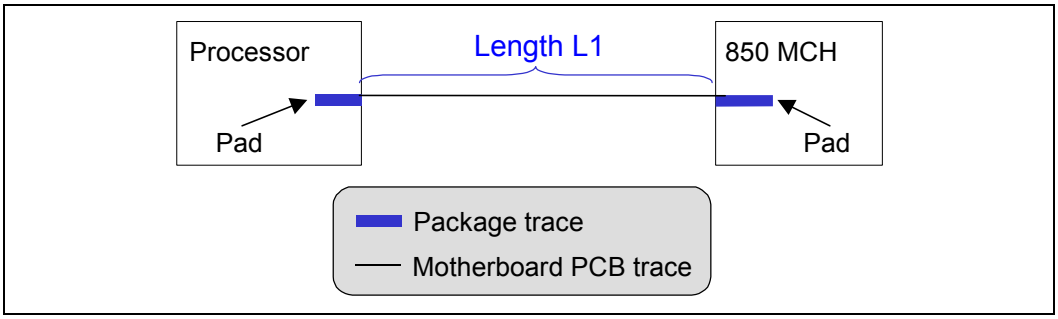
Data Strobes

A strobe and its complement (xSTBp/n#) should be routed to ±25 mils of the same length. It is recommended to simulate skew in order to determine the length that best centers the strobe for a given system.

Common Clock

Common clock signals should be routed to a minimum pin to pin motherboard length of 6 inches and a maximum motherboard length of 10 inches.

Figure 33. Processor Topology



5.3.1.2 Design Considerations

Intel has found that the following recommendations aid in the routing of the processor, given the example stack-up shown in Figure 9.

- Line width is 7.0 mil.
- Trace to trace spacing is 13.0 mil (except in component breakout where spacing is constrained where 5 mil spacing is acceptable)

Table 12. Processor Package Lengths

Net Name	Intel® Pentium® 4 Processor in 478-pin Package Length (inches)	Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Package Length (inches)
Address Group 0		
ADSTB#[0]	0.201	0.219
A#[03]	0.344	0.393
A#[04]	0.249	0.281
A#[05]	0.139	0.170
A#[06]	0.394	0.436
A#[07]	0.279	0.330
A#[08]	0.130	0.157
A#[09]	0.369	0.374
A#[10]	0.323	0.330
A#[11]	0.230	0.261
A#[12]	0.382	0.407
A#[13]	0.396	0.420
A#[14]	0.335	0.362

Net Name	Intel® Pentium® 4 Processor in 478-pin Package Length (inches)	Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Package Length (inches)
A#[15]	0.230	0.253
A#[16]	0.192	0.204
REQ#[0]	0.407	0.448
REQ#[1]	0.181	0.232
REQ#[2]	0.246	0.294
REQ#[3]	0.317	0.357
REQ#[4]	0.352	0.360
Address Group 1		
ADSTB#[1]	0.208	0.220
A#[17]	0.463	0.477
A#[18]	0.409	0.399
A#[19]	0.290	0.316
A#[20]	0.235	0.257
A#[21]	0.335	0.333
A#[22]	0.382	0.394
A#[23]	0.446	0.470
A#[24]	0.152	0.160
A#[25]	0.362	0.396
A#[26]	0.268	0.294
A#[27]	0.411	0.423
A#[28]	0.156	0.177
A#[29]	0.495	0.491
A#[30]	0.202	0.232
A#[31]	0.277	0.293
Data Group 0		
DSTBN#[0]	0.311	0.365
DSTBP#[0]	0.291	0.362
D#[00]	0.393	0.434
D#[01]	0.456	0.494
D#[02]	0.517	0.559
D#[03]	0.583	0.634
D#[04]	0.365	0.407
D#[05]	0.360	0.411
D#[06]	0.505	0.565

Net Name	Intel® Pentium® 4 Processor in 478-pin Package Length (inches)	Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Package Length (inches)
D#[07]	0.433	0.495
D#[08]	0.493	0.537
D#[09]	0.568	0.612
D#[10]	0.249	0.298
D#[11]	0.174	0.232
D#[12]	0.562	0.616
D#[13]	0.439	0.485
D#[14]	0.157	0.209
D#[15]	0.527	0.572
DBI#[0]	0.286	0.332
Data Group 1		
DSTBN#[1]	0.290	0.312
DSTBP#[1]	0.298	0.313
D#[16]	0.263	0.281
D#[17]	0.479	0.481
D#[18]	0.351	0.365
D#[19]	0.407	0.428
D#[20]	0.437	0.449
D#[21]	0.496	0.521
D#[22]	0.505	0.521
D#[23]	0.589	0.605
D#[24]	0.164	0.188
D#[25]	0.514	0.535
D#[26]	0.413	0.412
D#[27]	0.162	0.181
D#[28]	0.235	0.254
D#[29]	0.391	0.410
D#[30]	0.303	0.323
D#[31]	0.467	0.479
DBI#[1]	0.455	0.460
Data Group 2		
DSTBN#[2]	0.250	0.254
DSTBP#[2]	0.268	0.265
D#[32]	0.310	0.291

Net Name	Intel® Pentium® 4 Processor in 478-pin Package Length (inches)	Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Package Length (inches)
D#[33]	0.224	0.227
D#[34]	0.177	0.180
D#[35]	0.380	0.361
D#[36]	0.270	0.273
D#[37]	0.460	0.448
D#[38]	0.443	0.431
D#[39]	0.380	0.386
D#[40]	0.169	0.162
D#[41]	0.352	0.333
D#[42]	0.388	0.373
D#[43]	0.338	0.321
D#[44]	0.428	0.412
D#[45]	0.381	0.379
D#[46]	0.222	0.219
D#[47]	0.289	0.269
DBI#[2]	0.443	0.439
Data Group 3		
DSTBN#[3]	0.293	0.302
DSTBP#[3]	0.298	0.303
D#[48]	0.415	0.424
D#[49]	0.320	0.329
D#[50]	0.270	0.269
D#[51]	0.383	0.386
D#[52]	0.161	0.174
D#[53]	0.258	0.246
D#[54]	0.338	0.344
D#[55]	0.437	0.457
D#[56]	0.447	0.460
D#[57]	0.423	0.430
D#[58]	0.333	0.339
D#[59]	0.385	0.386
D#[60]	0.230	0.214
D#[61]	0.431	0.422
D#[62]	0.269	0.268
D#[63]	0.400	0.387

Net Name	Intel® Pentium® 4 Processor in 478-pin Package Length (inches)	Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Package Length (inches)
DBI#[3]	0.203	0.201
BCLK		
BCLK[0]	0.540	0.596
BCLK[1]	0.539	0.598

5.4 Routing Guidelines for Asynchronous GTL+ and Other Signals

This section describes layout recommendations for signals other than data, strobe and address. Table 13 lists the signals covered in this section.

Table 13. Miscellaneous Signals (Signals That Are Not Data, Address, or Strobe)[1,3]

Signal Name	Type	Direction	Topology	Driven by	Received by	Notes
A20M#	Asynchronous GTL+	I	2	ICH2	Processor	
BR0#	AGTL+	I/O	4	Processor		2
COMP[1:0]	analog	I	5	External logic	Processor	
FERR#	Asynchronous GTL+	O	1a	Processor	ICH2	2
IGNNE#	Asynchronous GTL+	I	2	ICH2	Processor	
INIT#	Asynchronous GTL+	I	2a	ICH2	Processor /FWH	2
LINT0/INTR LINT1/NMI	Asynchronous GTL+	I	2	ICH2	Processor	
PROCHOT#	Asynchronous GTL+ OD	O	1b	Processor	External logic	2
PWRGOOD	Asynchronous GTL+ OD	I	2-b	ICH2	Processor	2
RESET#	AGTL+ OD	I	4	MCH	Processor	2
SLP#	Asynchronous GTL+	I	2	ICH2	Processor	
SMI#	Asynchronous GTL+	I	2	ICH2	Processor	
STPCLK#	Asynchronous GTL+	I	2	ICH2	Processor	
THERMTRIP#	Asynchronous GTL+	O	1b	Processor	External logic	2
VCCA	power	I	3	External logic	Processor	
VCCIOPLL	power	I	3	External logic	Processor	
VCC_SENSE	other	O		Processor		
VID[4:0]	other	O		Processor	V_{REG}	
VSSA	power	I	3	Ground	Processor	
VSS_SENSE	other	O		Processor		

NOTES:
1. For more information on these signals, refer to Chapter 11.
2. All miscellaneous signals that require a pull up should be pulled up to VCC_CPU.

All signals must meet the AC and DC specifications as documented in the processor datasheet.

5.4.1 Topologies

The following sections describe the topologies and layout recommendations for the miscellaneous signals.

5.4.1.1 Topology 1: Asynchronous GTL+ Signals Driven by the Processor

These signals (FERR#, PROCHOT# and THERMTRIP#) should adhere to the following routing and layout recommendations. Figure 34 and Figure 35 illustrate the recommended topologies. If THERMTRIP# and PROCHOT# are routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Table 14. Layout Recommendations for FERR# Signals (Topology 1a)

Trace Zo	Trace Spacing	L1	L3	Rpu
60 Ω	7 mil	1–12”	3” max	62 ±5% Ω

Figure 34. Routing Illustration for FERR#

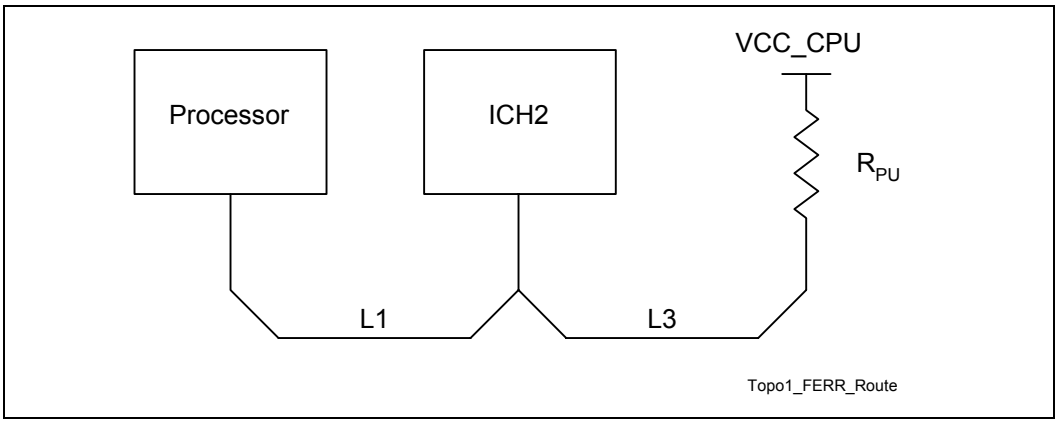
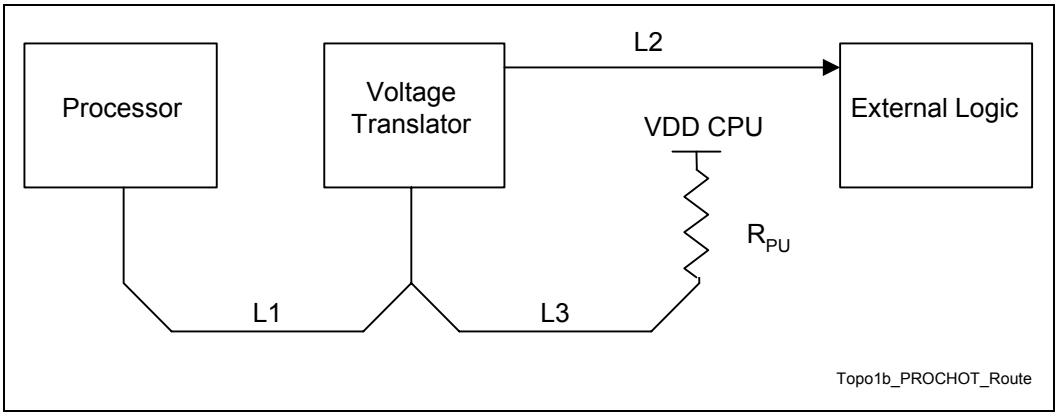


Table 15. Layout Recommendations for PROCHOT# and THERMTRIP# Signals (Topology 1b)

Trace Zo	Trace Spacing	L1	L2	L3	Rpu
60 Ω	7 mil	1–17”	10” max	3” max	62 Ω ±5%

Figure 35. Routing Illustration for PROCHOT# and THERMTRIP# (Topology 1B)



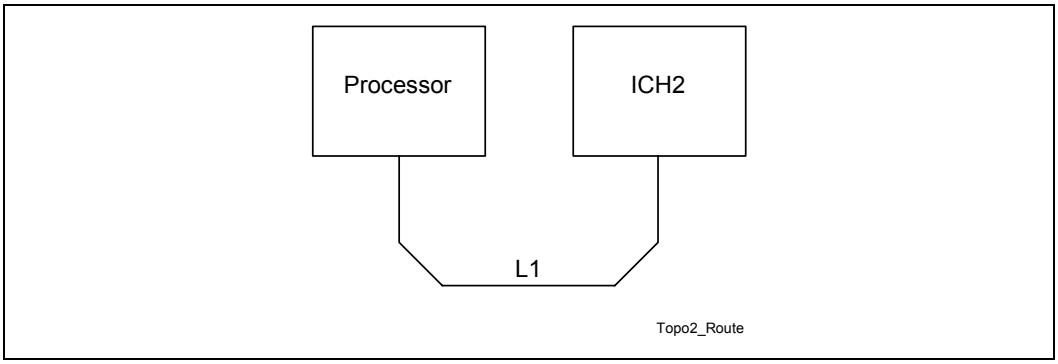
5.4.1.2 Topology 2: Asynchronous GTL+ Signals Driven by Intel® ICH2

These signals (A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#) should adhere to the following routing and layout recommendations. Figure 36 illustrates the recommended topology.

Table 16. Layout Recommendations for Miscellaneous Signals (Topology 2)

Trace Zo	Trace Spacing	L1	Rpu
60 Ω	7 mil	12 inches max	None

Figure 36. Routing Illustration for A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#

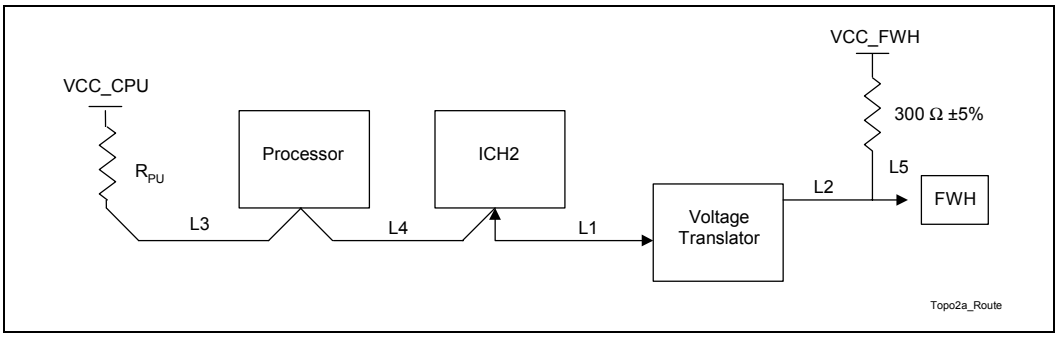


5.4.1.3 Topology 2A: INIT#

Table 17. Layout Recommendations for INIT# (Topology 2A)

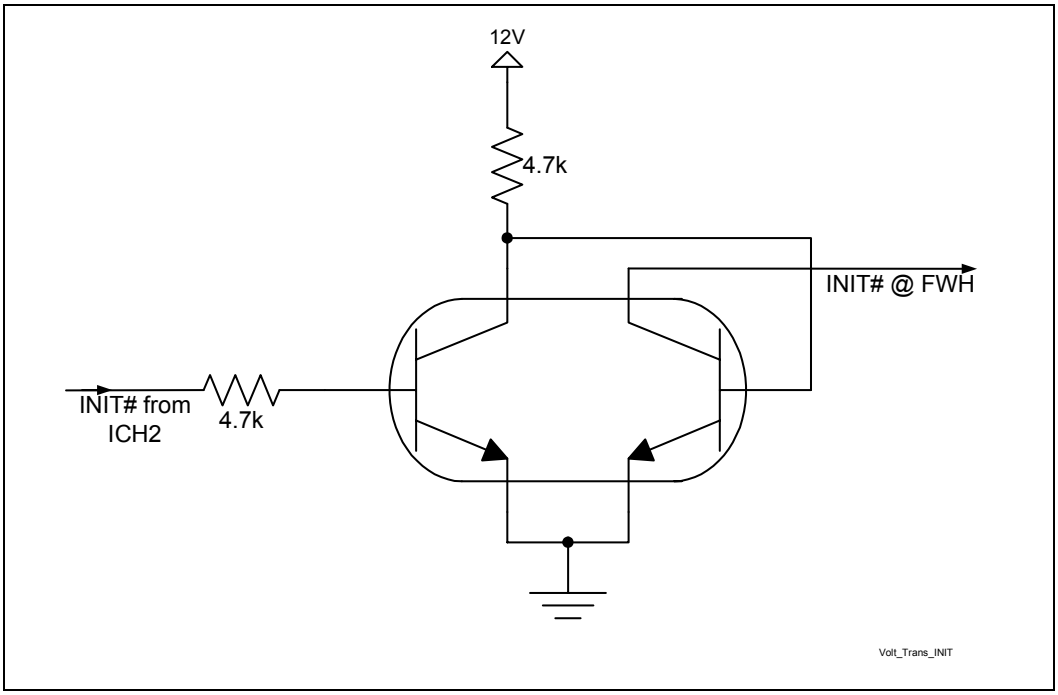
Trace Zo	Trace Spacing	L1	L2	L3	L4	L5	Rpu
60 Ω	7 mil	2” max	10” max	3” max	17” max	3” max	300 Ω 5%

Figure 37. Routing Illustration for INIT#



Level shifting is required for the INIT# signal to the FWH in order to meet the input logic levels of the FWH. Figure 38 illustrates one method of implementing this level shifting.

Figure 38. Voltage Translation of INIT#



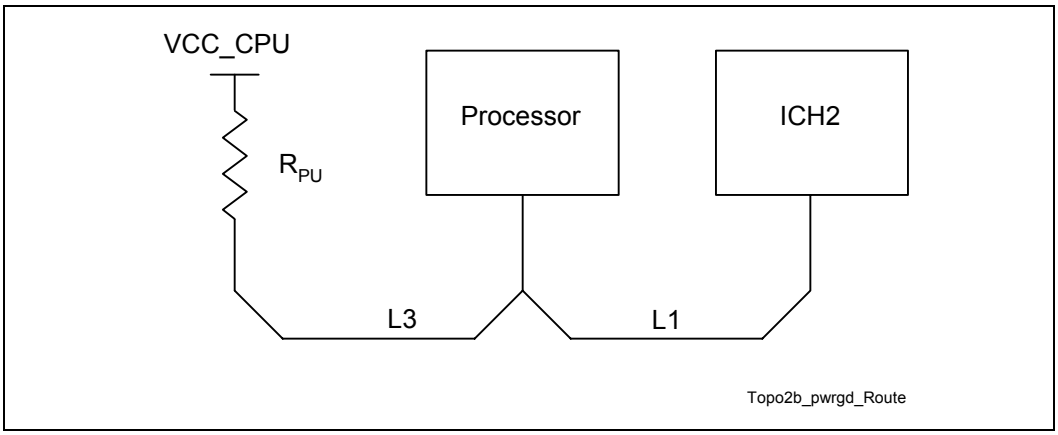
5.4.1.4 Topology 2B: Asynchronous GTL+ Signals Driven by Intel® ICH2

This signal (Open Drain; PWRGOOD) should adhere to the following routing and layout recommendations. Figure 39 illustrates the recommended topology.

Table 18. Layout Recommendations for Miscellaneous Signals (Topology 2B)

Trace Zo	Trace Spacing	L1	L3	Rpu
60 Ω	7 mil	1–12"	3" max	300 Ω ±5%

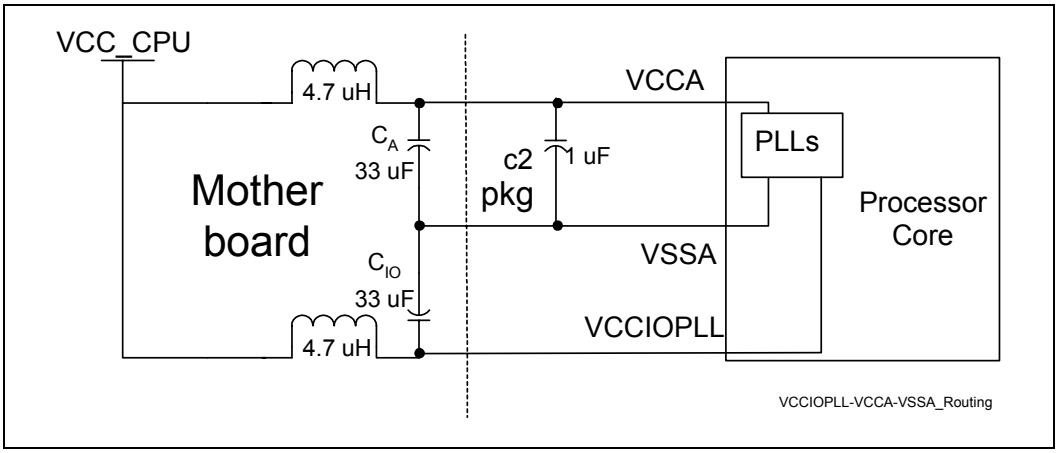
Figure 39. Routing Illustration for PWRGOOD



5.4.1.5 Topology 3: VCCIOPLL, VCCA and VSSA

VCCIOPLL and VCCA are isolated power for internal PLLs. It is critical that they have clean, noiseless power on their input pins. Keep these signals away from noisy or high frequency signals. Keep their traces as short as possible. Follow the recommendations in Figure 40 for layout guidelines. VSSA should not be connected directly to ground on the system board. Further details can be found in Section 11.4.

Figure 40. Routing Illustration for VCCIOPLL, VCCA and VSSA



5.4.1.6 Topology 4: BR0# and RESET#

Since the processor **does not have on-die termination on the BR0# and RESET# signals**, it is necessary to terminate using discrete components on the system board. Connect the signals between the components as shown in Figure 41. The Intel 850 chipset has on-die termination and thus it is necessary to terminate only at the processor end. The value of Rt should be 51 Ω ±5% for RESET#. The value of Rt should be 150–220 Ω ±5% for BR0#.

Figure 41. Routing Illustration for BR0# and RESET#

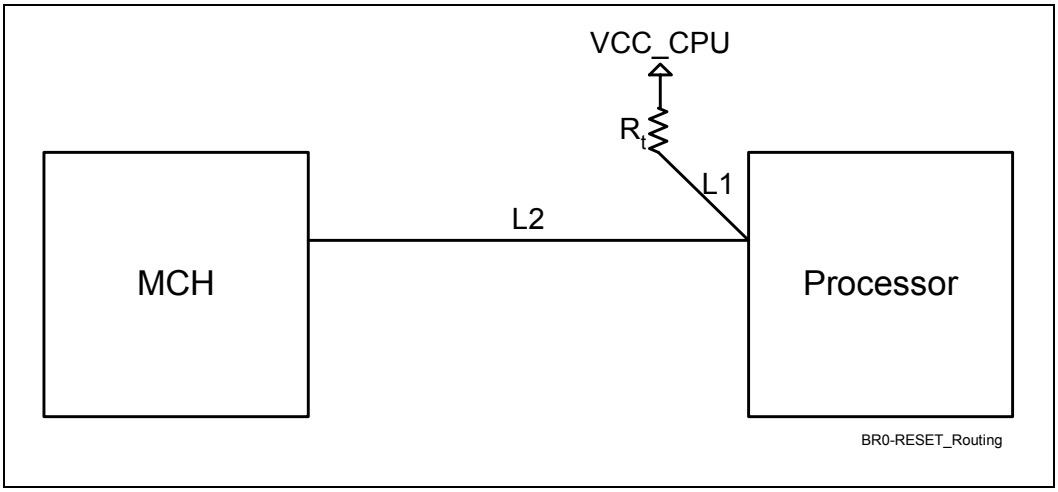


Table 19: BR0# and RESET# Lengths

Signal	Rt	L1	L2
RESET#	51 Ω	≤ 1–2”	6–10”
BR0#	150–220 Ω	≤ 1–2”	6–10”

5.4.1.7 Topology 5: COMP[1:0] Signals

Terminate the COMP[1:0] pins to ground through a 51 Ω ±1% resistor as close as possible to the pin. Do not wire COMP pins together, connect each pin to its own termination resistor.

5.4.1.8 Topology 6a: BSEL[1:0] Termination – 400 MHz System Bus Only

The BSEL[1:0] signals on the processor should be left as no-connect. The CK00 part should be configured for 100 MHz BCLK[1:0]operation.

5.4.1.9 Topology 6b: BSEL[1:0] Termination – 533/400 MHz System Bus

The BSEL0 signal on the processor should be routed to the CK00 Sel100/133 pin. BSEL1 can be left as a no-connect. See Figure 17.

5.4.1.10 Topology 7: THERMDA/THERMDC Routing Guidelines

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the processor for thermal management/long term die temperature change monitoring purpose. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Routing guidelines for THERMDA/THERMDC:

Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. Below are some guidelines:

- Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4 to 8 inches away as long as the worst noise sources such as clock generators, data buses and address buses etc. are avoided.
- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.
- Leakage currents due to system board contamination must be considered. Error can be introduced by the leakage current.
- Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. A width of 10 mils and spacing of 10 mils is recommended.

5.4.1.11 Topology 8: TESTHI and RESERVED Pins

The TESTHI pins should be tied to the processor VCC using a matched resistor, where a matched resistor has a resistance value within +- 20% of the impedance of the board transmission line traces. For example, If the trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω is required.

The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. a matched resistor should be used for each group:

- TESTHI[1:0]
- TESTHI[5:2]
- TESTHI[10:8]
- TESTHI[12:11]

Additionally, if the ITPCLKOUT[1:0] pins are not used then they may be connected individually to VCC using matched resistors or grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1k ohm resistors is acceptable. Tying ITPCLKOUT[1:0] directly to VCC or sharing a pull-up resistor to VCC will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

As an alternative, group 2 (TESTHI [5:2]), and the ITPCLKOUT[1:0] pins may be tied directly to the processor VCC. This has no impact on system functionality. TESTHI[0] and TESTHI[12] may also be tied directly to processor VCC if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0], directly tying to VCC is strongly discouraged for system boards that do not implement an onboard debug port.

5.4.1.12 Topology 9: Processor Voltage Regulator Sequencing Requirements

The Pentium 4 processor with 512KB L2 cache on .13 micron process requires a 1.2 V supply to the VCCVID pin to support the on-die VID generation circuitry. The current requirements for this voltage is 30 mA. A linear regulator is recommended to generate this voltage. The on-die VID generation circuitry also has some power sequencing requirements. Figure 45 shows a block diagram of a power sequencing implementation. Figure 46 and Figure 47 illustrate timing diagrams of the power sequencing requirements.

5.4.1.13 VCCVID Regulator Recommendations

- The output of the voltage regulator used to generate VCCVID should be no more than 1.5 inches away from pin AF4 of the processor.
- The trace connecting the voltage regulator output to pin AF4 should be as wide as practical, but not less than 0.025 inches.
- The trace connecting the voltage regulator output to pin AF4 should have both a 0.1 µF and 1.0 µF capacitor for decoupling. The 1.0 µF capacitor should be located as close as possible to the output of the voltage regulator. The 0.1 µF capacitor should be located as close as possible to pin AF4 on the processor.
- If an integrated voltage regulator such as the MIC5248 is used, the voltage input (pin 1) should be connected to the system board's VCC or 3.3 V rails through a zero ohm resistor. The input of the voltage regulator should also be decoupled with a 0.1µF capacitor at the pin. The trace connecting the voltage regular input to the zero resistor should be equal to or greater than the voltage regulator output trace connected to the processor (i.e., if the connection to the processor is 0.025 inches than the trace width to the input of the voltage regulator should be 0.025 inches or greater). The voltage regulator power good signal (pin 4) should be connected to the voltage regulator output (pin 5) through a 10 kΩ resistor.
- During power-on the rising edge of the VCCVID power supply needs to be monotonic. Examples of an acceptable monotonic and an unacceptable non-monotonic rising edge are show below for reference.

Figure 42. Passing Monotonic Rising Edge Voltage Waveform

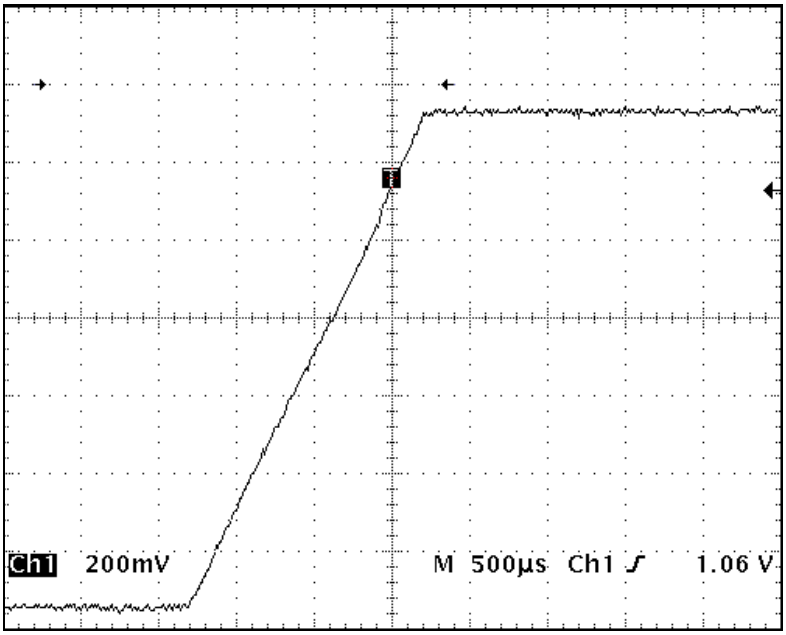
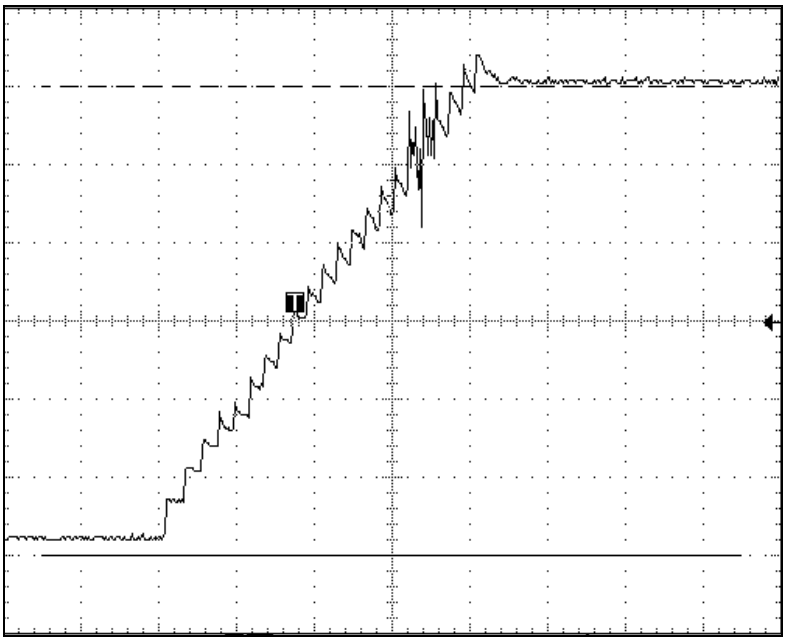


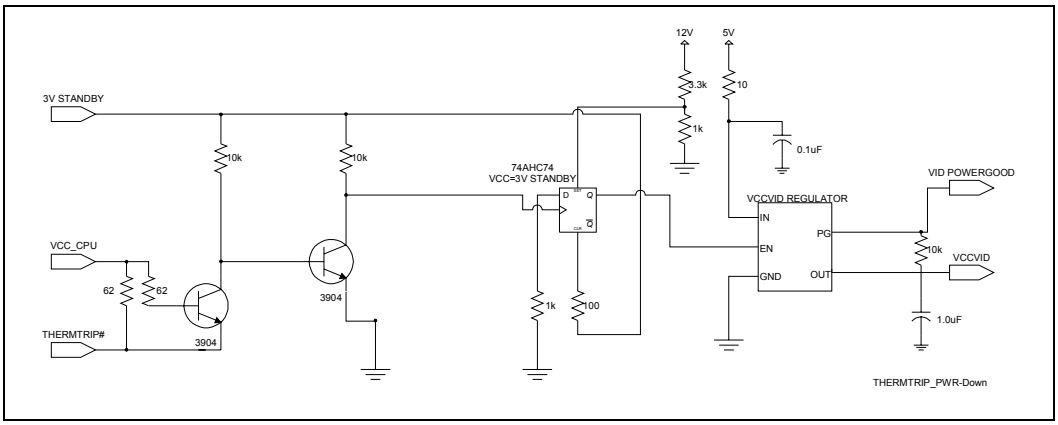
Figure 43. Failing Non-monotonic Rising Voltage Waveform



5.4.1.14 Topology 10: THERMTRIP# Power Down Circuit

It is required that power is removed from the processor core within 0.5 seconds of the assertion of the THERMTRIP# signal. Below is an example circuit that will power down the processor voltage regulator when THERMTRIP# is asserted.

Figure 44. THERMTRIP# Power Down Circuit



In the above drawing, VID POWERGOOD is a signal that is connected to the output enable of the processor voltage regulator controller.

Figure 45. Power Sequencing Block Diagram

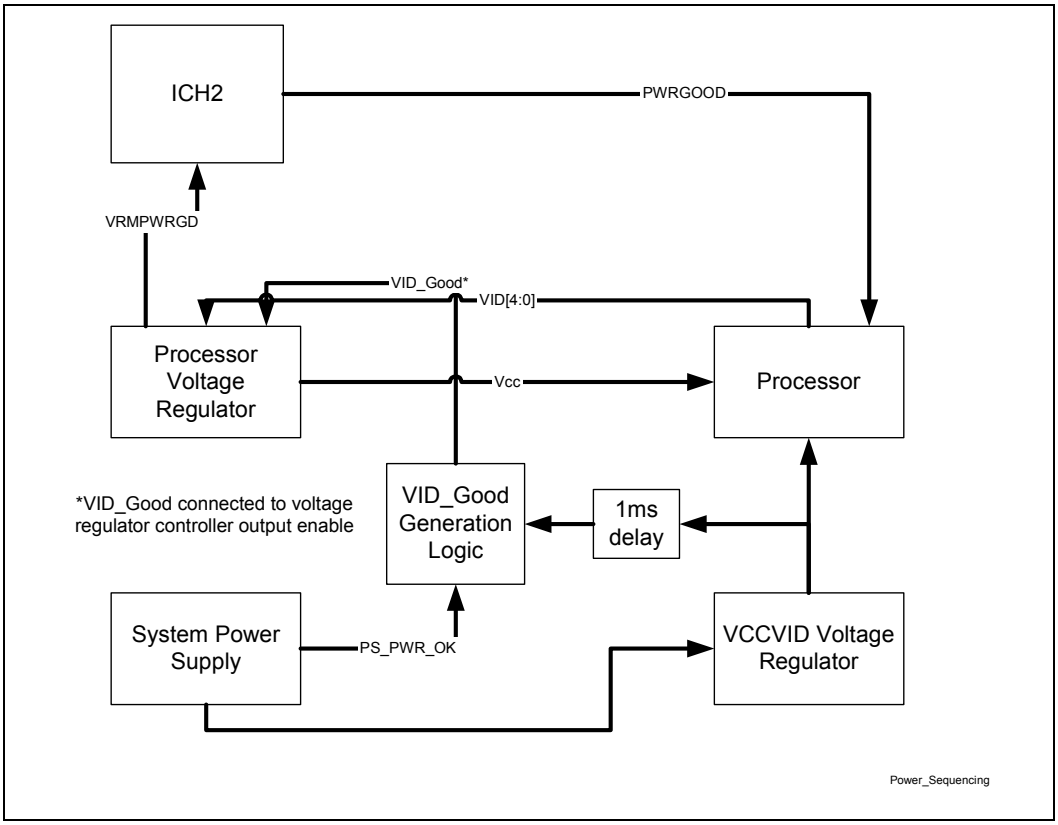


Figure 46: Power-on Sequence Timing Diagram

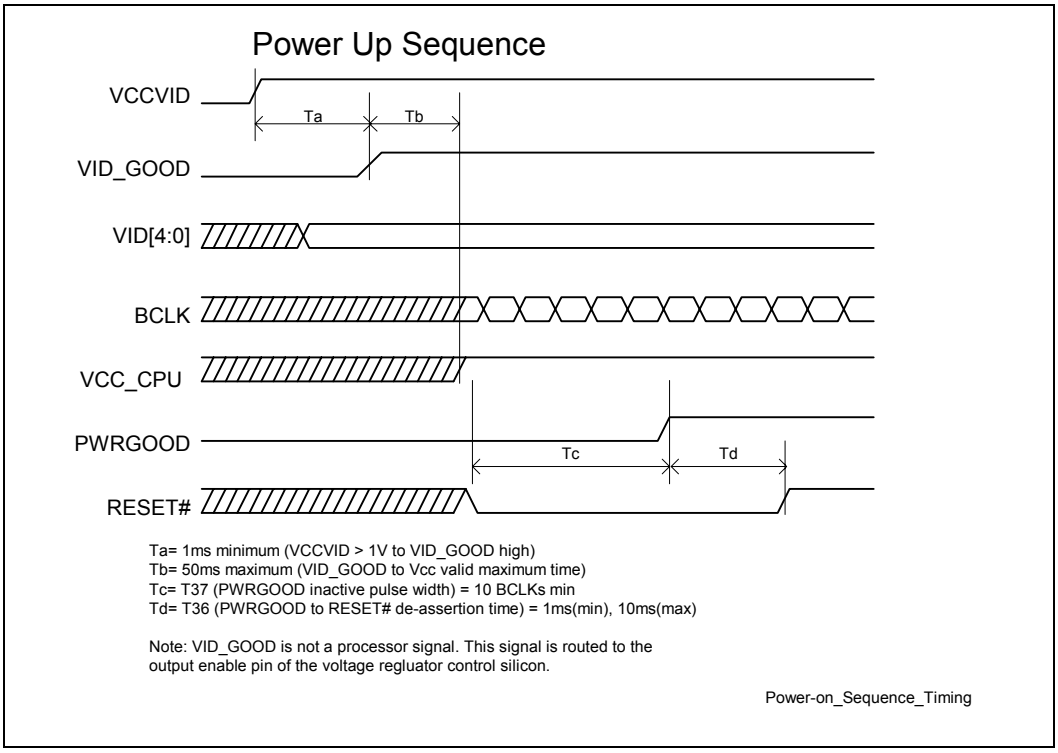


Figure 47. Power-off Sequence Timing Diagram

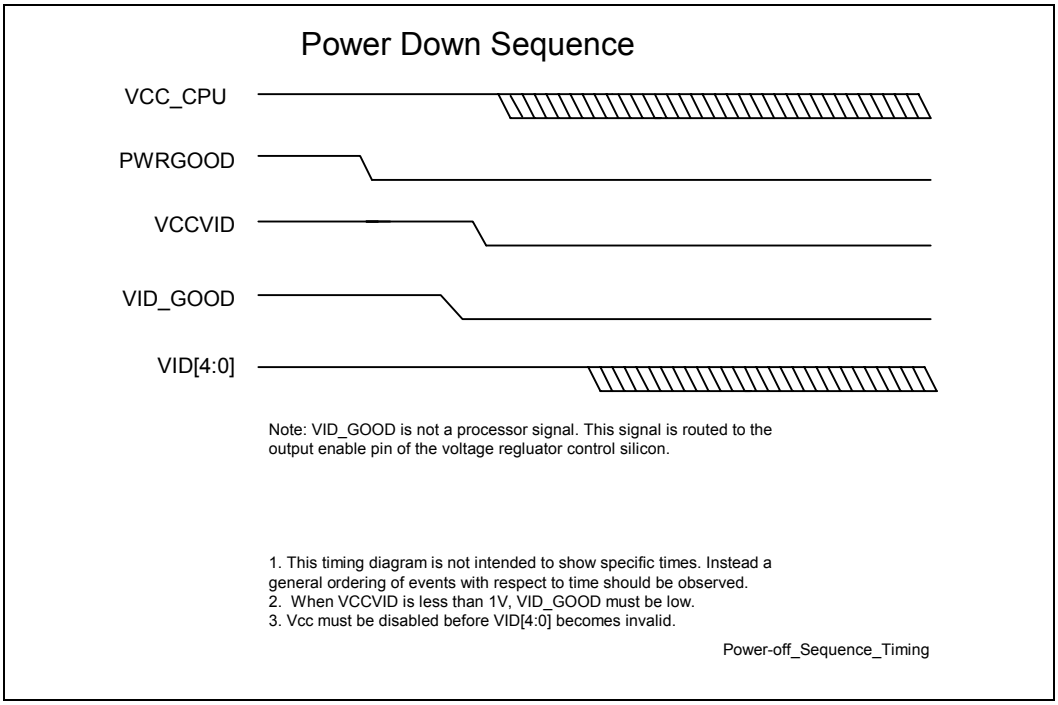
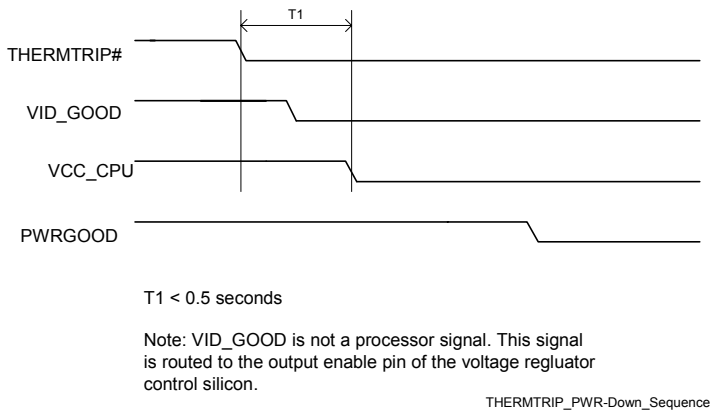


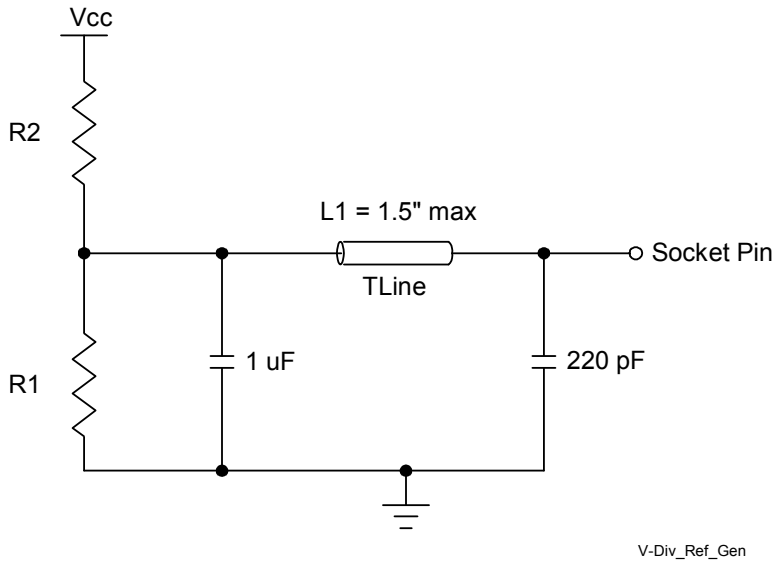
Figure 48. THERMTRIP# Power Down Sequence



5.5 Intel® MCH System Bus Interface

A voltage divider network should supply host interface reference voltages locally as shown in Figure 49, Figure 50 and as specified by Table 20.

Figure 49. Voltage Divider Network for Reference Voltage Generation



NOTES:
1. The MCH has only one dedicated voltage divider.
2. Decouple the voltage divider with a 1 µF capacitor.
3. Keep the voltage divider within 1.5 inches of the MCH Vref ball

Figure 50. Pull-Down Circuit

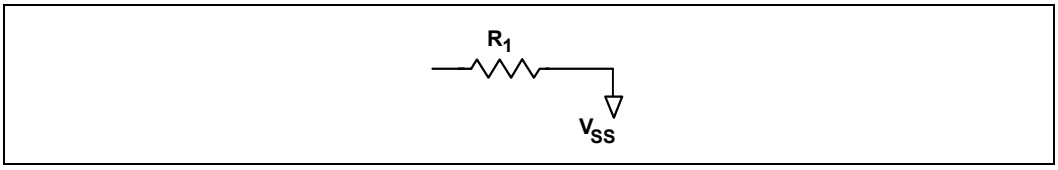


Table 20. Reference Voltage Network Values

Signal	R1	R2	Tolerance	Figure	Notes
HDVREF[3:0]	100 Ω	50 Ω	±1%	Figure 49	1,2
HAVREF[1:0]	100 Ω	50 Ω	±1%	Figure 49	1,2
CCVREF	100 Ω	50 Ω	±1%	Figure 49	1,2
HRCOMP[1:0]	25 Ω	—	±1%	Figure 50	3
HSWNG[1:0]	50 Ω	100 Ω	±1%	Figure 49	4

NOTES:
1. 2/3 VTT Resistor Network
2. Single voltage divider for these signals.
3. Independent of board impedance.
4. 1/3 VTT Resistor Network

5.5.1 Intel® MCH System Bus I/O Decoupling Requirements

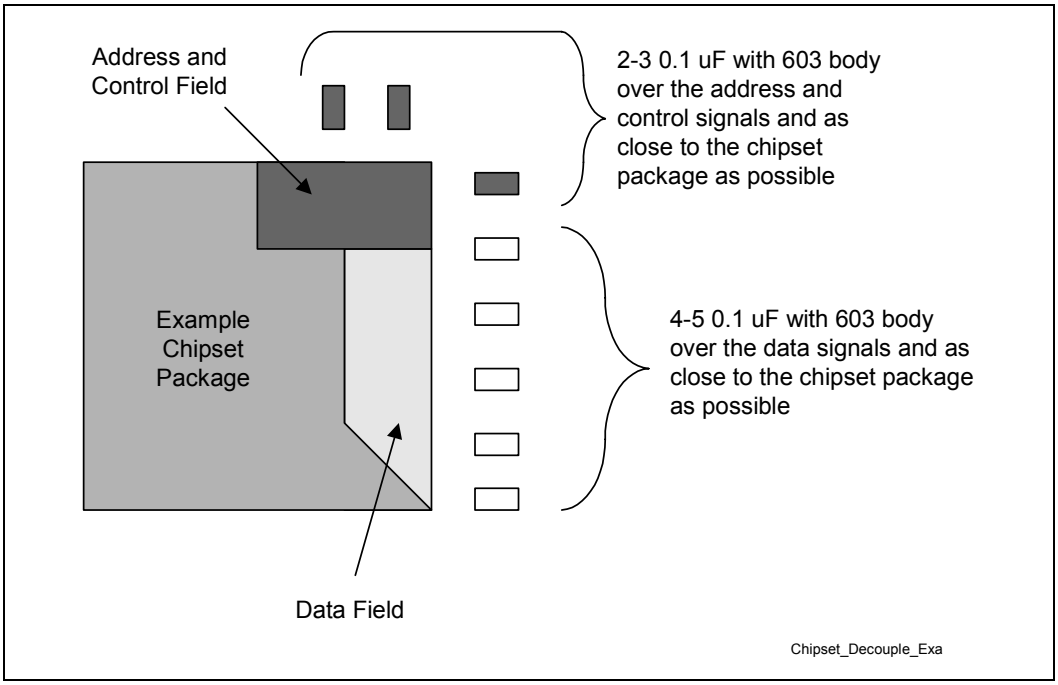
The primary objective of the decoupling requirements for the chipset is to provide clean power delivery to the System Bus I/O ring. The split plane nature of chipsets creates this power delivery concern.

The secondary objective of decoupling at the chipset is to minimize the impact of return path discontinuities that may occur between the chipset package and the system board. A return path discontinuity occurs in systems whose signals reference either power or ground, but not both. While the chipset uses symmetric stripline interconnects that reference the signal to both VCC_CPU and VSS. Systems that have this type of referencing should use the larger number of decoupling capacitors listed in the below guidelines for the chipset.

The requirements for the chipset are:

- 4 minimum, 5 preferred 0.1 µF capacitors with 603 packages distributed evenly over the System Bus data lines
- 2 minimum, 3 preferred 0.1 µF capacitors with 603 packages distributed evenly over the System Bus address and control lines
- All capacitors placed as close as possible to the MCH package (within 150 mils)

Figure 51. Example Intel® MCH Decoupling Guidelines for Chipset



5.6 System Bus Routing Guidelines - Four-Layer Motherboard

The following are descriptions and illustrations of system bus routing on the 4-layer customer reference board.

Figure 52. Customer Reference Platform System Bus Routing – Top Layer

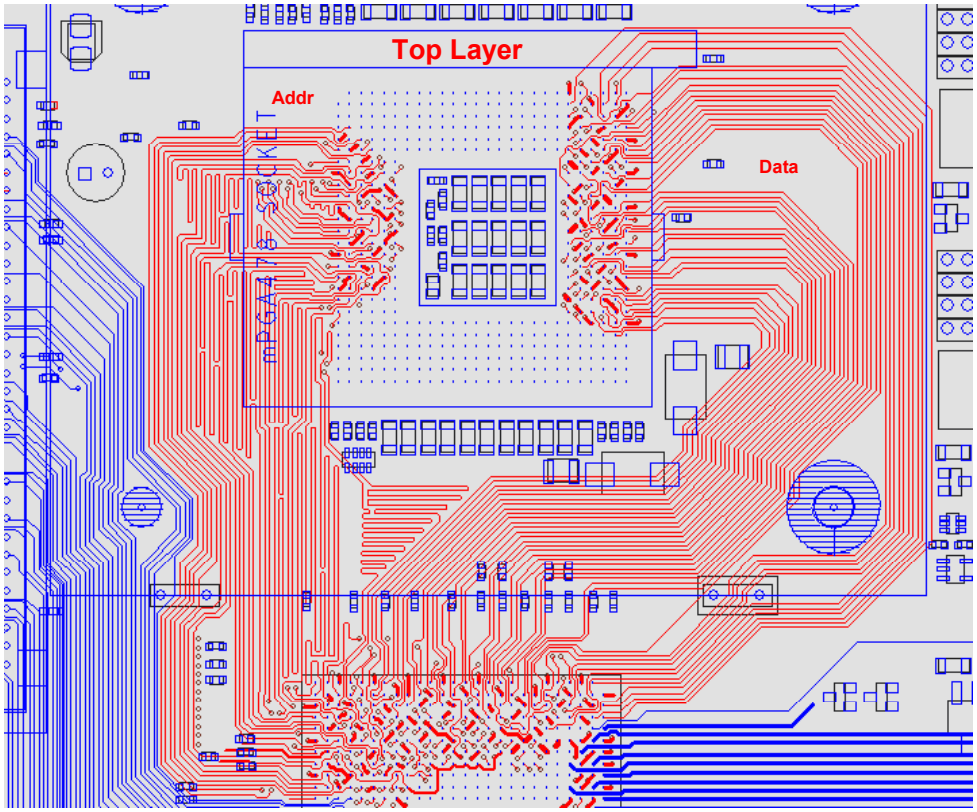
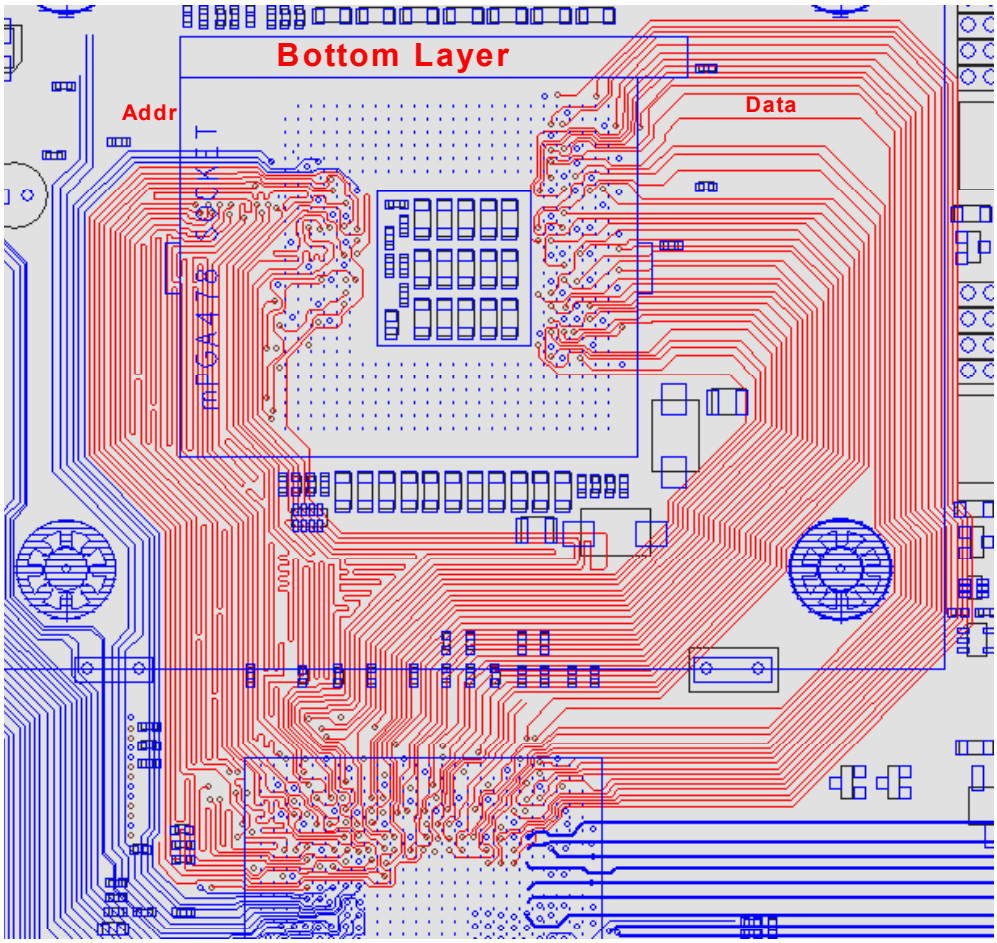


Figure 53, Customer Reference Platform System Bus Routing – Bottom Layer



Roughly half of the signals are routed on the bottom of the board referenced to GND, and the other half of the signals are routed on the top of the board referenced to V_{CCP}. The signals are routed from the MCH to both sides of the processor socket. No signals are routed through the center of the socket.

Careful attention must be paid when routing the system bus signal in order to maintain good power delivery for the processor. It is important that the V_{CCP} and GND flood is continuous from the OSCONs to the high frequency ceramic capacitors to help minimize the inductance of the power and ground planes.

5.6.1 Processor Power Delivery

Power must be distributed as a plane. This plane can be constructed as an *island* on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Processor power should never be distributed by traces alone. Intel recommends that a minimum of four planes be dedicated to power delivery in the power delivery area for Intel Pentium 4 processor system boards.

The voltage island from the source of power to the load should not have any breaks, so as to minimize inductance in the plane. Also, it should completely surround all of the pins of the power source and all of the pins in the power pin area of the Pentium 4 processor in the 478-pin package. For more information about processor power delivery, please reference the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Design Guide.*

Figure 54. Processor Power Delivery on Layer 2

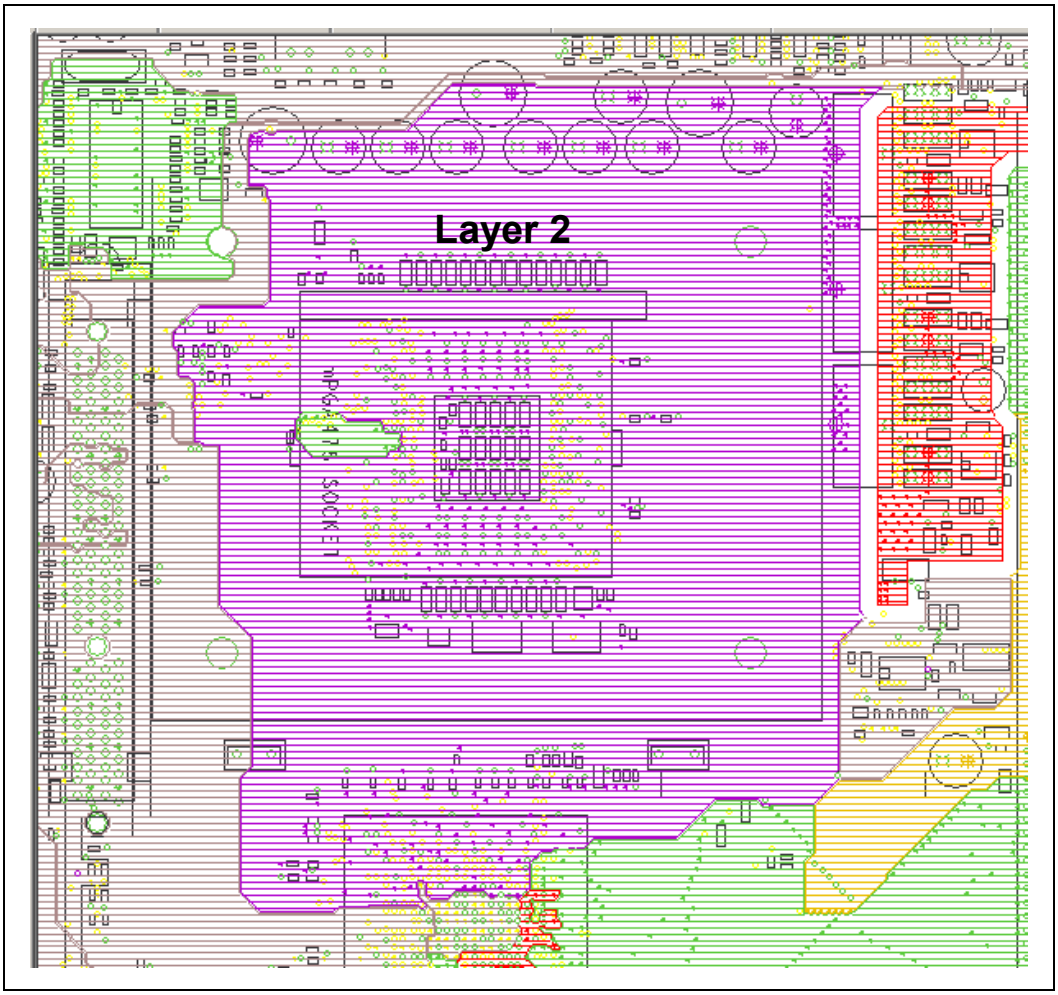
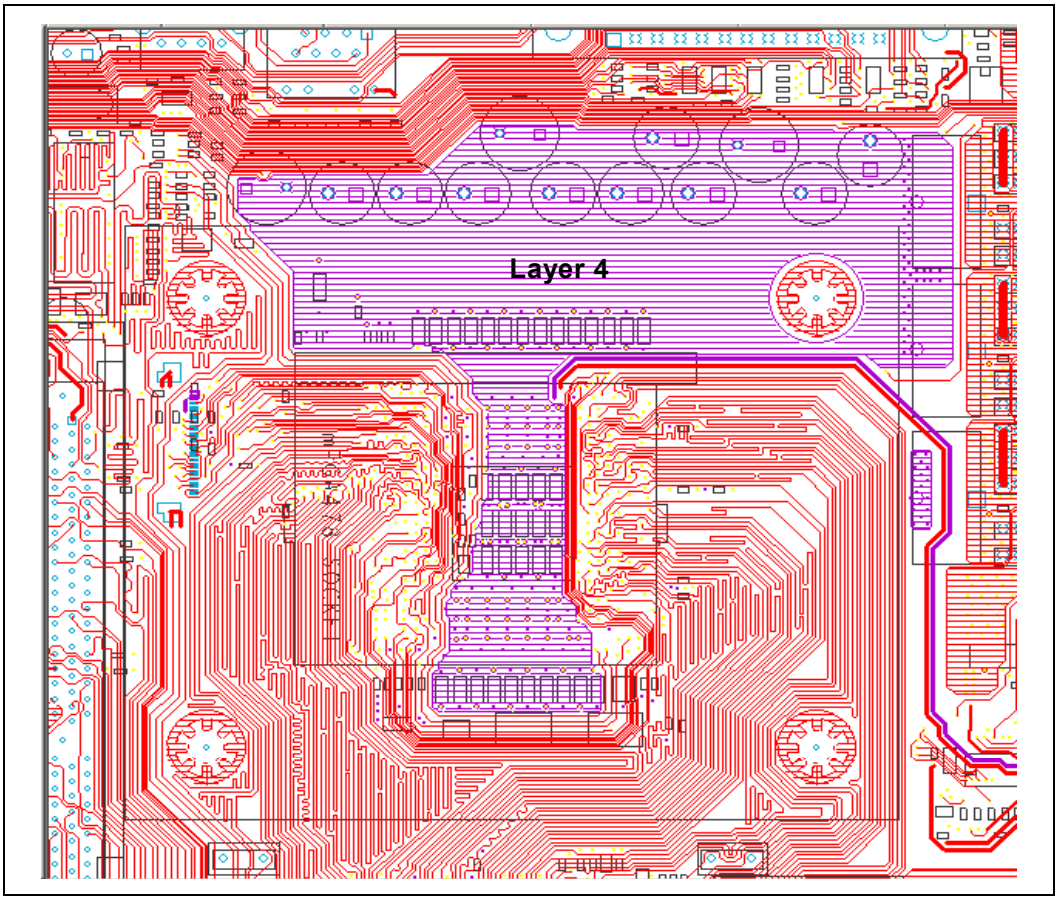


Figure 55. Processor Power Delivery on Layer 4



6 Memory Interface Routing

The Direct Rambus channel is a multi-symbol interconnect. Due to the length of the interconnect and frequency of operation, this bus is designed to allow multiple command and data packets to be present on a signal wire at any given instant. For example, the driving device can send the next data out before the previous data has left the bus.

The nature of the multi-symbol interconnect forces many requirements on the bus design and topology. First and foremost, a drastic reduction in reflected voltage levels is required. The interconnect transmission lines must be terminated at their characteristic impedance. Otherwise, the reflected voltage resulting from a mismatch in impedance will degrade signal quality. These reflections reduce noise margins, timing margins and the maximum operating frequency of the bus. Second, coupled noise can greatly affect the performance of high-speed interfaces. Just as in source synchronous designs, odd and even mode propagation velocity change can create skew between the clock lines, the data lines or command lines which reduces the maximum operating frequency of the bus. Efforts must be made to significantly decrease crosstalk, as well as the other sources of skew.

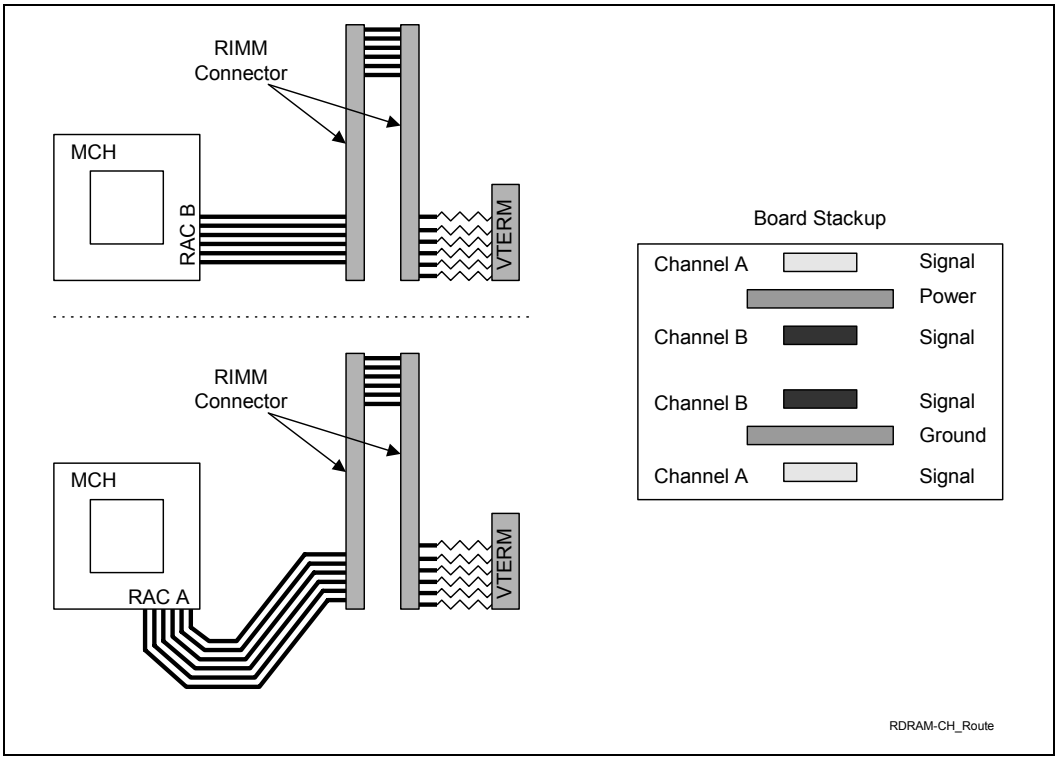
To achieve these bus requirements, all components, including the individual RDRAM devices, are incorporated into the design to create a uniform bus structure that can support up to 33 devices (including the MCH) running at 800 MegaTransfers/second (MT/s). The following sections will document the design guidelines to help ensure a robust Direct Rambus channel design.

Refer http://www.rambus.com/html/direct_docs.html for more information regarding RDRAM technology.

6.1 Rambus RDRAM* Device Routing Guidelines

The MCH has two Direct Rambus channels. The layout guidelines presented below are applicable for each channel. One channel should be routed entirely microstrip (outer layers) or stripline (inner layers). Figure 56 illustrates an example routing topology for the MCH.

Figure 56. Intel® MCH Direct Rambus Channel Routing Example



The signals on the Direct Rambus channel are broken into three groups: Rambus Signaling Level (RSL) signals, CMOS signals and clocking signals. The signal groups are documented in Table 21.

Table 21. Direct Rambus Channel Signal Groups

Group	Signal
RSL Signals	DQA[8:0]
	DQB[8:0]
	RQ[7:0]
CMOS Signals	CMD(1)
	SCK*(1)
	SIO
Clocking Signals	CTM
	CTM#
	CFM
	CFM#

NOTES:
1. These are high-speed CMOS signals

6.1.1 Rambus Signaling Level (RSL) Signals

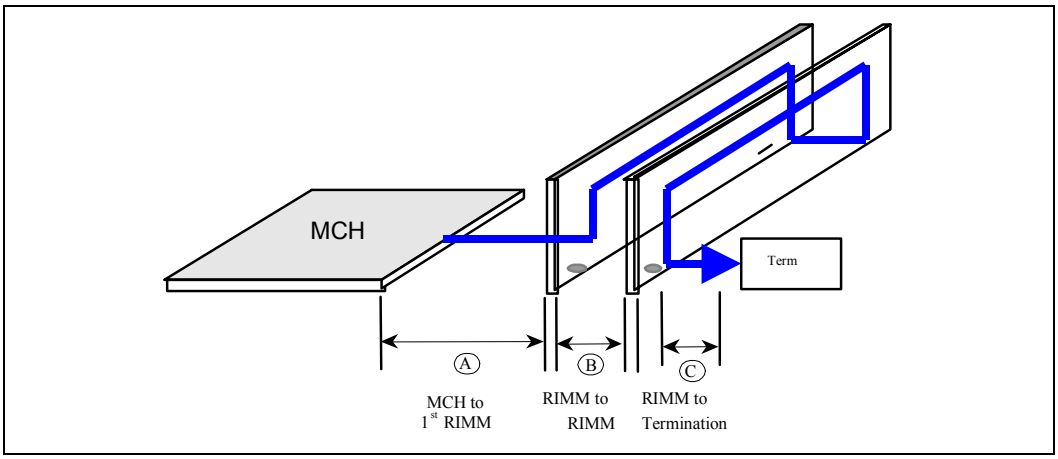
The Direct Rambus channel RSL signals are high-speed signals that transmit data between the MCH and RDRAM component at speeds up to 1066 MHz. These signals start at the MCH, enter the first RIMM connector, propagate through the RIMM module, and then exit on the opposite side. The RSL signals continue through the second RIMM connector until they are terminated at V_{term}. All unpopulated RIMM connectors must have continuity modules in place to ensure signals propagate to the termination at the end of the Direct Rambus channel.

Note: **For 850E / 533 MHz (PC1066) RDRAM technology platforms, if a continuity module (C-RIMM) is used, it must be installed in the #2 RIMM slot only – never in the #1 RIMM slot.**

The perfect matching of transmission line impedance and uniform trace length are essential for the Direct RDRAM device interface to work properly. Maintaining 28 Ω ± 10% loaded impedance for every RSL signal requires some changes to the standard trace width and board prepreg thickness. Typically, to achieve 28 Ω nominal impedance with 7 mil prepreg, it will require 28 mil wide traces. 28 mils wide traces are too wide to break out of the rows of RSL signals on the MCH. In order to reduce the trace width, a thinner pregreg is required. For example, a prepreg thickness of 4.0 to 4.5 mils allows 18 mil wide traces to meet the 28 Ω ± 10% nominal impedance requirement.

The following figure and table document the Direct Rambus channel topology for a 28 Ω channel.

Figure 57. Example Direct Rambus Channel Routing



NOTE: This diagram only illustrates the routing of one Direct Rambus channel. However, the example routing shown can be applied to both channels.

Table 22. Direct Rambus RSL Signal Lengths for Rambus RIMM* Connectors on Motherboard

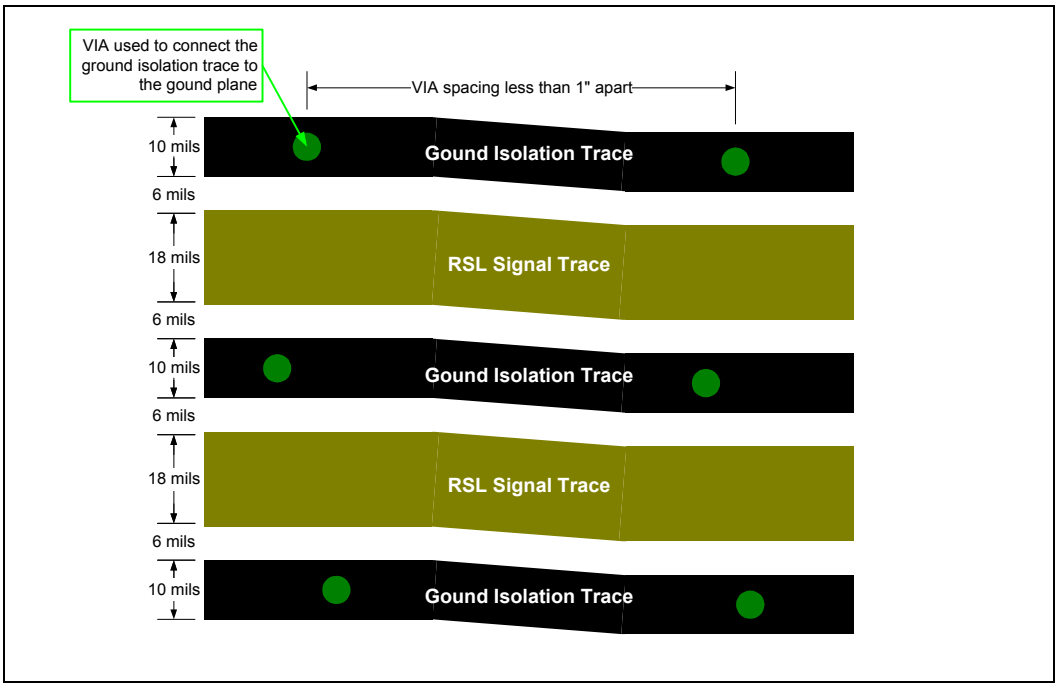
Reference Section	Trace Description	Trace Length 300/400 MHz RDRAM Technolgty	Trace Length 533 MHz RDRAM Technology (Microstrip)	Trace Length 533 MHz RDRAM Technology (Stripline)
A	MCH to first RIMM* connector for Channel A or first RIMM connector for Channel B	1 to 6 inches	1 to 4 inches	1 to 4 inches
B	RIMM connector to RIMM connector for the same channel.	0.4 to 1 inches	0.4 to 1 inches	0.4 to 1 inches
C	RIMM connector to Termination	0 to 2 inches(1)	0 to 2 inches(1)	0 to 2 inches(1)
D	A+B	7 inches max	4.4 inches max	4.4 inches max

NOTES:
1. Place termination resistors between RIMM connectors of the same channel to decrease trace length if possible.
2. For MCH to first RIMM connector measurement, use CFM/CFM# (CTM/CTM# use a different trace length calculation based on the formulas specified in Section 6.1.2.3)

To ensure a solid memory subsystem design, the RSL signals routing rules need to be followed. Below is a break down of the key areas to watch when design your platform.

- To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace between adjacent RSL signals (see Figure 58). The 10 mil ground isolation traces must be connected to ground with vias distributed less than every 1 inch. A via must be placed within less than 0.5 inches of the beginning and end of the ground isolation trace. A 6 mil gap is required between RSL signals and ground isolation trace.
- RSL signals must be length matched to ±10 mils in section "A" and ±2 mils in sections "B" using the trace length matching methods described in the next section. There is no trace length-matching requirement for traces in section 'C'. If signals are routed on inner and outer layers, the trace velocity differences need to be accounted for to minimize channel skew.
- RSL signals must have the same number of vias. It may be necessary to place additional vias (dummy vias) on certain RSL signals - even if vias are not needed - to meet the via loading (equal number of vias) requirement.

Figure 58. RSL Routing Diagram Showing Ground Isolation Traces with VIA Around RSL Signals



NOTE: For the Intel 850 chipset customer reference board (CRB), both inner and outer layer RSL trace width is 18 mils. Inner layer RSL trace width may vary depending on the board stack-up used. RSL signals should be no wider than 18 mils to prevent neck-down in the RIMM connector pin field.

6.1.2 Rambus* Signaling Level (RSL) Channel Compensation

The RSL and clocking signals require special compensation for any discontinuities introduced in the channel. Since the Direct Rambus channel only allows for 125ps of interconnect skew, it is critical to minimize skew and to match the skew on RSL and clocking signals within a given channel. The next few sections will show how to compensate for skew due to package trace differences, vias, differential clock routing and connector.

When compensating a channel, the compensating techniques must be performed in the following layout order:

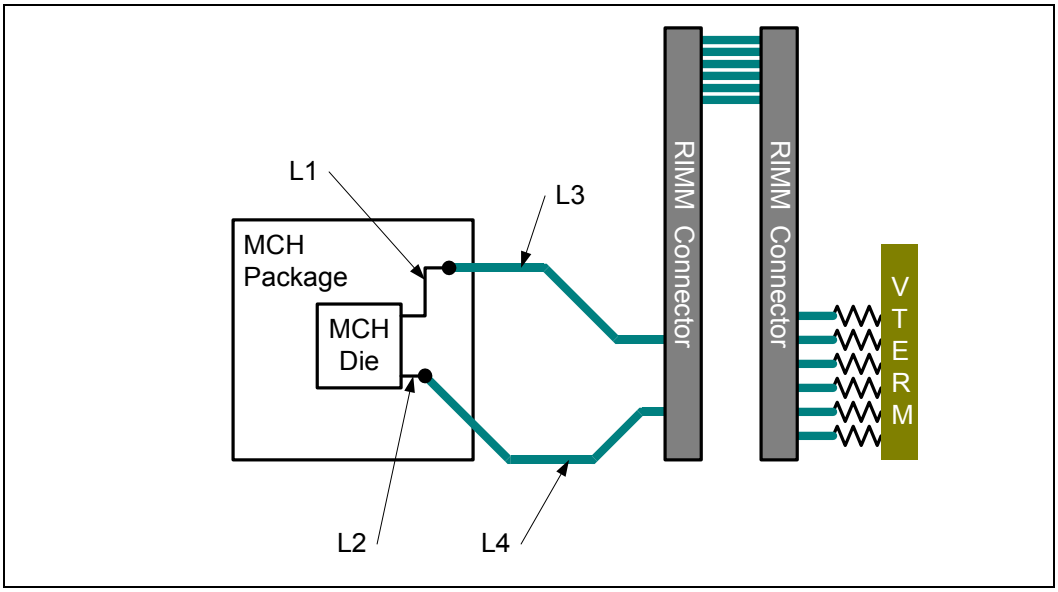
1. Package trace compensation
2. Via compensation
3. Differential clock compensation
4. Alternating signal layer for RIMM connector pin compensation
5. RIMM connector impedance compensation

6.1.2.1 Package Trace Compensation (RSL and Clocking Signals)

All RSL and clocking signals require pad-to-pin length matching between the MCH to the first RIMM connector to minimize skew. All RSL and clocking signals for a given channel required pad-to-pin trace matching within ±10 mils.

The RIMM connector to RIMM connector trace length match requirement is ±2 mils.

Figure 59. Direct Rambus Channel Trace Length Matching Example



NOTE: This diagram only illustrates the routing of one Direct Rambus channel. However, the example routing shown can be applied to both channels.

Listed below are a few definitions.

- **Package Dimension (ΔL_{PKG}):** a representation of the length from the pad to the ball.
- **Board Trace Length (L_{MB}):** the trace length on the board.
- **Nominal Length:** the length to which all signals are matched.

As Figure 59 shows, L1 plus L3 must be length matched to L2 plus L4 within ±10 mils.

Equation 2. Compensated Trace Length Calculation

$$\Delta L_{PCB} = (\Delta L_{PKG} * \text{Package}_{\text{TRACE VELOCITY}}) / \text{PCB}_{\text{TRACE VELOCITY}}$$

The PCB trace length for each signal is a calculated value, and may vary with designs. The nominal MCH package trace velocity is 167.64 ps/in. The $\text{PCB}_{\text{TRACE VELOCITY}}$ is board and layer dependent. $\text{PCB}_{\text{TRACE VELOCITY}}$ can change depending on which layer the board designer plans to route the RSL channel. Below is the $\text{PCB}_{\text{TRACE VELOCITY}}$ for stripline and microstrip routing used on the Intel 850 chipset customer reference board (CRB).

- Stripline velocity typically equals 172 ps/in
- Microstrip velocity typically equals 154 ps/in

The MCH package trace length information is contained in the *Intel® 850 Chipset: 82850 Memory Controller Hub (MCH) Datasheet*. The package trace length information presented in this document is normalized to the longest package trace length. The RSL and clocking signal lengths (ΔL_{PKG}) can be renormalized to any signal using Equation 3.

Equation 3. Normalized Trace Length Calculation

$$\text{New } \Delta L_{PKG} = \Delta L_{PKG} - \Delta L_{\text{NORMALIZED RSL}}$$

It is not necessary to account for CMOS signals package compensation. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be kept as minimum as possible.

6.1.2.2 Via Compensation

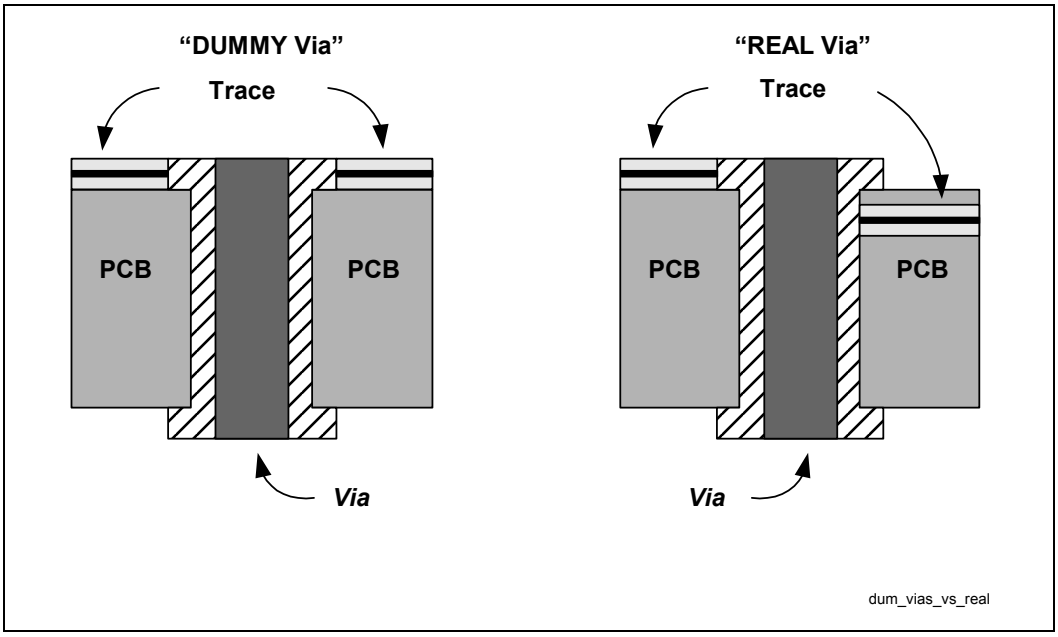
All RSL and clocking signals must have the same number of vias. As a result, each trace will have at least one via because some of the RSL signals must be routed on other layers of the motherboard. The via should be placed as close as possible to the MCH package ball. For the channel routed on outer layers (microstrip), it will be necessary to place “dummy” via on all signals routed on the top layer. The electrical characteristics between “dummy” and “real” vias are not exact, so additional compensation is needed on each signal that has “dummy” vias.

“Dummy” vias are not required on the channel routed on the inner layers (stripline) because all signals will require a “real” via.

Each signal with a dummy via must have 25 mils of additional trace length . The additional 25 mils trace length must be added to the signal routed on the top layer, after length matching.

“Real” via = “Dummy” via + 25 mils of trace length

Figure 60. "Dummy" vs. "Real" Vias



6.1.2.3 Differential Clock Compensation

If the RDRAM device clocks (CTM, CTM#, CFM and CFM#) are routed differential, the clock signals must be longer than the RSL signals due to their increased trace velocity because they are routed as a differential pair. To calculate the length for each clock, use Equation 4 for microstrip and Equation 5 for stripline routing.

Equation 4. Clock Trace Length Calculation for Microstrip

300/400 MHz RDRAM technology:

CFM/CFM# Clock Length = Nominal RSL Signal Length (package + board)* 1.030[(1)]

CTM/CTM# Clock Length = Nominal RSL Signal Length (package + board)* 1.030[(1)]

533 MHz RDRAM technology:

CFM/CFM# Clock Length = Nominal RSL Signal Length (package + board)* 1.030[(1)]

CTM/CTM# Clock Length = Nominal RSL Signal Length (package + board)* 1.030 + 45 pS[(1)]

Note: This compensation factor is based on the Intel 850 chipset customer reference board (CRB) stack-up.

The lengthening of the clock signals, to compensate for their trace velocity change, only applies to routing between the MCH and first RIMM connector. The clock signals should be matched in length to the RSL signals between RIMM connectors.

Equation 5. Clock Trace Length Calculation for Stripline

300/400 MHz RDRAM technology:

CFM/CFM# Clock Length = Nominal RSL Signal Length (package + board)* 1.009[(1)]

CTM/CTM# Clock Length = Nominal RSL Signal Length (package + board)* 1.009[(1)]

533 MHz RDRAM technology:

CFM/CFM# Clock Length = Nominal RSL Signal Length (package + board)* 1.009[(1)]

CTM/CTM# Clock Length = Nominal RSL Signal Length (package + board)* 1.009 + 45 pS[(1)]

Note: This compensation factor is based on the Intel 850 chipset customer reference board (CRB) stack-up.

The lengthening of the clock signals, to compensate for their trace velocity change, only applies to routing between the MCH and first RIMM connector. The clock signals should be matched in length to the RSL signals between RIMM connectors.

6.1.2.3.1 Non-Differentially Routed Clocks – 533 MHz Rambus RDRAM* Technology

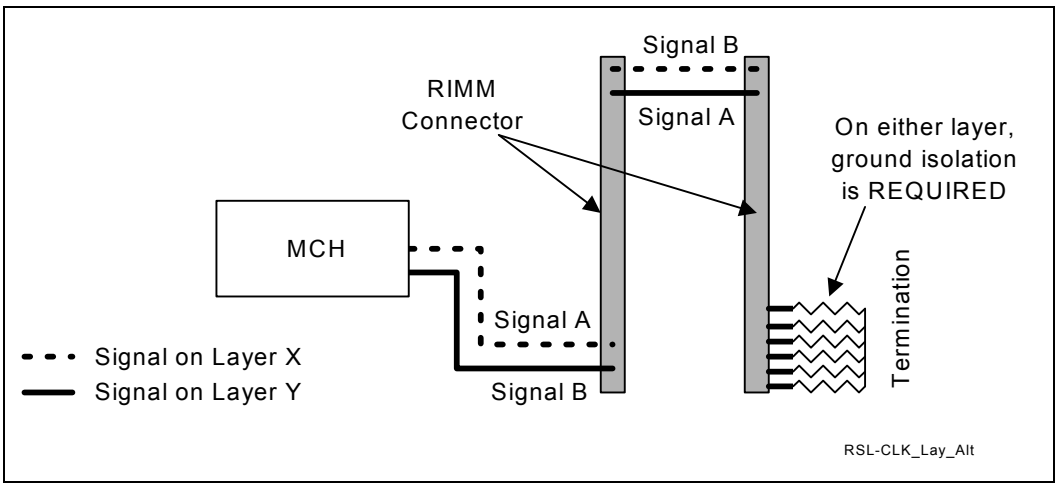
For 533 MHz (PC1066) RDRAM technology, if the clock signals CTM/CTM# and CFM/CFM# are not routed differentially, then an additional 10pS per inch should be added to CTM/CTM# - MCH to first RIMM connector guideline only.

6.1.2.4 Signal Layer Alternation for Rambus RIMM Connector Pin Compensation

RSL and clocking signals must alternate layers as they are routed through the channel to compensate for signals on bottom layer having to travel a longer distance through the pin connector. This is illustrated in Figure 61. For example if a signal is routed on the top layer from the MCH to the first RIMM connector, it must be routed on the bottom layer from the first RIMM connector to the second RIMM connector. This rule also holds true for inner layer routing. If a signal is routed on the top inner layer from the MCH to the first RIMM connector, it must be routed on the bottom inner layer from the first RIMM connector to the second RIMM connector.

All RSL and clocking signals from the second RIMM connector to the termination resistor should be routed on the top layer.

Figure 61. RSL and Clocking Signal Layer Alteration



6.1.2.5 Rambus RIMM Connector Impedance Compensation

The RIMM connector inductance has been shown to cause an impedance discontinuity on the Direct Rambus channel. This can reduce voltage and timing margin. In order to compensate for the inductance of the connector, a compensating capacitance is required on each RSL and clocking connector pin. This compensating capacitance must be added to the following connector pins at each connector

- LCTM
- LCTM#
- RCTM
- RCTM#
- CMD
- LCFM
- LCFM#
- RCFM
- RCFM#
- SCK
- LROW[2:0]
- RROW[2:0]
- LCOL[4:0]
- RCOL[4:0]
- RDQA[8:0]
- LDQA[8:0]
- RDQB[8:0]
- LDQB[8:0]

The amount of capacitance needed depend on the length the signals have to travel though the RIMM connector pin (i.e., a signal on the bottom layer has to travel though more of the RIMM connector pin than a signal on the top layer). This can be achieved on the motherboard by adding a copper tab to the specified RSL pins at each connector.

Table 23. RSL and Clocking Signal Rambus RIMM* Connector Capacitance Requirement

RSL and Clocking Signal Routing Layer	Capacitance (pF) [1]
Top	0.8
Inner 1	0.9
Inner 2	1.23
Bottom	1.35

NOTE: [1]These numbers are based on a six layer stack-up.

The copper tab area for the recommended stack-up was determined through simulation. The amount of capacitance required is determined by the layer the RSL or clocking signal is routed on. The placement of the copper tabs can be on any signal layer, independent of the layer on which the RSL signal is routed.

Capacitance for a different stack-up assuming a 62mil board thickness can be computed by linear interpolation. The equation for determining the amount of capacitance needed on any stripline layer can be found by Equation 6.

Equation 6. Calculation for a Stripline C-tab

$$Ctab_{LayerX} = .8pF + (1.35pF - .8pF)(X/62)$$

Where

- X is the distance in mils from the top of the board to the stripline signal layer in which the RSL or clocking signals are routed on.

Equation 7 is an approximation that can be used for calculating copper tab area on the outer layer.

Equation 7. Copper Tab Capacitance Calculation

$$\text{Length} * \text{Width} = \text{Area} = [C_{plate} * \text{Thickness of prepreg}] / [\varepsilon_0 * \varepsilon_r * 1.1]$$

Where:

- C_{plate} = Capacitance of the plates
- $\varepsilon_0 = 2.25 \times 10^{-16}$ Farads/mil
- ε_r = Relative dielectric constant of prepreg material
- Thickness of prepreg = Stack-up dependent
- Length, Width = Dimensions in mils of copper plate to be added
- Factor of 1.1 accounts for fringe capacitance.

The following is an example calculation for a board where ε_r is 4.2 and thickness of prepreg is 4.5. Note these numbers will vary with differences in prepreg thickness.

Table 24. Copper Tab Area Calculation

Layer	Dielectric Thickness	Separation Between Signal Traces & Copper Tab	Minimum Ground Flood	Air Gap Between Signal & GND Flood	Compensating Capacitance in Cplate (pF)[1]	CTAB Area in sq mils
Top	4.5	6	10	6	0.8	~3460
Inner 1	4.5	6	10	6	0.9	~3900
Inner 2	4.5	6	10	6	1.23	~5300
Bottom	4.5	6	10	6	1.35	~5800

NOTE: [1]These numbers are based on a six layer stack-up.

Note that more than one copper tab shape may be used as shown in the following figures. The dimensions are based on copper area over the ground plane. The actual length and width of the tabs may be different due to routing constraints (e.g., if tab must extend to center of hole or anti-pad). The following figures show a routing example of tab compensation capacitors. Note, the capacitor tabs must not interrupt ground floods around the RIMM connector pins, and they must be connected to avoid discontinuity in the ground plane as shown.

Figure 62. Top Layer CTAB with RSL Signal Routed on the Same Layer (Ceff = 0.8 pF)

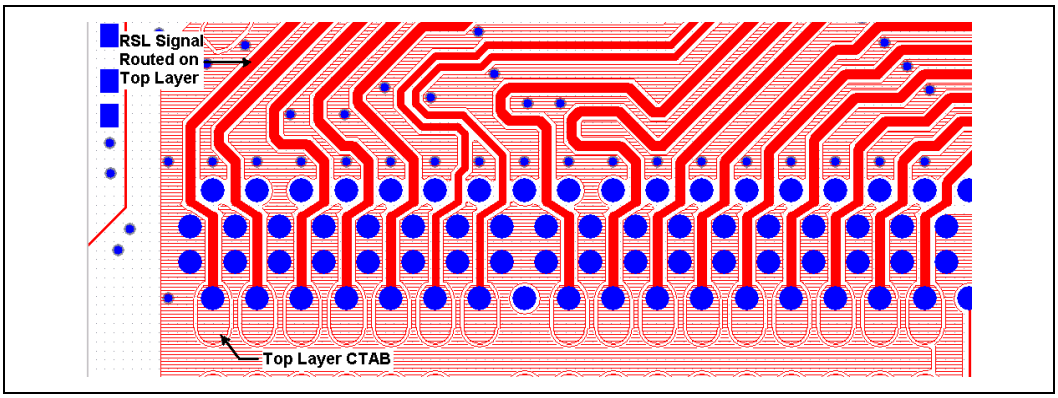
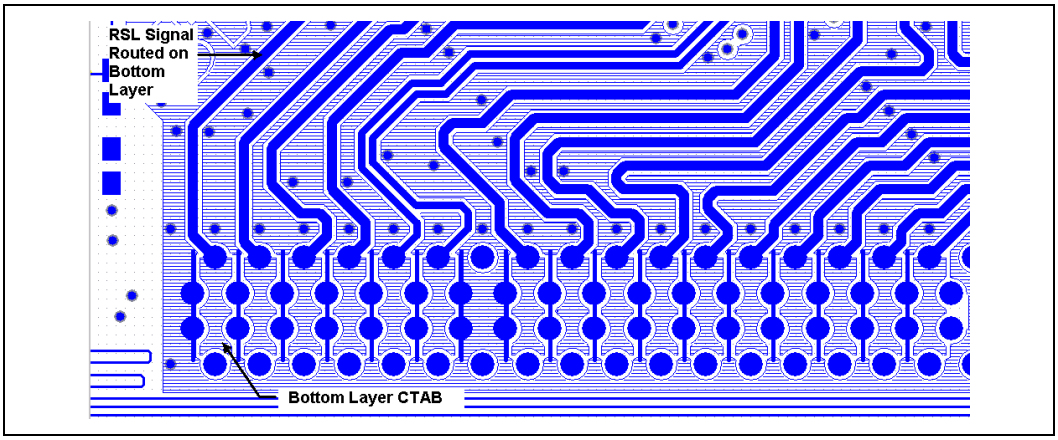
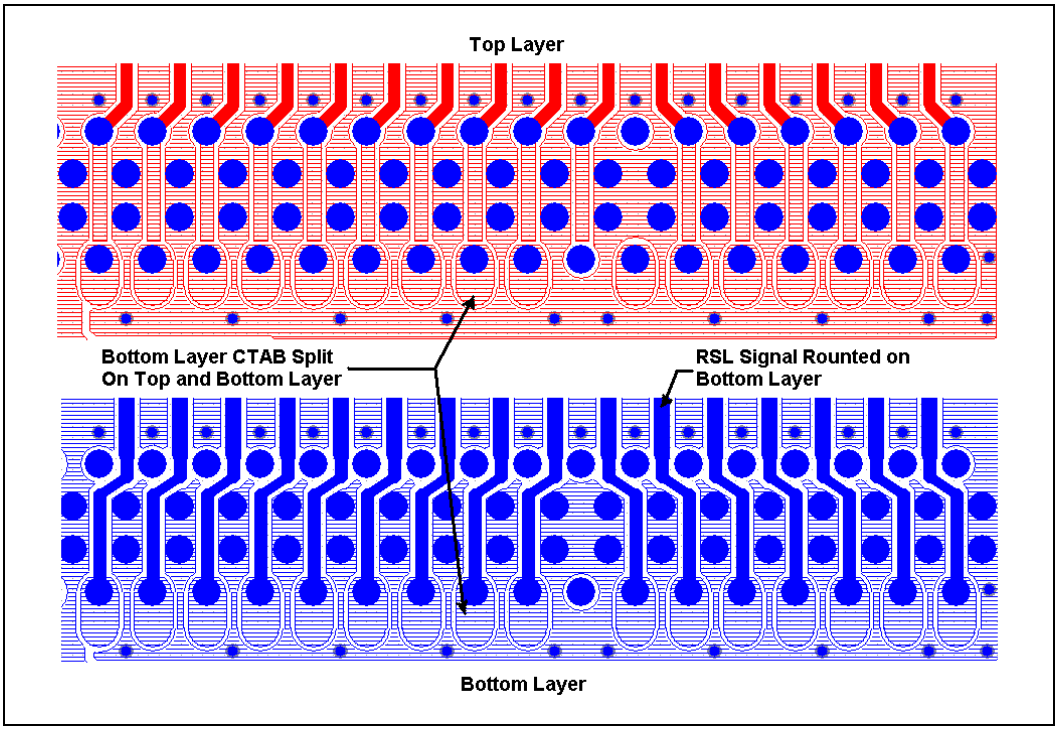


Figure 63. Bottom Layer CTAB with RSL Signal Routed on the Same Layer (Ceff = 1.35 pF)



The CTAB can be implemented on the multiple layers to minimize routing and space constrains. Figure 64 issues the use of CTABs on the top and bottom layer for bottom layer RSL and clocking signals routed between RIMM connectors.

Figure 64. Bottom Layer CTABs Split Across the Top and Bottom Layer to Achieve an Effect Ceff ~1.35 pF



6.1.3 RSL Signal Termination

All RSL signals must be terminated to 1.8 V (Vterm) using 27 Ω 1% or 28 Ω 2% resistors (300/400 MHz RDRAM technology) or 27 Ω 1% (533 MHz RDRAM technology) at the end of the channel opposite the MCH. Resistor packs are acceptable, however discrete resistors are recommended for increased margin. The RSL and clocking signals from the last RIMM connector to termination should be routed on the top layer. Vterm must be decoupled using high-speed bypass capacitors (one 0.1 µF ceramic chip capacitor per two RSL lines) near the terminating resistors. For margin improvement, the number of bypass capacitors can be increased to two 0.1µF ceramic chip capacitors per two RSL lines. Additionally, bulk capacitance is required. Assuming a linear regulator with approximate 20 µs response time, two 100 µF tantalum capacitors are recommended. The trace length between the last RIMM connector and the termination resistors should be less than 2 inches. Length matching in this section of the channel is not required. The Vterm power island should be AT LEAST 50 mils wide. This voltage is not required during Suspend-to-RAM (STR).

Figure 65. Direct Rambus RDRAM* Device Termination (Discrete Resistors Are Recommended)

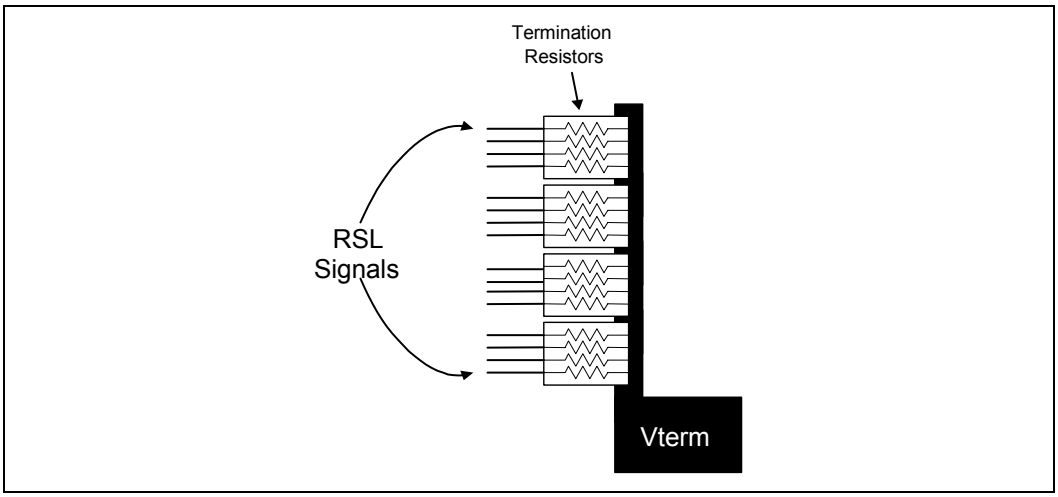
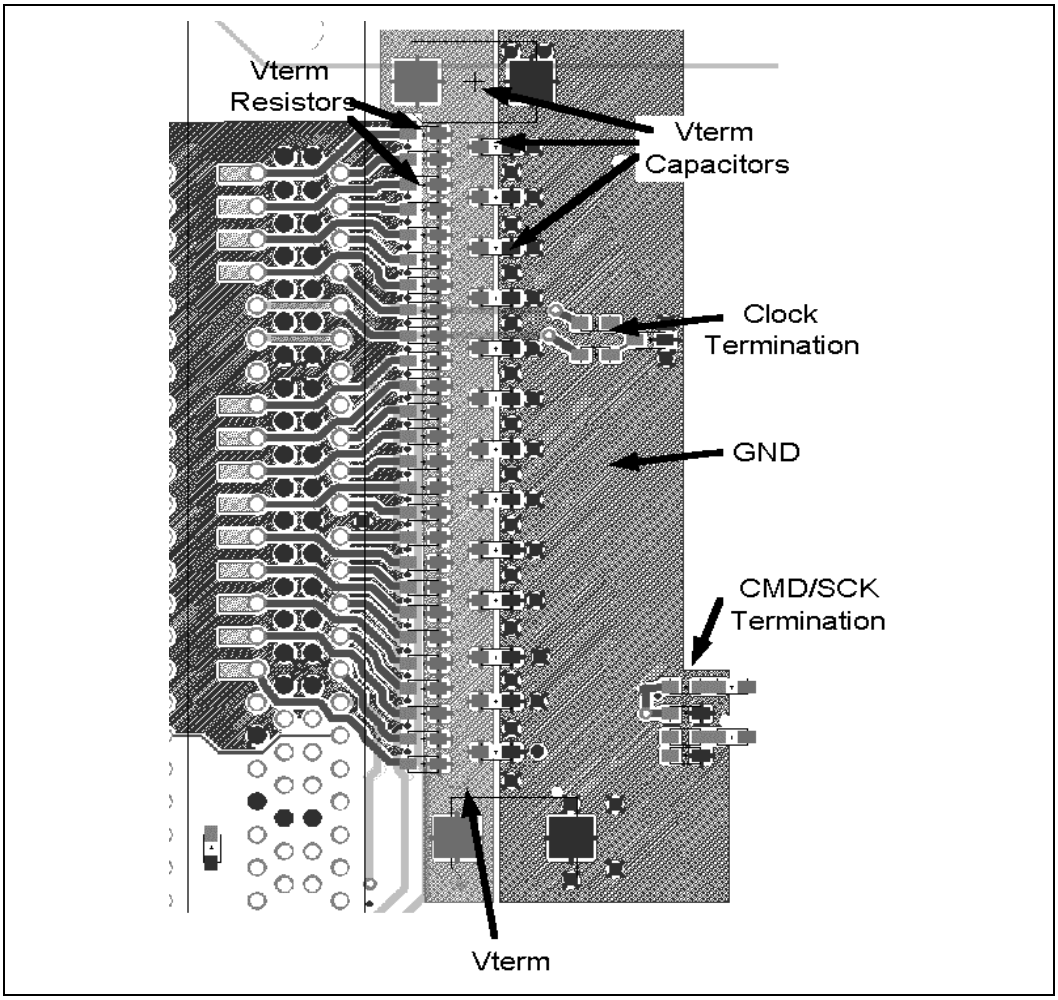


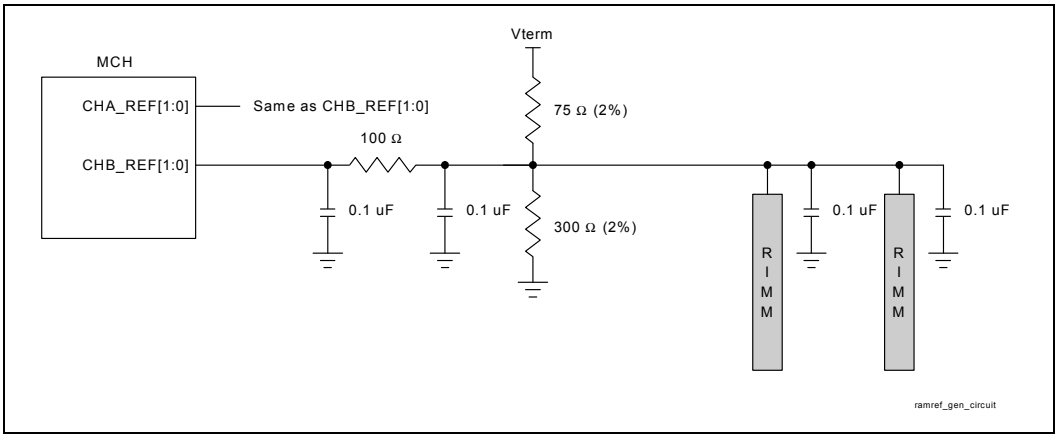
Figure 66. Direct Rambus RDRAM* Device Termination Example



6.1.4 Rambus RDRAM* Device Reference Voltage

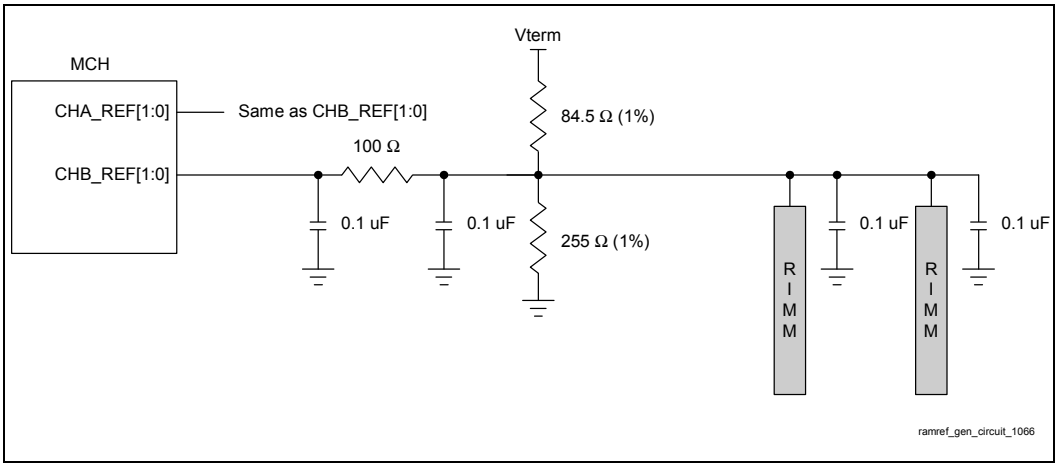
The RDRAM device reference voltage (RAMREF) must be generated as shown in Figure 67 for 300/400 MHz RDRAM technology designs and Figure 68 for 533 MHz RDRAM technology designs. RAMREF should be generated from a typical resistor divider using 2% tolerant resistors. Additionally, RAMREF must be decoupled locally at each RIMM connector, at the resistor divider network, and at the MCH. Finally, a 100 Ω series resistor is required near the MCH. The RAMREF signal should be routed with 10 mils wide traces.

Figure 67. RAMREF Generation Example Circuit for 300/400 MHz Rambus RDRAM* Technology



NOTE: The RAMREF Generation Circuit is not shown for Channel A in Figure 67, but is the same as the one shown for Channel B.

Figure 68. RAMREF Generation Example Circuit for 533 MHz Rambus RDRAM* Technology

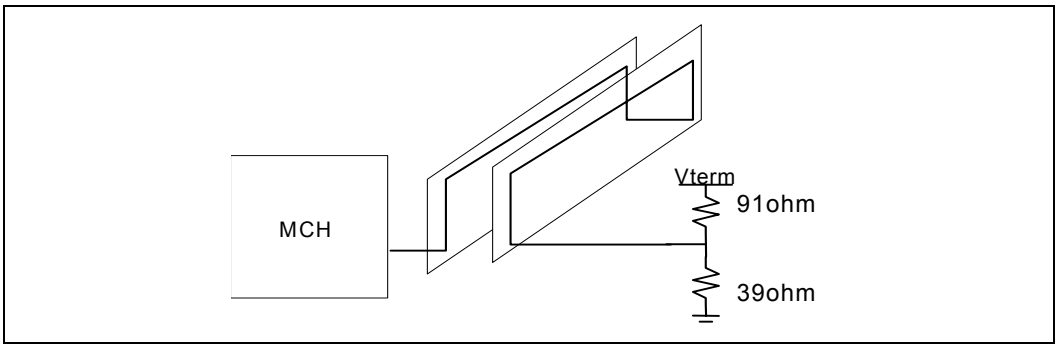


NOTE: The RAMREF Generation Circuit is not shown for Channel A in Figure 68, but is the same as the one shown for Channel B.

6.1.5 High-Speed CMOS Routing

Due to the synchronous requirements between RSL signals and high-speed CMOS signals, the CMOS signals should be routed as part of the RSL channel. They must be impedance matched and properly terminated (using a different termination scheme than the RSL signals). It is not necessary to perform the length match calculation for high-speed CMOS signals. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be kept as minimal as possible.

Figure 69. High-Speed CMOS RC Termination



A CMOS voltage must be supplied to each RIMM connector. This CMOS voltage is used by the RDRAM device CMOS interface. This voltage (Vcmos) must be 1.8 V, and the maximum load is 3 mA. Additionally, this voltage must be supplied during *Suspend to RAM*. Therefore, Vterm and Vcmos cannot be generated from the same source. Due to the low power requirements of Vcmos, it can be generated by a 36 / 100 Ω resistor divider from 2.5 V.

The high-speed CMOS signals require AC termination as shown Figure 69 with a 91 Ω pull-up and 39 Ω pull-down resistors.

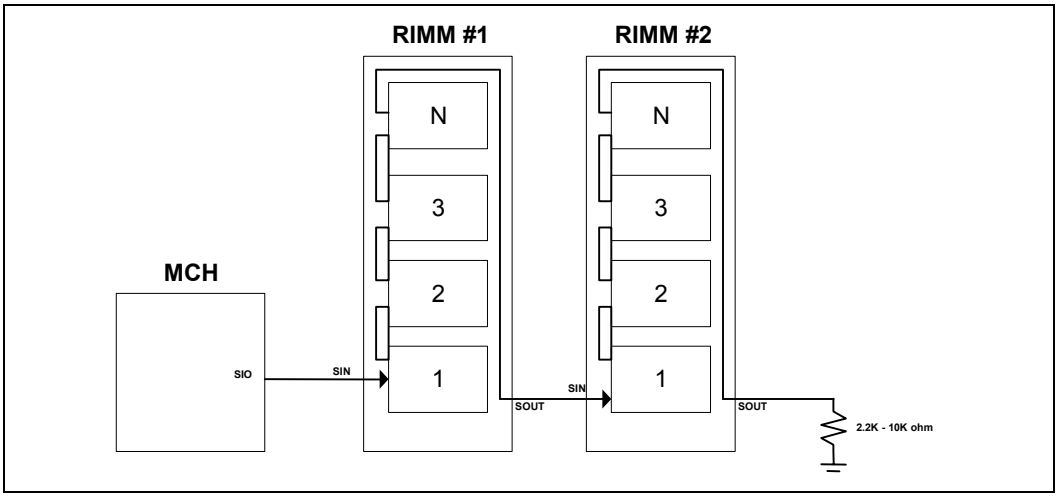
6.1.6 SIO Routing

The SIO signal is a bi-directional signal that operates at 1 MHz. This signal must be routed from MCH to RIMM connector to RIMM connectors as documented below and shown in Figure 70.

- MCH SIO ball to the first RIMM connector's SIN pin (RIMM #1 – Pin B36)
- First RIMM connector's SOUT pin (RIMM connector #1 – Pin A36) to the second RIMM connector's SIN pin (RIMM connector #2 – Pin B36)
- Second RIMM connector's SOUT pin (RIMM connector #1 – Pin A36) to terminating resistor that is tied to GND

The SIO signal enters the first RIMM connector, propagates through all the devices (this signal is buffered by each device) on the RIMM module and then exits the RIMM connector. A 2.2 kΩ–10 kΩ terminating resistor is required on the last RIMM connector's SOUT pin. This resistor needs to be tied to GND. The SIO is routed with a 5 mil wide, 60 Ω trace.

Figure 70. SIO Routing



6.1.7 Suspend-to-RAM Shunt Transistor

When the system enters or exits Suspend-to-RAM, power will be ramping to the MCH (i.e., it will be powering-up or powering-down). When power is ramping, the state of the MCH outputs is not guaranteed. Therefore, the MCH may drive the CMOS signals and issue CMOS commands. The only command RDRAM device would respond to is the power-down exit command. To avoid the MCH inadvertently taking the RDRAM devices out of power-down due to the CMOS interface being driven during power ramp, the SCK (CMOS clock) signal should be shunted to ground when the MCH is entering and exiting Suspend-to-RAM. This shunting can be accomplished using the NPN transistor having a sinking capability of 300 mA @ 400 mV. The transistor should also have a Cobo of 15 pF or less with a signal switching range of 0.1–1.5 V. Lastly, shunting transistors must not be having their bases tied directly together. See Figure 71. for the SCK/CMD circuitry.

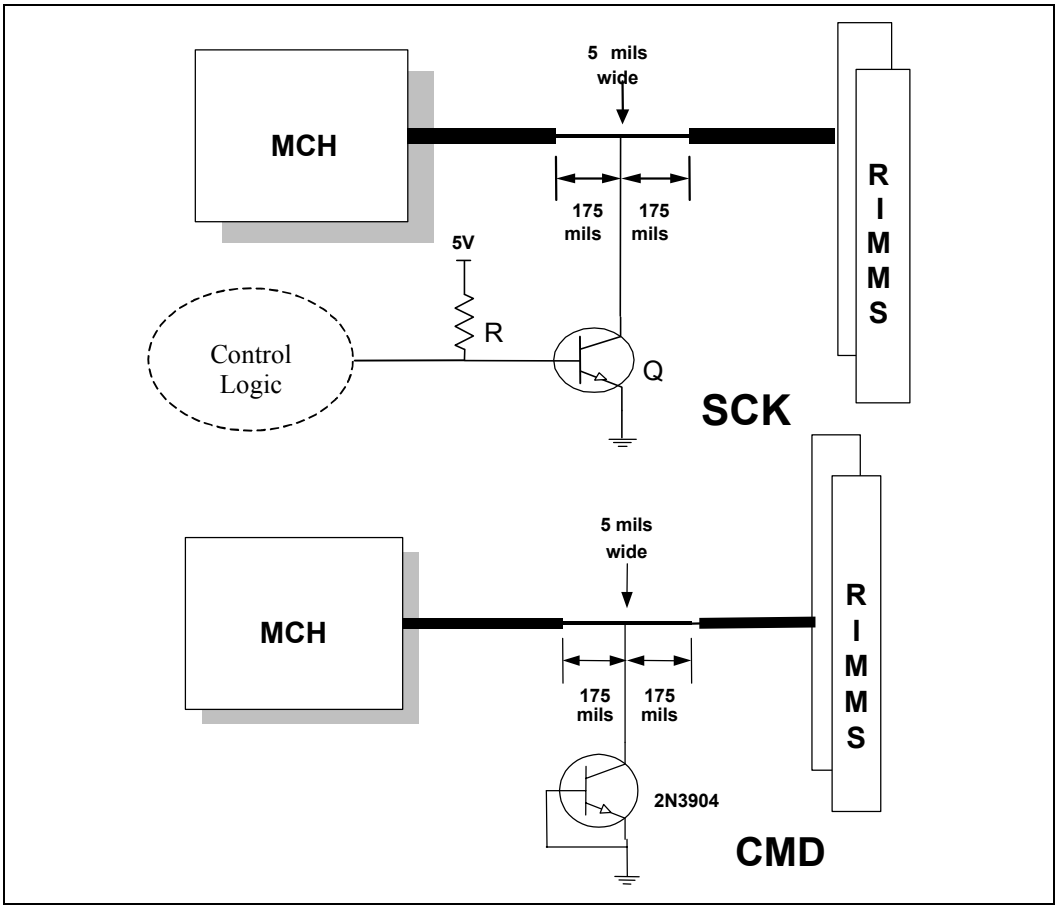
The following table lists sample transistors that can be used.

Single Package (Q)	Series Resistor (R)
MMBT2222LT1D	1 kΩ
MMBT100A	300 Ω
Dual Package	
MMDT2222A	1 kΩ

NOTE: The use of these transistors alone does not guarantee the above conditions will be met. Each design must ensure that the transistor can sink the appropriate amount of current by properly driving the base. Resistances should include source impedance driver.

To match the electrical characteristics on the SCK signal, the CMD signal needs a dummy transistor. This transistor's base should be tied to ground (i.e., always turned off). To minimize impedance discontinuities, the traces for CMD and SCK must have a neck down from 18 mil traces to 5 mil traces for 175 mils on either side of the SCK/CMD attach point as shown in Figure 71.

Figure 71. Rambus RDRAM* Device CMOS Shunt Transistor



This implementation is applicable for RIMM connectors down solution only and is not needed on the repeater channels. Also, this implementation is not necessary if Suspend-to-RAM is not supported within the system

6.1.8 Rambus RDRAM* Device Channel Margin Improvement

For Intel 850E / 533 MHz (PC1066) RDRAM device designs which exhibit less than optimum Rambus channel margins, margin improvement may be achieved by:

- Increasing the number of bypass capacitors from one 0.1µF ceramic chips capacitors per two RSL lines to two 0.1µF ceramic chip capacitors per two RSL lines. See Section 6.1.3.
- Insuring that the RIMM module with the most number of RDRAM devices is placed in the #1 RIMM connector.

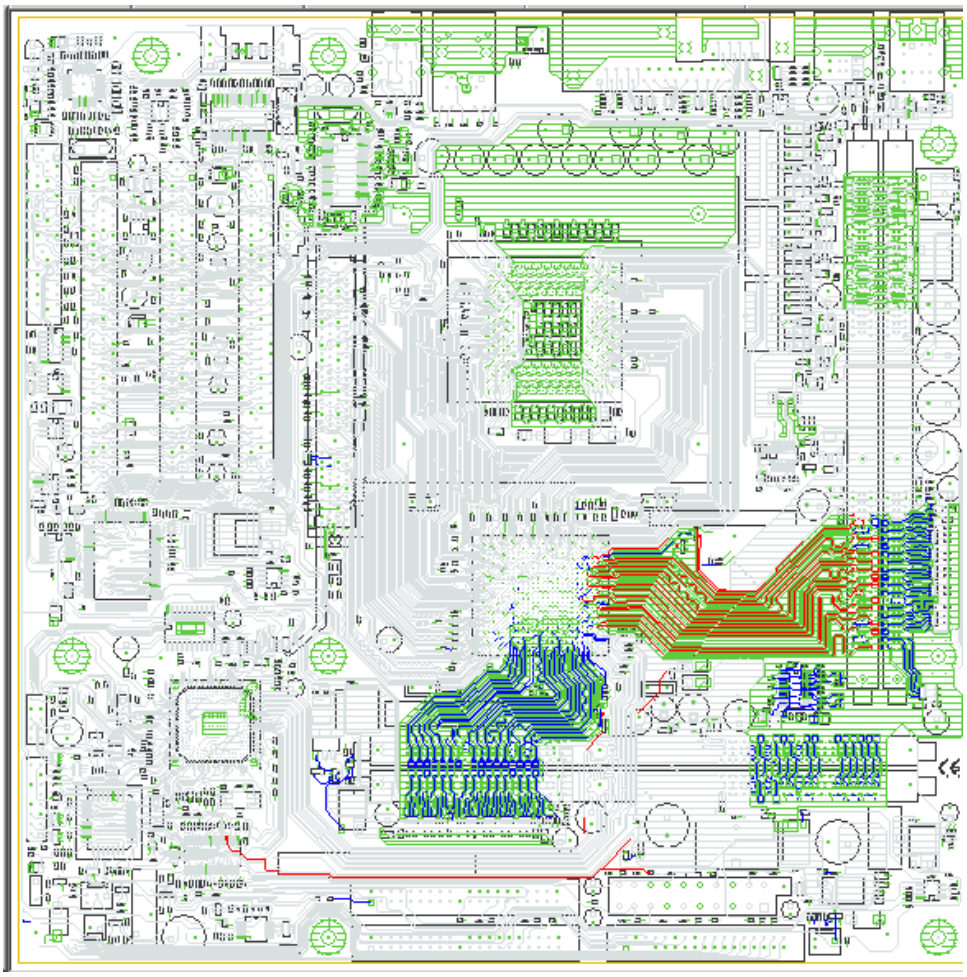
6.1.9 533 MHz (PC1066) Rambus RIMM Module Thermal Consideration

533 MHz (PC1066) RIMM modules will generate more heat than 400 MHz (PC800) RIMM modules. System designers should insure proper airflow to prevent overheating of memory or other components in the system environment when using PC1066 RIMM modules.

6.2 Rambus Technology Routing Guidelines - Four-Layer Motherboard

To enable a 4-layer design, the RIMM connectors on channel A are placed horizontal and form a 90 degree angle to the RIMM connectors on channel B. See figure below for placement information.

Figure 72. Rambus RIMM Connector Placement



The breakout of the RSL signals is also critical because it will impact the 1.8V MCH power delivery. RSL signals around the hub interface need to be routed on the top layer to maximize the 1.8V core and RAC power delivery. Follow the MCH Rambus technology breakout shown in the following figures.

Figure 73. Rambus Technology Intel® MCH Breakout (Top Layer)

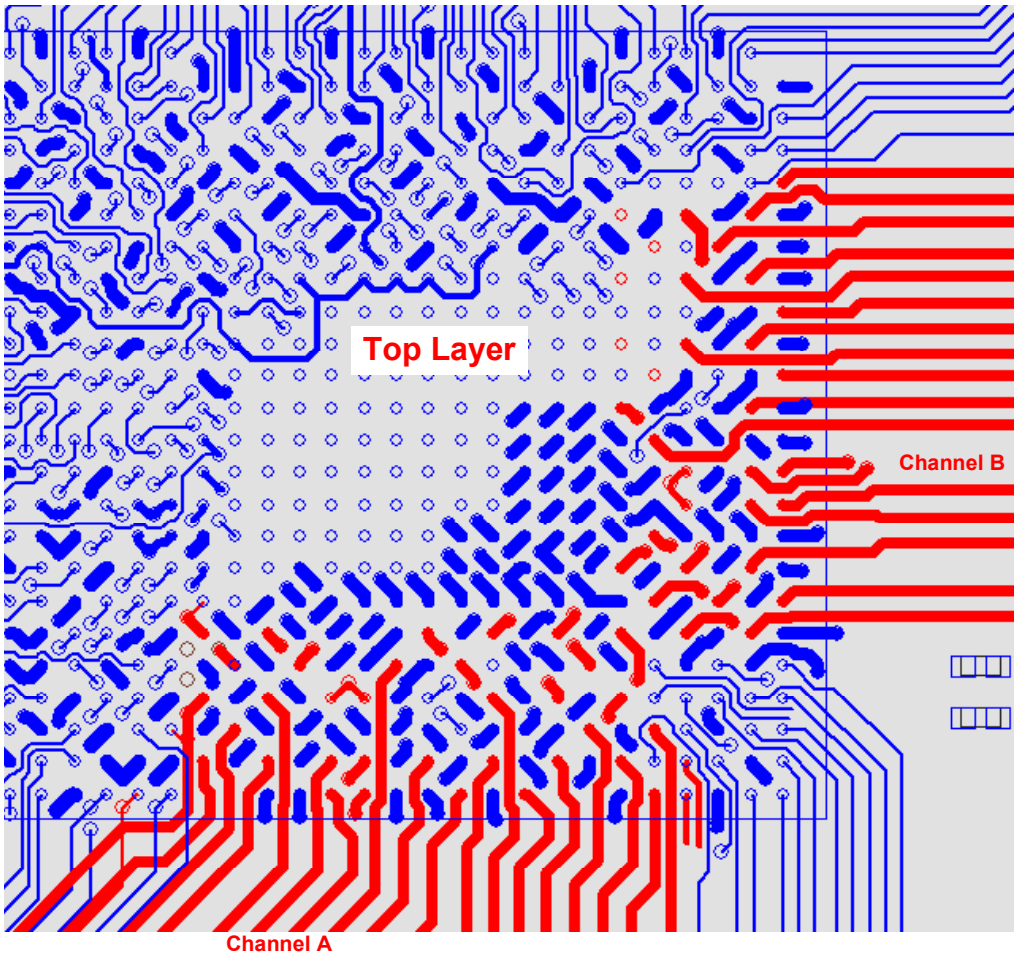
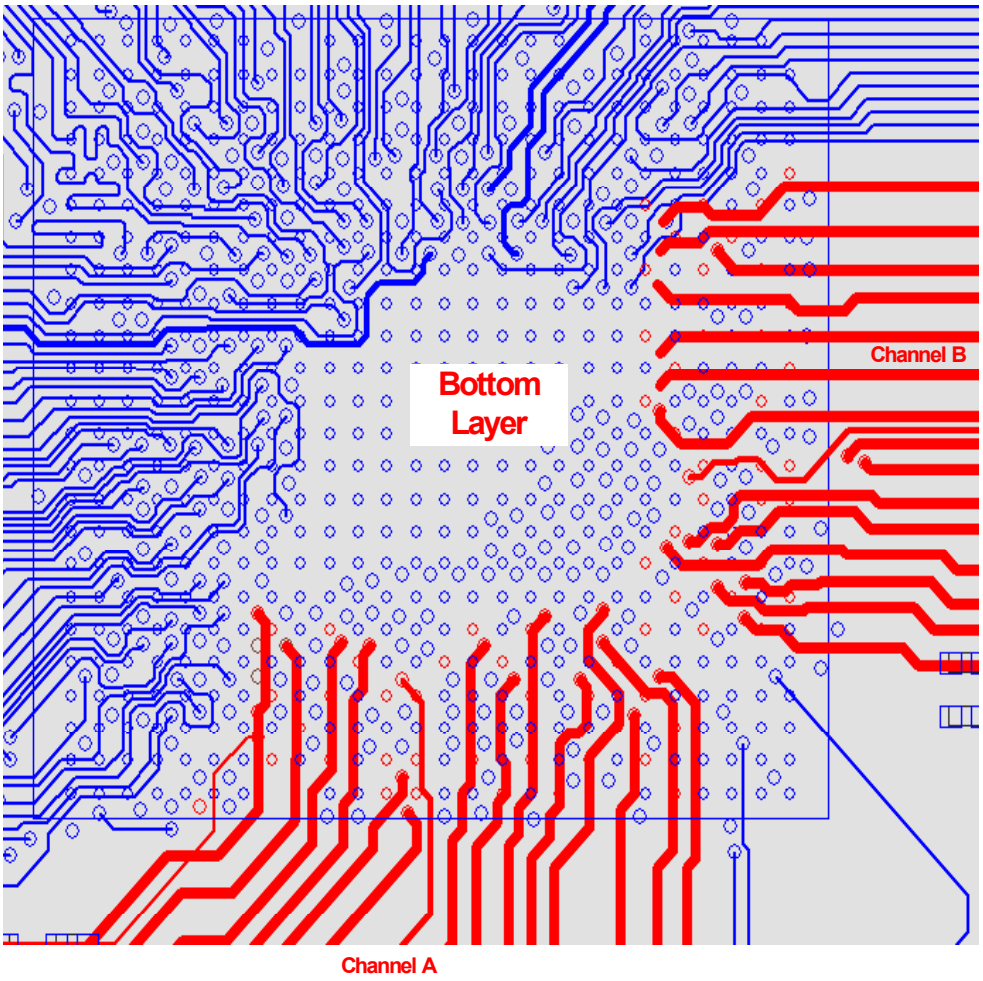


Figure 74. Rambus Technology Intel® MCH Breakout (Bottom Layer)



6.2.1 Optimized Rambus RDRAM* Device Routing Rules for a Four-Layer Motherboard Design

This section documents ONLY the routing guideline changes from the general guidelines outlined in the *Intel® Pentium® 4 Processor in the 478 Pin Package / Intel® 850 Chipset Family Platform Design Guide*.

General optimized routing guidelines that apply to Channel A and Channel B

- Do NOT implement dummy VIAs on RSL signals routed on the top layer.
- RSL signals routed on the top layer need to be routed 25mils longer than RSL signals on the bottom layer.

7 AGP Interface Routing

For detailed AGP Interface functionality (protocols, rules and signaling mechanisms, etc.) refer to the *AGP Interface Specification, Revision 2.0*, which can be obtained from http://www.agpforum.org. This design guide focuses only on specific Intel 850 chipset-based platform recommendations.

The latest *AGP Interface Specification* enhances the functionality of the original *AGP Interface Specification, Revision 1.0* by allowing 4x data transfers and 1.5 V operation. In addition to these enhancements, additional performance enhancement and clarifications, such as fast write capability, are included in the *AGP Interface Specification, Revision 2.0*. The Intel 850 chipset supports these enhanced features and 1.5 V signaling only.

The 4x mode of operation on the AGP interface provides for "quad-sampling" of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses. This means data is sampled four times during each 66 MHz AGP clock cycle or each data cycle is ¼ of 15 ns or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time not the clock cycle time. During 2x mode, data is sampled twice during a 66 MHz clock cycle; therefore, the data cycle time is 7.5ns. These high-speed data transfers are accomplished using source synchronous data strobing for 2x mode and differential source synchronous data strobing for 4x mode.

With data cycle times as small as 3.75 ns and setup/hold times of 1ns, it is important to minimize noise and propagation delay mismatch. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great or there is noise on the interface, incorrect data will be sampled. The AGP signals are broken into three groups: 1x timing domain and 2x/4x timing domain signals. In addition, the 2x/4x timing domain signals are divided into three sets of signals (#1–#3). All signals must meet the minimum and maximum trace length, width and spacing requirements. The trace length matching requirements are only applicable between the 2x/4x timing domain signal sets.

Table 25. AGP 2.0 Signal Groups

1x Timing Domain	2x/4x Timing Domain		Miscellaneous Signals
CLK	SET #1	AD[15:0]	USB+
RBF#		C/BE[1:0]#	USB-
WBF#		AD_STB0	OVRCNT#
ST[2:0]		AD_STB0#	PME#
PIPE#	SET #2	AD[31:16]	TYPDET#
REQ#		C/BE[3:2]#	PERR#
GNT#		AD_STB1	SERR#
PAR		AD_STB1#	INTA#
FRAME#	SET #3	SBA[7:0]	INTB#
IRDY#		SB_STB	
TRDY#		SB_STB#	
STOP#			
DEVSEL#			

Strobe signals are not used in the 1x AGP mode. In 2x AGP mode, AD[15:0] and C/BE[1:0]# are associated with AD_STB0, AD[31:16] and C/BE[3:2]# are associated with AD_STB1, and SBA[7:0] is associated with SB_STB. In 4X AGP mode, AD[15:0] and C/BE[1:0]# are associated with AD_STB0 and AD_STB0#, AD[31:16] and C/BE[3:2]# are associated with AD_STB1 and AD_STB1#, and SBA[7:0] is associated with SB_STB and SB_STB#.

7.1 AGP Routing Guidelines

The following section documents the recommended routing guidelines for Intel 850 chipset-based designs. All aspects of the interface will be covered from signal trace length to decoupling. These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

These guidelines are not intended to replace thorough system simulations and validation.

7.1.1 1X Timing Domain Signal Routing Guidelines

1x signals should adhere to the follow routing guidelines:

- All 1X timing domain signals maximum trace length is 7.5 inches
- 1X timing domain signals can be routed with 5 mil minimum trace separation
- No trace length matching requirements for 1X timing domain signals

7.1.2 2X/4X Timing Domain Signal Routing Guidelines

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6”) and long AGP interfaces (e.g., > 6” and < 7.25”) are documented separately. The maximum length that is allowed for the AGP interface is 7.25 inches.

7.1.2.1 Trace Lengths Less Than 6 Inches

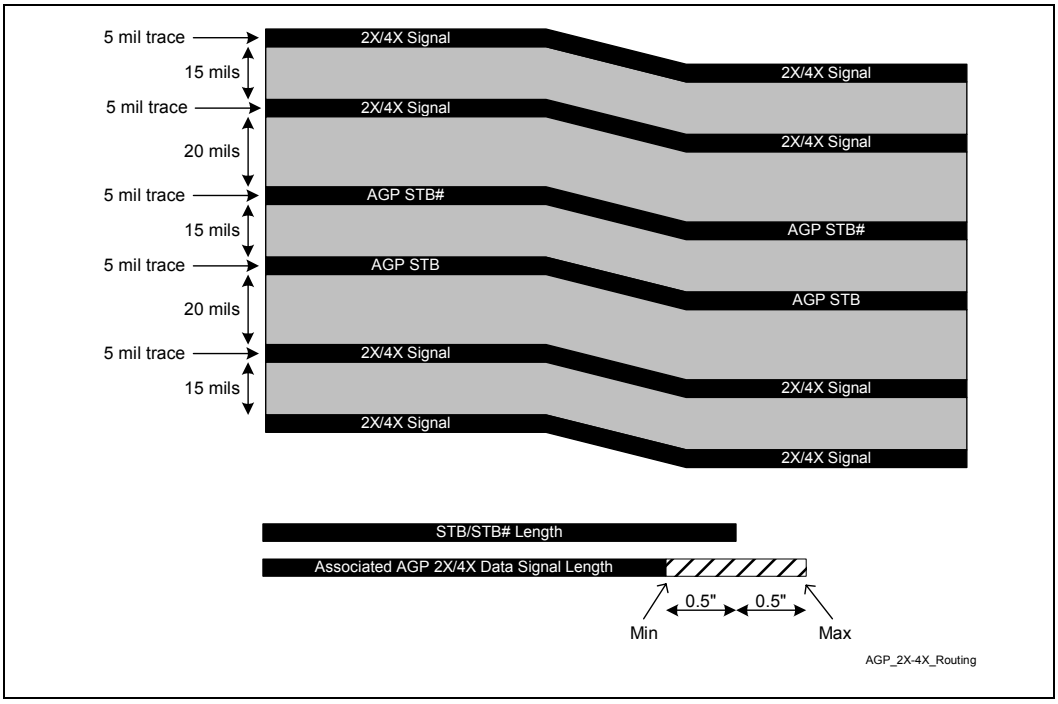
If the AGP interface is less than 6 inches with 60 Ω ±10% board impedance, at least 5 mil traces with at least 15 mils of space (1:3) between signals is required for 2X/4X lines (data and strobes). These 2X/4X signals must be matched to their associated strobe within ±0.25 inches. For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3 inches long, the data signals associated to those strobe signals (e.g., AD[15:0] and C/BE[2:0]#), can be 5.05 to 5.55 inches long. While another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 inches long and the data signals associated to those strobe signals (e.g., SBA[7:0]) can be 3.95 to 4.45 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source synchronous AGP interface; therefore special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least

20 mils (1:4). The strobe pair must be length matched to less than ±0.1 inches (i.e., a strobe and its compliment must be the same length within 0.1 inches).

If the board impedance is 15%, the trace spacing increases to 20 mils. See the AGP interfaces trace length summary section for detailed information regarding 15% tolerance signals.

Figure 75. AGP 2X/4X Routing Example for Interfaces < 6 Inches



7.1.2.2 Trace Lengths Greater Than 6 Inches and Less Than 7.25 Inches

Longer lines have more crosstalk. Therefore in order to reduce skew, longer line lengths require a greater amount of spacing between traces. For line lengths greater than 6 inches and less than 7.25 inches, 1:4 routing is required for all data lines and strobes with a 10% tolerance impedance. For these designs, the line length mismatch must be less than ±0.125 inches within each signal group (between all data signals and the strobe signals).

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5 inches long, the data signals that are associated to those strobe signals (e.g., AD[15:0] and C/BE[2:0]#), can be 6.475 inches to 6.625 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2 inches long, and the data signals that are associated to those strobe signals (e.g. SBA[7:0]), can be 6.075 inches to 6.325 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source synchronous AGP interface; therefore special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1 inches (that is, a strobe and its compliment must be the same length within 0.1 inches).

7.1.3 AGP Interfaces Trace Length Summary

The 2X/4X Timing Domain Signals can be routed with 5 mil spacing when breaking out of the MCH. The routing must widen to the documented requirements within 0.3 inches of the MCH package.

When matching trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

Reduce line length mismatch to insure added margin. In order to reduce trace to trace coupling (crosstalk), separate the traces as much as possible. All signals in a signal group should be routed on the same layer. The trace length and trace spacing requirements must not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.

Table 26. AGP 2.0 Routing Summary

Signal	Maximum Length	Trace Spacing (5 mil traces)	Length Mismatch	Relative To
1X Timing Domain	7.5 inches	5 mils	No requirement	N/A
2X/4X Timing Domain Set #1	7.25 inches	20 mils [3]	±0.125 inches [2]	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set #2	7.25 inches	20 mils [3]	±0.125 inches [2]	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set #3	7.25 inches	20 mils [3]	±0.125 inches [2]	SB_STB and SB_STB#
2X/4X Timing Domain Set #1	6 inches	15 mils [1,3]	±0.25 inches [2]	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set #2	6 inches	15 mils [1,3]	±0.25 inches [2]	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set #3	6 inches	15 mils [1,3]	±0.25 inches [2]	SB_STB and SB_STB#
2X/4X Timing Domain Set #1	6 inches	20 mils [1,4]	±0.25 inches [2]	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set #2	6 inches	20 mils [1,4]	±0.25 inches [2]	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set #3	6 inches	20 mils [1,4]	±0.25 inches [2]	SB_STB and SB_STB#

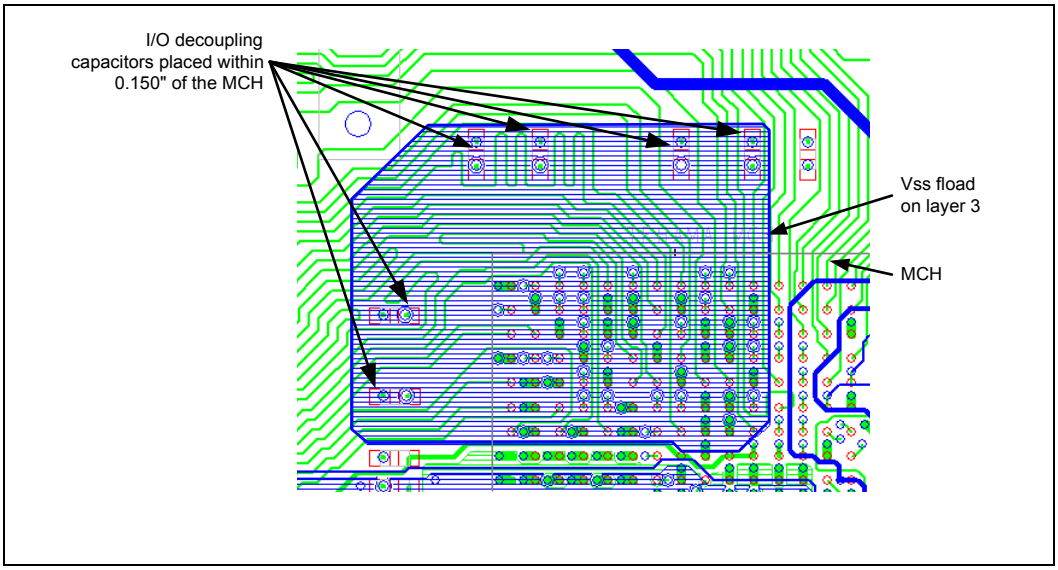
NOTES:
1. Each strobe pair must be separated from other signals by at least 20 mils.
2. Each strobe pair must be the same length.
3. These guidelines apply to board stack-ups with 10% impedance tolerance.
4. These guidelines apply to board stack-ups with 15% impedance tolerance

7.1.4 I/O Decoupling Guidelines

A minimum of six 0.01 µF capacitors are required for I/O decoupling. The designer should evenly distribute placement of decoupling capacitors among the AGP interface signal field and placed as close to the MCH as possible (no further than 0.15 inches from the edge of the MCH package). It is recommended that the designer use a low ESL ceramic capacitor, such as a 0603 body type, X7R dielectric.

To help lower the inductive path from the decoupling capacitor, pour a solid VSS plane under the VDDQ plane on layer 3 from the decoupling capacitors to the MCH. Figure 76 illustrates an example AGP decoupling layout with a VSS flood. This VSS flood that is referenced to VDDQ optimizes the mutual inductance between the two planes. The mutual inductance helps cancel out the self inductance from the power balls on the package to the decoupling caps.

Figure 76. AGP I/O Decoupling Example with a VSS Flood to Improve Power Delivery to the Intel® MCH



In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition AGP signal from one reference signal plane to another. One extra 0.01 µF capacitor is required per 10 vias. The capacitor should be placed as close to the center of the via field as possible.

The designer should ensure that the AGP connector is well decoupled as described in the revision 1.0 of the *AGP Design Guide*, Section 1.5.3.3.

7.1.5 Signal Power/Ground Referencing Recommendations

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the MCH to an AGP connector utilizing a minimum number of vias on each net; AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT# and ST[2:0].

In addition to the minimum signal set listed above, it is strongly recommended that half of all your AGP signals be referenced to ground depending on board layout. An ideal design would have the complete AGP interface signal field referenced to ground.

The recommendations above are not specific to any particular PCB stack-up, but are applicable to all Intel chipset designs.

7.1.6 VDDQ and TYPEDET#

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller and is always 3.3 V. VDDQ is the interface voltage. The Intel 850 chipset only supports an interface voltage of 1.5 V.

AGP 2.0 specification requires VCC and VDDQ to be tied to separate power planes and implements a TYPEDET# (type detect) signal on the AGP connector that determines the interface operating voltage (VDDQ). However, a motherboard based on the Intel 850 chipset only will only support 1.5 V add-in card. The 3 V add-in cards are not supported. Therefore, TYPEDET# detection on the motherboard is not required.

7.1.7 V_{REF} Generation

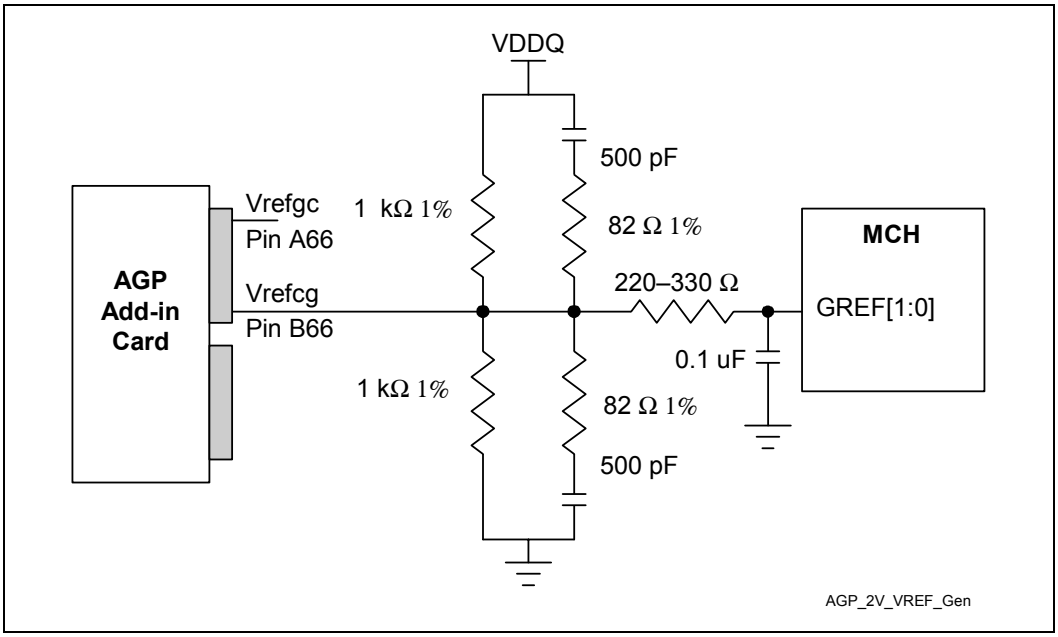
For 1.5 V add-in cards, both the graphics controller and MCH are required to generate VREF and distribute it through the connector. Two signals have been defined on the 1.5 V connector to allow V_{REF} delivery:

- VREFGC- VREF from the graphics controller to the chipset
- VREFCG- VREF from the chipset to the graphics controller

However, the usage of the source generated VREF at the MCH is not required per the *AGP Interface Specification, Revision 2.0*. Given this and the fact that the MCH requires the presence of V_{REF} when an AGP add-in card is present and not present, the following circuit is recommended for V_{REF} generation.

The V_{REF} divider network should be placed near the AGP interface. The minimum trace spacing around the V_{REF} signal must be 25 mils, in order to reduce cross talk and maintain signal integrity. Also, a 0.1 µF bypass capacitor should be placed within 150 mils of the MCH's GREF pins. The two GREF pins on the MCH (GREF[0:1]) should be tied together before connecting to the bypass capacitor. V_{REF} voltage must be 0.5 x VDDQ for 1.5 V operation.

Figure 77. AGP 2.0 V_{REF} Generation and Distribution for 1.5 V Cards



7.1.8 Intel® MCH AGP Interface Buffer Compensation

The MCH AGP interface supports resistive buffer compensation (GRCOMP[1:0]). The GRCOMP[1:0] signals must be tied to a 40 Ω ± 2% or 39 Ω ± 1% pull-down resistor to ground. This trace should be kept to 10 mils wide and less than 0.5 inches long.

7.1.9 AGP Pull-ups/Pull-down on AGP Signals

Some of the AGP signals may require either a pull-up resistor to VDDQ (not VCC3.3) or pull-down resistor to GND. This is to ensure stable values are maintained when agents are not actively driving the bus. The recommended AGP pull-up/pull-down resistor value is 8.2 Ω at 10% tolerance (4 kΩ ≤ R_{value} ≤ 16 kΩ). The AGP interface does not require external termination.

The trace stub length to the pull-up/pull-down resistor should be kept to a minimum to avoid signal reflection. This trace length is different for 1x and 2x/4x modes. Below are the recommended stub lengths for 1x and 2x/4x modes.

- 1x mode, trace stub to pull-up resistor should be kept to less than 0.5 inches
- 2x/4x mode, trace stub to pull-up resistor should be kept to less than 0.1 inches

Short stub lengths help minimize signal reflections from the stub. The strobe signals require pull-up/pull-down on the motherboard to ensure stable values when there are no agents driving the bus.

Note: The G_GNT# and G_PAR signals require pull-ups to VDDQ.

The MCH G_GNT# output signal will be tri-stated during RSTIN# assertion. This signal must have an external pull-up resistor to keep it from floating during the RSTIN# assertion. The recommended value is the same as the other AGP common clock signals.

The MCH G_PAR signal also needs an external pull-up resistor. This signal must have an external pull-up resistor to ensure that G_PAR remains at a valid logic level during AGP protocol transactions.

Table 27. AGP Pull-up/Pull-down Resistors

Signals	PU/PD Requirement
1x Timing Domain	
FRAME#	pull-up resistor to VDDQ
TRDY#	pull-up resistor to VDDQ
IRDY#	pull-up resistor to VDDQ
DEVSEL#	pull-up resistor to VDDQ
STOP#	pull-up resistor to VDDQ
SERR#	pull-up resistor to VDDQ
PERR#	pull-up resistor to VDDQ
RBF#	pull-up resistor to VDDQ
PIPE#	pull-up resistor to VDDQ
REQ#	pull-up resistor to VDDQ
GNT#	Pull-up resistor to VDDQ
WBF#	pull-up resistor to VDDQ
PAR#	Pull-up resistor to VDDQ
INTA#	pull-up resistor to 3.3 V
INTB#	pull-up resistor to 3.3 V
2x/4x Timing Domain	
AD_STB[1:0]	pull-up resistor to VDDQ
SB_STB	pull-up resistor to VDDQ
AD_STB[1:0]#	pull-down resistor to GND
SB_STB#	pull-down resistor to GND

7.1.10 AGP Signal Voltage Tolerance List

Table 28 documents 3.3 V tolerant signals and 5 V tolerant signals (Refer to the AGP Specification for more details) on the AGP interface. All other signals, in the VDDQ group, are not 3.3 V tolerant during 1.5 V AGP operation.

Table 28. 3.3 V and 5 V Tolerant Signals during 1.5 V Operation

3.3 V Tolerant Signals	5 V Tolerant Signals
PME#	USB+
INTA#	USB-
INTB#	OVRCNT#
PERR#	
SERR#	
CLK	
RST	

7.1.11 AGP Connector

Only 1.5 V add-in cards are supported. The 1.5 V uses the AGP 3 V connector and rotates it 180 degrees on the planar. Therefore, the key of the connector moves to the opposite side of the planar away from the I/O panel and will not allow 3 V add-in cards.

The designer should ensure that the AGP connector is well decoupled as described in the revision 1.0 of the *AGP Design Guide*, Section 1.5.3.3 (i.e., use a 0.01 µF capacitor for each power pin and a bulk 10 µF tantalum capacitor on VDDQ and 20 µF tantalum capacitor on VCC3_3 plane near the connector.).

7.2 AGP Universal Retention Mechanism (RM)

Environmental testing and field reports indicate that AGP cards may come unseated during system shipping and handling without proper retention. In order to avoid disengaged AGP cards, Intel recommends that AGP based platforms use the AGP retention mechanism (RM).

The AGP RM is a mounting bracket that is used to properly locate the card with respect to the chassis and to assist with card retention. The AGP RM is available in two different handle orientations; left-handed (see Figure 78) and right-handed. Most system boards accommodate the left-handed AGP RM. The manufacturing capacity of the left-handed RM currently exceeds the right-handed capacity, and as a result Intel recommends that customers design their systems to insure they can use the left-handed version of the AGP RM (see Figure 79). The right-handed AGP RM is identical to the left-handed AGP RM, except for the position of the actuation handle. This handle is located on the same end as the primary design, but extends from the opposite side (mirrored about the center axis running parallel to the length of the part). Figure 79 contains keep out information for the left hand AGP retention mechanism. Use this information to make sure that your motherboard design leaves adequate space to install the retention mechanism.

The AGP interconnect design requires that the AGP card must be retained to the extent that the card does not back out more than 0.99 mm (0.039 in) within the AGP connector. To accomplish this it is recommended that new cards implement an additional notch feature in the mechanical keying tab to allow an anchor point on the AGP card for interfacing with an AGP RM. The retention mechanism's round peg engages with the AGP card's retention tab and prevents the card from disengaging during dynamic loading. The additional notch feature in the mechanical keying tab is required for 1.5-volt AGP cards and is recommended for the new 3.3-volt AGP cards.

Figure 78. AGP Left Handed Retention Mechanism Drawing

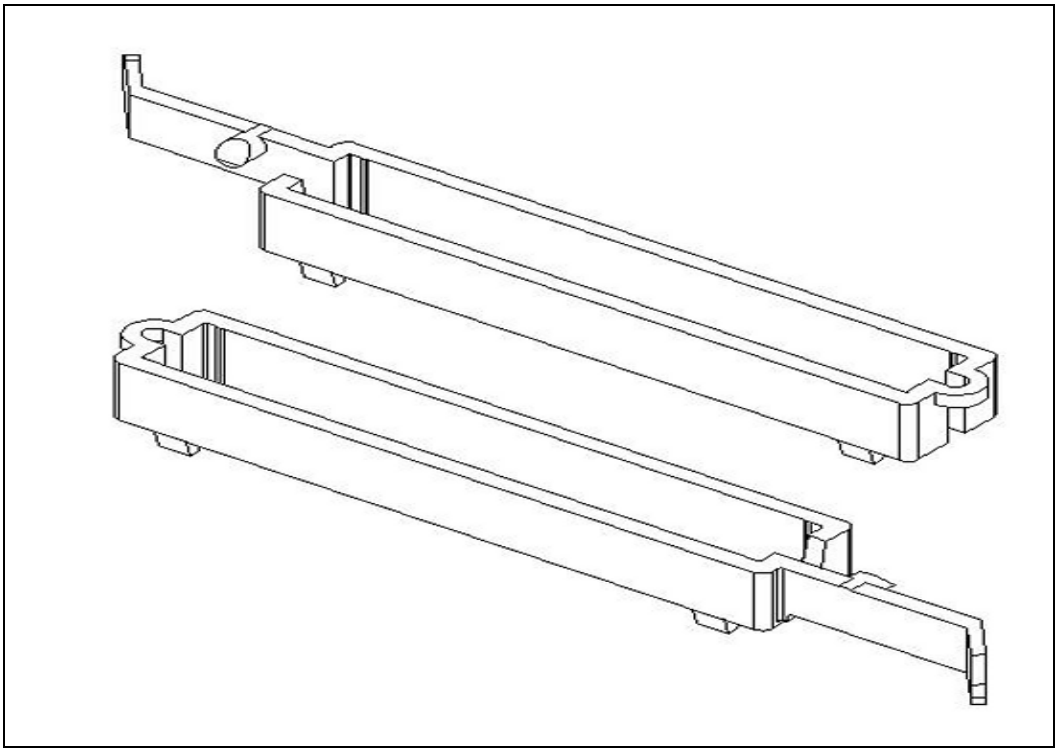
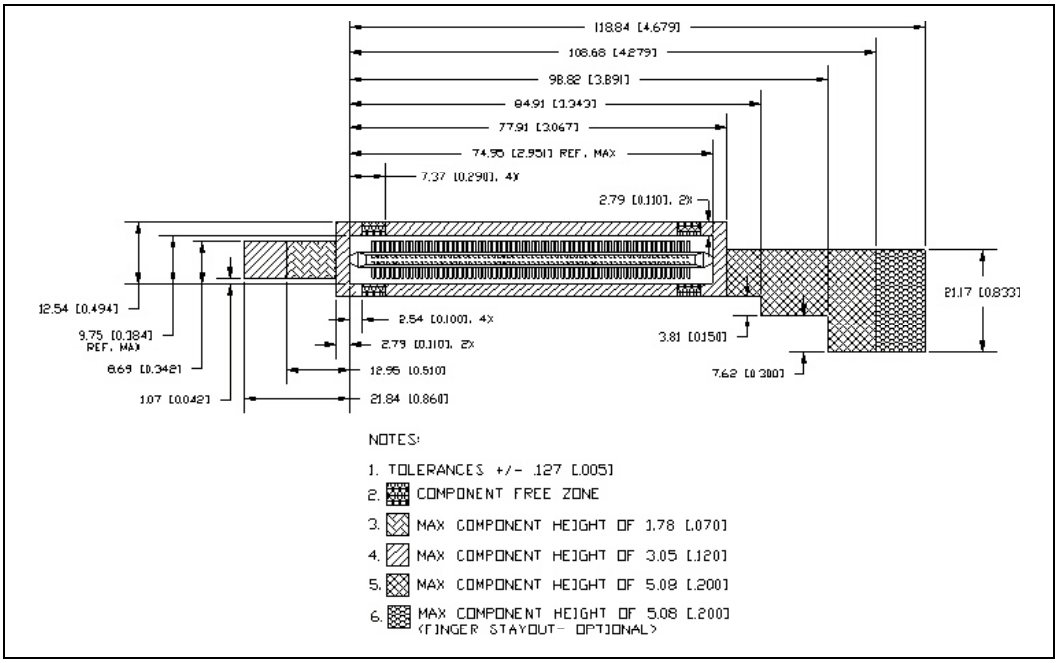


Figure 79. AGP Left Handed Retention Mechanism Keep-out Information



Engineering Change Request number 48 (ECR #48) of the AGP specification details the AGP RM, which is recommended for all AGP cards. These are approved changes to the *Accelerated Graphics Port (AGP) Interface Specification, Revision 2.0*. Intel intends to incorporate the AGP RM changes into later revisions of the AGP Interface Specification. In addition, Intel has defined a reference design of a mechanical device to utilize the features defined in ECR #48.

ECR #48 can be viewed off the Intel Web site at:
http://developer.intel.com/technology/agp/ecr.htm

More information regarding this component (AGP RM) is available from the following vendors.

Table 29 List of Vendors for Retention Mechanism

Resin Color	Supplier Part Number	"Left Handed" Orientation (Preferred)	"Right Handed" Orientation (Alternate)
Black	AMP P/N	136427-1	136427-2
	Foxconn P/N	006-0002-939	006-0001-939
Green	Foxconn P/N	009-0004-008	009-0003-008

7.3 AGP Routing Guidelines - Four-Layer Motherboard

AGP signals are routed on the bottom of the board reference GND. Signals routed on the top of the board are referenced to V_{DDQ}.

Figure 80. Example AGP Routing (Top Layer)

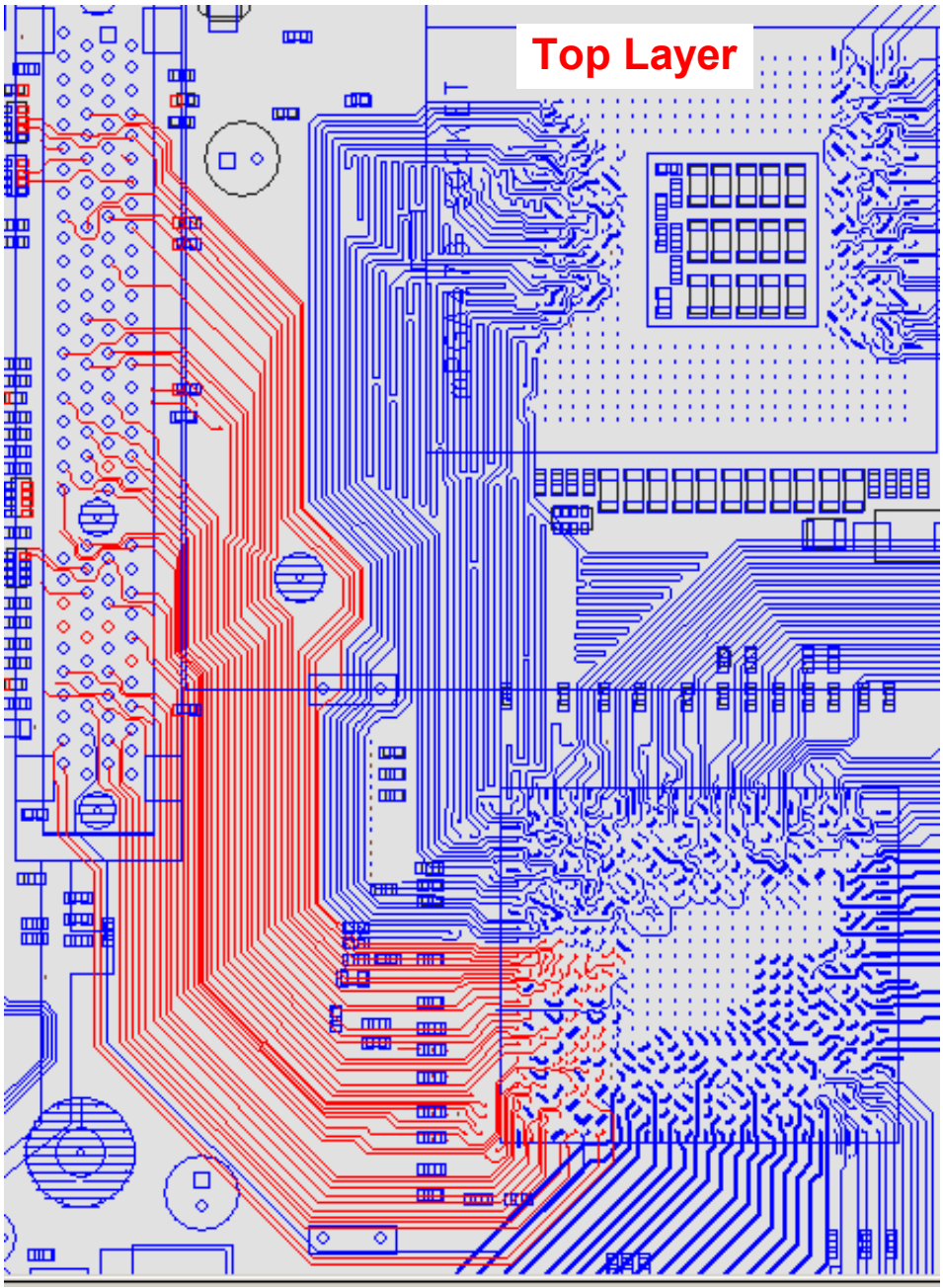


Figure 81. Example AGP Routing (Bottom Layer)

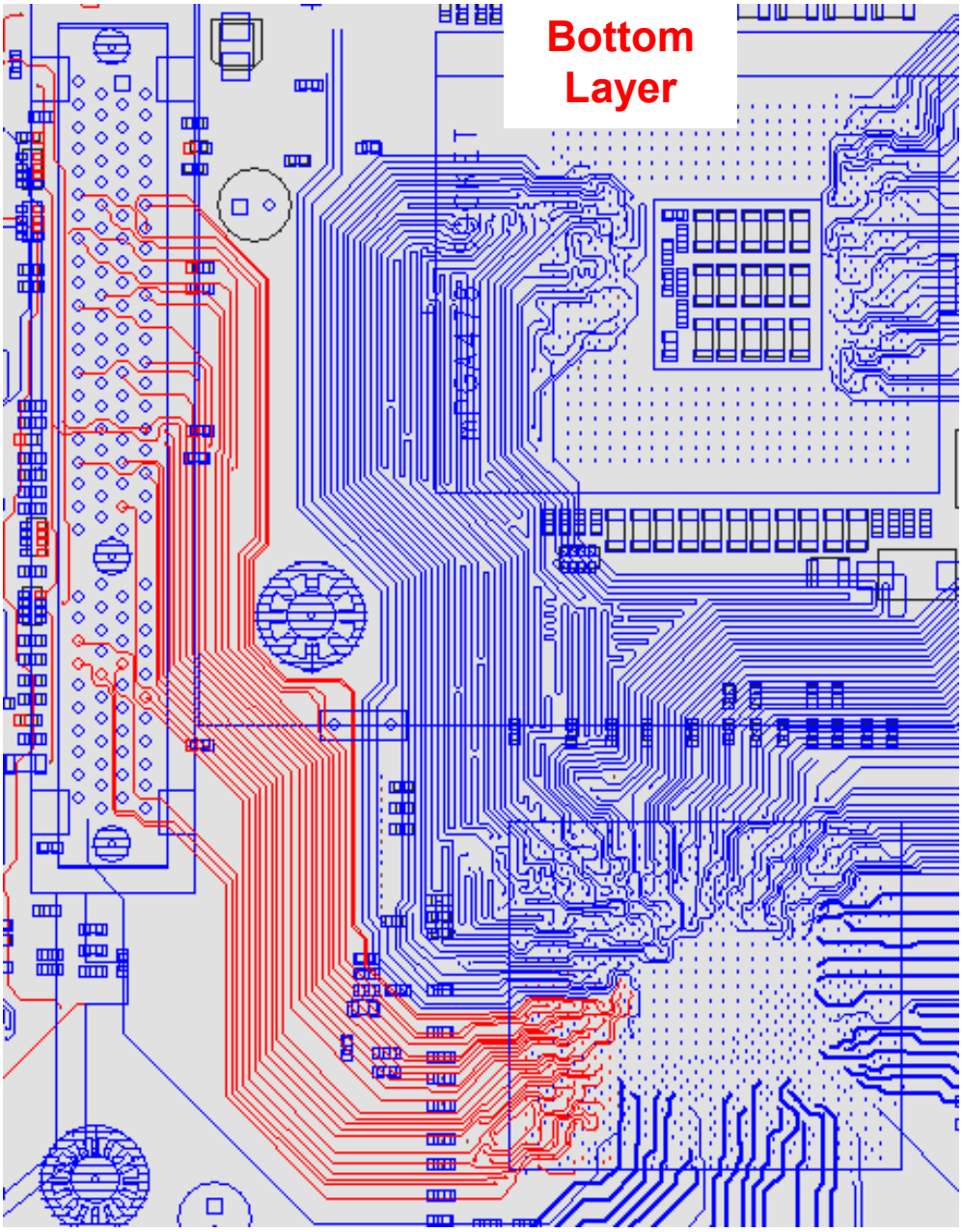
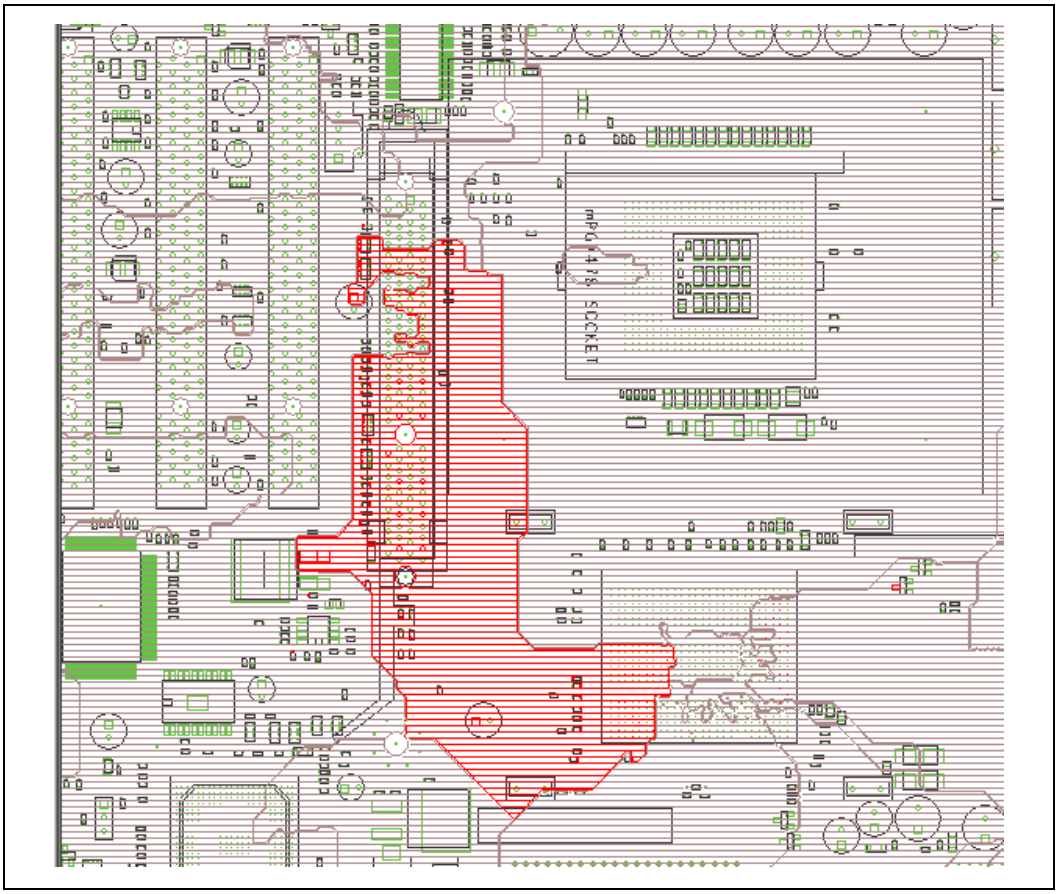


Figure 82. Example VDDQ Plane on Layer 2



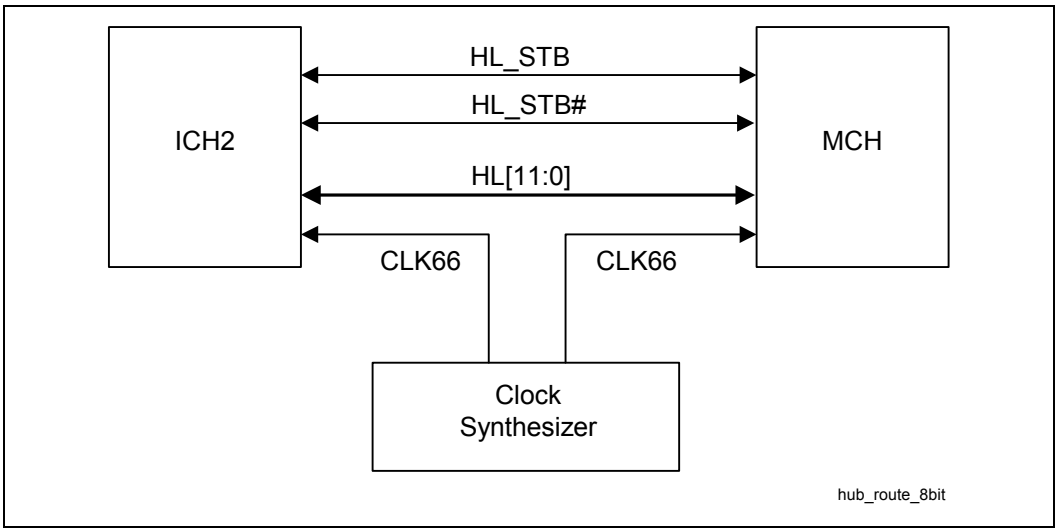
8 Hub Interface Routing

8.1 Hub Interface Routing Guidelines

The MCH and ICH2 ballout assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the hub interface signals be routed directly from the MCH to ICH2 with all signals referenced to VSS. Layer transition should be keep to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signal on the same layer.

The hub interface signals are broken into two groups: data signals (HL) and strobe signals (HL_STB). For the 8-bit hub interface, HL[0:7] are associated with HL_STB and HL_STB#.

Figure 83. 8-Bit Hub Interface Routing Example



8.2 8-Bit Hub Interface Routing Guidelines

This section describes the routing guidelines for the 8-bit hub interface. This hub interface connects the ICH2 to the MCH. This interface supports normal buffer mode. When the buffers are configured for normal mode, the trace impedance must equal 60 Ω ± 15%.

Table 30. 8-Bit Hub Interface Buffer Configuration Setting

Component	Hub Interface Buffer Mode	Trace Impedance	Strap
ICH2	Normal	60 Ω	HLCOMP pulled to VCC1_8 [1]
MCH	Normal	60 Ω	Default

NOTE: [1]Refer to Section 8.2.4 for the specific resistor value.

8.2.1 8-Bit Hub Interface Data Signals

The 8-bit hub interface data signal traces should be routed 5 mils wide with 20 mils trace spacing (5 on 20). These signals can be routed 5 on 15 for navigation around components or mounting holes. To break out of the MCH and ICH2 package, the hub interface data signals can be routed 5 on 5. The signal must be separated to 5 on 20 within 300 mils of the package. The maximum hub interface data signal trace length in normal buffer mode is 6 inches. Each data signal must be matched within ±0.1 inches of the HL_STB differential pair. There is no explicit matching requirement between the individual data signals.

8.2.2 8-Bit Hub Interface Strobe Signals

The hub interface strobe signals should be routed 5 mils wide with 20 mils trace spacing (5 on 20). This strobe pair should have a minimum of 20 mils spacing from any adjacent signals. The maximum length for the strobe signal in normal mode is 6 inches. Each strobe signal must be the same length, and each data signal must be matched within ±0.1 inches of the strobe signals.

8.2.3 8-Bit Hub Interface HIREF Generation/Distribution

HIREF is the hub interface reference voltage. The HIREF voltage requirement must be set appropriately for proper operation. See Table 31 for the HIREF voltage specifications for normal buffer mode and the associated resistor recommendations for the voltage divider circuit.

Table 31. 8-Bit Hub Interface HUBREF Generation Circuit Specifications

Buffer Mode	HIREF Voltage Specification (V)	Recommend Resistor Values for the HIREF Divider Circuit (ohm)
Normal	1/2 VCC1_8 ± 2%	R1 = R2 = 150 ± 1%

The single HIREF divider should not be located more than 3.5 inches away from either MCH or ICH2. If the single HIREF divider is located more than 3.5 inches away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HIREF divider should be bypassed to ground at each component with a 0.01µF capacitor located close to the component HUBREF pin. If the reference voltage is generated locally, the bypass capacitor needs to be close to the component HUBREF pin. Example HIREF divider circuits are shown in Figure 84 and Figure 85.

Figure 84. 8-Bit Hub Interface with a Shared Reference Divider Circuit (Normal Mode)

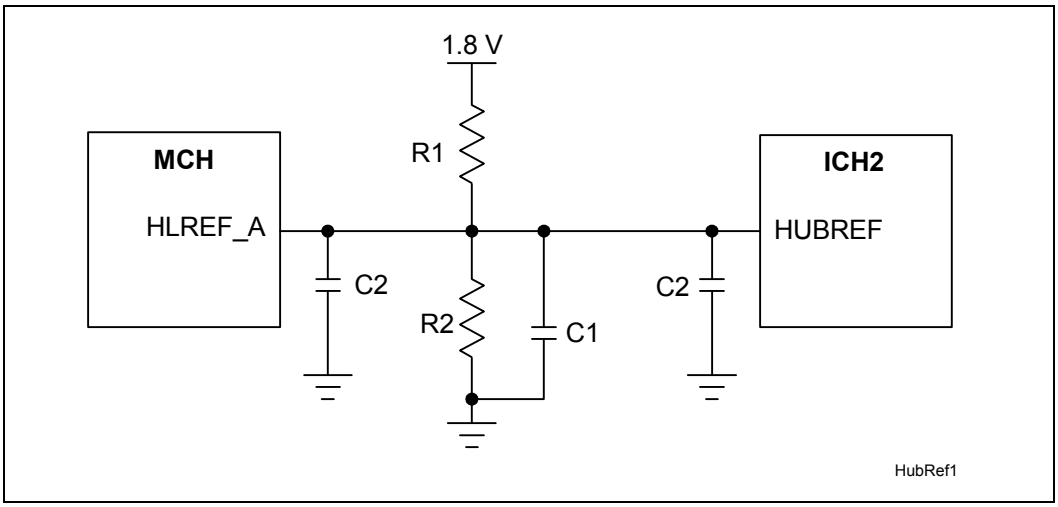
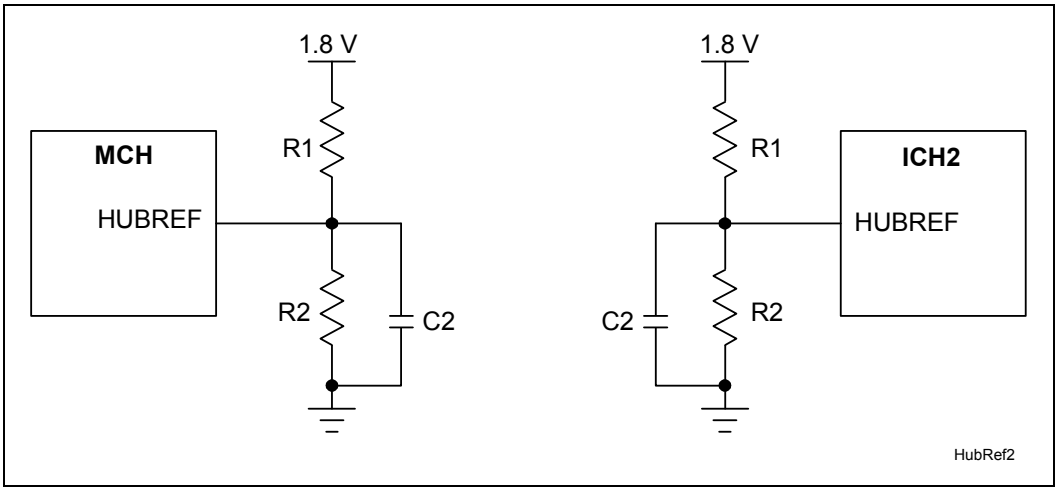


Figure 85. 8-Bit Hub Interface with Locally Generated Reference Divider Circuits



The resistor values, R1 and R2, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the above circuits) should be placed close to R1 and R2. Also, a 0.01 µF bypass capacitor (C2 in the above circuits) should be placed within 0.25 inches of each HUBREF pin. The trace length from the divider circuit to the HLREF pin must be no longer than 3.5 inches.

8.2.4 8-Bit Hub Interface Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires Resistive Compensation (RCOMP).

Table 32. 8-Bit Hub Interface RCOMP Resistor Values

Component	Hub Interface Buffer Mode	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied to
ICH2	Normal	60 Ω ± 15%	40 Ω ± 2% or 39 Ω ± 1%	VCC1_8
MCH	Normal	60 Ω ± 15%	40 Ω ± 2% or 39 Ω ± 1%	VSS

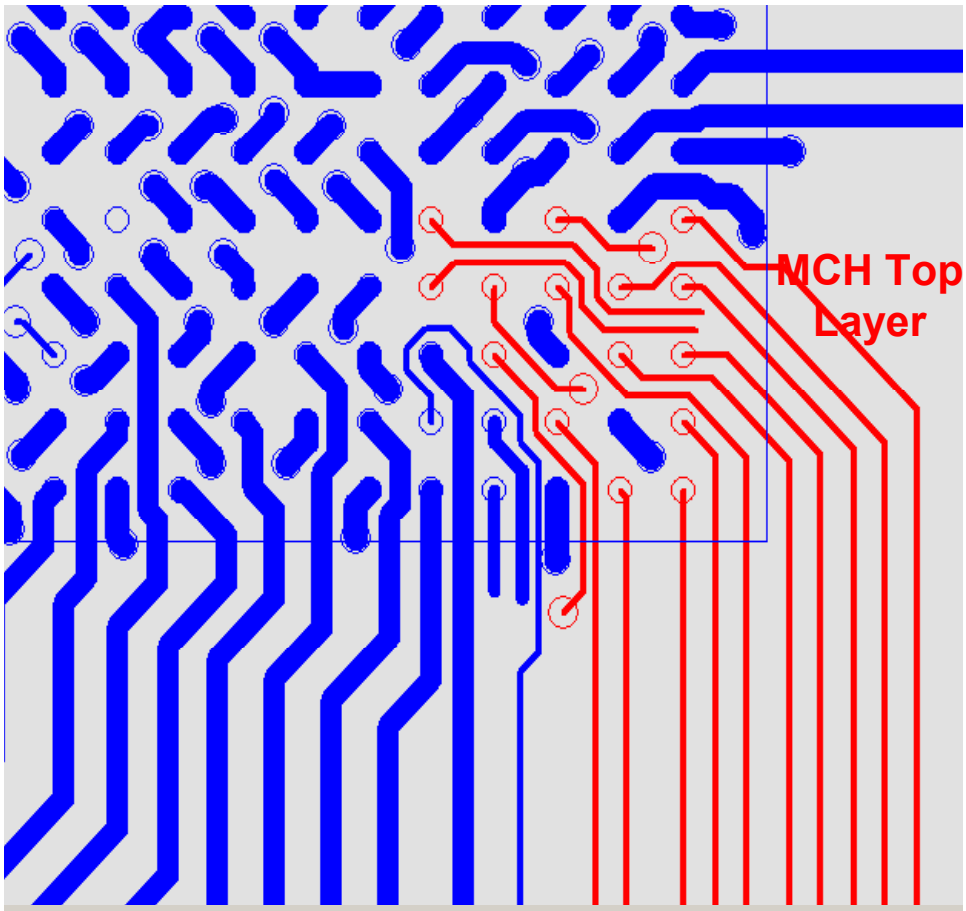
8.2.5 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per each component (i.e., the ICH2 and MCH). These capacitors should be placed within 150 mils from each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_8 side of the capacitors to the VCC1_8 power pins. Similarly, if layout allows, metal fingers running on the VCC1_8 side of the board should connect the ground side of the capacitors to the VSS power pins.

8.3 Hub Interface Routing Guidelines - Four-Layer Motherboard

To optimize the MCH 1.8V core and RAC power delivery, the hub interface should be routed on the top layer. The 1.8V power pins within the hub interface pin field should have VIAs to the 1.8V power plane on layer 2 and 4 as well as attach to the high reference decoupling capacitors. See the below graphic for more details.

Figure 86. Example Hub Interface Breakout / 1.8 V MCH Fingers



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9 I/O Controller Hub 2

9.1 This Chapter Provides Information on the Intel® 82801BA I/O Controller Hub 2 (ICH2) IDE Interface

This section contains guidelines for connecting and routing the ICH2 IDE interface. The ICH2 has two independent IDE channels. This section provides guidelines for IDE connector cabling and system board design, including component and resistor placement, and signal termination for both IDE channels. The ICH2 has integrated series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. We do not anticipate requiring additional series termination, but OEMs should verify system board signal integrity through simulation. Additional external 0 ohm resistors can be incorporated into the design to address possible noise issues on the system board. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5 mil traces on 7 mil spaces, and with a maximum trace length of 8 inches long (from ICH2 to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5 inches shorter than the longest IDE signal (on that channel).

9.1.1 IDE Cable

The IDE cabling specifications and requirements are listed below:

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the system board ground and hard disk drives.
- **ICH2 Placement:** The maximum trace length from the ICH2 to the ATA connector(s) is 8 inches.
- **PC ’99 requirement:** Support Cable Select for master-slave configuration is a system design requirement for Microsoft PC99. The CSEL signal of each ATA connector must be grounded at the host side.

9.1.2 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH2 IDE Controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5. The ICH2 needs to determine the type of cable that is present, in order to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

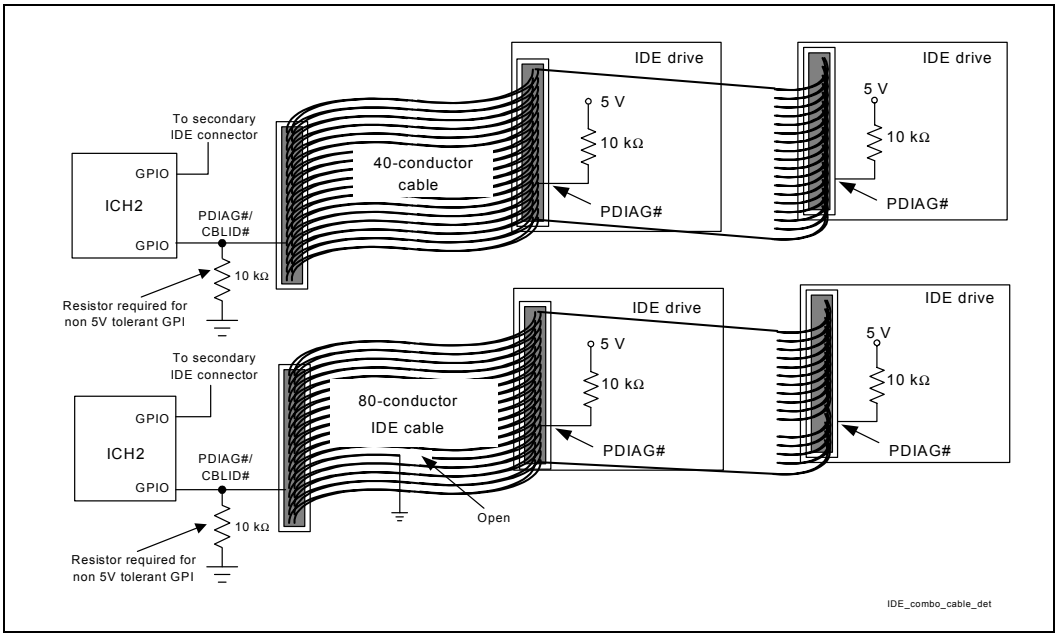
To determine if ATA/66 or ATA/100 mode can be enabled, the ICH2 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be done using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system, since this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

9.1.2.1 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the ATA/ATAPI-4 Standard, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 87. All IDE devices have a 10 kΩ pull-up resistor to 5 volts on this signal. Not all of the GPI and GPIO pins on the ICH2 are 5-volt tolerant. If non 5-volt tolerant inputs are used, a resistor divider is required to prevent 5 volts on the ICH2 or FWH pins. The proper value of the divider resistor is 10 kΩ (as shown in Figure 87).

Figure 87. Combination Host-Side/Device-Side IDE Cable Detection



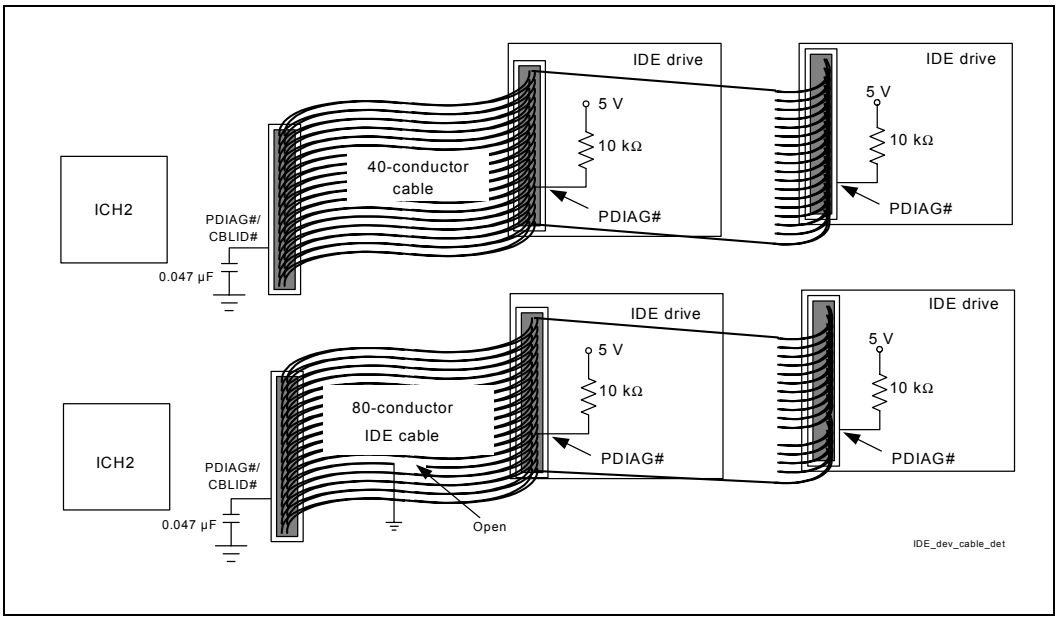
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high then there is 40-conductor cable in the system and ATA modes 3, 4, and 5 must not be enabled.

If PDIAG#/CBLID# is detected low, then there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is a 1, then an 80-conductor cable is present. If this bit is 0, then a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present, and notify the user of the problem.

9.1.2.2 Device-Side Cable Detection

For platforms that must implement Device-Side detection *only* (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 88. This capacitor *should not be populated* when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described above.

Figure 88. Device-Side IDE Cable Detection

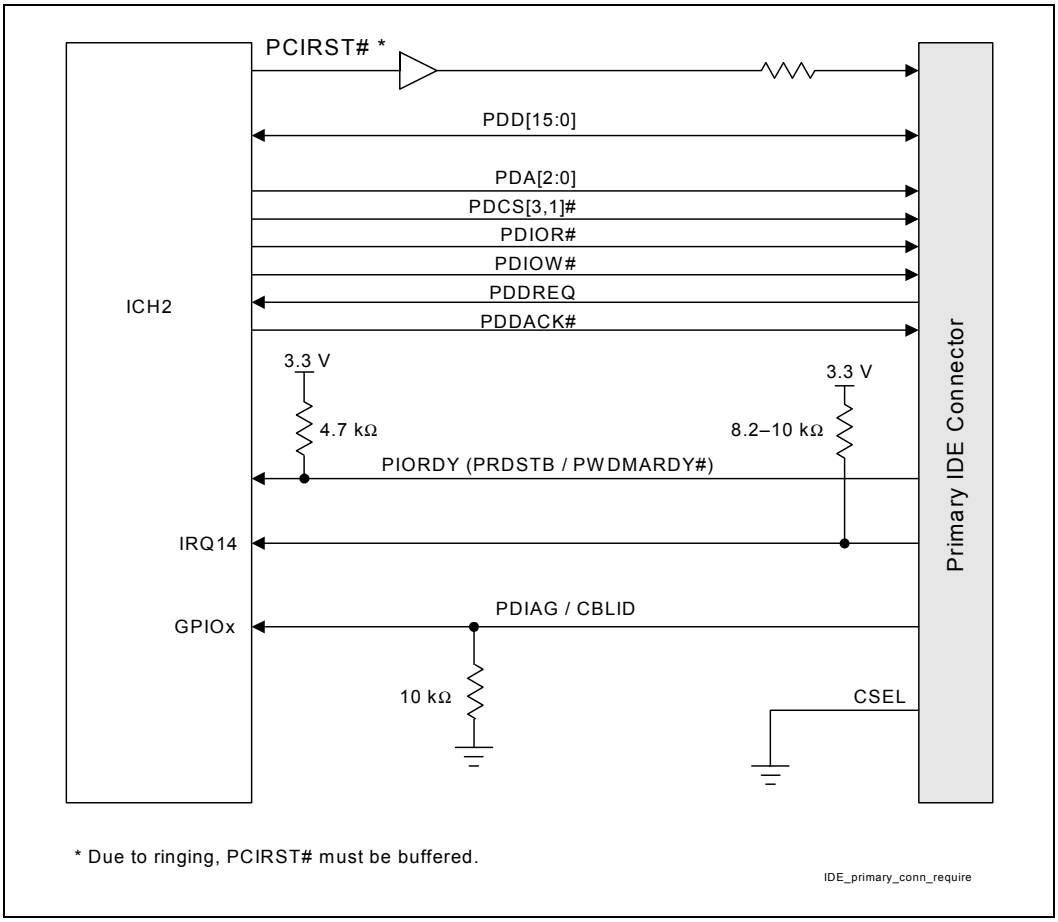


This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3, 4, or 5 drive will drive PDIAG#/CBLID# low and then release it (pulled up through a 10kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host and therefore the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore the signal will rise more slowly, as the capacitor charges. The drive can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

9.1.3 Primary IDE Connector Requirements

The 10 kΩ resistor to ground on the PDIAG/CBLID signal is now required on both the Primary and Secondary Connectors. This change is to prevent the GPI pin from floating if a device is not present on either IDE interface.

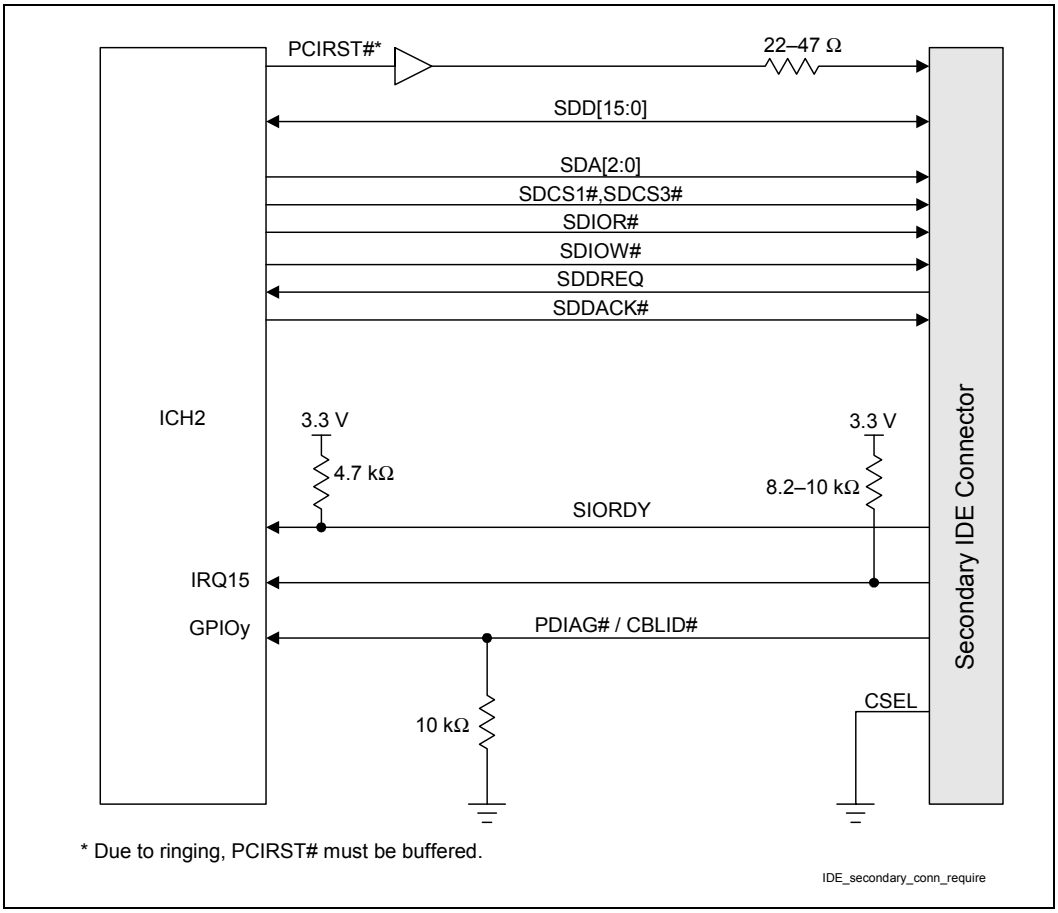
Figure 89. Connection Requirements for Primary IDE Connector



- 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3_3.
- A 4.7 kΩ pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are place as close to the connector as possible. Values are determined for each unique motherboard design.

9.1.4 Secondary IDE Connector Requirements

Figure 90. Connection Requirements for Secondary IDE Connector



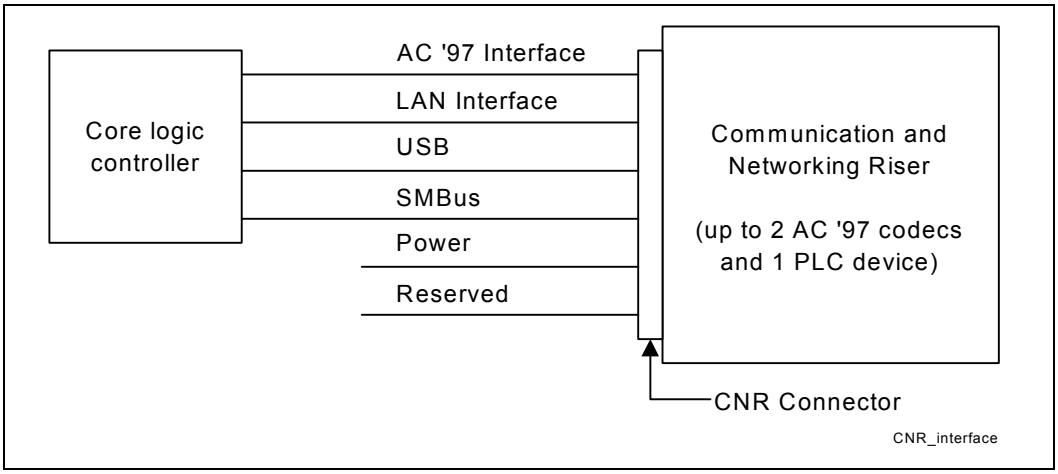
- 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3_3.
- A 4.7 kΩ pull-up resistor to VCC3_3 is required on PIORDY and SIORDY
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are place as close to the connector as possible. Values are determined for each unique motherboard design.

9.2 Communication and Networking Riser (CNR)

The Communication and Networking Riser (CNR) Specification defines a hardware scalable Original Equipment Manufacturer (OEM) system board riser and interface. This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, and 10/100 Ethernet based networking. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium.

Figure 91 indicates the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN Connection (PLC) can either be a 82562ET, 82562EM, or 82562EH component. It is required that the CNR A0–A2 pins be set to a unique address, so that the CNR EEPROM can be accessed. Refer to the CNR specification for additional information.

Figure 91. CNR Interface



9.2.1 CNR Placement

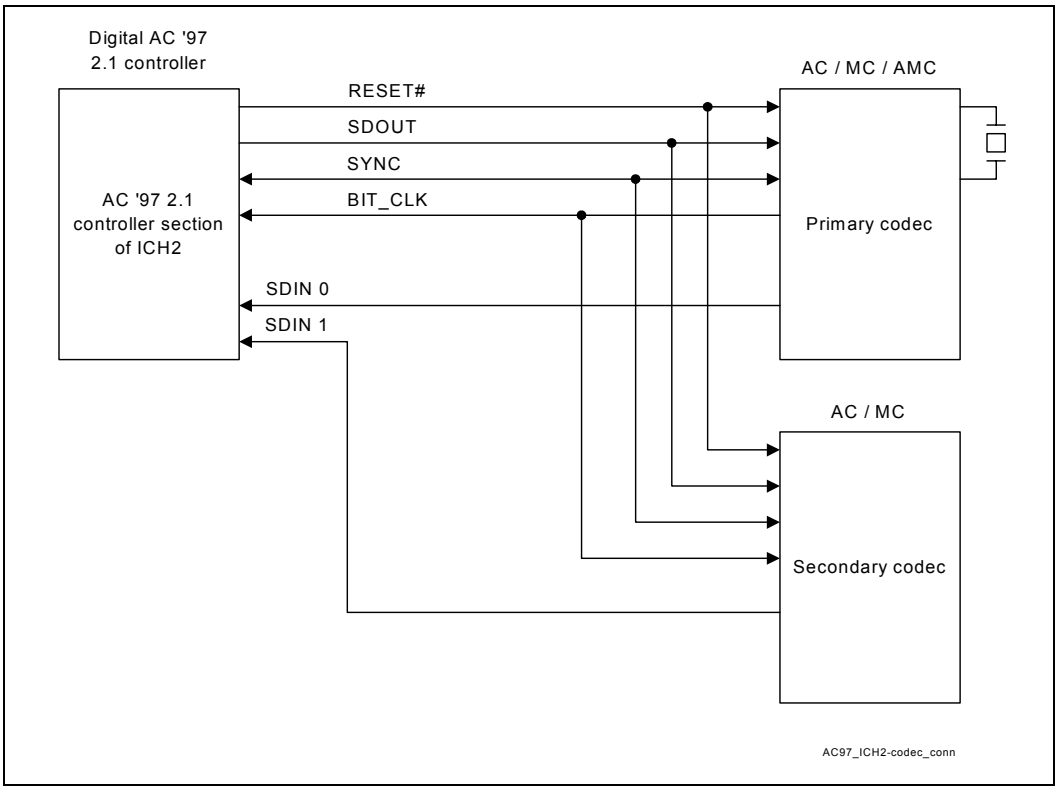
Refer to the *Communication and Network Riser Specification, Revision 1.0* for CNR placement.

9.3 Intel® AC'97

The ICH2 implements an AC'97 2.1 compliant digital controller. Any codec attached to the ICH2 AC-link must be AC'97 2.1 compliant as well. Contact your codec vendor for information on 2.1 compliant products. The AC'97 2.1 specification is on the Intel website: http://developer.intel.com/pc-supp/platform/ac97/index.htm

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH2 AC-link allows a maximum of two codecs to be connected. Figure 92 shows a two-codec topology of the AC-link for the ICH2.

Figure 92. Intel® ICH2 AC'97 - Codec Connection



In a lightly loaded system (e.g., single codec down), AC'97 signal integrity should be evaluated to confirm that the signal quality on the link is acceptable to the codec used in the design. A series resistor at the driver and a capacitor at the codec can be implemented in order to compensate for any signal integrity issues. The values used will be design dependent and should be verified for correct timings. The ICH2 AC-link output buffers are designed to meet the AC'97 2.1 specification with the specified load of 50 pF.

The ICH2 supports the following combinations of codecs:

Figure 93. Audio Codec

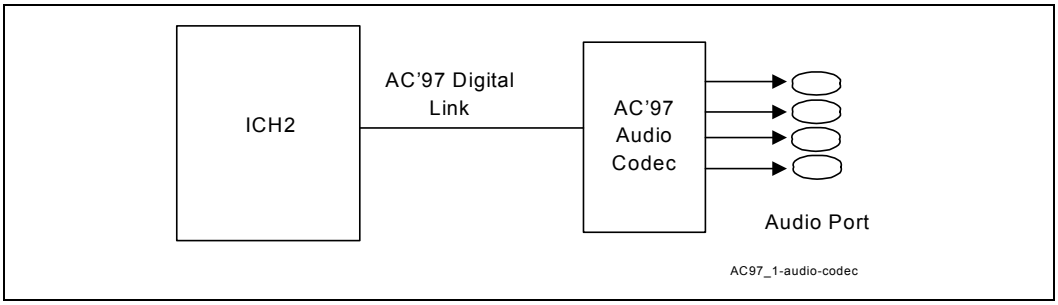


Figure 94. Modem Codec

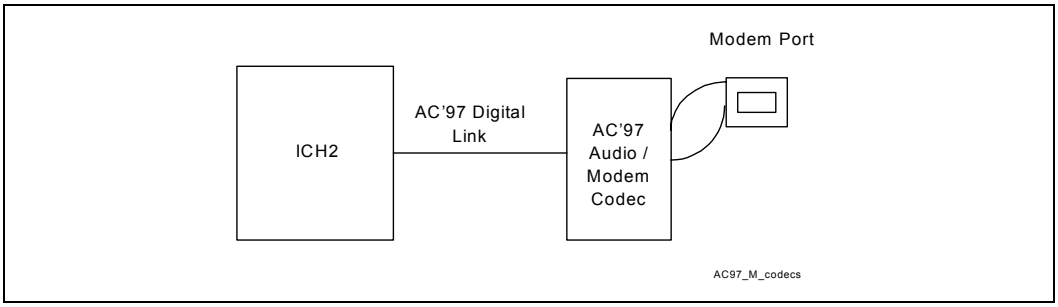


Figure 95. Audio/Modem Codec

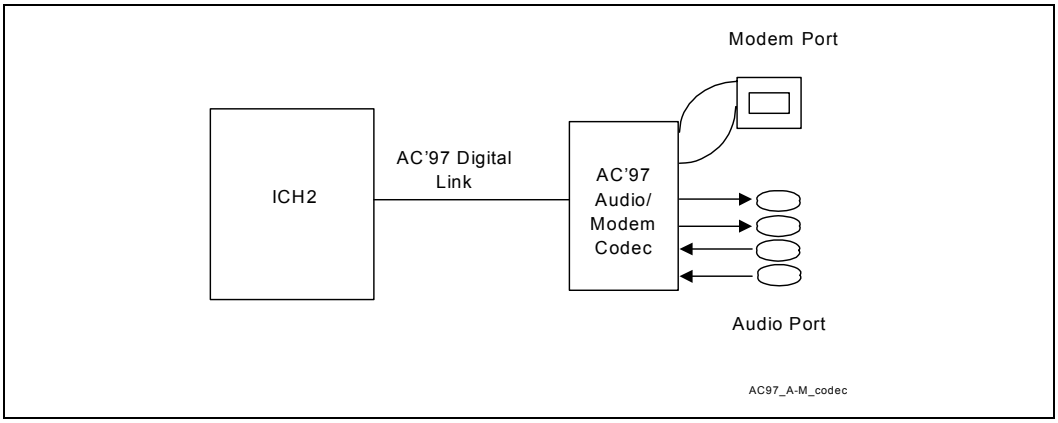


Figure 96. Modem Codecs

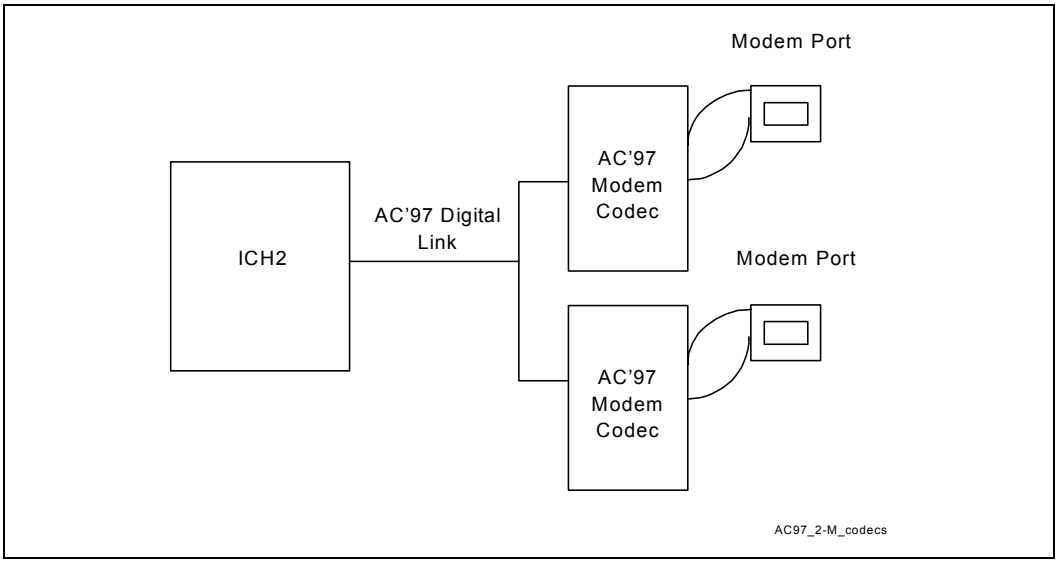


Figure 97. Audio and Modem Codecs

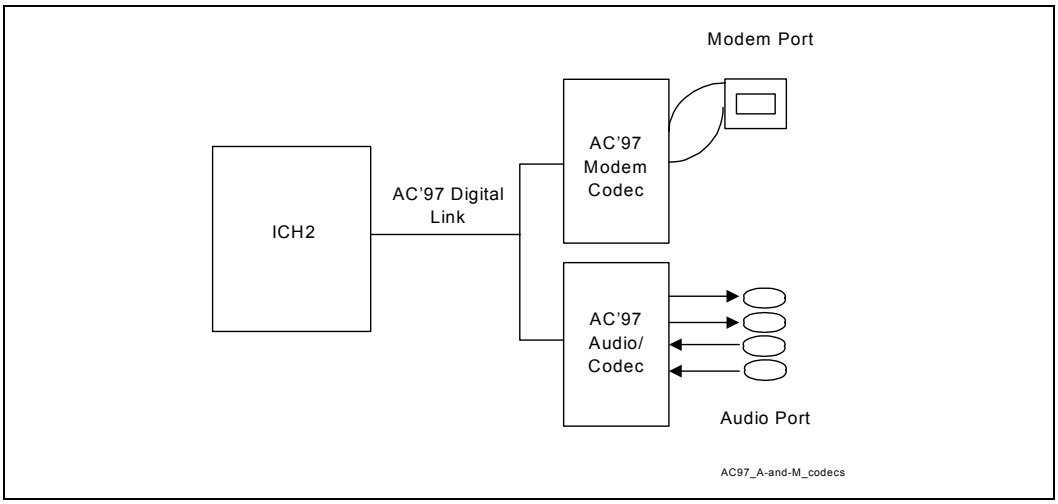


Figure 98. Audio Codecs

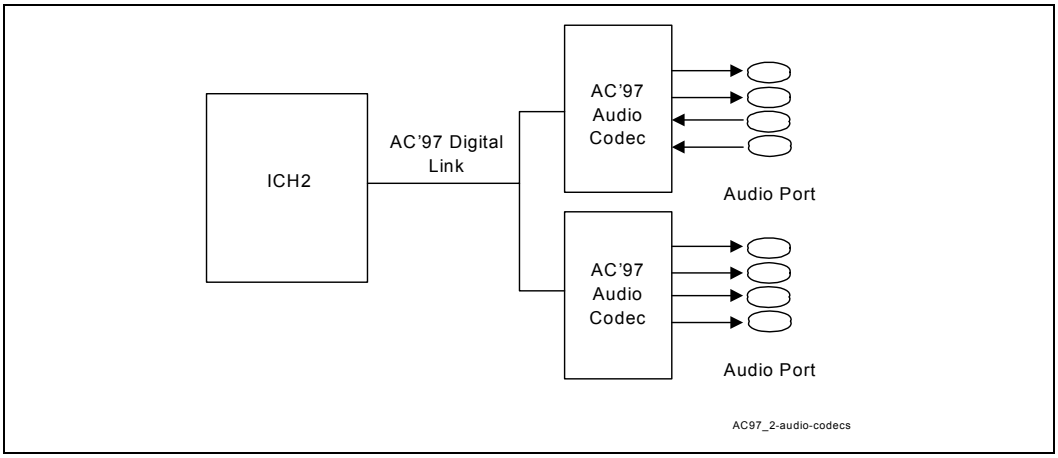
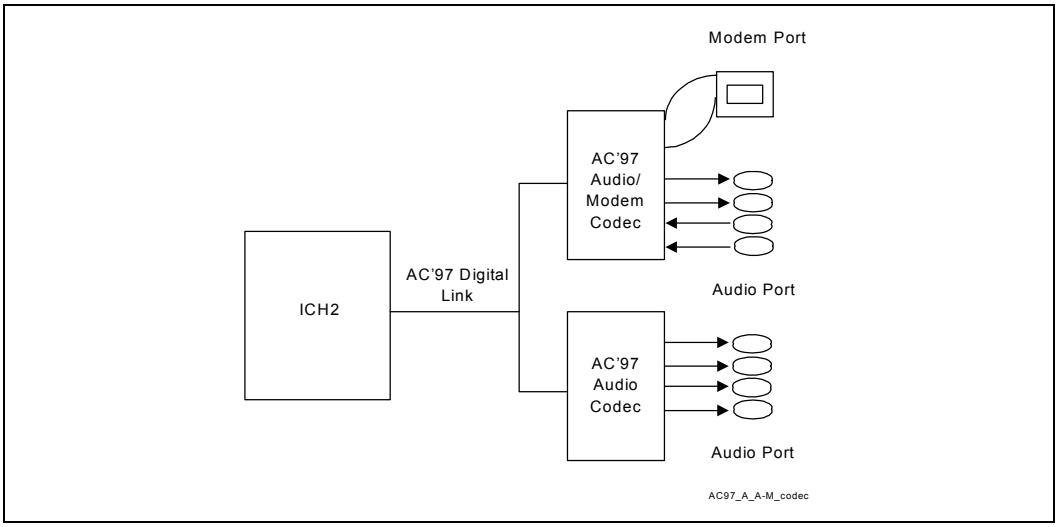


Figure 99. Audio and Audio/Modem Codecs



The AC'97 interface can be routed using 5 mil traces with 5 mil space between the traces. Maximum length between ICH2 to CODEC/CNR is 14 inches in a tee topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4 inches for the AC-link. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$

Intel has developed an advanced common connector for both AC'97 as well as networking options. This is known as the Communication Network Riser (CNR).

Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH2), and any other codec present. That clock is used as the timebase for latching and driving data.

The ICH2 supports wake on ring from S1-S5 via the AC-link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH2 has weak pull-downs/pull-ups that are only enabled when the AC-Link Shut Off bit in the ICH2 is set. This will keep the link from floating when the AC-link is off, or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, the codec and ICH2 will drive BITCLK and AC_SDOUT, respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec. If there is one or no CODEC onboard, then the unused AC_SDINx pin(s) should have a weak (10 kΩ) pull-down to keep it from floating.

Table 33. Intel® AC'97 SDIN Pull-down Resistors

System Solution	Pull-up Requirements
On-board Codec Only	Pull-down the SDIN pin that is NOT connected to the codec
AMR Only	Pull-down BOTH SDIN pins
BOTH AMR and On-board Codec	Pull-down any SDIN pin that could be NC*

NOTE: If the on-board codec can be disabled, both SDIN pins must have pull-downs. If the on-board codec can not be disabled, only the SDIN not connected to the on-board codec requires a pull-down.

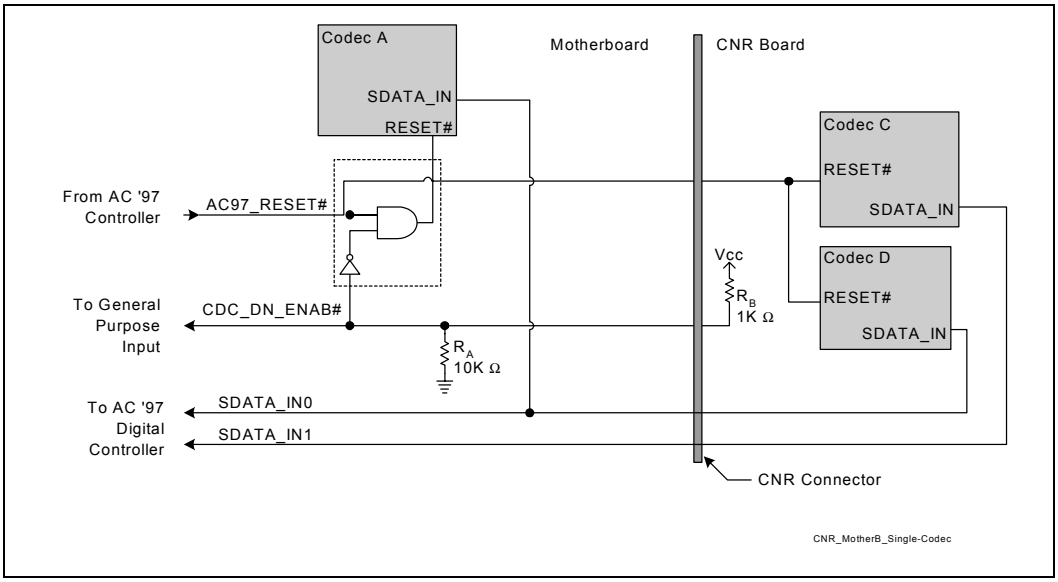
9.3.1 AC'97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Refer to Intel's White Paper *Recommendations for ICHx/AC'97 Audio (Motherboard and Communication and Network Riser)* for Intel's recommended codec configurations.

To support more than two channels of audio output, the ICH2 allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC'97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

The following circuits (Figure 100 through Figure 103) show the adaptability of a system with the modification of R_A and R_B combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration and allows the configuration of the link to be determined by the BIOS so that the correct PnP IDs can be loaded.

Figure 100. CDC_DN_ENAB# Support Circuitry for a Single Codec Motherboard



As shown in Figure 100 when a single codec is located on the motherboard, the resistor R_A and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented, on the motherboard. This circuitry is required in order to disable the motherboard codec when a CNR is installed which contains two AC ’97 codecs (or a single AC ’97 codec which must be the primary codec on the AC-link).

By installing resistor R_B (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset) and the codec(s) on the CNR take control of the AC-link. One possible example of using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

The architecture shown in Figure 101 has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor R_B on the CNR to 100 kΩ). An example of one such upgrade is increasing from two-channel to four or six-channel audio.

Both Figure 101 and Figure 102 show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_INn line as to not conflict with the motherboard codec(s).

Figure 101. CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade

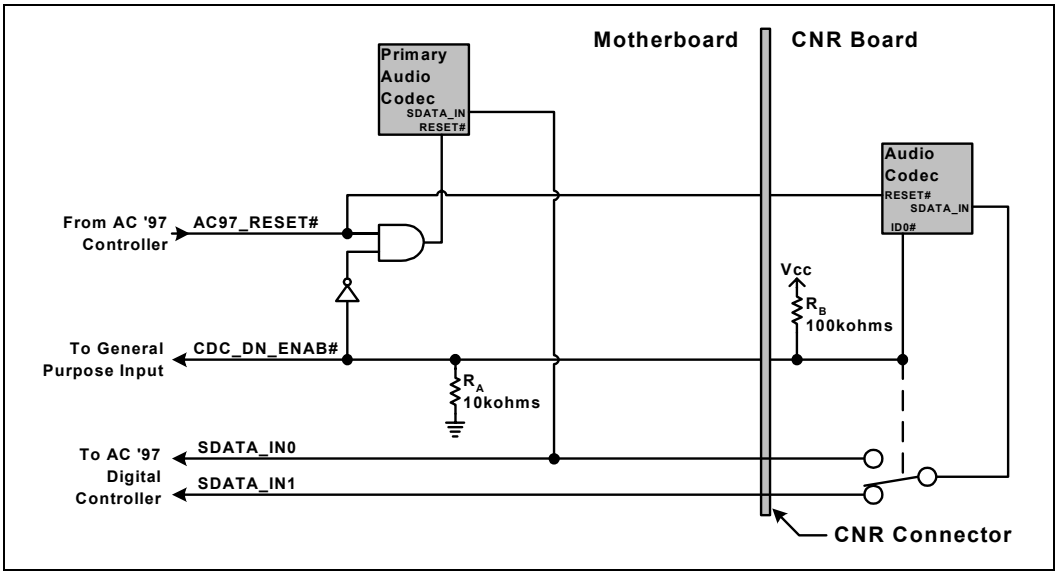


Figure 102 shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration the resistor, R_B, has been changed to 100 kΩ.

Figure 102. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / One-Codec on CNR

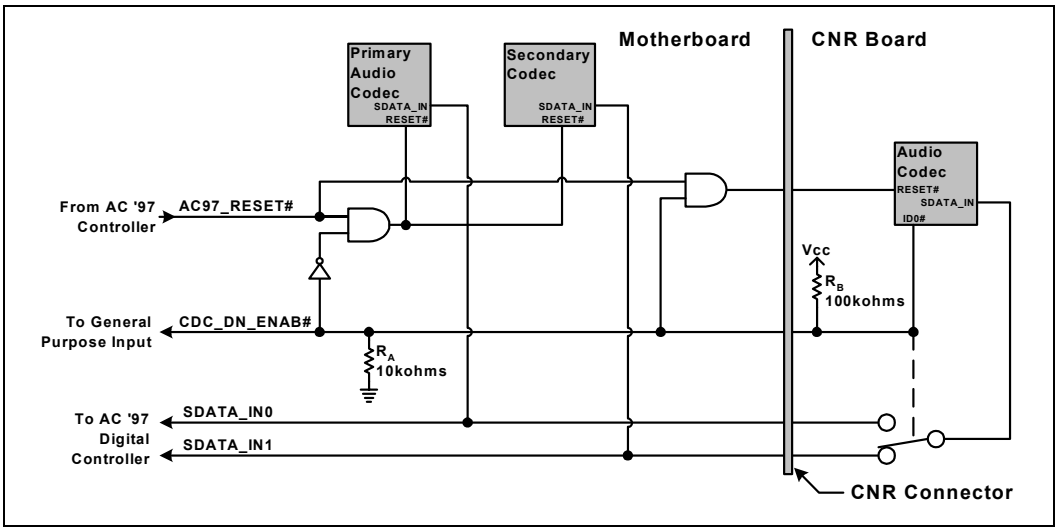
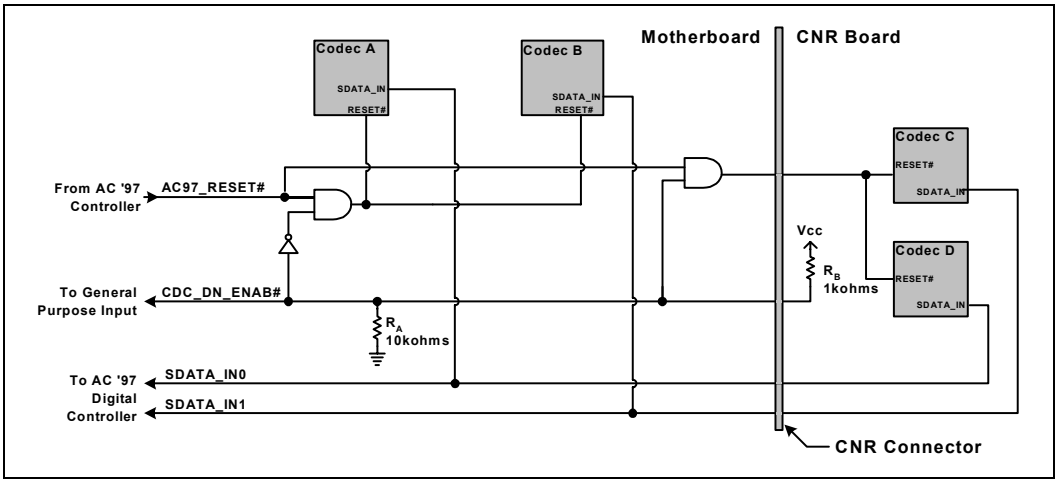


Figure 103 shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by R_A being 10 kΩ and R_B being 1 kΩ.

Figure 103. CDC_DN_ENAB# Support for Two-Codecs on Motherboard / Two-Codecs on CNR



Circuit Notes

- All CNR designs include resistor R_B. The value of R_B is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
- Any CNR with two codecs must implement R_B with value 1 kΩ. If there is one Codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff R_B. If implemented, R_B must be connected to the same power well as the codec so that it is valid whenever the codec has power.
- A motherboard with one or more codecs down must implement R_A with a value of 10 kΩ.
- The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is *required* to be connected to a GPI; a connection to a GPIO is *strongly recommended* for testing purposes.

Table 34. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC '97 Interface.
AC97_RESET#	Reset signal from the AC '97 Digital Controller (ICH2).
SDATA_INn	AC '97 serial data from an AC '97-compliant codec to an AC '97-compliant controller (i.e., the ICH2).

9.3.2 Valid Codec Configurations

Table 35. Codec Configurations

Valid Codec Configurations
AC(Primary)
MC(Primary)
AMC(Primary)
AC(Primary) + MC(Secondary)
AC(Primary) + AC(Secondary)
AC(Primary) + AMC(Secondary)

Invalid Codec Configurations
MC(Primary) + X(any other type of codec)
AMC(Primary) + AMC(Secondary)
AMC(Primary) + MC(Secondary)

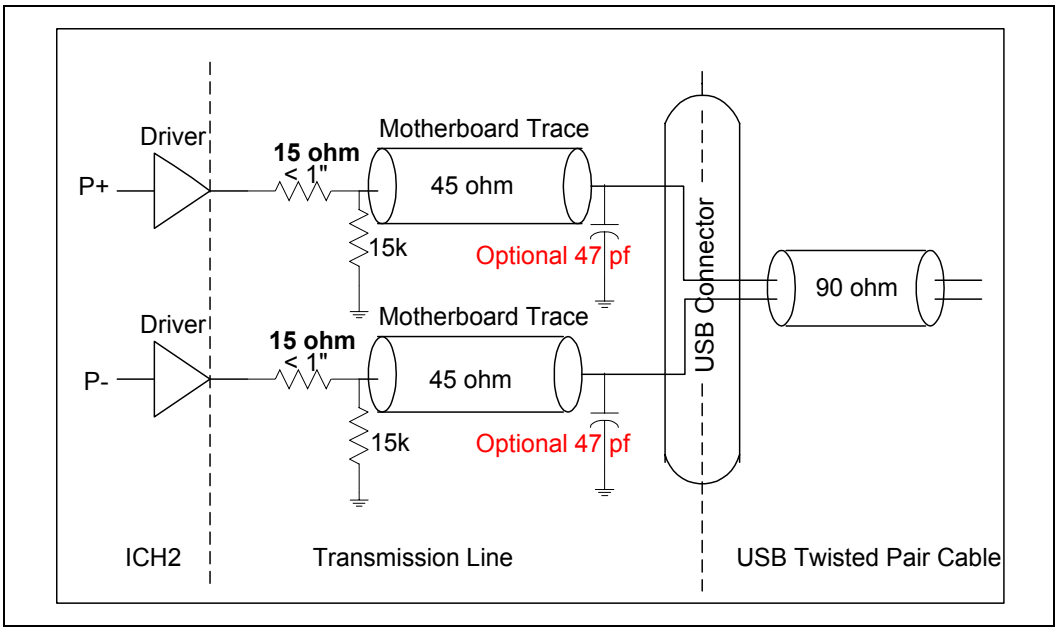
9.4 USB Guidelines

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both P+/P- data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH2 (<1 inch). These series resistors are required for source termination of the reflected signal.
- Optional 47 pF capacitors must be placed as close to the ICH2 as possible and on the ICH2 side of the series resistors on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). These capacitors are there for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kΩ ±5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0+/- … P3+/-), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0+/-… P3+/- signals should be 45 Ω (to ground) for each USB signal P+ or P-. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90 Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting 45-Ω impedance. The trace impedance can be controlled by carefully selecting the line width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. Lastly, do not route over plane splits.

Figure 104 illustrates the recommended USB schematic:

Figure 104. USB Data Signals



The following are Recommended USB Trace Characteristics.

- Impedance 'Z0' = 45.4 Ω
- Line Delay = 160.2 ps
- Capacitance = 3.5 pF
- Inductance = 7.3 nH
- Res @ 20° C = 53.9 m Ω

9.5 IOAPIC Design Recommendations

The IOAPIC bus is not required in these designs.

- Processor:
  - The processor does not have these pins defined. It receives interrupts for servicing via the System Bus interrupt delivery mechanism.
- On the ICH2
  - Tie PICCLK directly to ground
  - Tie PICD0, PICD1 to ground via 1 k Ω to 10 kΩ resistor

9.6 SMBus/SMLink Interface

The SMBus interface on the ICH2 is the same as that on the ICH2. It uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH2. If the SMBus is used only for the RAMBUS SPD EEPROMs (one on each RIMM connector), both signals should be pulled up with a 4.7 kΩ resistor to 3.3 V.

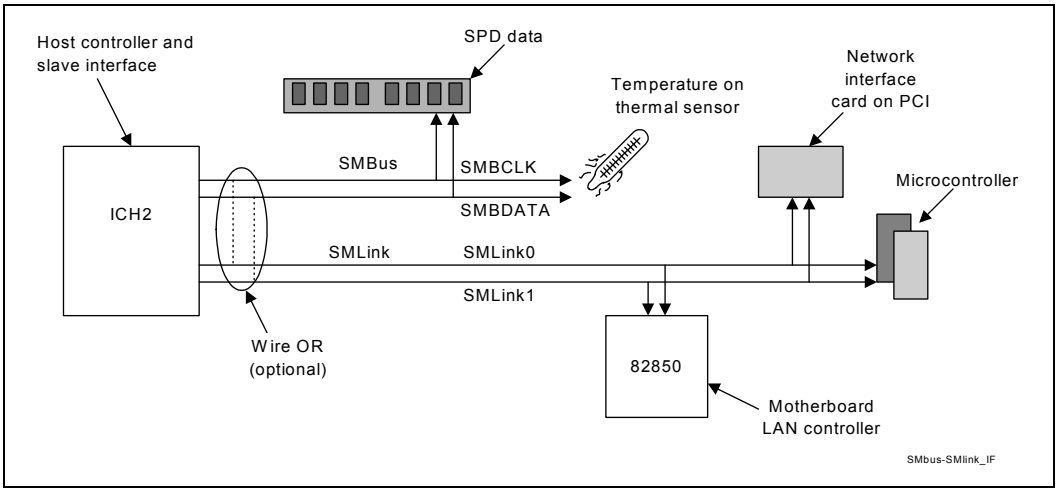
The ICH2 incorporates a new SMLink interface supporting AOL*, AOL2* and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. Internally the SMLINK signals are connected to the following:

- ICH2 Slave Interface
- ICH2 TCO Host Controller
- ICH2 Integrated LAN Slave Interface

For Alert on LAN* (AOL*) functionality, the TCO Host Controller transmits heartbeat and event messages over the interface. When using the 82562EM LAN Connect Component, the ICH2's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, AOL2-enabled LAN Controller (i.e., 82550) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH2 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the TCO Host Controller obey the SMBus protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (e.g., 82550) to access targets on the SMBus as well as the ICH2 Slave interface. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA. See Figure 105.

Figure 105. SMBUS/SMLink Interface



Note: Intel does not support external access of the ICH2's Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH2's SMBus Slave Interface by the ICH2's SMBUS Host Controller.

Refer to the *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

9.6.1 SMBus Architecture and Design Considerations

9.6.1.1 SMBus Design Considerations

There are several possibilities for designing a SMBus using the ICH2. Designs can be grouped into three major categories based on the power supply source for the SMBus microcontrollers. This includes two unified designs, where all devices are powered by either VCC_Core or VCC_Suspend, and a mixed design where some devices are powered by each of the two supplies.

Primary considerations in choosing a design are based on:

- Are there devices that must run in STR?
- Amount of VCC_Suspend current available, i.e. minimizing load of VCC_Suspend

9.6.1.2 General Design Issues / Notes

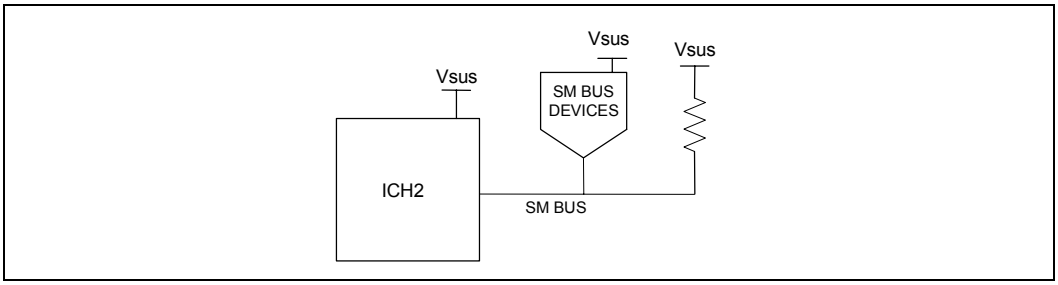
Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the number of devices present on the bus. A typical value is 8.2k ohms. This should prevent the SMBus signals from floating, which could cause leakage in the ICH2 and other devices.
- RIMM modules have a separate power source from the RDRAM device array for the SPD device. If this SPD device needs to operate in STR, then it should be connected to the VCC_Suspend supply.
- The ICH2 does not run SMBus cycles while in STR.
- SMBus devices that can operate in STR must be powered by the VCC_Suspend supply.

9.6.1.3 The Unified VCC_ Suspend Architecture

In this design all SMBus devices are powered by the VCC_Suspend supply. Consideration must be made to provide enough VCC_Suspend current while in STR.

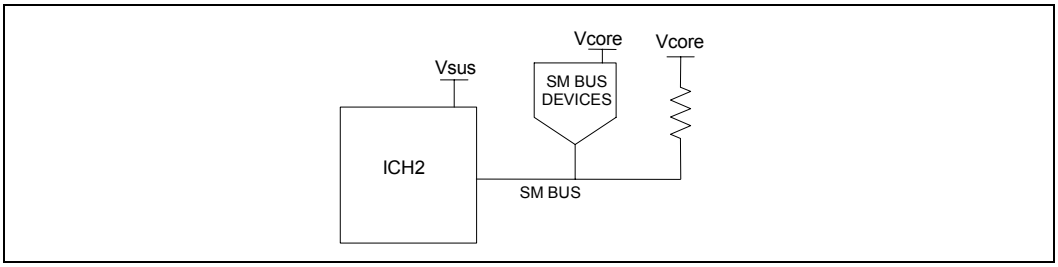
Figure 106. Unified VCC_Suspend Architecture



9.6.1.4 The Unified VCC_Core Architecture

In this design, all SMBUS devices are powered by the VCC_Core supply. This architecture allows none of the devices to operate in STR, but minimizes the load on VCC_Suspend. See Figure 107.

Figure 107. Unified VCC_Core Architecture



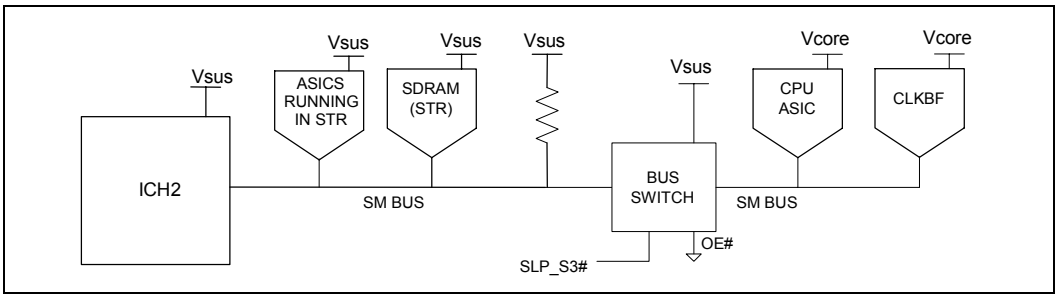
NOTES:

1. The SMBus device needs to be back-drive safe while its supply (Vcore) is off and VCC_Suspend is still powered.
2. In suspended modes where VCC_Core is OFF and VCC_Suspend is on, the VCC_Core node will be very near ground. In this case the input leakage of the ICH2 will be approximately 10 uA.

9.6.1.5 Mixed Architecture

This design allows for SMBus devices to communicate while in STR, yet minimizes VCC_Suspend leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a “bus switch” to isolate the devices powered by the core and suspend supplies. See Figure 108.

Figure 108. Mixed VCC_Suspend/VCC_Core Architecture



Added Considerations for Mixed Architecture:

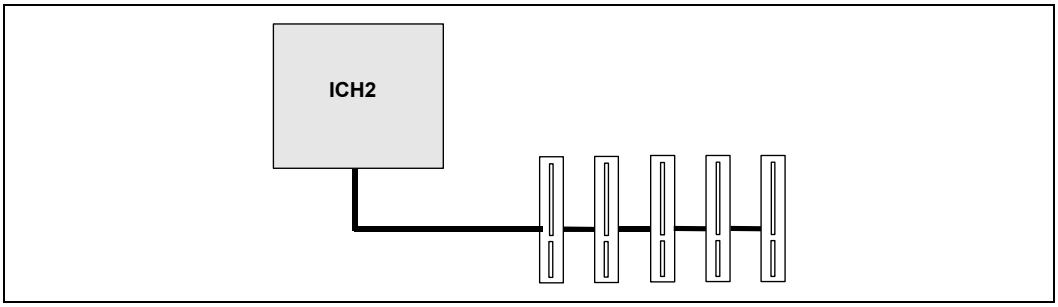
- The bus switch must be powered by VCC_Suspend
- If there are 5 V SMBus devices used, then an added level translator must be used to separate those devices driving 5 V from those driving 3 V signal levels.
- Devices that are powered by the VCC_Suspend well must not drive into other devices that are powered off. This is accomplished with the “bus switch”.

9.7 PCI

The ICH2 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH2 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

The ICH2 supports six PCI Bus masters (excluding the ICH2), by providing six REQ#/GNT# pairs. In addition, the ICH2 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 109. PCI Bus Layout Example



9.7.1 PCI Routing – Four-Layer Motherboard

PCI signals are routed with 5mil trace width and 5mil trace to trace spacing. The PCI signals are routed on the bottom side of the boards and should be referenced to VCC3.3. Minimize the number of PCI signals that cross power splits.

Figure 110. Example PCI Power Planes on Layer 2

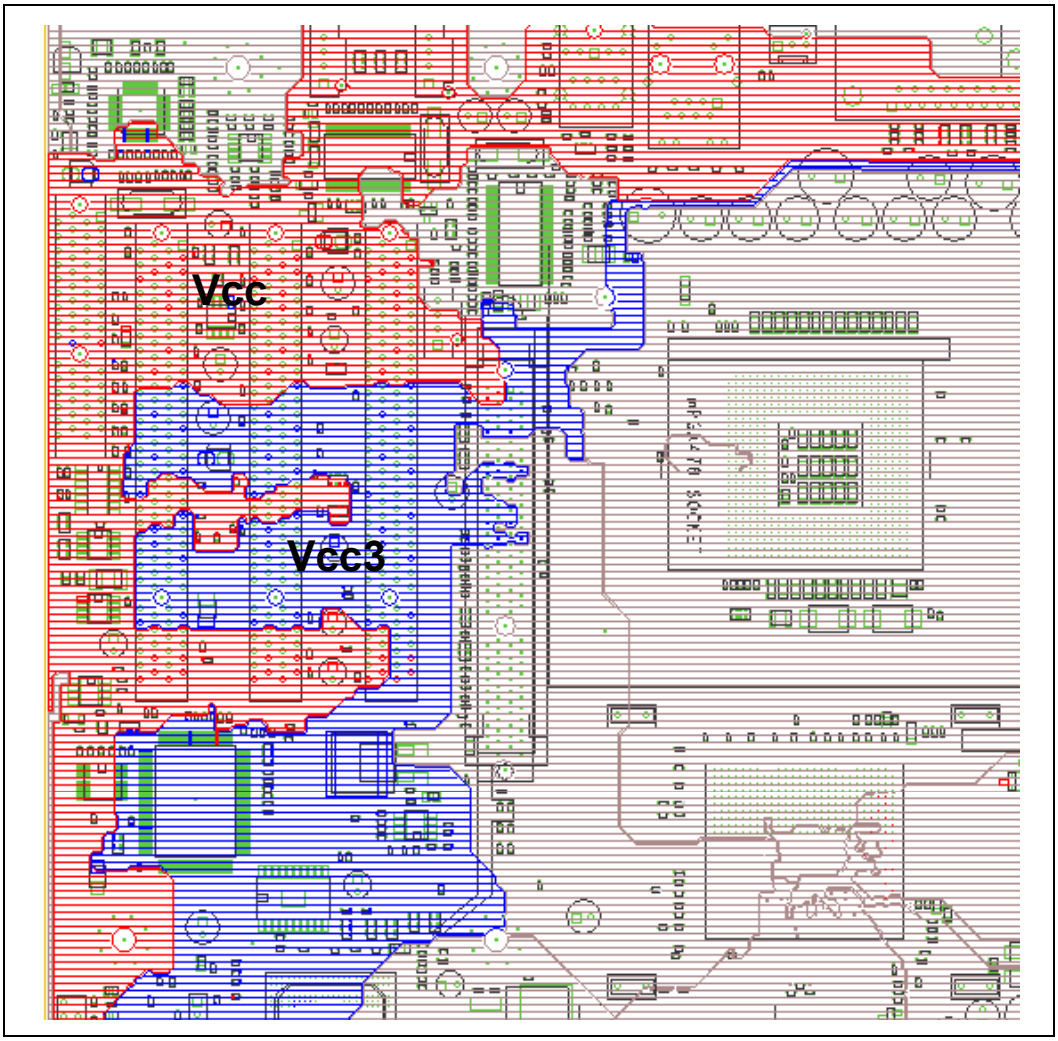


Figure 111. Example PCI Routing on Layer 1

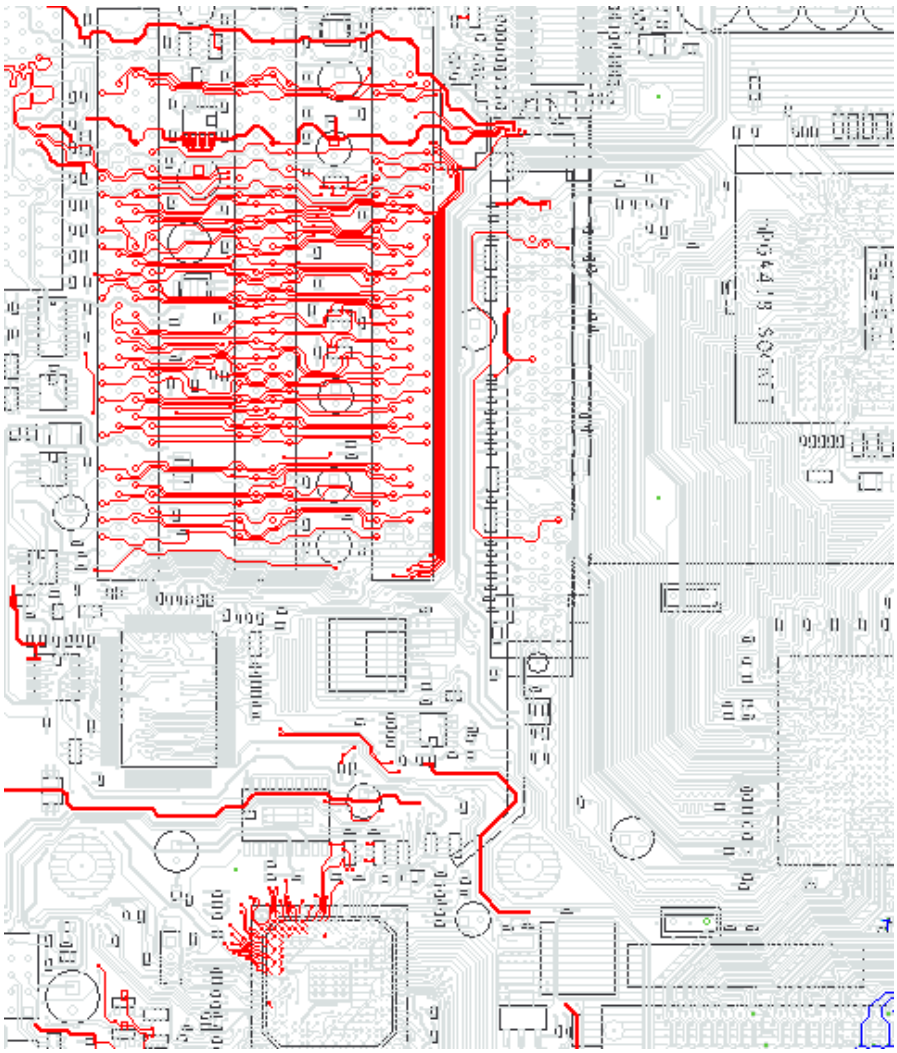
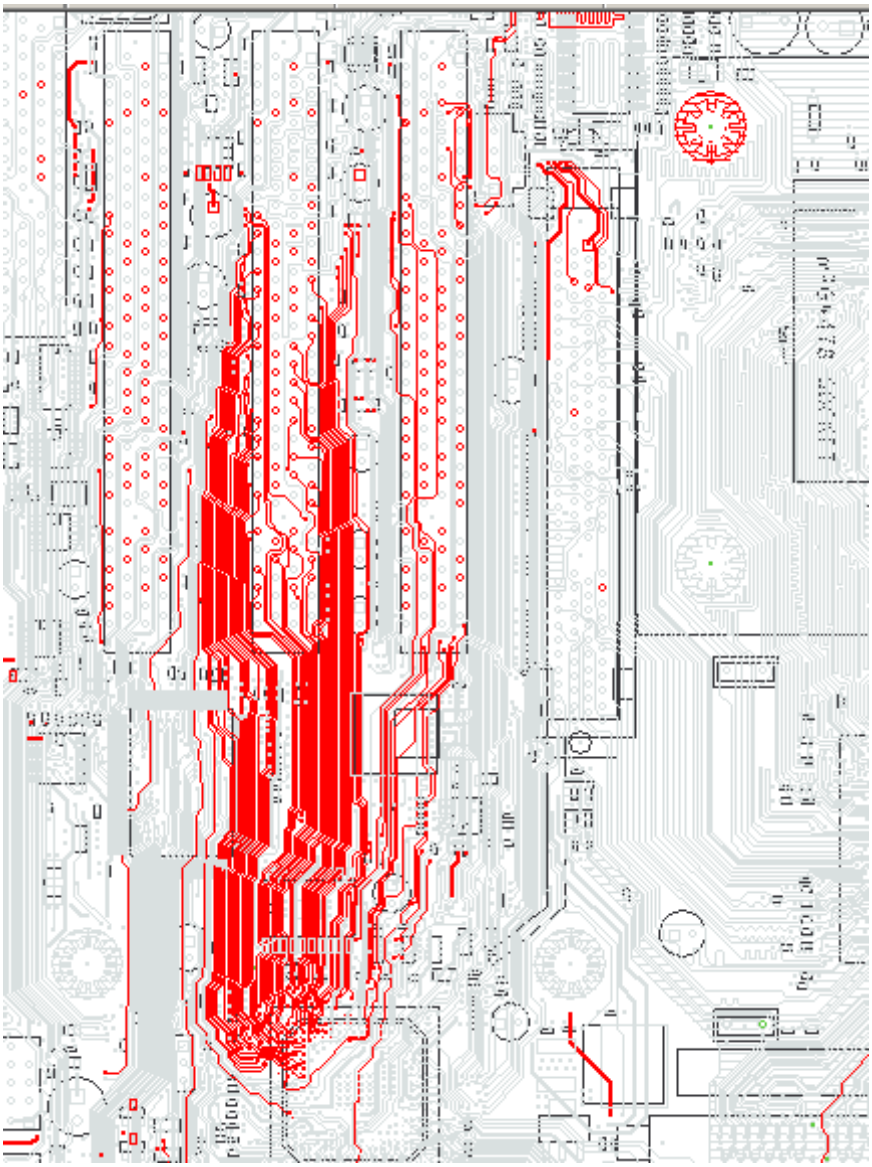


Figure 112. Example PCI Routing on Layer 4



9.8 RTC

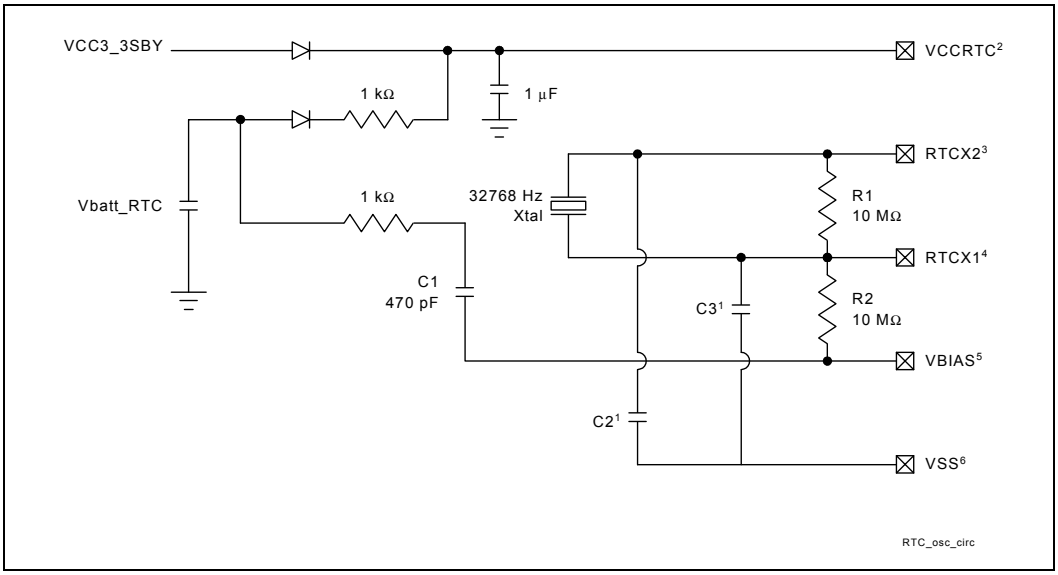
The ICH2 contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

This section will present the recommended hookup for the RTC circuit for the ICH2. **This circuit is not the same as the circuit used for the PIIX4.**

9.8.1 RTC Crystal

The ICH2 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins. Figure 113 shows the external circuitry that comprises the oscillator of the ICH2 RTC.

Figure 113. External Circuitry for the Intel® ICH2 RTC



NOTES:

1. The exact capacitor value needs to based on what the crystal maker recommends.
2. V_{CC} RTC: Power for RTC Well
3. RTCX2: Crystal Input 2 – Connected to the 32.768 kHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current that is mirrored throughout the oscillator and buffer circuitry.
6. VSS: Ground

9.8.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C1 needs to be 0.047 µF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC will be.

Equation 9-1 can be used to choose the external capacitance values (C2 and C3):

Equation 9-1. External Capacitance Values

$$C_{LOAD} = (C_2 * C_3)/(C_2+C_3) + C_{PARASITIC}$$

Note: C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain the 32.768 kHz.

9.8.3 RTC Layout Considerations

- Keep the RTC lead lengths as short as possible; around ¼ inch is sufficient.
- Minimize the capacitance between X_{IN} and X_{OUT} in the routing.
- Put a ground plane under the XTAL components.
- Do not route switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean; use a filter, such as a RC lowpass, or a ferrite inductor.

9.8.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH2 is not powered by the system.

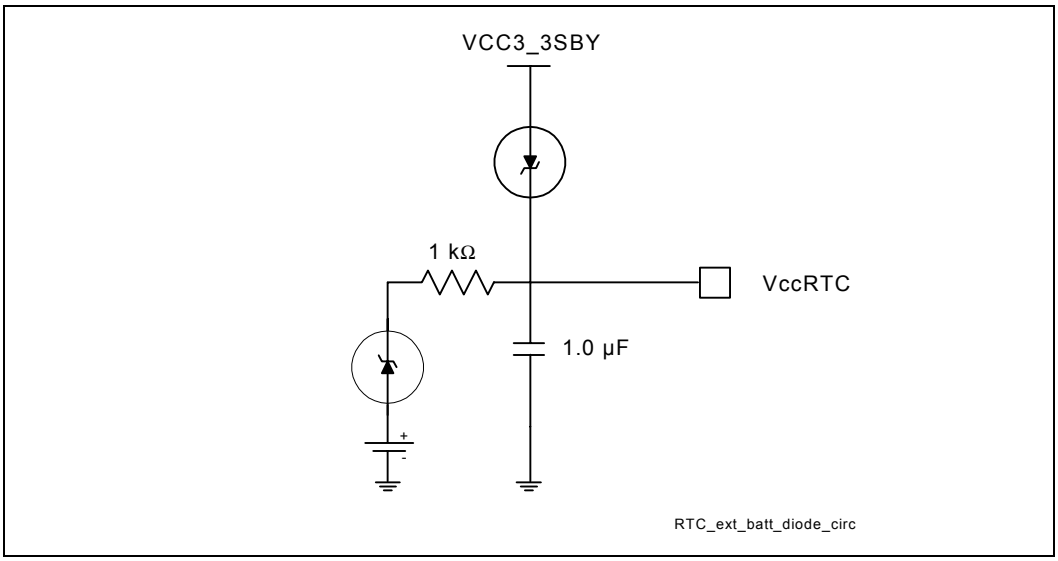
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 uA, the battery life will be at least:

170,000 uAh / 3 uA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0v to 3.3v.

The battery must be connected to the ICH2 via an isolation schottky diode circuit. The Schottky diode circuit allows the ICH2 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 114 is an example of a diode circuitry that is used.

Figure 114. Diode Circuit to Connect RTC External Battery



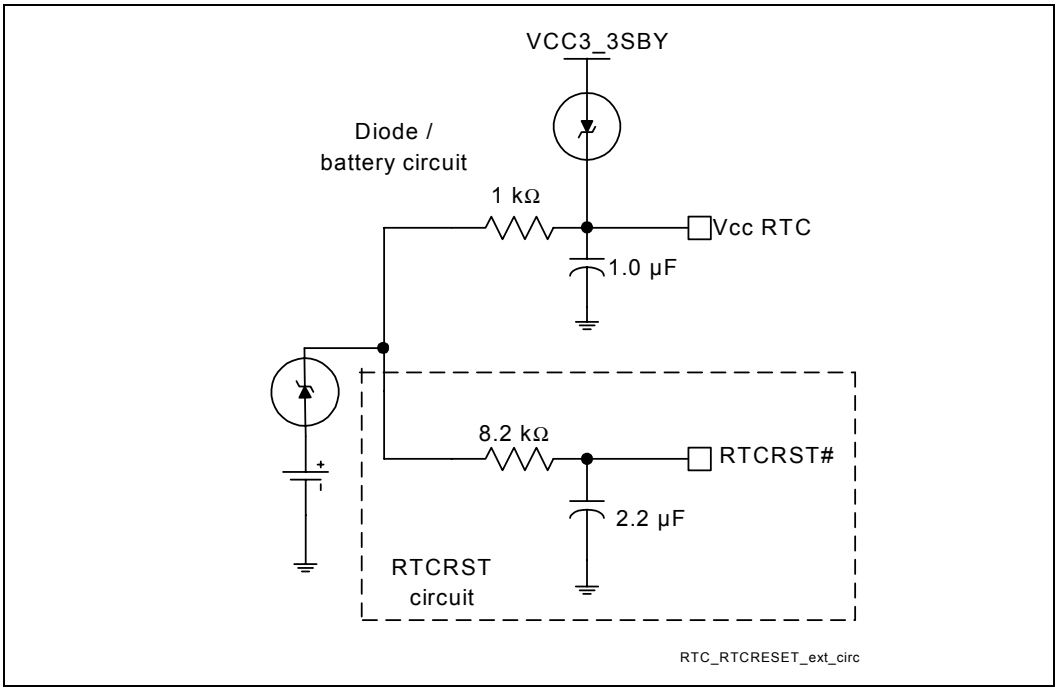
A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

9.8.5 RTC External RTCRST Circuit

The ICH2 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10-20ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (Figure 114) which allows the RTC well to be powered by the battery when the system power is not available. Figure 115 is an example of this circuitry that is used in conjunction with the external diode circuit.

Figure 115. RTCRST External Circuit for the Intel® ICH2 RTC



9.8.6 RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1 inch, the shorter the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them).
- Put a ground plane under all of the external RTC circuitry.
- Do not route any switching signals under the external components (unless on the other side of the ground plane).

9.8.7 VBIAS DC Voltage and Noise Measurements

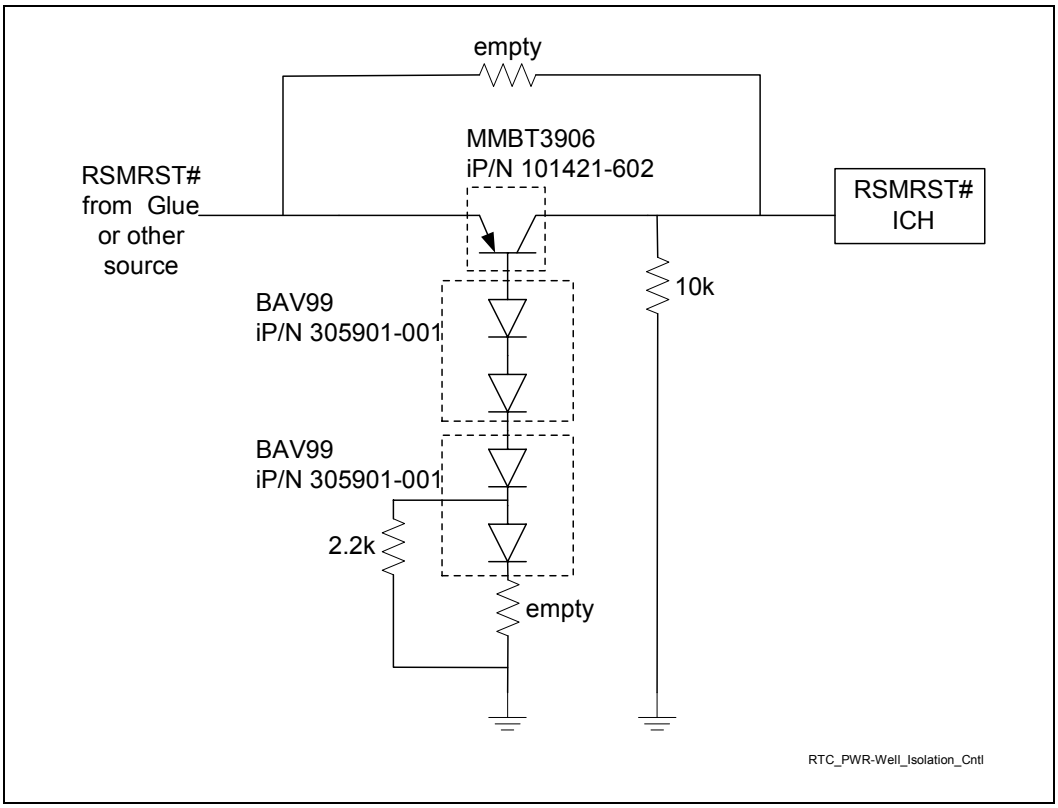
- Steady state VBIAS will be a DC voltage of about 0.38 V ±0.06 V
- VBIAS will be “kicked” when the battery is inserted to about 0.7–1.0 V, but it will come back to its DC value within a few ms
- Noise on VBIAS must be kept to a minimum, 200 mV or less.
- VBIAS is very sensitive and cannot be directly probed, it can be probed through a 0.01 µF capacitor.
- Excess noise on VBIAS can cause the ICH2 internal oscillator to misbehave or even stop completely.
- To minimize noise of VBIAS It is necessary to implement the routing guidelines described above and the required external RTC circuitry as described in the *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet.*

9.8.8 Power-Well Isolation Control

The RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 116 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

The circuit shown in Figure 116 below should be implemented to control well isolation between the 3.3 V resume and RTC power-wells. Failure to implement this circuit may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power).

Figure 116. RTC Power-Well Isolation Control



9.8.9 Power Supply PS_ON Consideration

- If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10–100 ms) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.
- The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).
- The platform designer must ensure that the power supply used with the platform is not affected by this issue.

9.9 LAN Layout Guidelines

The ICH2 provides several options for integrated LAN capability. The platform supports several components depending on the target market. These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

Table 36. Integrated LAN Options

LAN Connect Component	Connection	Features
82562EM	Advanced 10/100 Ethernet	AOL* & Ethernet 10/100 Connection
82562ET	10/100 Ethernet	Ethernet 10/100 Connection
82562EH	1Mb HomePNA* LAN	1Mb HomePNA* connection

Intel developed a dual footprint for 82562ET and 82562EH to minimize the required number of board builds. A single layout with the specified dual footprint will allow the OEM to install the appropriate LAN connect component to meet the market need. Design guidelines are provided for each required interface and connection. Refer to Figure 117 and Table 37. LAN Design Guide Section Reference.

Figure 117. Intel® ICH2 / LAN Connect Section

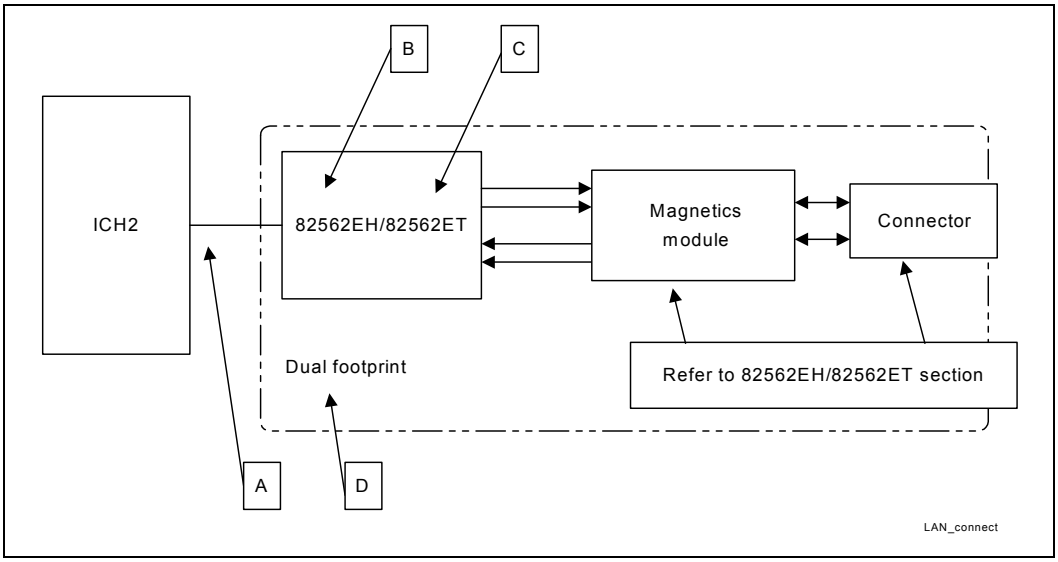


Table 37. LAN Design Guide Section Reference

Layout Section	Figure 117	Design Guide Section
ICH2 – LAN Interconnect	A	9.9.1 ICH2 – LAN Interconnect Guidelines
General Routing Guidelines	B,C,D	9.9.2 General LAN Routing Guidelines and Considerations
82562EH	B	9.9.3 Intel® 82562EH Home/PNA* Guidelines
82562ET /82562EM	C	9.9.4 Intel® 82562ET / 82562EM Guidelines
Dual Layout Footprint	D	9.9.6 82562ET / 82562EH Dual Footprint Guidelines

9.9.1 Intel® ICH2 – LAN Interconnect Guidelines

This section contains guidelines to the design of motherboards and riser cards to comply with LAN Connect. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the **LAN_CLK** traces to those of the other signals, as shown below. The following are guidelines for the ICH2 to LAN component interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports both 82562EH and 82562ET/82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by both components. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when 82562EH is installed Dual footprint guidelines are described in Section 9.9.6.

9.9.1.1 Bus Topologies

The LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH2 and the LAN component
- Dual Footprint (See Section 9.9.6)
- LOM/CNR Implementation

9.9.1.2 Point-to-Point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EH, 82562ET, or CNR are installed.

Figure 118. Single Solution Interconnect

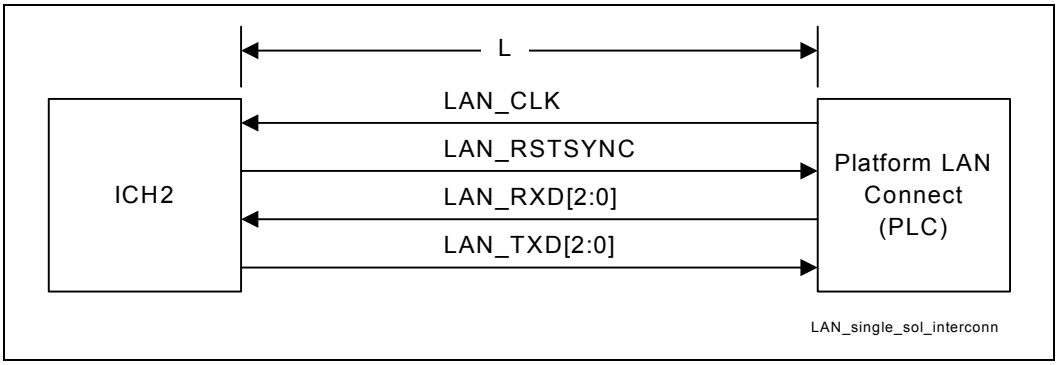


Table 38. Length Requirements for Single Solution Interconnect

Component	Minimum (inches)	Maximum (inches)	Notes
82562EH	L=4.5	L=10	Signal Lines LAN_RXD[2:1] and LAN_TXD[2:1] not connected
82562ET	L=3.5	L=10	
CNR	L=3	L=9	

NOTE: Length of trace from connector to LOM should be 0.5 to 3 inches.

9.9.1.3 LOM/CNR Interconnect

The following guidelines allow for an all inclusive motherboard solution. This layout combines LOM, dual footprint, and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on motherboard option can be implemented at one time. The recommended trace routing lengths are shown in Figure 119. LOM/CNR Interconnect.

Figure 119. LOM/CNR Interconnect

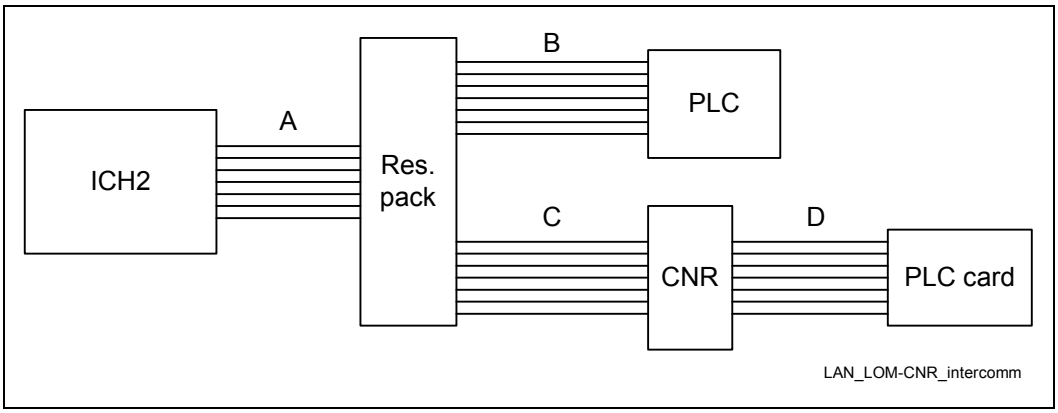


Table 39. Length Requirements for LOM/CNR Interconnect

Configuration	Segment A (inches)	Segment B (inches)	Segment C (inches)	Segment D (inches)
82562EH	0.5 to 6.0	4 to 10 - A	—	—
82562ET	0.5 to 7	3 to 10 - A	—	—
Dual Footprint	0.5 to 6	4 to 10 – A	—	—
82562ET/EH Card [1]	0.5 to 6.5	—	2.5 to 9 – A	0.5 to 3

NOTES: [1]Total trace length should not exceed 13 inches.

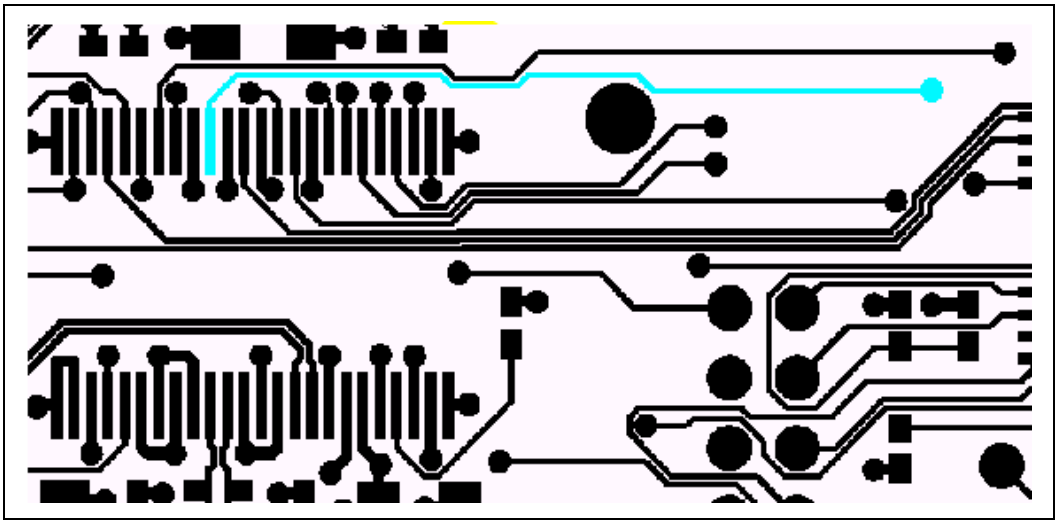
Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 Ω or 22 Ω.
- LAN on motherboard PLC can be a dual footprint configuration.

9.9.1.4 Signal Routing and Layout

LAN Connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 120. LAN_CLK Routing Example



9.9.1.5 Crosstalk Considerations

Noise due to crosstalk must be minimized. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter.

9.9.1.6 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ±15% is strongly recommended; otherwise, signal integrity requirements may be violated.

9.9.1.7 Line Termination

Line termination mechanisms are not specified for the LAN Connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

9.9.2 General LAN Routing Guidelines and Considerations

9.9.2.1 General Trace Routing Considerations

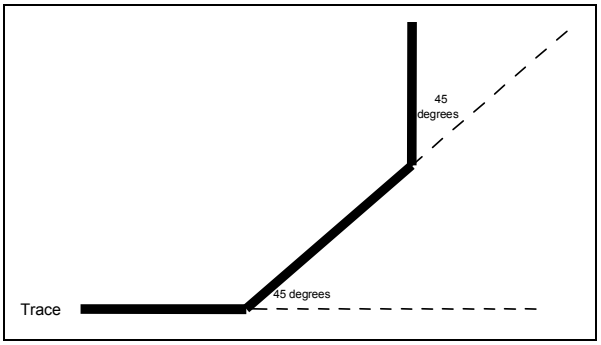
Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance:

Note: Some suggestions are specific to a 4.5 mil stack-up.

- Maximum mismatch between the length of the clock trace and the length of any data trace is 0.5 inches.
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER.]
- Do not route the transmit differential traces closer than 70 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 70 mils to the differential traces.
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 121.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 121. Trace Routing



9.9.2.1.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 0.030 inches (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/ magnetics/ edge of the board.

9.9.2.1.2 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 70 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

9.9.2.2 Power and Ground Connections

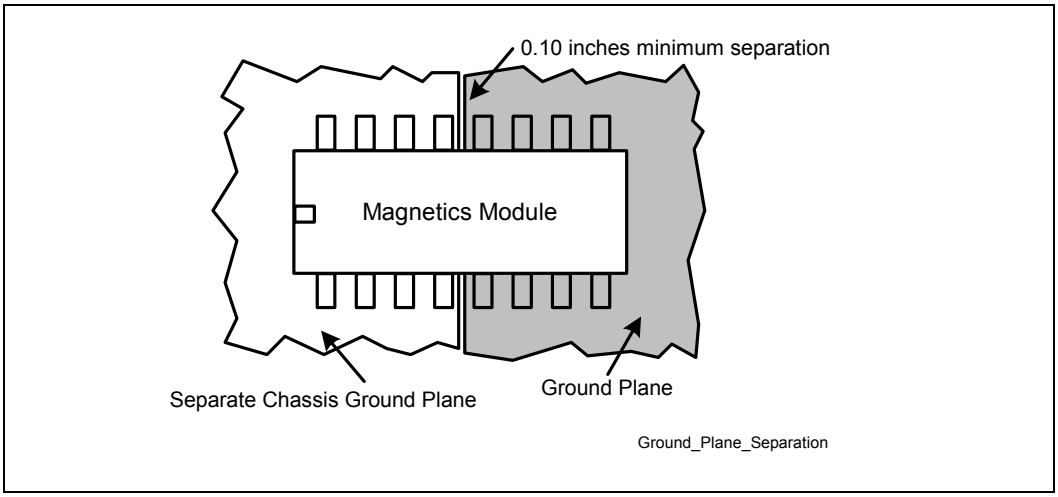
Some rules and guidelines to follow for power and ground connections:

- All VCC pins should be connected to the same power supply.
- All VSS pins should be connected to the same ground plane.
- Use one decoupling capacitor per power pin for optimized performance.
- Place decoupling as close as possible to power pins.

9.9.2.2.1 General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 122. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both backplanes and motherboards.

- *Route traces over a continuous plane with no interruptions (do not route over a split plane).* If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- *Separate noisy digital grounds from analog grounds to reduce coupling.*
- Noisy digital grounds may effect sensitive DC subsystems.
- *All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential.* This helps reduce circuit inductance.
- *Physically locate grounds between a signal path and its return.* This will minimize the loop area.
- *Avoid fast rise/fall times as much as possible.* Signals with fast rise and fall times contain many high frequency harmonics , which can radiate EMI.
- *The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it.* By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.
- *Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.6 mm (59.0 mil).* This is a ***critical*** requirement needed to past FCC part 68 testing for phoneline connection. Note: For worldwide certification, a trench of 2.5 mm is required. In North America, the spacing requirements is 1.6mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5 mm spacing.

9.9.2.3 Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. [Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.] Asymmetry can create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (less than or equal to one inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.

5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45/11, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or Application Note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. [To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close† to each other the edge coupling can lower the effective differential impedance by 5 to 20 Ω. A 10 to 15 Ω drop in impedance is common.] Short traces will have fewer problems if the differential impedance is a little off.
10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a capacitor is put in either of these locations. If a capacitor is used, it should almost certainly be less than 22 pF. [6 pF to 12 pF values have been used on past designs with reasonably good success.] These capacitors are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close† to each other. Keeping them close† helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces. † Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.008 inch to 0.012 inch trace-to-trace spacing is recommended.

9.9.3 Intel® 82562EH Home/PNA* Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.9.2. Additional guidelines for implementing an 82562EH Home/PNA* LAN connect component are provided below.

9.9.3.1 Power and Ground Connections

Some rules to follow for power and ground connections:

- For best performance place decoupling capacitors on the backside of the PCB directly under the 82562EH with equal distance from both pins of the capacitor to power/ground.

The analog power supply pins for 82562EH (VCCA, VSSA) should be isolated from the digital VCC and VSS through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between VCC and VSS, and VCCA and VSSA power supplies.

9.9.3.2 Guidelines for Intel® 82562EH Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the HomePNA* LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA* LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.9.3.3 Crystals and Oscillators

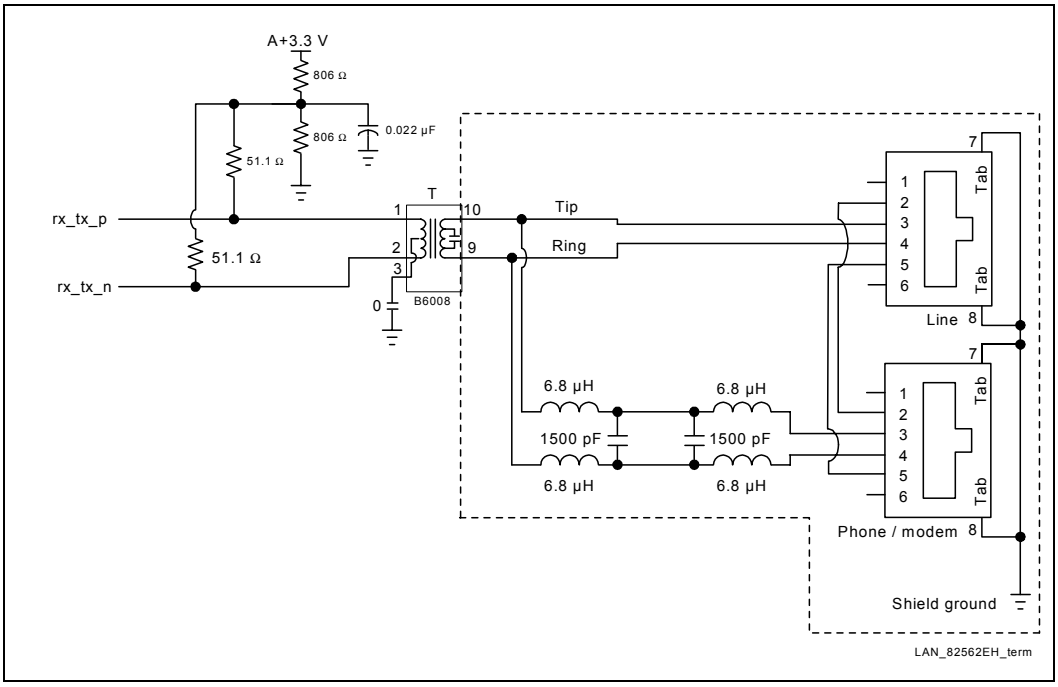
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the *HomePNA* magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to 82562EH, keeping the length as short as possible and do not route any noisy signals in this area.

9.9.3.4 Phoneline HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1Ω (1%) resistors. This parallel termination should be placed close to the 82562EH. The center, common point between the 51.1 Ω resistors is connected to a pair of 806 Ω resistors and a single 0.022 µF capacitor. The opposite end of one 806 Ω resistor is tied to VCCA (3.3 V), and the opposite end of the other 806 Ω resistor and the capacitor are connected to ground. The termination is shown in Figure 123.

Figure 123. Intel® 82562 EH Termination



The filter and magnetics component T1, integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA* LAN interface.

One RJ-11 jack (labeled "LINE" in Figure 123) allows the node to be connected to the phoneline, and the second jack (labeled "PHONE" in Figure 123) allows other downline devices to be connected at the same time. The second connector is not required by the *HomePNA*. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter, setup in-line with the second RJ-11 jack is also recommended by the HomePNA* to minimize interference between the HomeRun connection and a POTs voice or modem connection on the second jack. This places a restriction of the type of devices connected to the second jack as the pass-band of this filter is set approximately at 1.1 MHz. Refer to the HomePNA* website: www.homepna.org for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA* certifications.

9.9.3.5 Critical Dimensions

There are three dimensions to consider during layout. Distance 'B' from the line RJ11 connector to the magnetics module, distance 'C' from the phone RJ11 to the LPF (if implemented), and distance 'A' from 82562EH to the magnetics module (See Figure 124).

Figure 124. Critical Dimensions for Component Placement

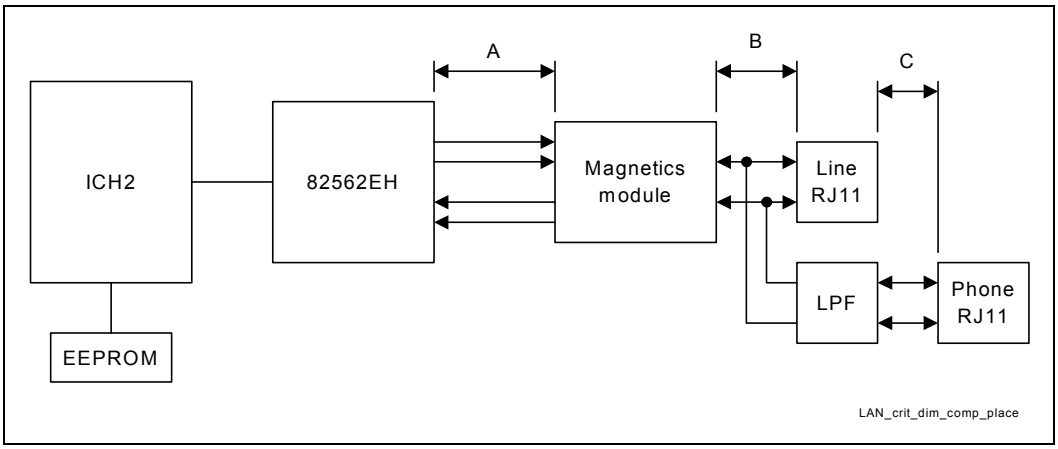


Table 40. Critical Dimension Values

Distance	Priority	Guideline
B	1	< 1 inch
A	2	< 1 inch
C	3	< 1 inch

9.9.3.5.1 Distance from Magnetics Module to Line RJ11

This distance 'B' should be given highest priority and should be less then 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

9.9.3.5.2 Distance from Intel® 82562EH to Magnetics Module

Due to the high-speed of signals present, distance 'A' between the 82562EH and the magnetics should also be less than 1 inch, but should be second priority relative to distance form connects to the magnetics module.

And in general, any section of trace that is intended for use with high-speed signals should observe proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between device and traces route. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

9.9.3.5.3 Distance from LPF to Phone RJ11

This distance 'C' should be less then 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side

9.9.4 Intel® 82562ET / 82562EM Guidelines

For correct LAN performance, designers must follow the general guidelines outlined in Section 9.9.2. Additional guidelines for implementing a 82562ET or 82562EM LAN connect component are provided below.

9.9.4.1 Guidelines for Intel® 82562ET / 82562EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.9.4.2 Crystals and Oscillators

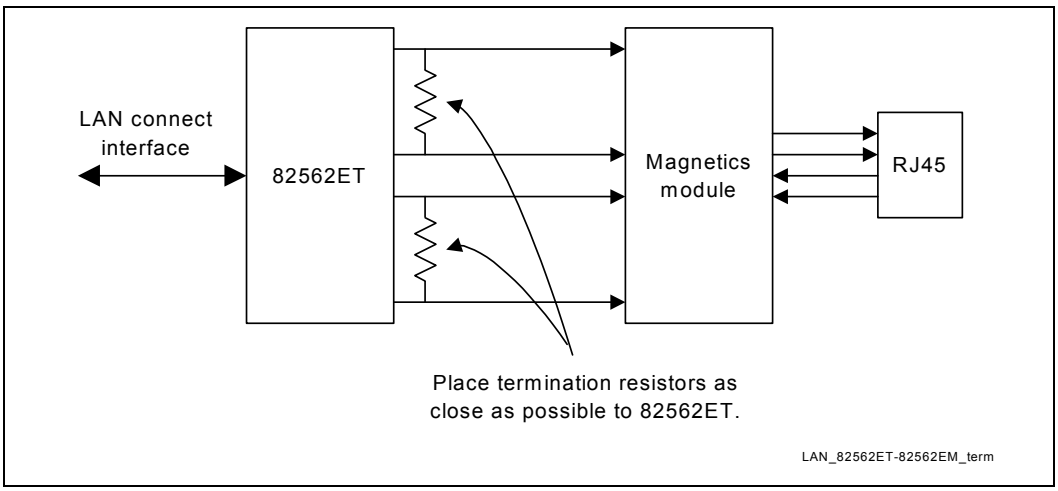
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562ET or 82562EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

9.9.4.3 Intel® 82562ET / 82562EM Termination Resistors

The 100 Ω 1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120 Ω 1% receive differential pairs (RDP/RDN) should be placed as close to the LAN connect component (82562ET or 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

Figure 125. Intel® 82562ET/ 82562EM Termination



9.9.4.4 Critical Dimensions

There are two dimensions to consider during layout. Distance ‘B’ from the line RJ45 connector to the magnetics module and distance ‘A’ from the 82562ET or 82562EM to the magnetics module (See Figure 126).

Figure 126. Critical Dimensions for Component Placement

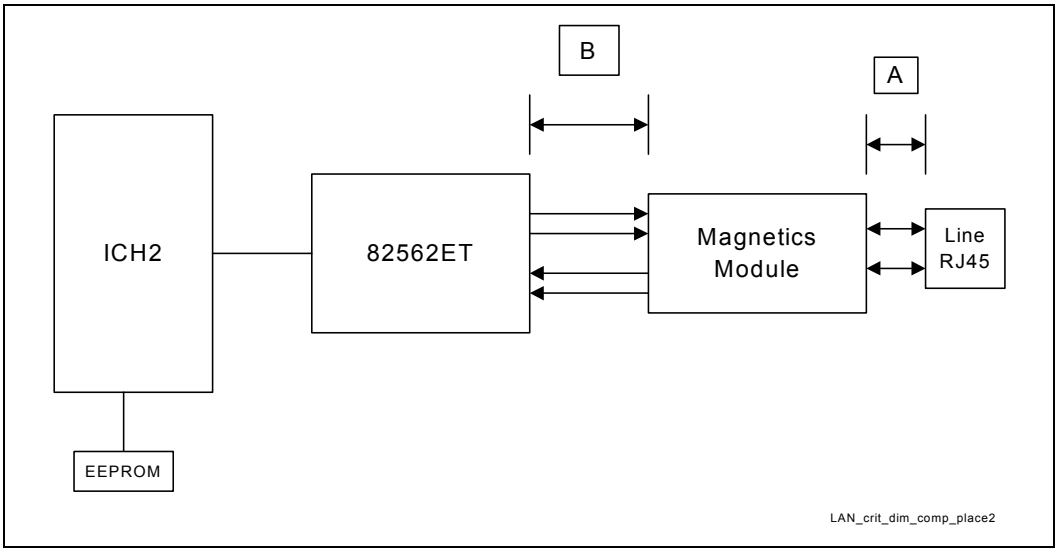


Table 41. Critical Dimension Values

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

9.9.4.4.1 Distance from Magnetics Module to RJ45

The distance A in Figure 126 above should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation.

The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 ohms. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562ET and RJ45 will as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105–110 Ω should compensate for second order effects.

9.9.4.4.2 Distance from Intel® 82562ET to Magnetics Module

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

9.9.4.5 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high frequency harmonics, that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

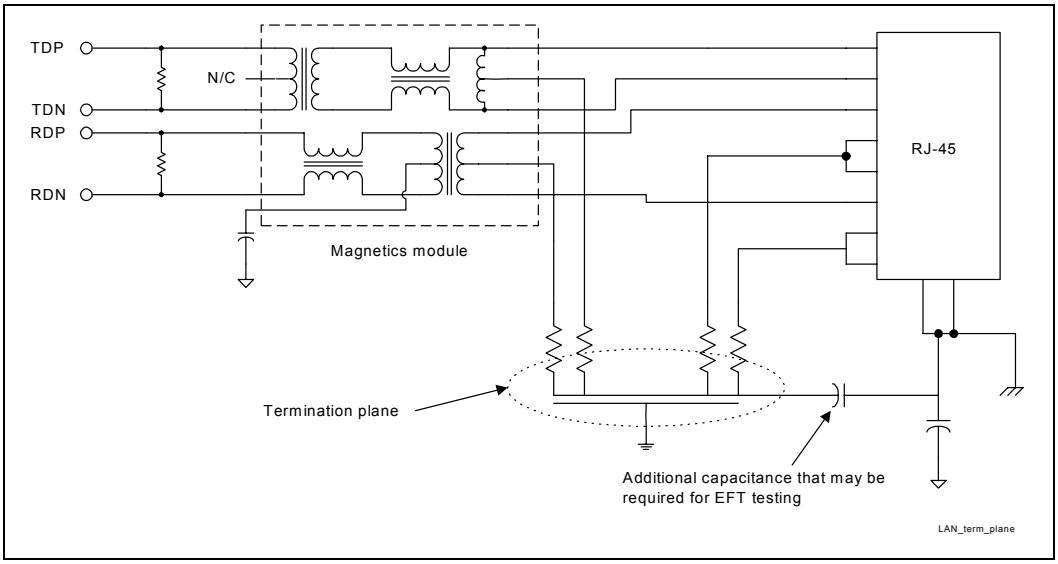
9.9.4.6 Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

9.9.4.6.1 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

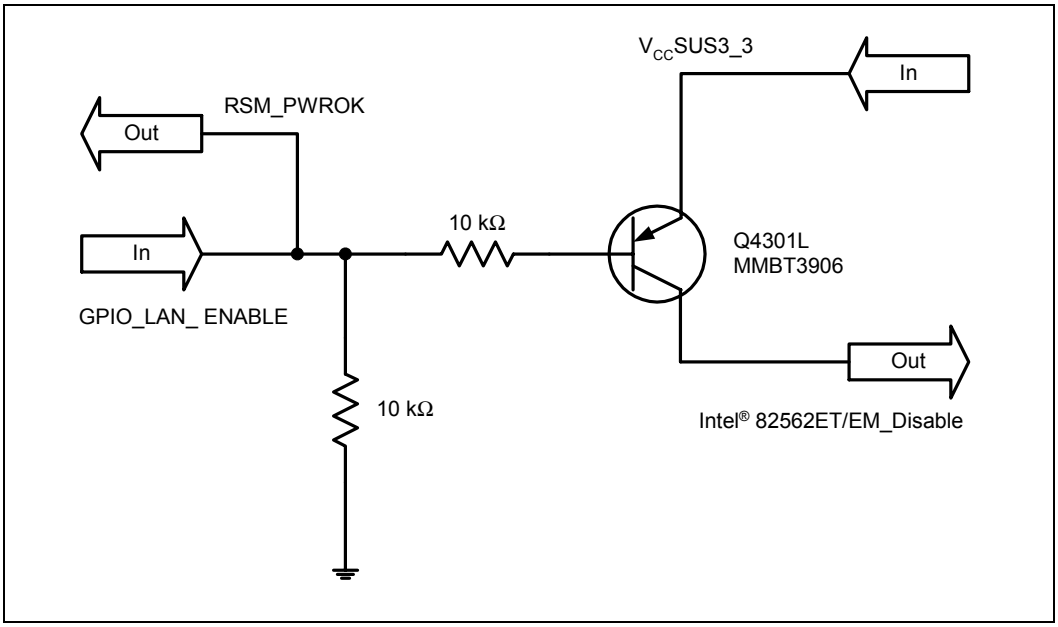
Figure 127. Termination Plane



9.9.5 Intel® 82562 ET/EM Disable Guidelines

To disable the 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit (see Figure 128) will allow this behavior. BIOS by controlling the GPIO can disable the LAN microcontroller.

Figure 128. Intel® 82562ET/EM Disable Circuit



There are 4 pins which are used to put the 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

The four control signals shown in the above table should be configured as follows: Test_En should be pulled-down thru a 100 Ω resistor. The remaining 3 control signals should each be connected thru 100 Ω series resistors to the common node “82562ET/EM_Disable” of the disable circuit.

9.9.6 82562ET / 82562EH Dual Footprint Guidelines

These guidelines characterize the proper layout for a dual footprint solution. This configuration enables the developer to install either the 82562EH or the 82562ET/82562EM components while having only one motherboard design. The following are guidelines for the 82562ET/82562EH Dual Footprint option. The dual footprint for this particular solution uses a SSOP footprint for 82562ET and a TQFP footprint for 82562EH. The combined footprint for this configuration is shown in Figure 129 and Figure 130.

Figure 129. Dual Footprint LAN Connect Interface

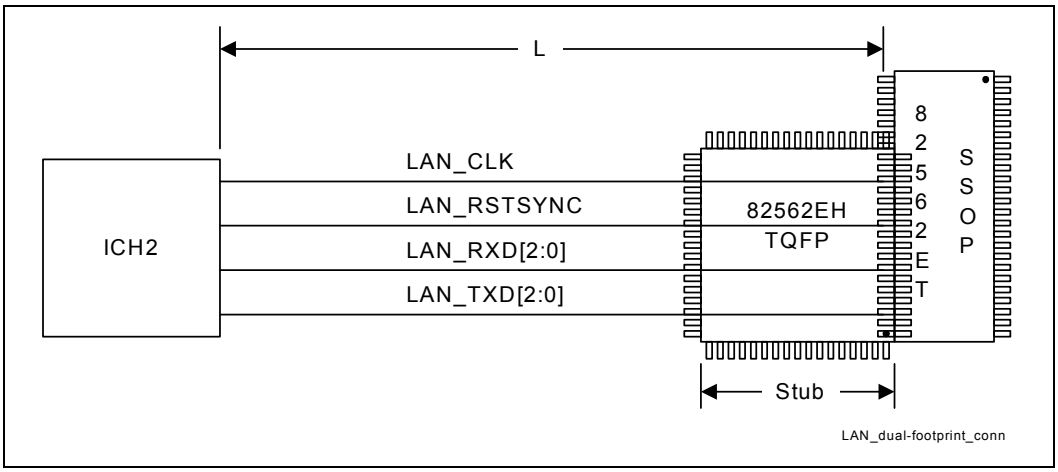
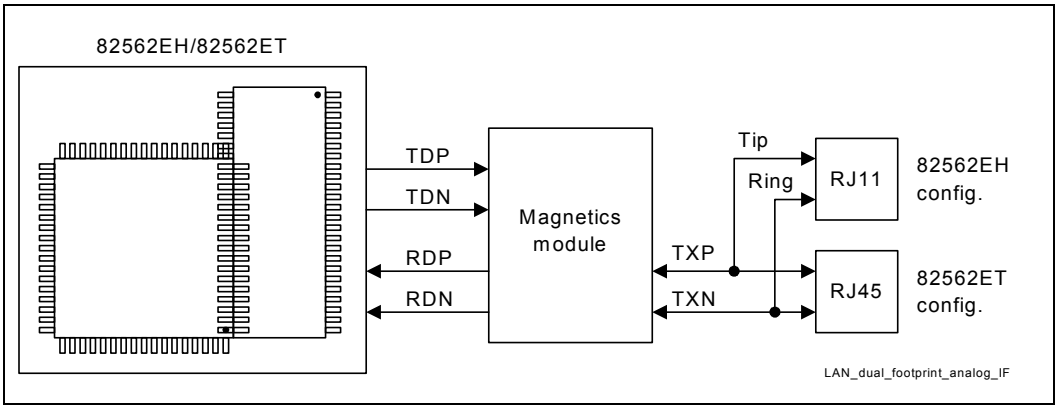


Figure 130. Dual Footprint Analog Interface



The following are additional guidelines for this configuration:

- L = 3 .5 to 4.5 inches
- Stub < 0.5 inches
- Either 82562EH or 82562ET/82562EM can be installed. Not both
- 82562ET pins 28,29, and 30 overlap with 82562EH pins 17,18, and 19.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.
- The 82562EH and 82562ET configurations share signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/Ring, and RXN/Tip.
- No stubs should be present when 82562ET is installed.
- Packages used for the Dual Footprint are TQFP for 82562EH and SSOP for 82562ET.
- A 22Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- Resistor should be placed as close as possible to the component.
- Use components that can satisfy both the 82562ET and 82562EH configurations (i.e., magnetics module).
- Install components for either the 82562ET or the 82562EH configuration. Only one configuration can be installed at a time.
- Route shared signal lines such that stubs are not present or are kept to a minimum.
- Stubs may occur on shared signal lines (i.e., RDP and RDN). These stubs are due to traces routed to an uninstalled component. In an optimal layout, there should be no stubs.
- Use 0 Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.
- Traces from magnetics to connector must be shared and not stubbed. An RJ-11 connector that fits into the RJ-45 slot is available. Any amount of stubbing will destroy both HomePNA* and Ethernet performance.

9.10 Intel® ICH2 Routing Guidelines – Four-Layer Motherboard

Figure 131. Example Intel® ICH2 Top Layer Breakout Using Standard Size Vias

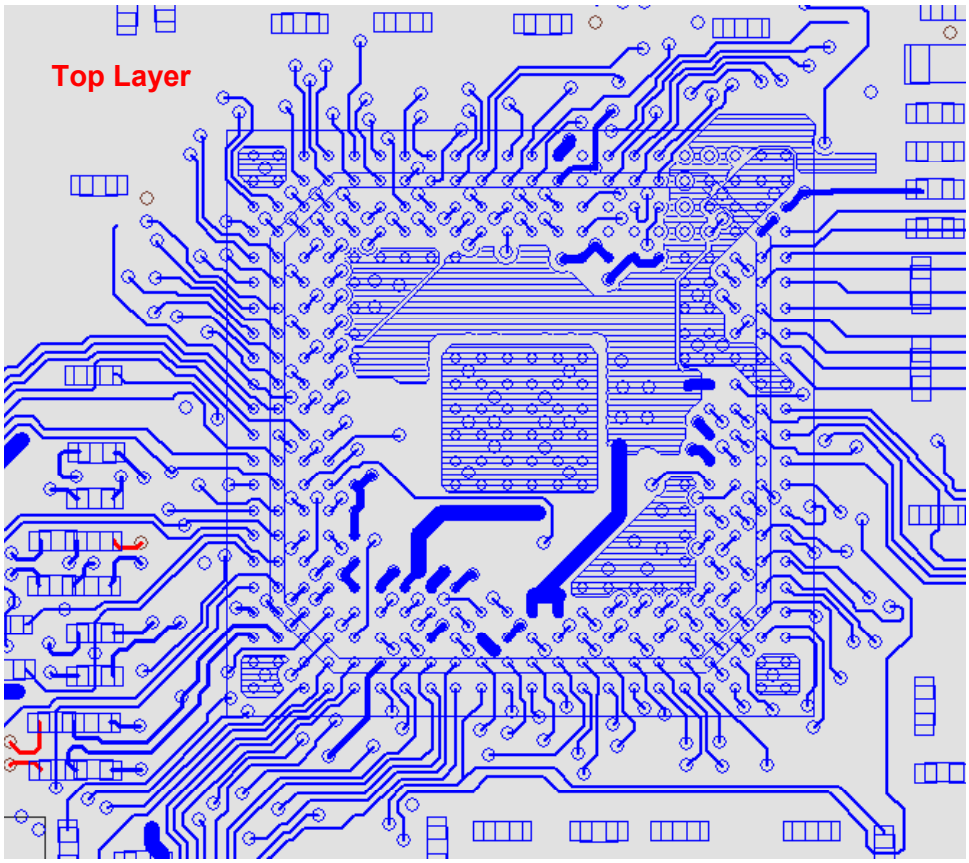
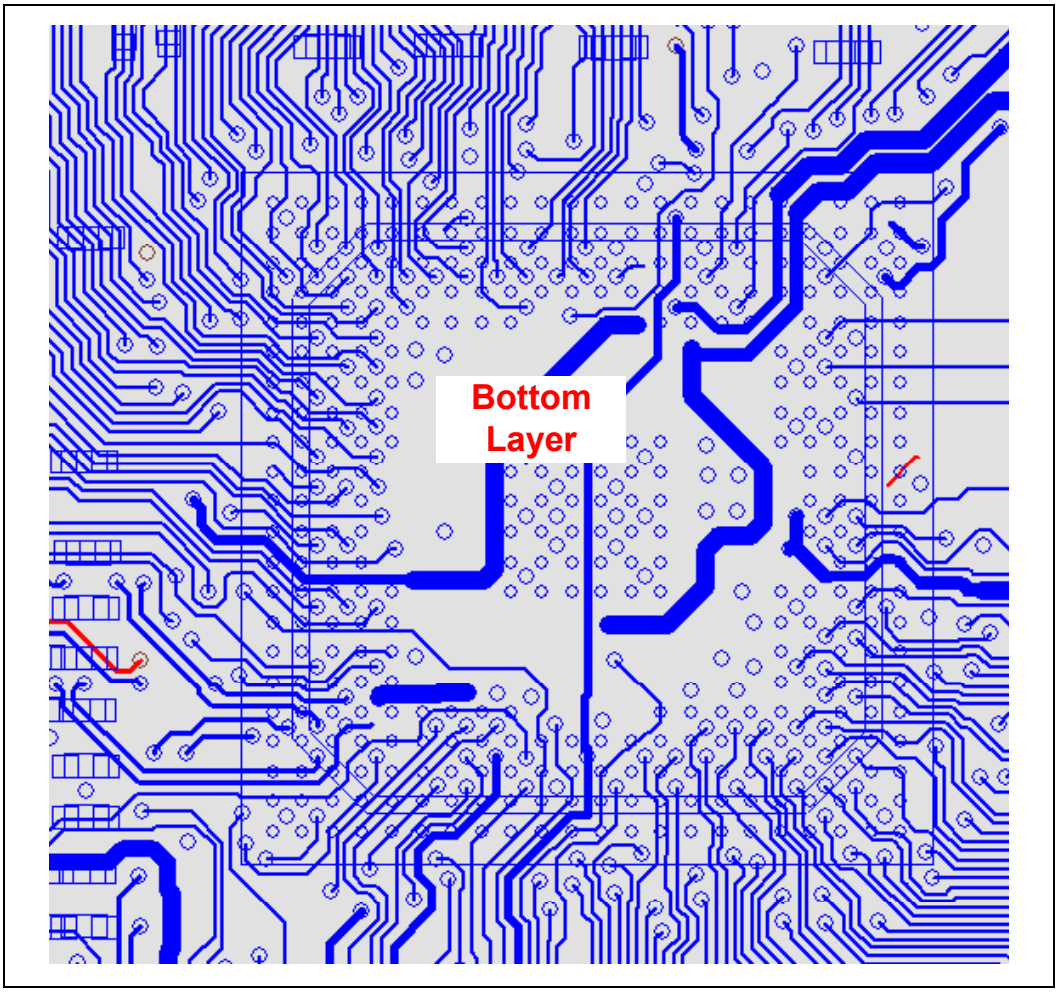


Figure 132. Example Intel® ICH2 Bottom layer Breakout Using Standard Size Vias



9.11 FWH Guidelines

9.11.1 FWH Decoupling

A 0.1 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

9.11.2 In Circuit FWH Programming

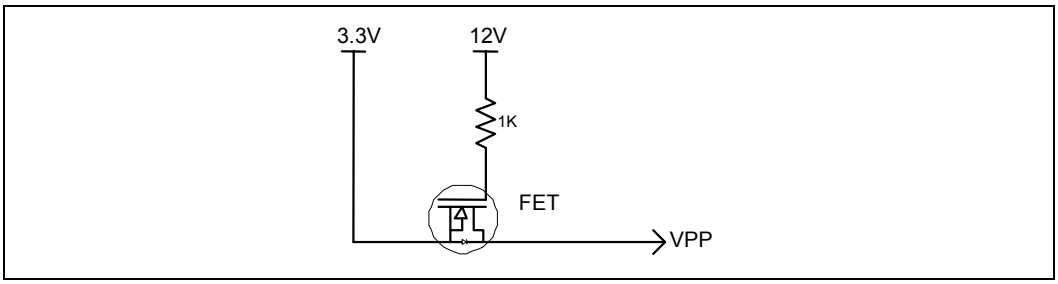
All cycles destined for the FWH will appear on PCI. The ICH2 hub interface to PCI Bridge will put all processor boot cycles out on PCI (before sending them out on the FWH interface). If the ICH2 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from of a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH2 in subtractive decode mode. If a PCI boot card is inserted and the ICH2 is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot off a ROM behind the 82380AB. Once you have booted from the PCI card, you could potentially program the FWH in circuit and program the ICH2 CMOS.

9.11.3 FWH Vpp Design Guidelines

The Vpp pin on the FWH is used for programming the flash cells. The FWH supports Vpp of 3.3 V or 12 V. If Vpp is 12 V the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 V Vpp for 80 hours. The 12 V Vpp would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 133. FWH VPP Isolation Circuitry



9.12 Intel® ICH2 Decoupling Recommendations

The ICH2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in Table 42 to ensure the component maintains stable supply voltages. Also the capacitors should be placed as close to the package as possible. Maximum distance allowed is 400 mils. It is recommended that the motherboard designer include pads for extra decoupling capacitors should the recommendation not work on their board.

Table 42. Decoupling Capacitor Recommendation.

Power Plane	# Decoupling Capacitors	Capacitor Value
3.3 V Core	6	0.1 µF
3.3 V Stand By	1	0.1 µF
VCC_CPU	1	0.1 µF
1.8 V Core	2	0.1 µF
1.8 V Stand By	1	0.1 µF
5 V Reference	2	0.1 µF and 1 µF
5 V Reference Stand By	1	0.1 µF

9.13 Glue Chip 4 (Intel® ICH2 Glue Chip)

In order to reduce the component count and BOM cost of the Intel 850 chipset based-platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The Glue Chip 4 is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Glue Chip 4 Features:

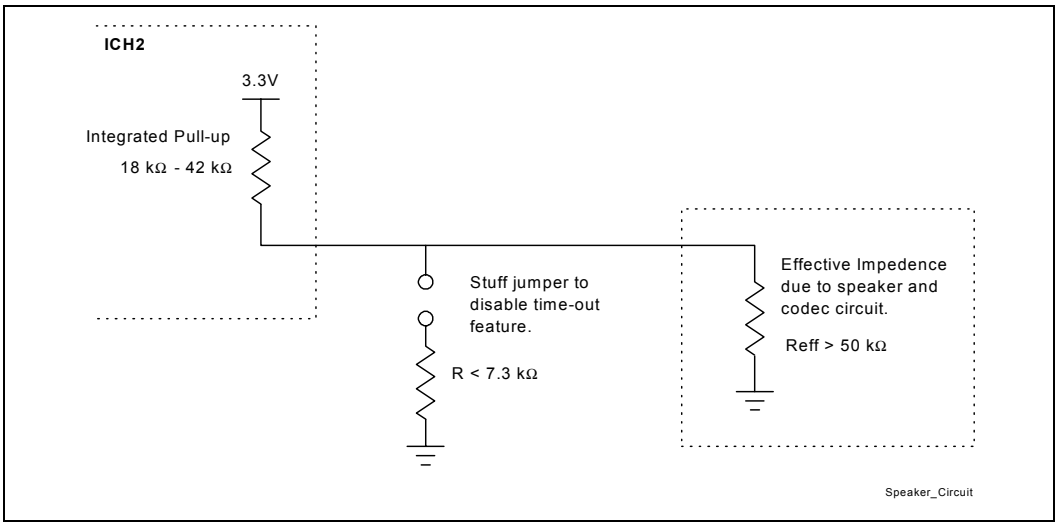
- PWROK signal generation
- Control circuitry for Suspend To RAM
- Power Supply power up circuitry
- RSMRST# generation
- Backfeed cutoff circuit for Suspend to RAM
- 5 V reference generation
- Flash FLUSH# / INIT# circuit
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- Voltage translation for Audio MIDI signal
- Audio-disable circuit
- Voltage translation for DDC to monitor
- Tri-state buffers for test

More information regarding this component is available from your field representative

9.14 SPKR Pin Consideration

The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 kΩ. Failure to due so will cause the TCO Timer Reboot function to be erroneously disabled. SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of POWEROK. When enabled, the ICH2 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull up resistor (the resistor is only enabled during boot/reset). Therefore it's default state when the pin is a "no connect" is a logical one or enabled. To disable the feature, a jumper can be populated to pull the signal line low (see figure). The value of the pull-down must be such that the voltage divider caused by the pull down and integrated pull up resistors will be read as logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or lower than the integrated pull up resistor. It is therefore strongly recommended that the effective impedance be greater than 50 kΩ and the pull-down resistor be less than 7.3 kΩ.

Figure 134. SPKR Circuit



It should be noted that this is not the only solution to this problem. Board designers can also isolate the load from the SPKR pin until POWEROK is in a stable high state. This would allow a weak effective load to be implemented.

9.15 1.8 V and 3.3 V Power Sequence Requirement

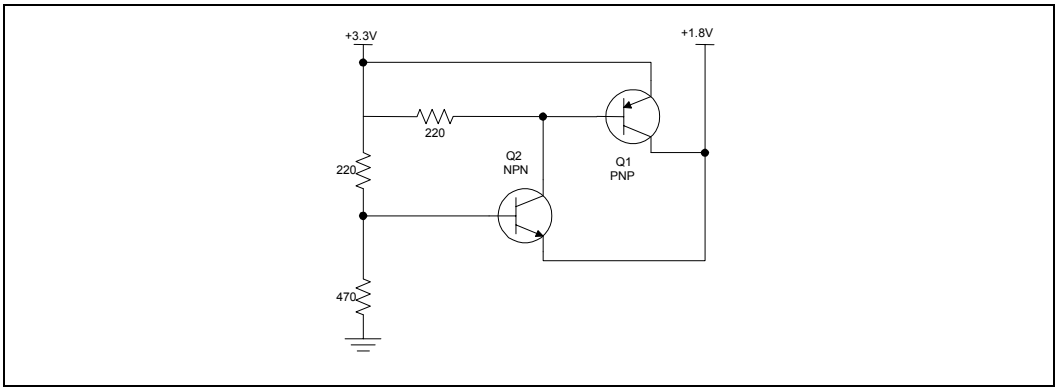
The ICH2 has two pairs of associated 1.8 V and 3.3 V supplies. These supplies are Vcc1_8, Vcc3_3 and VccSus1_8, VccSus3_3. These pairs are assumed to power up and power down together. The difference between the two associated supplies must never be greater than 2.0 V. The 1.8 V supply may come up before the 3.3 V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.8 V supply is typically derived from the 3.3 V supply by means of a linear regulator).

One serious consequence of violation of this "2V Rule" is electrical overstress of oxide layers, possibly resulting in component damage.

The majority of the ICH2 I/O buffers are driven by the 3.3 V supplies, but are controlled by logic that is powered by the 1.8 V supplies. If the 3.3 V supply powers up first, the I/O buffers will be in an undefined state until the 1.8 V logic is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled, and the ICH2 may unexpectedly drive these signals if the 3.3 V supply is active while the 1.8 V supply is not.

Figure 135 is an example power-on sequencing circuit that ensures the “2V Rule” is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.8 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8 V plane, current will not flow from the 3.3 V supply into 1.8 V plane when the 1.8 V plane reaches 1.8 V.

Figure 135. Example Power-On 3.3 V / 1.8 V Sequencing Circuit



When analyzing systems that may be "marginally compliant" to the 2V Rule, pay close attention to the behavior of the ICH2's RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells
- LAN_PWROK controls isolation between the LAN wells and the Resume wells

If one of these signals goes high while one of its associated power planes is active and the other is inactive, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging internal currents.

9.16 PIRQ Routing

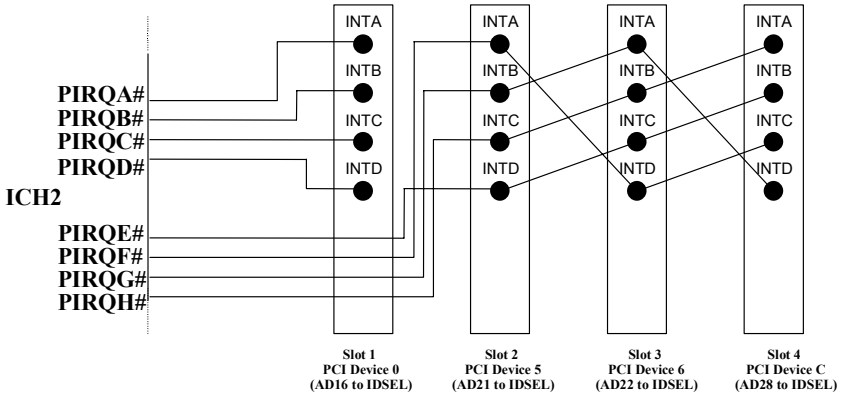
PCI interrupt request signals E-H are new to the ICH2. These signals have been added to lower the latency caused by having multiple devices on one Interrupt line. With these new signals, each PCI slot can have an individual PCI interrupt request line (Assuming that the system has four PCI slots). Table 43 shows how the ICH2 uses the PCI IRQ when the IOAPIC is active.

Table 43. IOAPIC Interrupt Inputs 16 Through 23 Usage

IOAPIC INTIN PIN	Function in Intel® ICH2 using the PCI IRQ in IOAPIC
IOAPIC INTIN PIN 16 (PIRQA)	
IOAPIC INTIN PIN 17 (PIRQB)	AC'97, Modem and SMBUS
IOAPIC INTIN PIN 18 (PIRQC)	
IOAPIC INTIN PIN 19 (PIRQD)	USB Controller #1
IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN Device
IOAPIC INTIN PIN 21 (PIRQF)	
IOAPIC INTIN PIN 22 (PIRQG)	
IOAPIC INTIN PIN 23 (PIRQH)	USB Controller #2 (starting from ICH2 B0 silicon)

Interrupts B, D, E, and H service devices internal to the ICH2. Interrupts A, C, F, and G are not used and can be used by PCI slots. Figure 136 shows an example of IRQ line routing to the PCI slots.

Figure 136. Example PCI IRQ Routing



The PCI IRQ Routing shown in Figure 136 allows the ICH2 internal functions to have a dedicated IRQ(Assuming add-in cards are single function devices and use INTA). If a P2P bridge card or a multifunction device uses more than one INTn# pin on the ICH2 PCI Bus, the ICH2 internal functions will start sharing IRQs.

Figure 136 is an example. It is up to the board designer to route these signals in a way that is the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH2's internal device/functions.

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10 Additional Design Considerations

This section documents system design considerations not addressed in previous sections.

10.1.1 Retention Mechanism Placement and Keepouts

The RM requires a keepout zone for a limited component height area under the RM. Figure 137 and Figure 138 show the relationship between the RM mounting holes and pin one of the socket. In addition they also document the keepouts. A 0.409 inch diameter routing keepout should be maintained on the secondary side of the board.

The retention holes should be a non-plated hole. Figure 139 illustrates the hole locations and keepouts for the Intel 850 chipset heatsink retention mechanism. For heatsink volumetric information refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines*.

Figure 137. RM Keepout Drawing 1

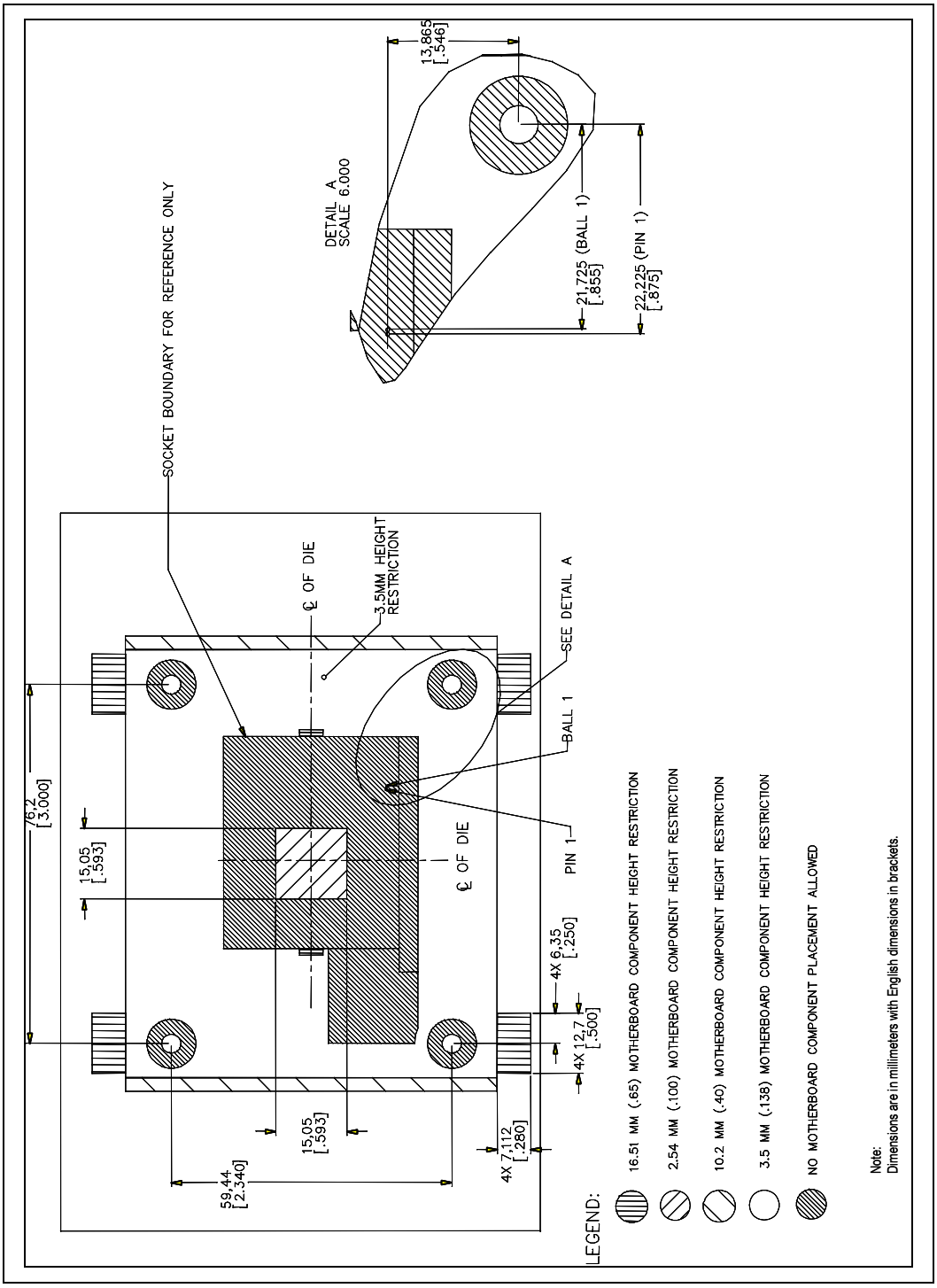


Figure 138. RM Keepout Drawing 2

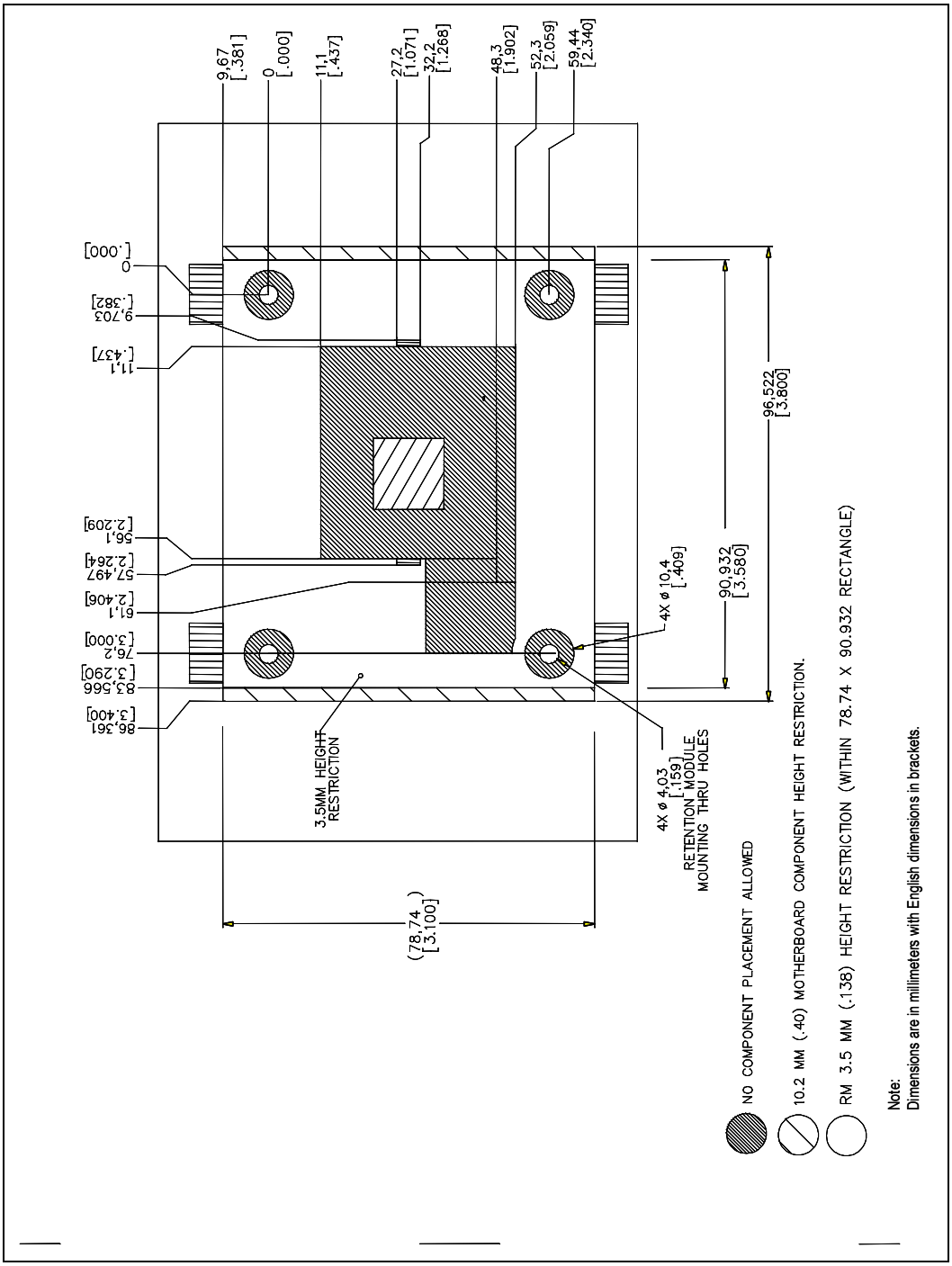
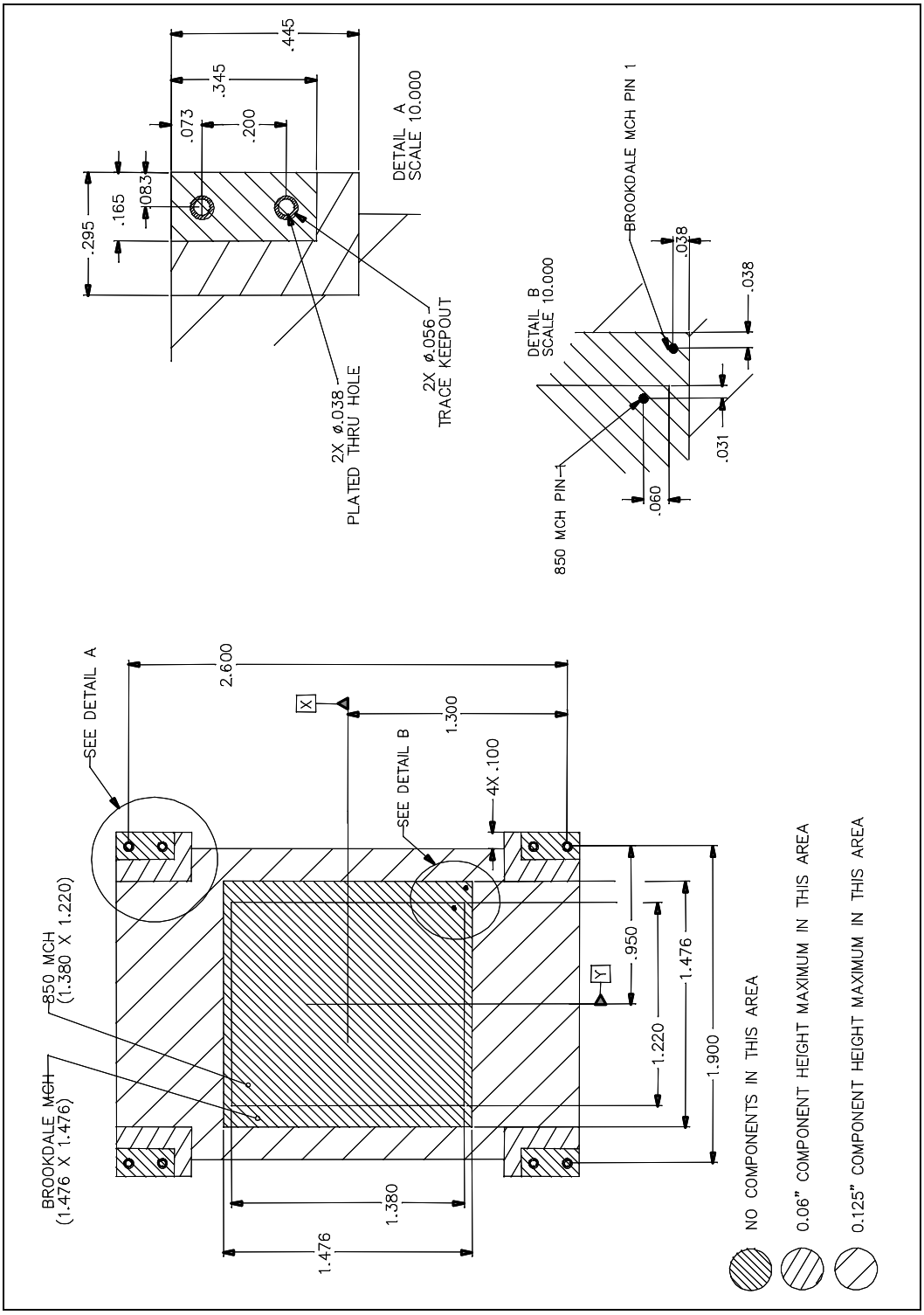


Figure 139. Intel® MCH Keepouts and RM Hole Locations



10.1.2 Power Header for Active Cooling Solutions

The Intel reference-design heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden*/Molex 22-01-3037, AMP* 643815-3 or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in Table 44.

Table 44. Reference Solution Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	No Connect

The Intel boxed processor heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden*/Molex* 22-23-2037, AMP* 640456-3 or equivalent. The integrated fan requires the system board to supply a minimum of 740mA at 12V for proper operation. The fan connector pinout is described in Table 45.

Table 45. Boxed Processor Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	SENSE

The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. The system board requires a pull-up resistor to provide the appropriate Voh level to match the fan speed monitor. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 should be tied to GND.

For more information on boxed processor requirements, refer to the processor datasheet.

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11 Intel® Pentium® 4 Processor in the 478-Pin Package Processor Power Distribution Guidelines

11.1 Power Requirements

Intel recommends using an *Intel® Pentium® 4 Processor VR Down Design Guidelines*-compliant regulator for the processor system board designs that meets FMB2 requirements (refer to Section 1.6 for airflow requirements). An *Intel® Pentium® 4 Processor VR Down Design Guidelines*-compliant regulator may be integrated as part of the system board or on a module. The system board designer should properly place high frequency and bulk-decoupling capacitors as needed between the voltage regulator and the processor to ensure voltage fluctuations remain within the *Intel® Pentium® 4 Processor in the 478-pin Package Electrical, Mechanical, and Thermal Specifications* and the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process EMTS*. See Section 11.1.3 and 11.1.4 for recommendations on the amount of decoupling needed.

Specifications for the processor voltage are contained in the *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process EMTS* and the *Intel® Pentium® 4 Processor in the 478-Pin Package Electrical, Mechanical and Thermal Specifications*. These specifications are for the processor die. For guidance on correlating the die specifications to socket level measurements, refer to the socket loadlines in the *Intel® Pentium® 4 Processor VR Down Design Guidelines*.

The voltage tolerance of the loadlines contained in the above mentioned documents help the system designer to achieve a flexible motherboard design solution for many different frequencies of the processor. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable.

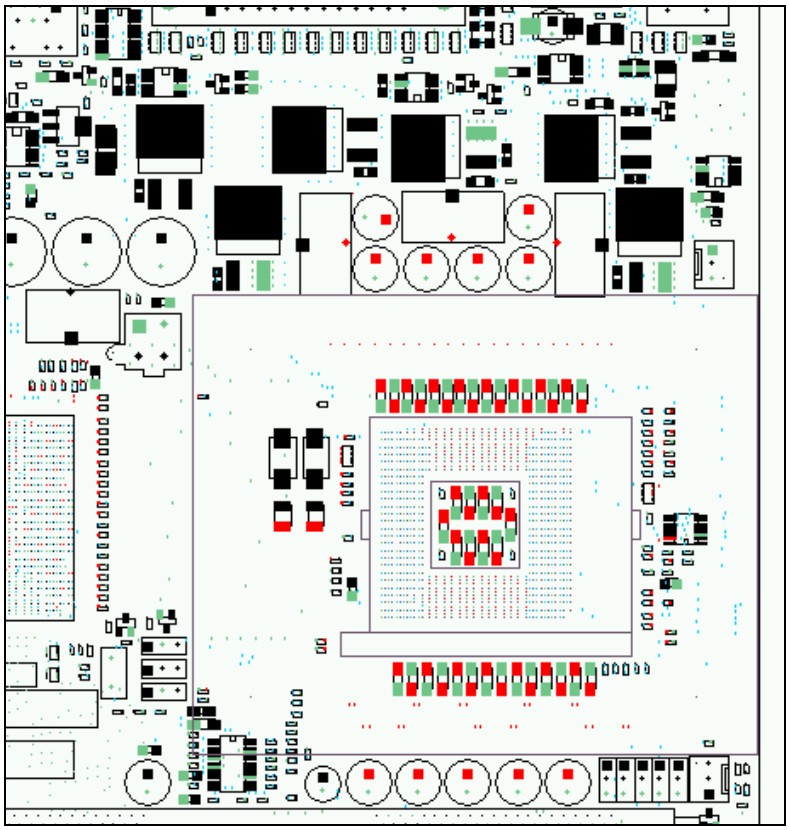
Note: For maximum flexibility in system design, it is recommended to use an FMB1 or FMB2 compliant regulator. Example regulator designs that meet FMB1 or FMB2 specifications are shown below. Each of these designs has their benefit as well as drawbacks.

The processor requires local regulation due to its higher current requirements, and to maintain power supply tolerance. For example, an on-board DC-to-DC converter converts a higher DC voltage to a lower level using either a linear or a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R). More importantly however, a discrete regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the processor voltage. Figure 140 (FMB1), and Figure 141 and Figure 142 (FMB2) and shows an example of the placement of the local voltage regulation circuitry.

In this section, North and South are used to describe a specific side of the socket based on the placement of the customer reference board shown in Figure 140 (FMB1) and Figure 141 and Figure 142 (FMB2) and North refers to the side of the processor closest to the back panel and South refers to the side of the processor closest to the system memory.

11.1.1 FMB1 VR Component Placement

Figure 140. FMB1 VR Component Placement



11.1.2 FMB2 VR Component Placement

Figure 141. Four-Phase VR Component Placement

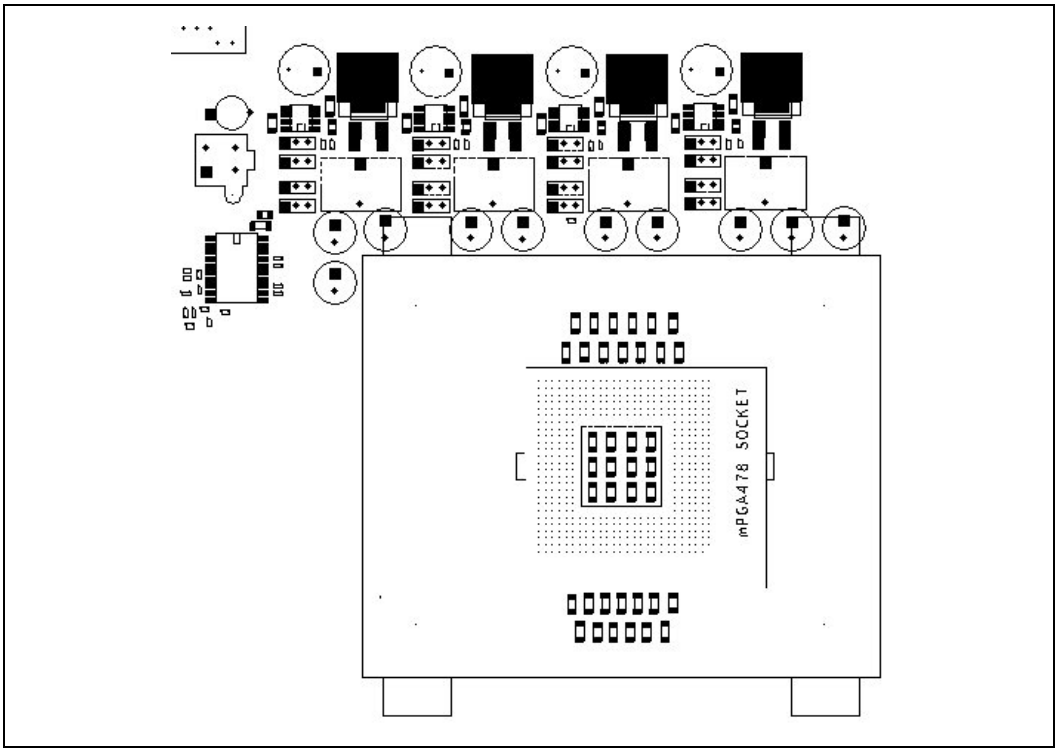
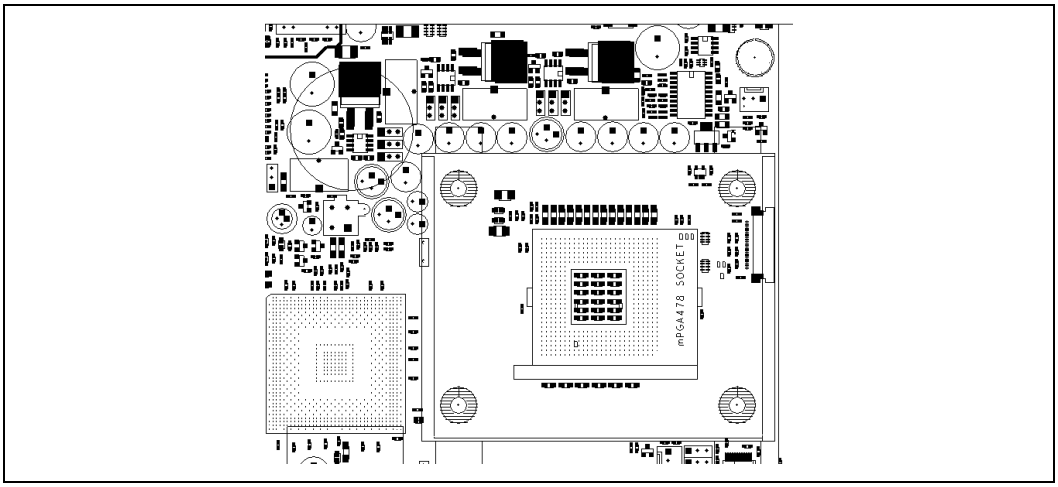


Figure 142. Three-Phase VR Component Placement



11.1.3 FMB1 Decoupling Requirements

For the processor voltage regulator circuitry to meet the transient specifications of the processor, proper bulk and high frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are shown in Table 46.

Table 46. Decoupling Requirements

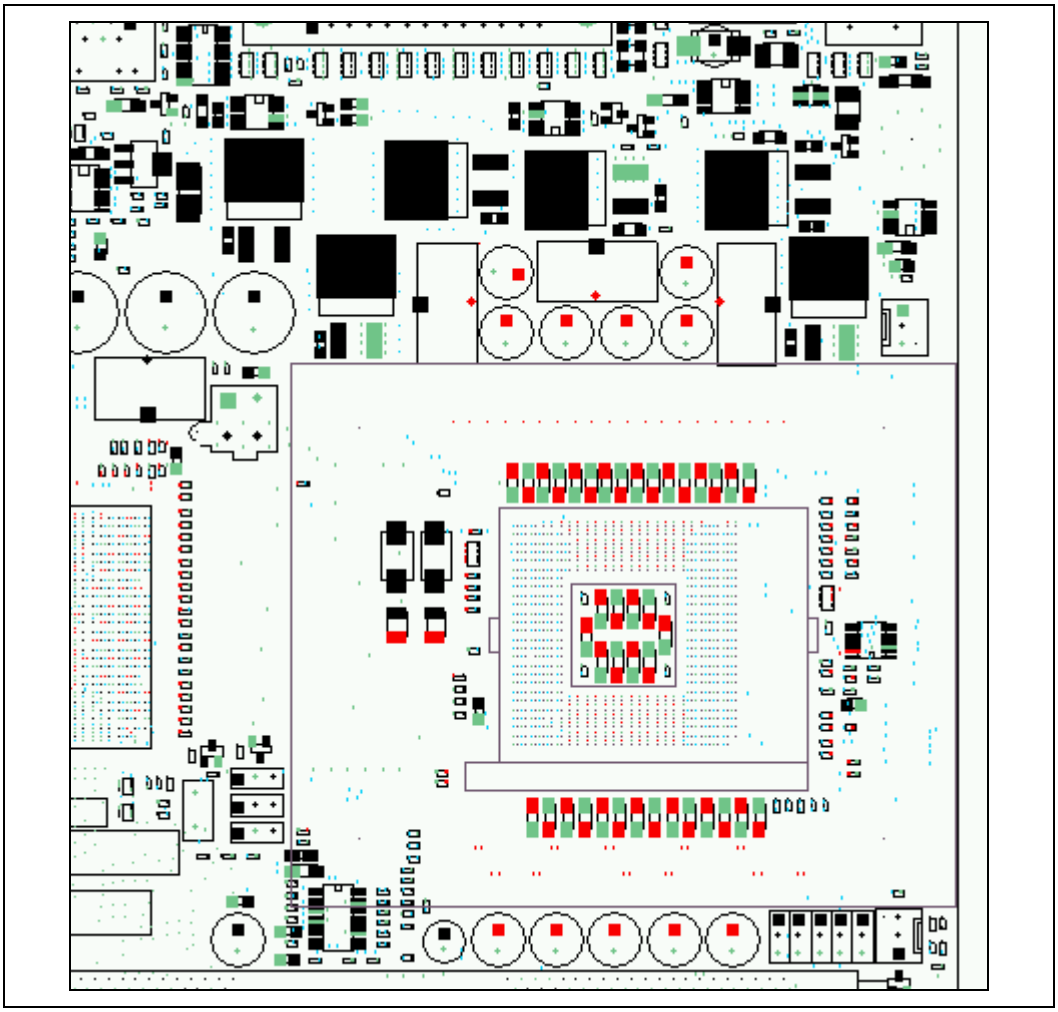
Capacitance	ESR (each)	ESL (each)	Ripple Current Rating (each)	Notes
10 OS-CONs*, 560 µF	9.28 mΩ, max	6.4 nH, max	4.080 A_{rms}	1
30 1206 package, 10 µF	3.5 mΩ, typ.	1.15 pH, typ		1

NOTES:
1. The ESR, ESL and ripple current values in this table are based on the values used in power delivery simulation by Intel and they are not vendor specifications.
2. The decoupling should be placed as close as possible to the processor power pins. Table 46 and Table 47 illustrate the recommended placement. The placement drawings shows sites for 11 OS-CONs* and 38 1206 package 10 µF capacitors. The sites are populated as shown in Table 47 and the remaining sites are unpopulated. The voltage regulator designer should ensure that an adequate amount of decoupling is present such that the circuit meets the processor specifications.

Table 47. Decoupling Locations

Type	Number	Location
560 µF OS-CONs*	5	North side of the processor as close as possible to the keepout area for the retention mechanism
560 µF OS-CONs*	5	South side of the processor as close as possible to the keepout area for the retention mechanism
1206 package, 10 µF	10	North side of the processor as close as possible to the processor socket
1206 package, 10 µF	10	Inside the processor socket cavity
1206 package, 10 µF	10	South side of the processor as close as possible to the processor socket

Figure 143. Decoupling Placement



11.1.4 FMB2 Decoupling Requirements

In order for the processor voltage regulator circuitry to meet the transient specifications of the processor, proper bulk and high frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are described in Table 48 and Table 49.

Table 48. Four-Phase Decoupling Requirements

Capacitance	ESR (Each)	ESL (Each)	Ripple Current Rating (Each)	Notes:
10 OSCONs*, 560 µF	9.28 mΩ, max	6.4 nH, max	4.080 A	1
38 1206 package, 10 µF	3.5 mΩ, typ	1.15 nH, typ		1

NOTES:
1. The ESR, ESL and ripple current values in this table are based on the values used in power delivery simulation by Intel and they are not vendor specifications.

Table 49. Three-Phase Decoupling Requirements

Capacitance	ESR (Each)	ESL (Each)	Ripple Current Rating (Each)	Notes:
9 OSCONs*, 560 µF	9.28 mΩ, max	6.4 nH, max	4.080 A	1
3 Al Electrolytic, 3300 µF	12 mΩ	5 nH		1
24 0805 package, 10 µF				1,2
14 1206 package, 10 µF	3.5 mΩ, typ	1.15 nH, typ		1,2

NOTES:
1. The ESR, ESL and ripple current values in this table are based on the values used in power delivery simulation by Intel and they are not vendor specifications.
2. If only 1206's are used, 38 are needed.

The decoupling should be placed as close as possible to the processor power pins. Table 50 and Table 51 and Figure 144 and Figure 145 describe and illustrate the recommended placement.

Table 50. Four-Phase Decoupling Locations

Type	Number	Location
560 µF OSCONs*	10	North side of the processor as close as possible to the keep-out area for the retention mechanism
1206 package, 10 µF	13	North side of the processor as close as possible to the processor socket
1206 package, 10 µF	12	Inside the processor socket cavity
1206 package, 10 µF	13	South side of the processor as close as possible to the processor socket

Table 51. Three-Phase Decoupling Locations

Type	Number	Location
560µF OSCONs*	9	North side of the processor as close as possible to the keep-out area for the retention mechanism
Al Electrolytic, 3300 µF	3	North side of the processor as close as possible to the keep-out area for the retention mechanism
1206 package, 10 µF	14	North side of the processor as close as possible to the processor socket
0805 package, 10 µF	18	Inside the processor socket cavity
0805 package, 10 µF	6	South side of the processor as close as possible to the processor socket

NOTES:
1. If (38) 1206s are used, place 14 North, 10 inside, and 14 South of the socket.

Figure 144. Four-Phase Decoupling Placement

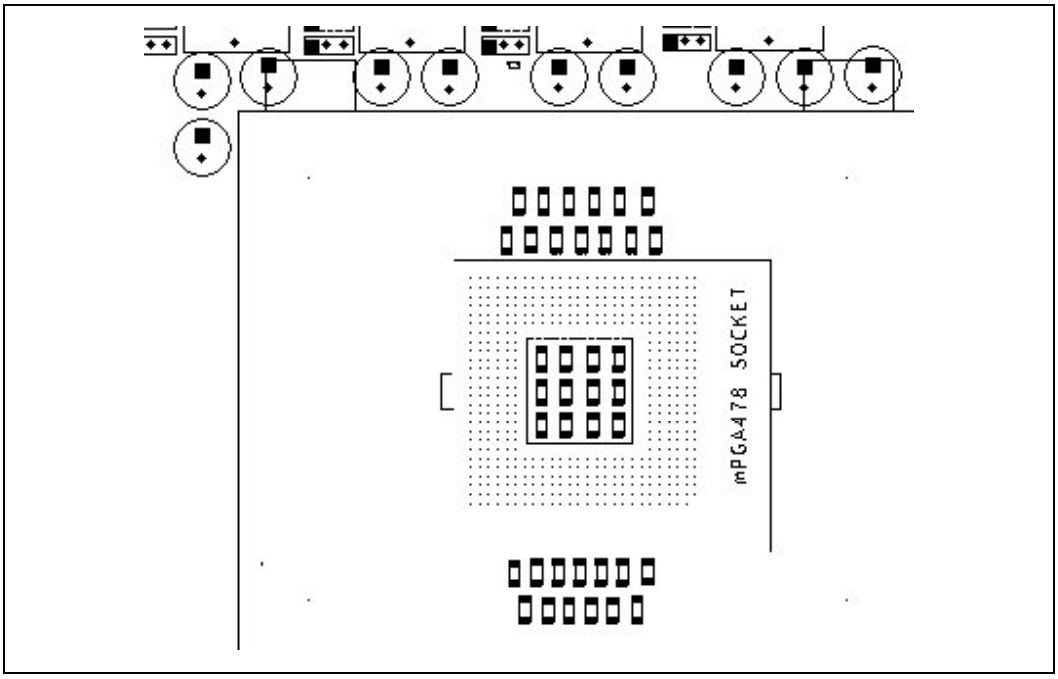
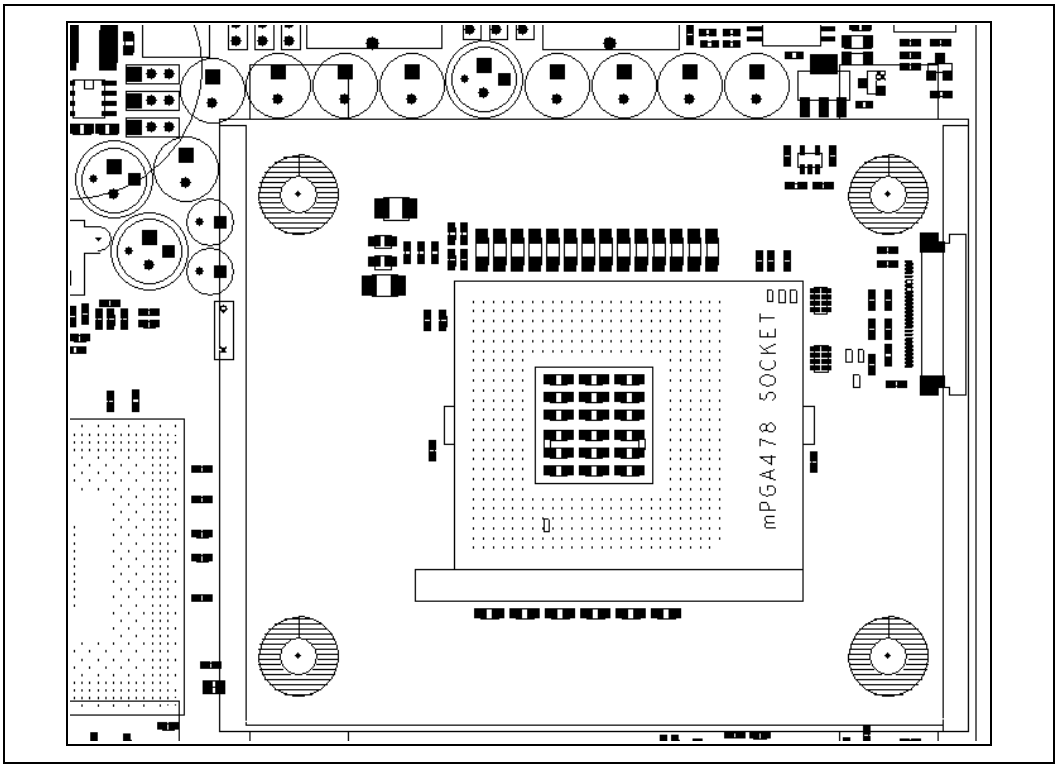


Figure 145. Three-Phase Decoupling Placement



11.1.5 FMB1 Layout (6-Layer Board)

All six layers in the processor area should be used for power delivery. Four layers should be used for VCC_CPU and two layers should be used for ground. Traces are not sufficient for supplying power to the processor due to the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements shapes that encompasses the power delivery part of the processor pin field are required. Figure 146 through Figure 151 show examples of how to use shapes to delivery power to the processor.

Figure 146. Top Layer Power Delivery Shape (VCC_CPU)

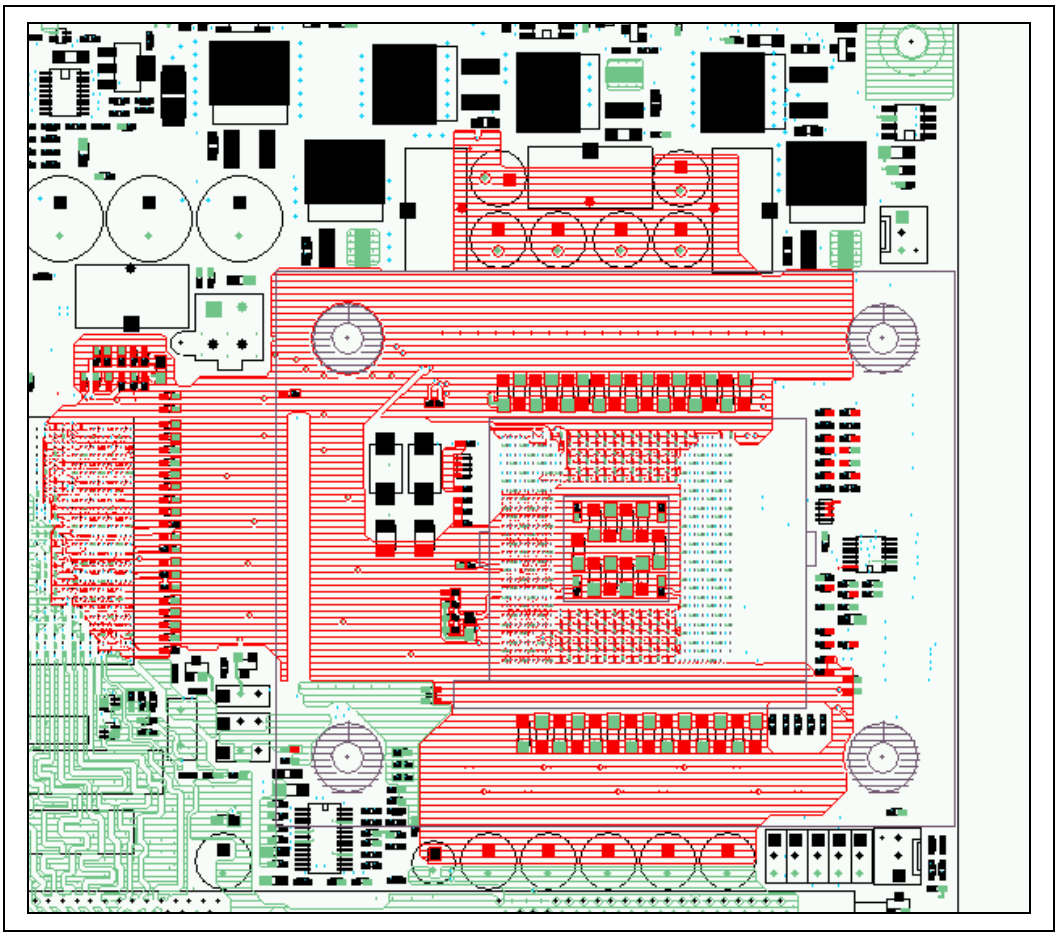


Figure 147. Layer 2 Power Delivery Shape (VSS)

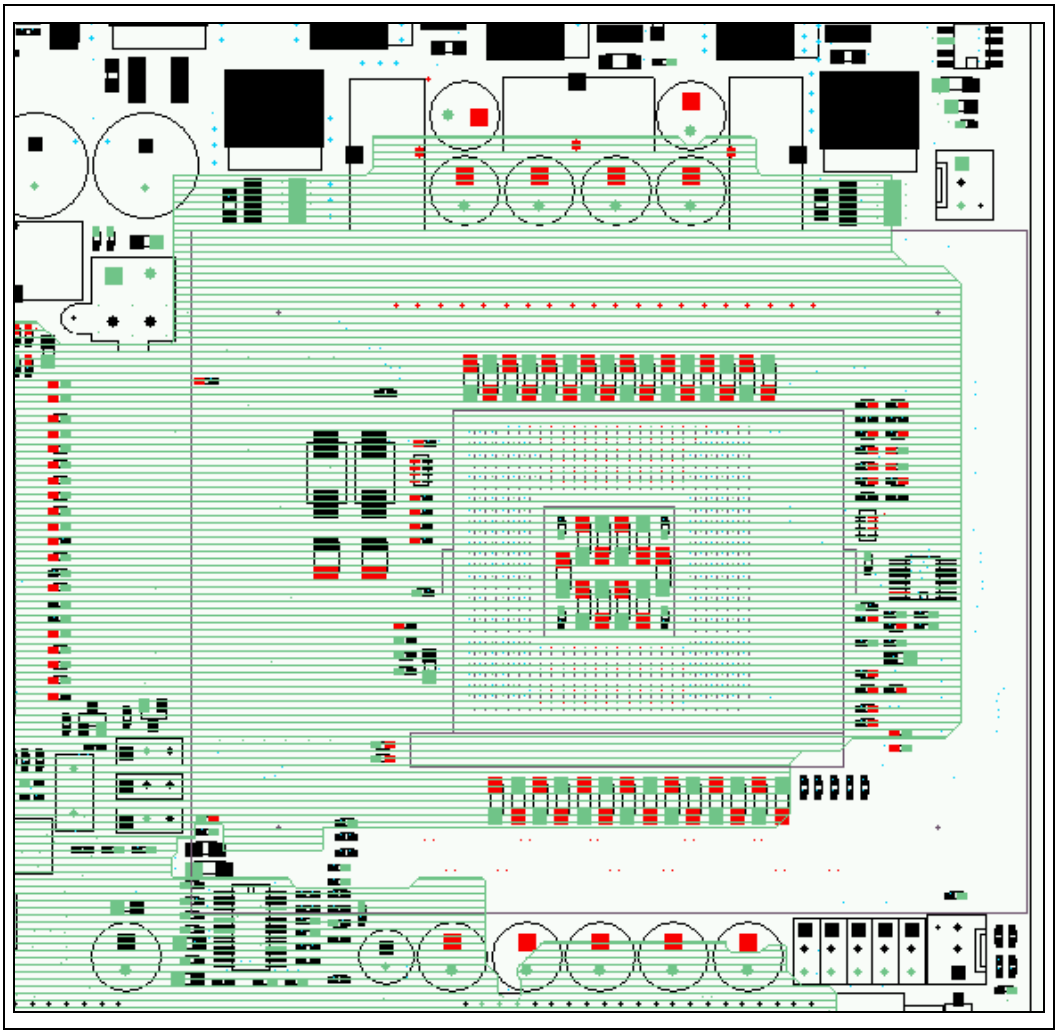


Figure 148. Layer 3 Power Delivery Shape (VCC_CPU and VSS)

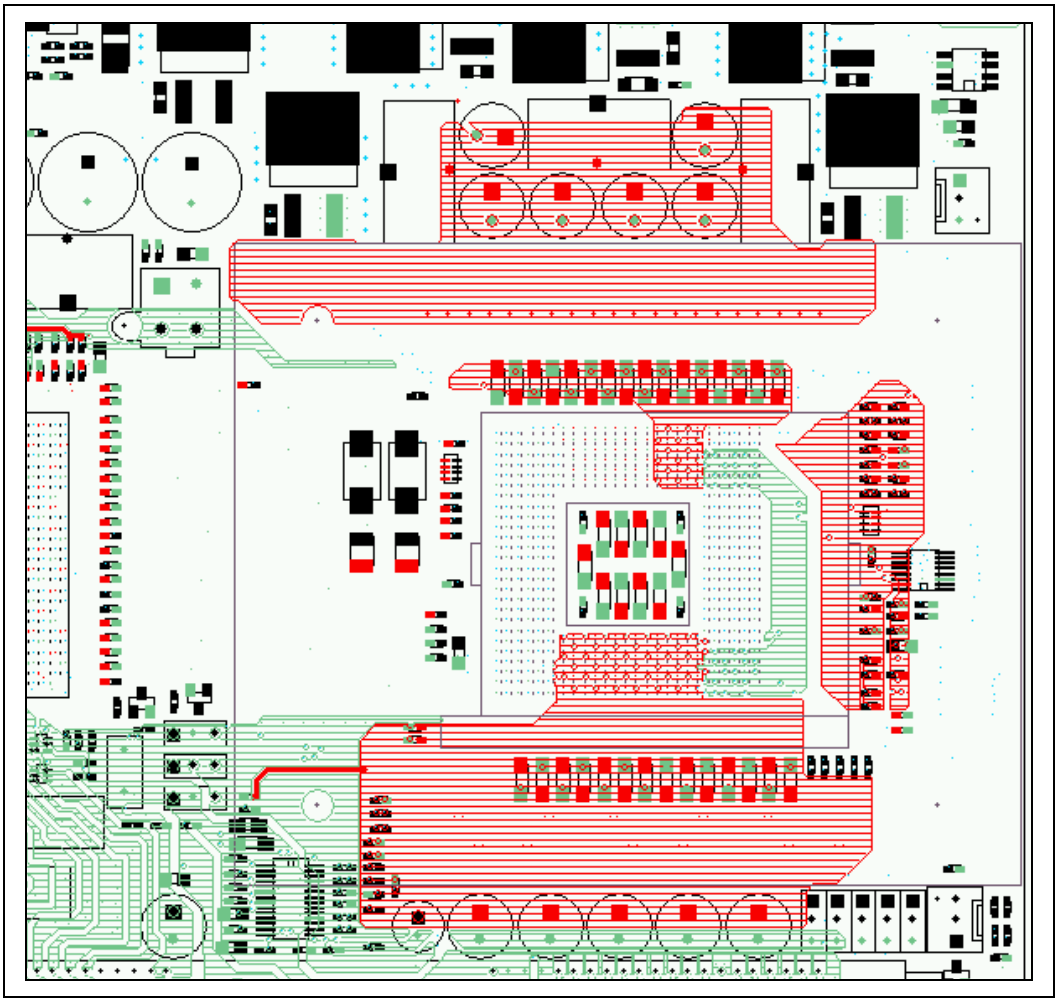


Figure 149. Layer 4 Power Delivery Shape (VCC_CPU and VSS)

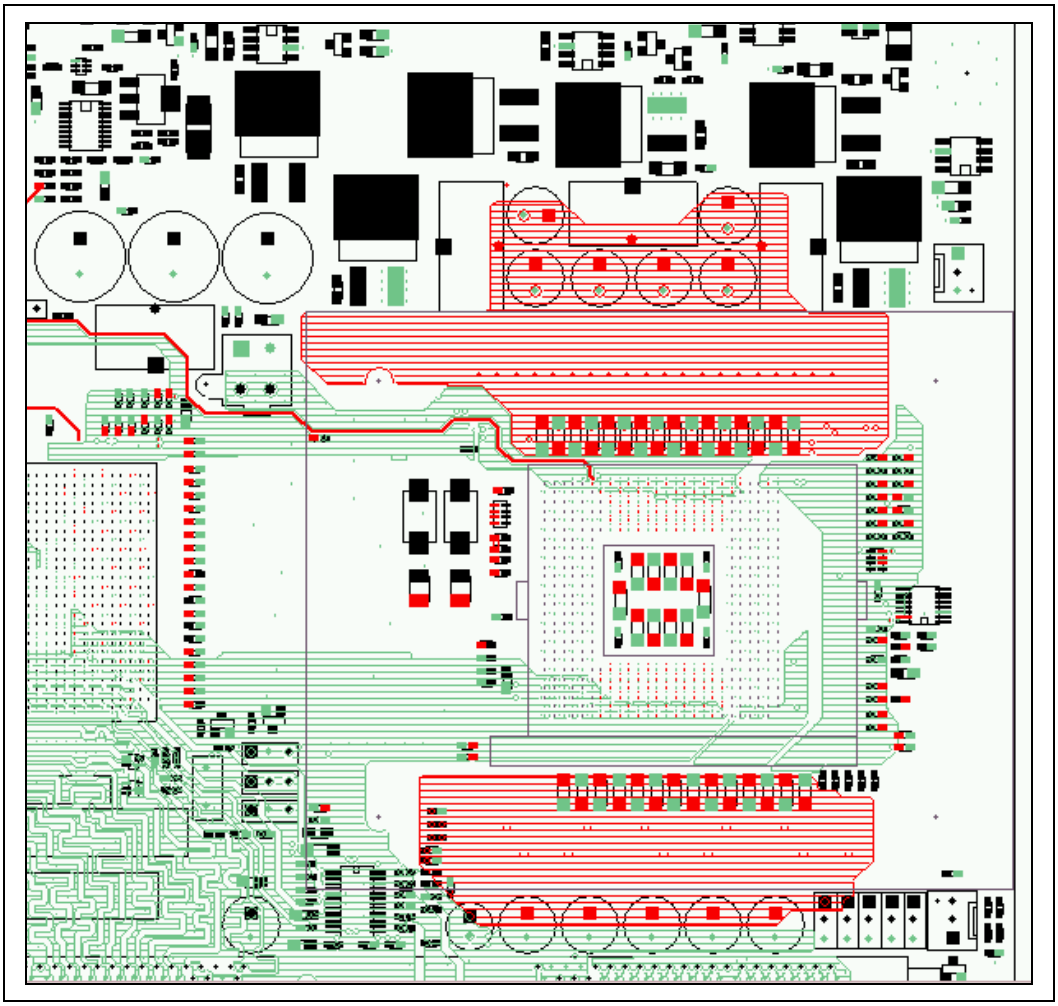


Figure 150. Layer 5 Power Delivery Shape (VSS)

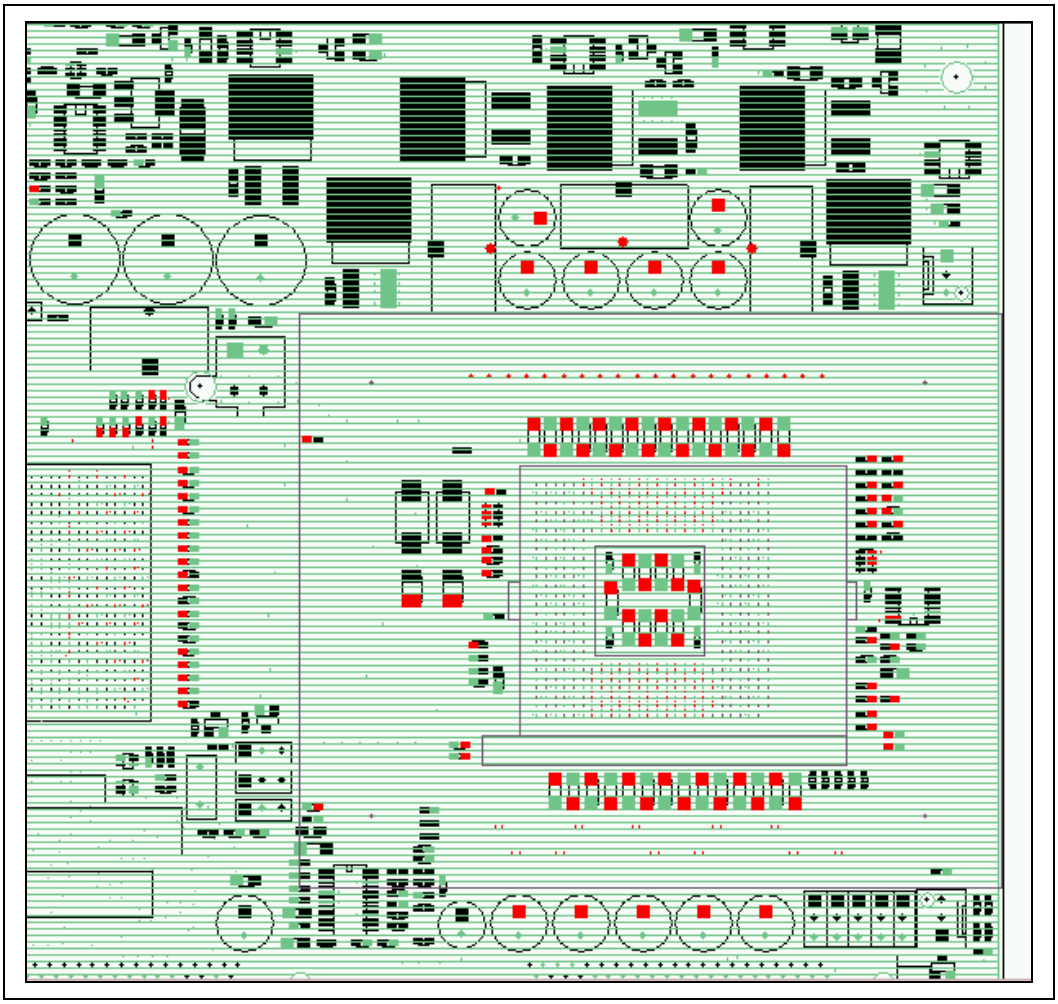
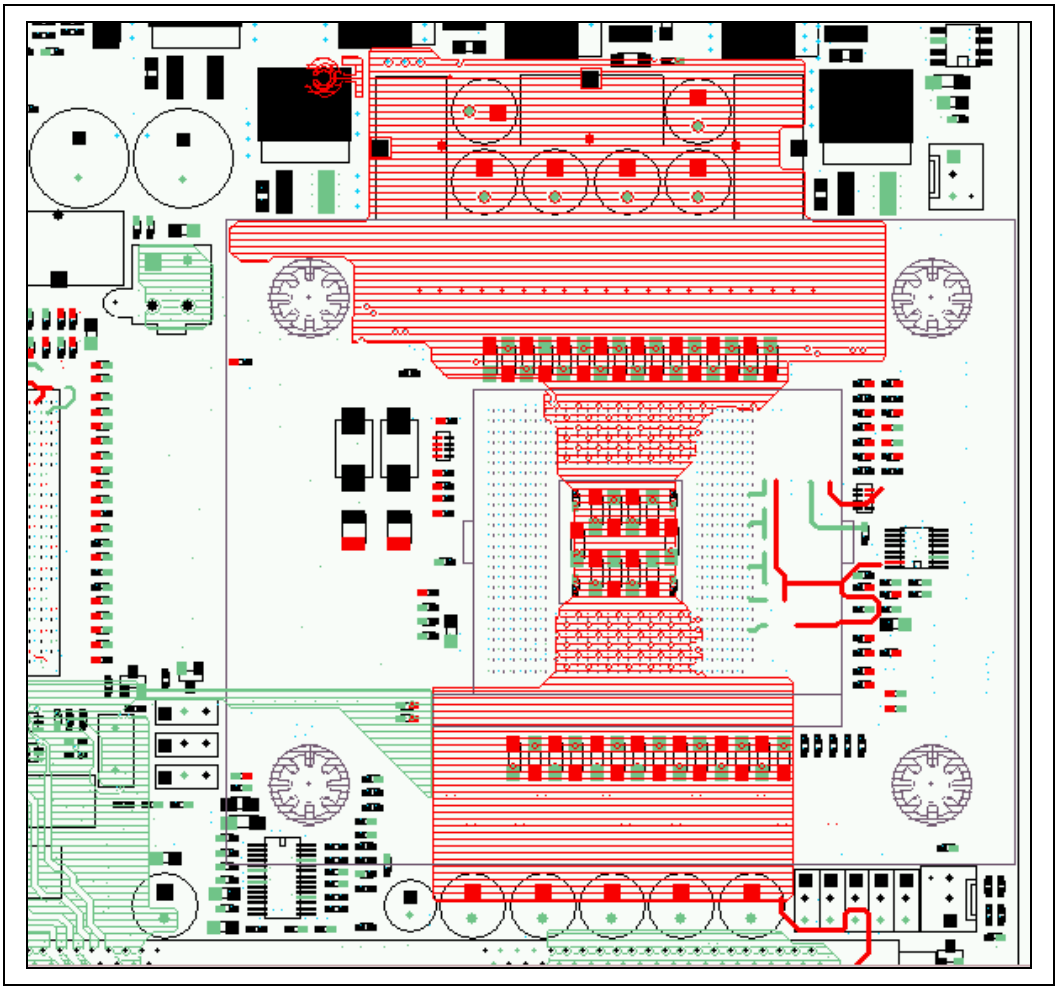
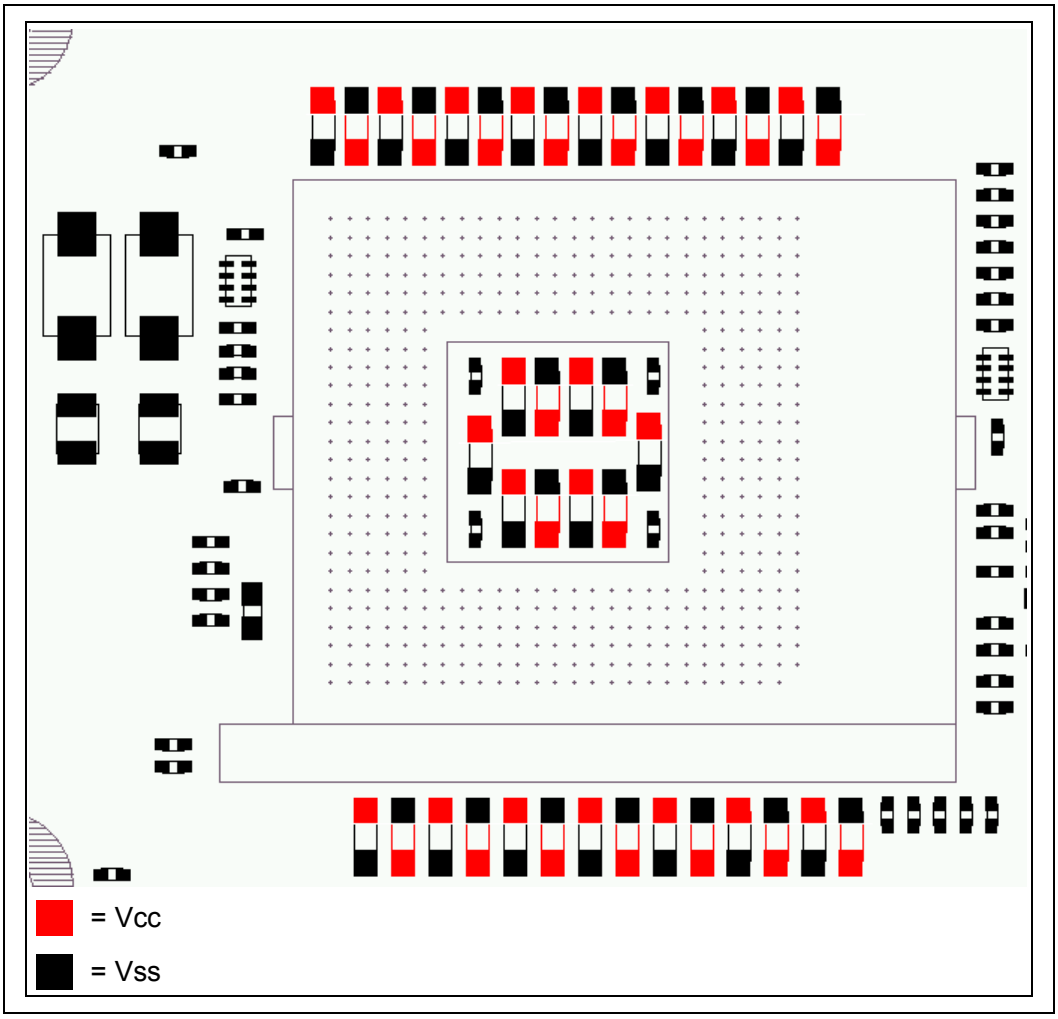


Figure 151. Bottom Layer Power Delivery Shape (VCC_CPU)



The high frequency decoupling capacitors should be placed with alternating VCC_CPU and VSS to provide a better path for power delivery through the capacitor field. An example of this placement is shown in Figure 152.

Figure 152. Alternating VCC_CPU/VSS Capacitor Placement



11.1.6 FMB2 Four–Phase Layout (4-Layer Board)

All four layers in the processor area should be used for power delivery. Two layers should be used for VCC_CPU and two layers should be used for ground. Traces are not sufficient for supplying power to the processor due to the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements shapes that encompass the power delivery part of the processor pin field are required. The following figures show examples of how to use shapes to delivery power to the processor.

Figure 153. Top Layer Power Delivery Shape (VCC_CPU)

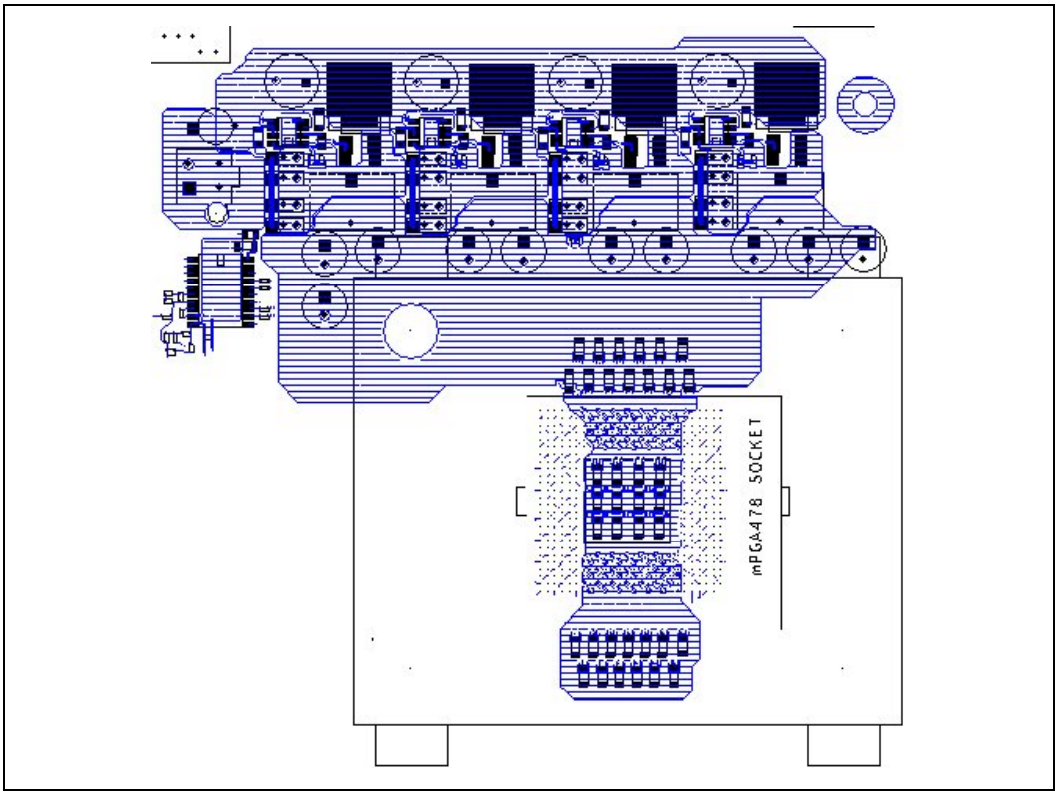


Figure 154. Layer 2 Power Delivery Shape (VSS)

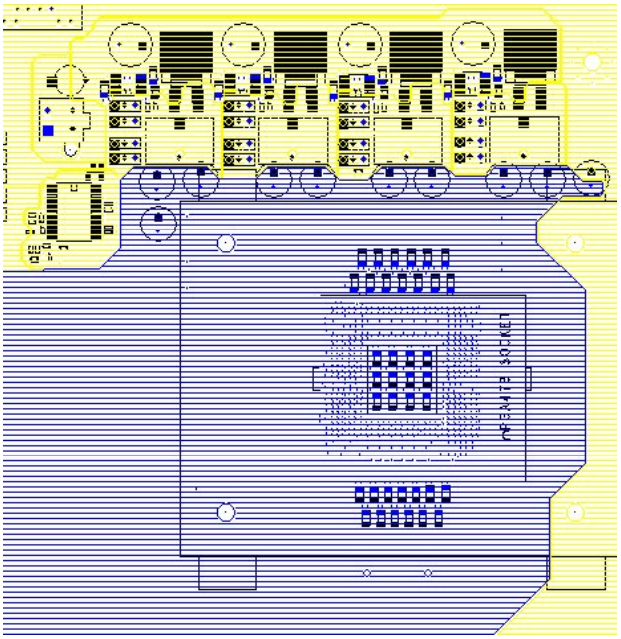


Figure 155. Layer 3 Power Delivery Shape (VSS)

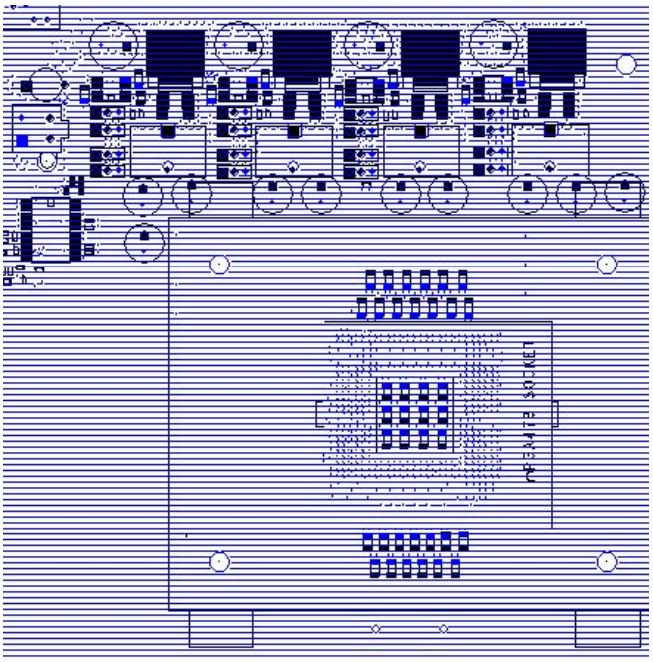
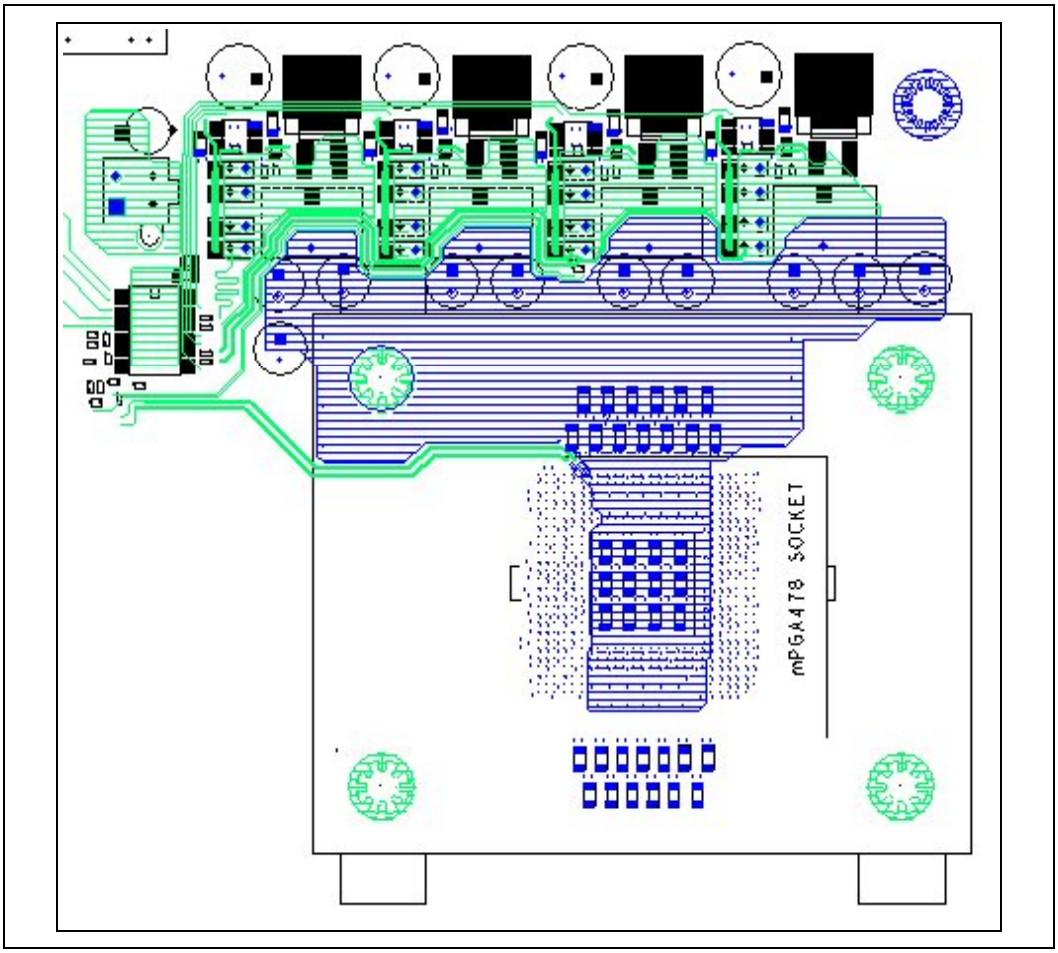


Figure 156. Bottom Layer Power Delivery Shape (VCC_CPU)



11.1.7 FMB2 – Three-Phase Layout (4-Layer Board)

All four layers in the processor area should be used for power delivery. Two layers should be used for VCC_CPU and two layers should be used for ground. Traces are not sufficient for supplying power to the processor due to the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements shapes that encompass the power delivery part of the processor pin field are required. The following figures show examples of how to use shapes to delivery power to the processor.

Figure 157. Top Layer Power Delivery Shape (VCC_CPU)

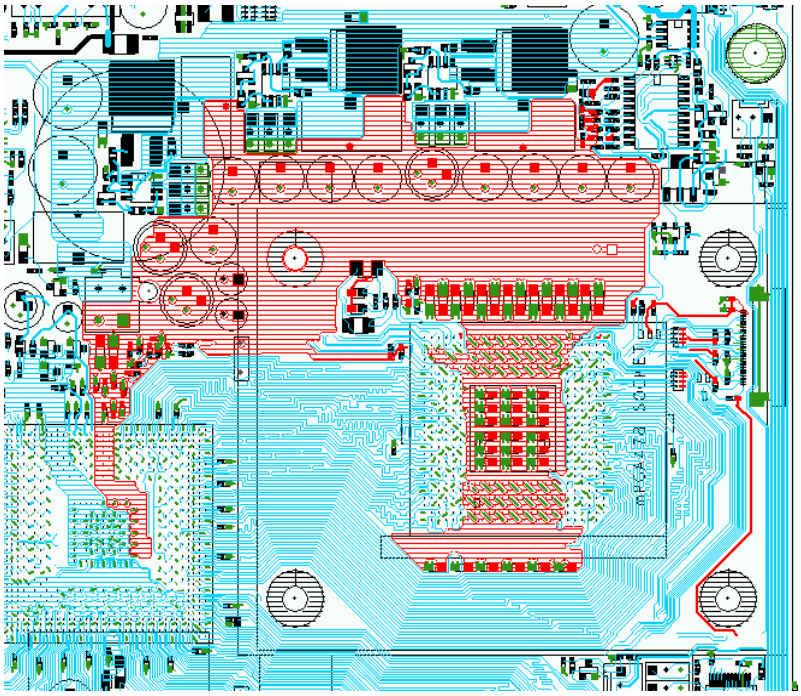


Figure 158. Layer 2 Power Delivery Shape (Vss)

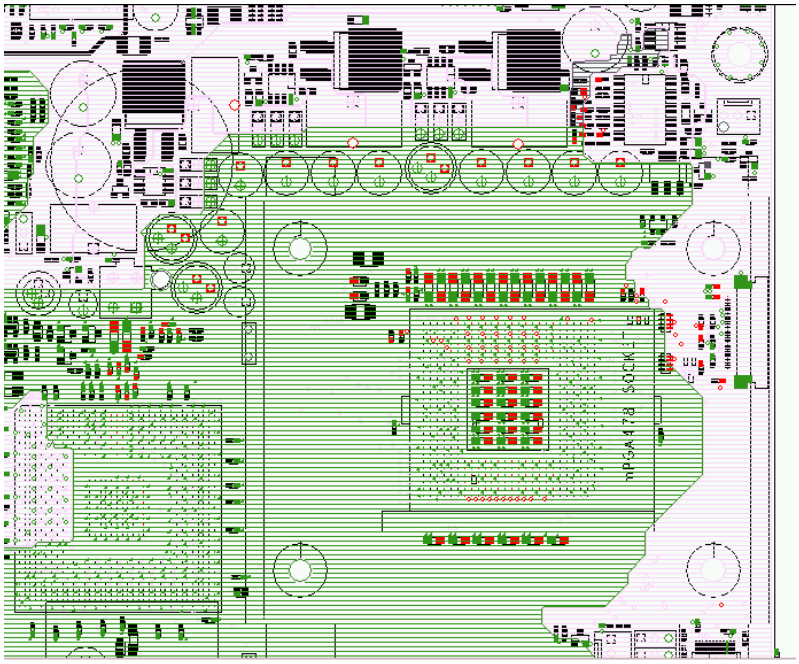


Figure 159. Layer 3 Power Delivery Shape (Vss)

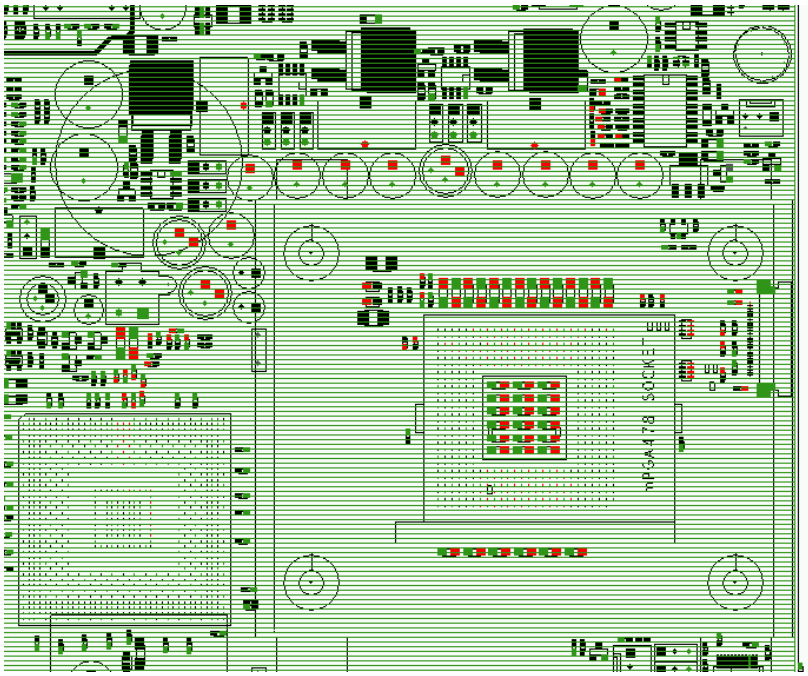
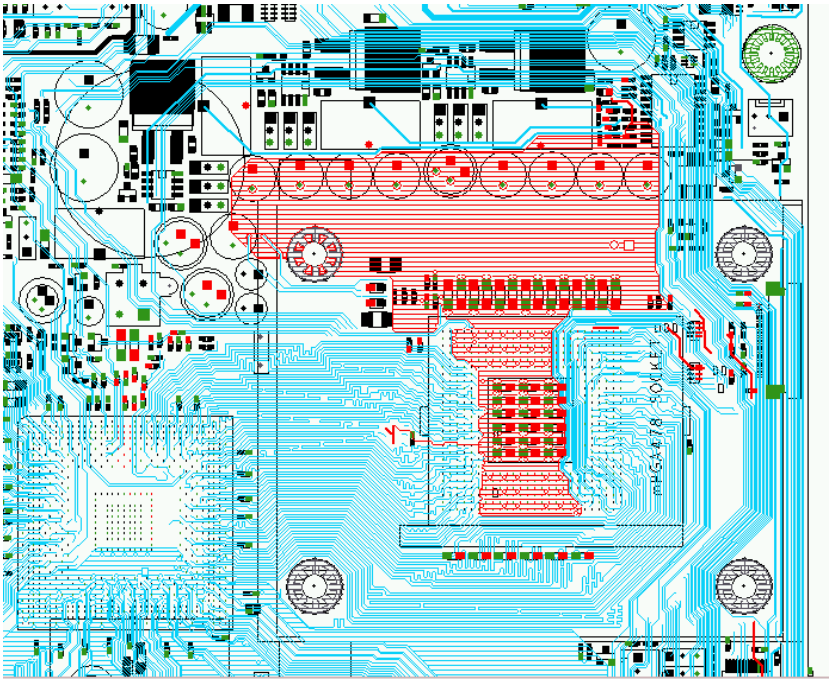


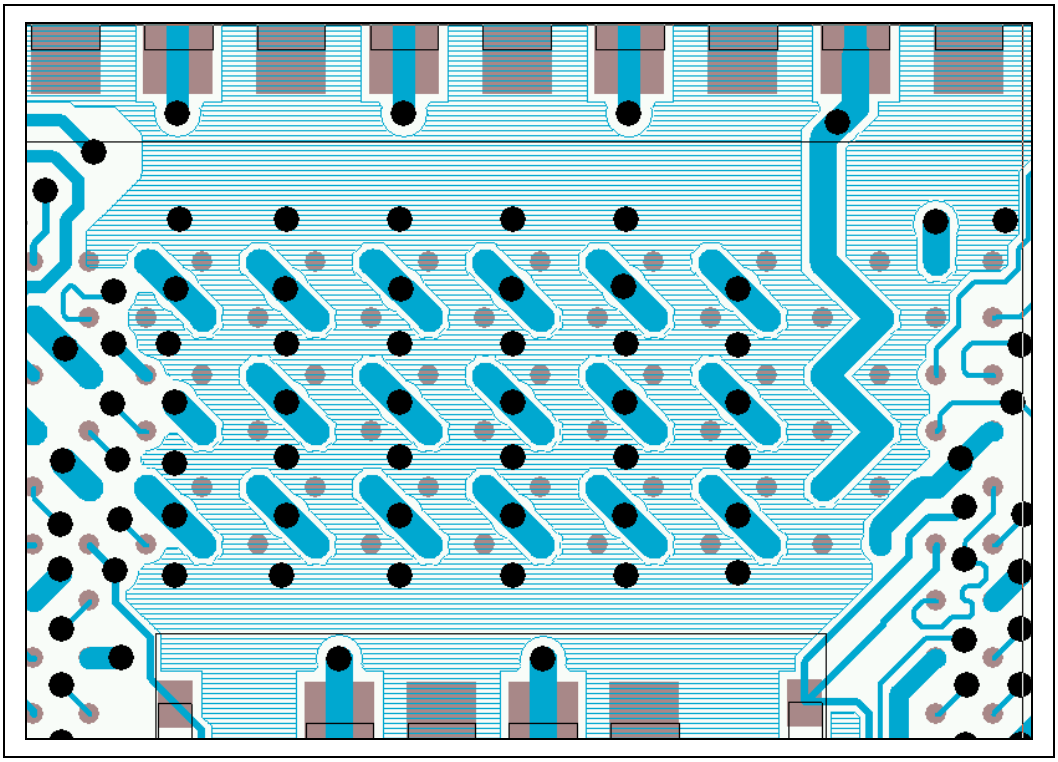
Figure 160. Bottom Layer Power Delivery Shape (VCC_CPU)



11.1.8 FMB1 – Common Layout Issues

The processor socket has 478 pins with 50-mil pitch. The routing of the signals, power and ground pins will require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance of these planes. In order to provide the best path through the via field, it is recommended that vias are shared for every two processor ground pins and for every two processor power pins. Figure 161 illustrates this via sharing.

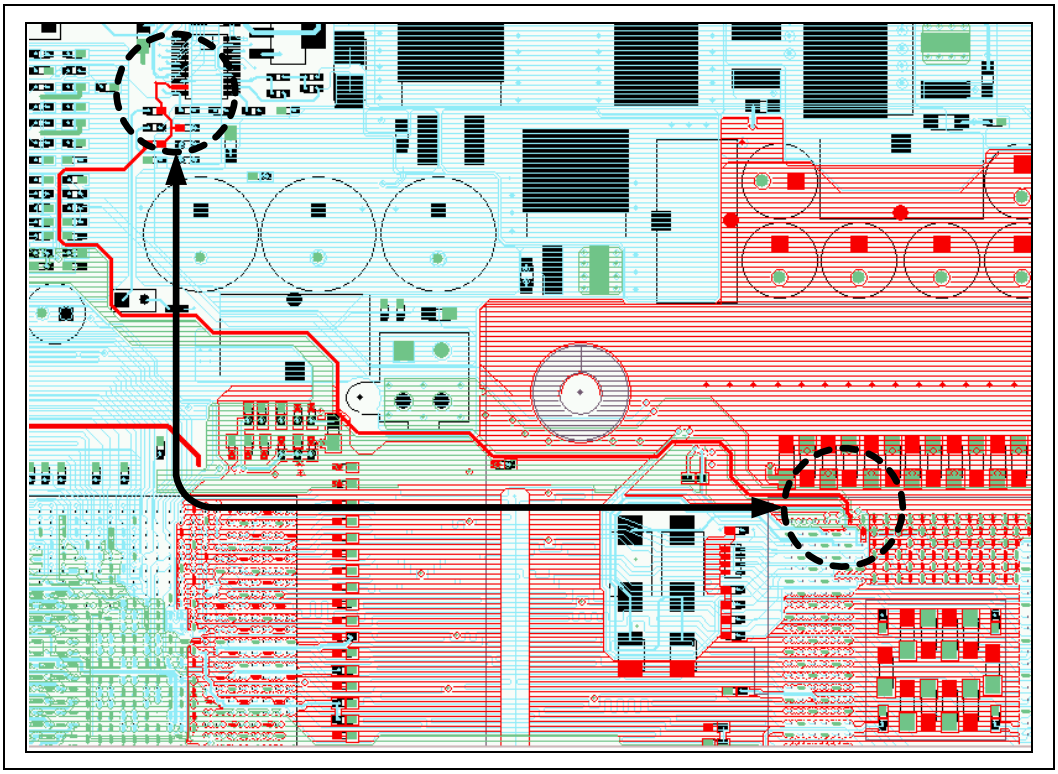
Figure 161. Shared Power and Ground Vias



The switching voltage regulators typically used for processor power delivery require the use of a feedback signal for output error correction. The VCC_SENSE and VSS_SENSE pins on the processor should not be used for generating this feedback. These pins should be used as measurement points for lab measurements only. They can be routed to a test point or via on the back of the motherboard with a trace that is a maximum length of 100 mils for this purpose. The socket loadline defined in the *Intel® Pentium® 4 Processor in the 478-pin Package VR Down Design Guidelines* is defined from pins AC14 (VCC_CPU) and AC15 (VSS) and should be validated from these pins as well. This pins are located approximately in the center of the pin field on the North side of the processor. Feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape.

Figure 162 shows an example routing of the feedback signal. It is routed as a trace from the 1206 capacitor in the Northwest corner of the processor back to the voltage regulator controller. Because the feedback in this case is not taken from the exact point that defines the socket loadline (pins AC14/AC15), it is important to consider any voltage drop from the feedback point to these pins in the design.

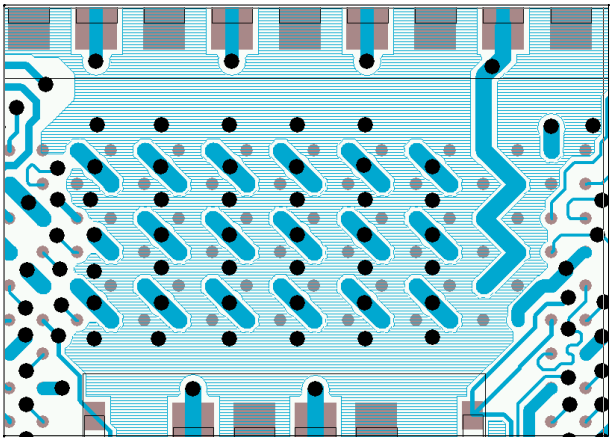
Figure 162. Routing of VR Feedback Signal



11.1.9 FMB2 - Common Layout Issues

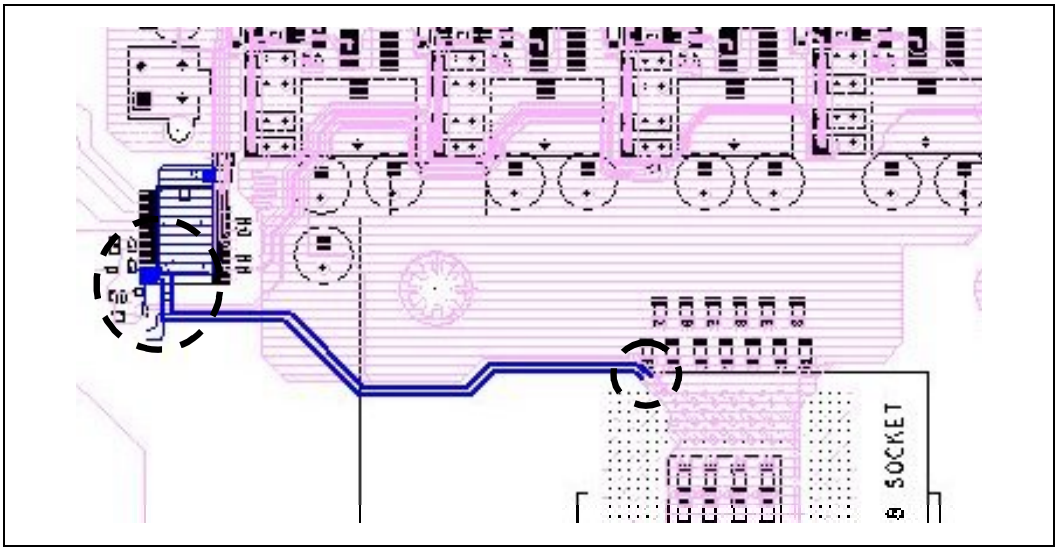
The processor socket has 478 pins with 50-mil pitch. The routing of the signals, power and ground pins will require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance of these planes. To provide the best path through the via field, it is recommended that vias are shared for every two processor ground pins and for every two processor power pins. The following illustrates this via sharing.

Figure 163. Shared Power and Ground Vias



The switching voltage regulators typically used for processor power delivery require the use of a feedback signal for output error correction. The VCC_SENSE and VSS_SENSE pins on the processor should not be used for generating this feedback. These pins should be used as measurement points for lab measurements only. They can be routed to a test point or via on the back of the motherboard with a trace that is a maximum length of 100 mils for this purpose. The socket loadline defined in the *Intel® Pentium® 4 Processor VR Down Design Guidelines* is defined from pins AC14 (VCC_CPU) and AC15 (VSS) and should be validated from these pins as well. These pins are located approximately in the center of the pin field on the North side of the processor. Feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape. Figure 164 shows an example routing of the feedback signal. It is routed as a trace from the 1206 capacitor in the Northwest corner of the processor back to the voltage regulator controller. Because the feedback in this case is not taken from the exact point that defines the socket loadline (pins AC14/AC15), it is important to consider any voltage drop from the feedback point to these pins in the design.

Figure 164. Routing of VR Feedback Signal



11.2 Thermal Considerations

11.2.1 FMB1

For a power delivery solution to meet the flexible motherboard (FMB) requirements, it must be able to delivery a fairly high amount of current. This high amount of current also requires that the solution is able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow and layout to ensure adequate thermal performance of the processor power delivery solution.

11.2.2 FMB2

For a power delivery solution to meet the flexible motherboard (FMB2) requirements, it must be able to delivery a high amount of current. This high amount of current also requires that the solution is able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow and layout to ensure adequate thermal performance of the processor power delivery solution.

The table below shows the required amount of airflow needed for the documented designs to meet FMB2 specifications and component thermal requirements.

Table 52. Airflow Requirements

Design Example	Minimum Airflow	Notes
Three-Phase	110 LFM	1
Four-Phase	0 LFM	2

NOTES:
1. Assumes dedicated fan for Voltage Regulator (VR).
2. Assumes expanded layout area as compared to the three-phase VR design.

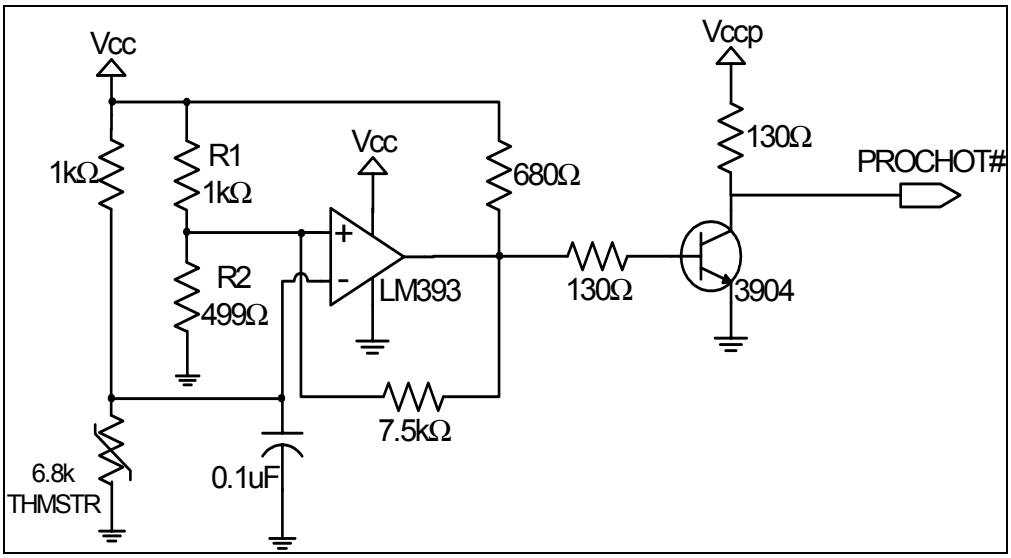
11.2.3 FMB2 - Voltage Regulator Thermal Protection Circuit

Intel recommends that the 845 and 850 chipset system boards be designed to support the full *Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process FMB2 Guidelines.* These guidelines include an ICC_MAX of 70 A and a VR_TDC (VR thermal design Current) of 63 A. The processor voltage regulator (VR) solution should be designed to support the ICC_MAX of 70 A electrically for brief time periods. The voltage regulator solution should also be designed to support a minimum of 63 A VR_TDC indefinitely within the envelope of operating conditions of the system. The VR_TDC limits of the system board are typically governed by the system board thermal limits. Intel recommends that system boards designed to the above guidelines implement a VR thermal monitor circuit.

Note: The specifications for the Pentium 4 processor with 512-KB L2 Cache on 0.13 micron process are contained in the In*tel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Processor Electrical, Mechanical, and Thermal Specifications (EMTS).* In the event the above numbers differ from the EMTS, the EMTS numbers should be considered correct.

The bi-directional PROCHOT# pin on the processor may be used to implement a thermal monitor for the processor VR. When PROCHOT# is asserted by a VR thermal monitor the thermal control circuit in the processor will activate and will reduce the current consumption of the processor. This mechanism should only be used as a safety mechanism for the VR. The thermal monitor circuit should not degrade the processor performance during normal operation. PROCHOT# should only be asserted in the event of a failure that causes VR over temperature. In order for this type of thermal monitor to act as a safety device for the system board, it is important that the thermal time constant of the VR is longer than the thermal time constant of the processor combined with its thermal solution.

Figure 165. Example Circuit That Can Be Used As a Thermal Monitor



3.

For this circuit implementation, the thermistor (THMSTR) should be placed in the hottest area of the VR. As the thermistor heats up its resistance goes down. This creates an error voltage based on the resistance of the thermistor and the voltage reference provided by R1 and R2. The values of R1 and R2 should be adjusted to calibrate the circuit for a specific system board design so that it asserts PROCHOT# when the VR reaches its thermal limit. The values for R1 and R2 in Figure 1 are included as an example. The value of R2 is adjusted to calibrate the circuit so that PROCHOT# is asserted when the VR reaches its thermal limit in the system that it is intended to operate. An adequate VR cooling solution should be implemented such that VR_TDT current levels can be maintained indefinitely.

11.3 Simulation

11.3.1 FMB1

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 166.

Figure 166. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board

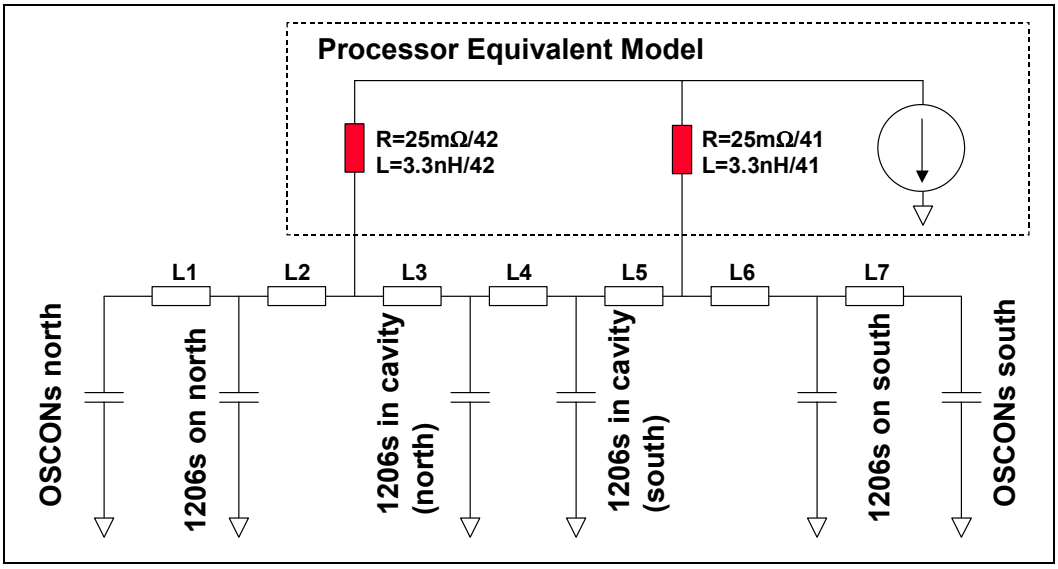


Table 53 lists model parameters for the system board shown in Figure 166.

Table 53. Intel® Pentium® 4 Processor Power Delivery Model Parameters

Segment	Resistance	Inductance
L1	0.24 mΩ	29 pH
L2	0.23 mΩ	37 pH
L3	0.293 mΩ	68 pH
L4	0.144 mΩ	27 pH
L5	0.293 mΩ	68 pH
L6	0.14 mΩ	35 pH
L7	0.14 mΩ	28 pH

11.3.2 FMB2

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 167.

Figure 167. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board

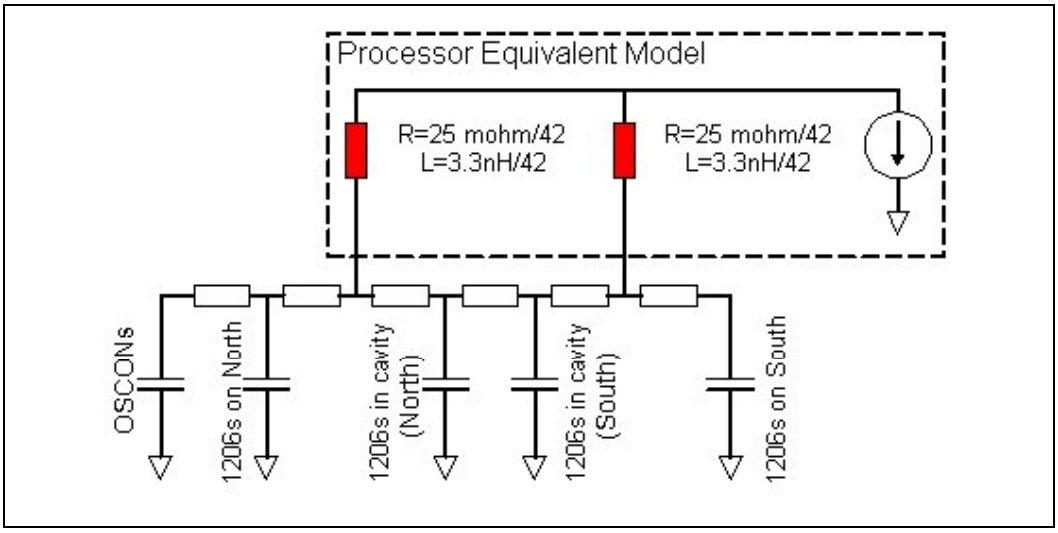


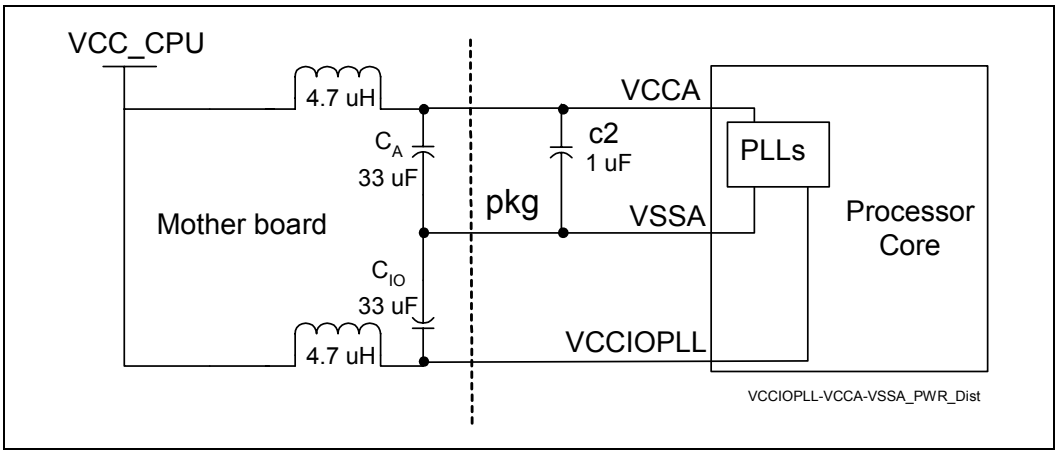
Table 54. Intel® Pentium® 4 Processor Power Delivery Model Parameters

Segment	Resistance	Inductance
L1	0.27 mΩ	80 pH
L2	0.33 mΩ	11.3 pH
L3	0.392 mΩ	104 pH
L4	0.196 mΩ	52 pH
L5	0.392 mΩ	104 pH
L6	0.64 mΩ	200 pH

11.4 Filter Specifications For VCCA, VCCIOPLL, and VSSA

VCCA and VCCIOPLL are power sources required by the PLL clock generators on the processor silicon. Since these PLLs are analog in nature they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation these supplies must be low pass filtered from VCC_CPU. The general desired filter topology is shown in Figure 168. Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

Figure 168. Typical VCCIOPLL, VCCA and VSSA Power Distribution



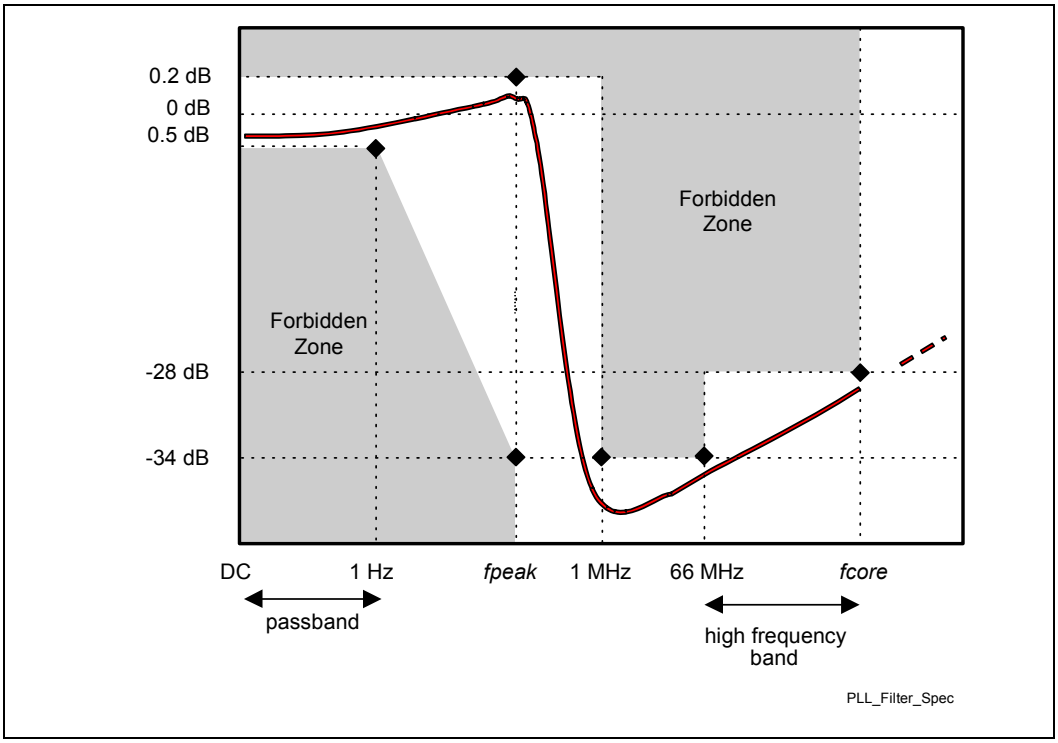
The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity this document will address the recommendation for the VCCA filter design. The same characteristics and design approach is applicable for the VCCIOPLL filter design.

Note: The 1 µF package capacitor in Figure 168 does not exist on the Pentium 4 processor in the 478-pin package. It is present for the Pentium 4 processor with 512-KB L2 cache on .13 micron process only.

The AC low-pass recommendation, with input at VCC_CPU and output measured across the capacitor (C_A or C_{IO} in Figure 168), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- 34 dB attenuation from 1 MHz to 66 MHz
- 28 dB attenuation from 66 MHz to core frequency
- The filter recommendation (AC) is graphically shown in Figure 169.

Figure 169. Filter Recommendation



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore* (core frequency).
3. *fpeak*, if existent, should be less than 0.05 MHz.

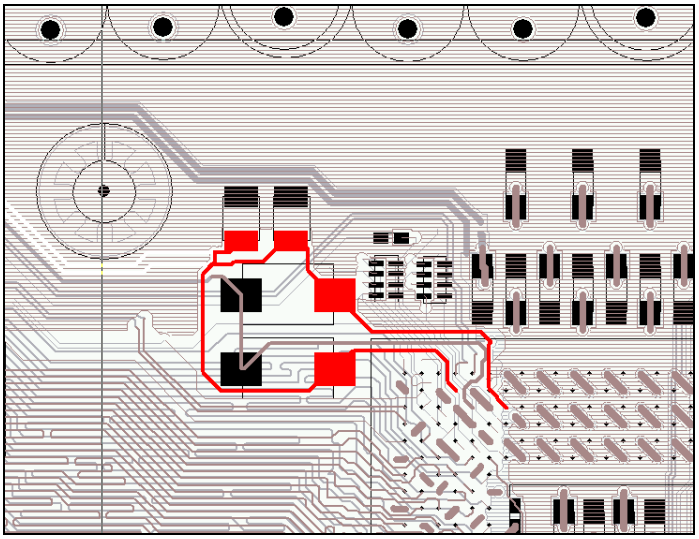
Other Recommendations

- Use shielded type inductors to reduce crosstalk
- Capacitors for the filter can be any value between 22 µF and 100 µF as long components with ESL ≤ 5 nH and ESR < 0.3 Ω are used.
- Values of either 4.7 uH or 10 uH may be used for the inductor. Filter should support DC current > 60 mA
- DC voltage drop from VCC_CPU to VCCA should be < 60 mV
- In order to maintain a DC drop of less than 60 mV, the total DC resistance of the filter from VCC_CPU to the processor socket should be a maximum of 1 Ω.

Other Routing Requirements

- C should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in Figure 170.
- VCCA route should be parallel and next to VSSA route (minimize loop area)
- A minimum of a 12 mil trace should be used to route from the filter to the processor pins.
- L should be close to C

Figure 170. Example Component Placement for PLL Filter



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12 Power Distribution Guidelines

12.1 Definitions

Suspend-To-RAM (STR) In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.

Full-power operation: During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state and the S1 (CPU stop-grant state) state.

Suspend operation: During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).

Core power rail: A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply.

Standby power rail: A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is: 5VSB (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.

Derived power rail: A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator.

Dual power rail: A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

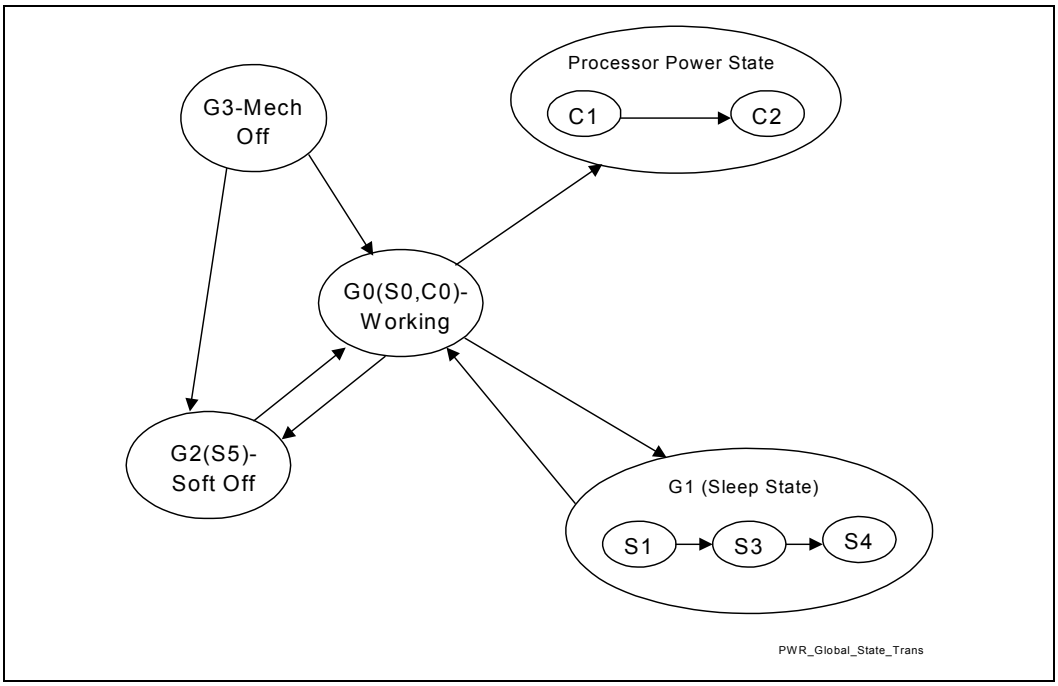
12.2 Power Management

The Intel 850 chipset-based platform implements the ACPI mechanisms software and hardware that enables the system to minimize system power consumption, manage system thermal limits, and maximize the battery life. This implementation involves tradeoffs among system speed and noise.

12.2.1 ACPI Hardware Model

The Intel 850 chipset-based desktop supports both legacy and ACPI operations, which involves sequencing the platform between the various global system states (G0–G3). Figure 171 depicts global states and the transitions. For complete detail of the mechanisms involved in transition from any of the global states refer to the *ACPI Interface Specification 1.0a, Section 4.5*.

Figure 171. Global System Power States and Transition



12.2.2 Thermal Design Power

The thermal design power numbers are estimation of the maximum expected power generated by a component in a realistic application. It is based on extrapolations in both hardware and software technology over the product life. It does not represent the expected power generated by a power virus. The ICC max sustained (WCRA) numbers are estimation of the maximum expected current generated within a die section in a realistic application such as an application that executes extensive memory reads/writes.

Refer to the *Intel® 850 Chipset: Thermal Considerations Application Note (AP-720)* and the *Intel® 850 Chipset: 82850 Memory Controller Hub (MCH) Datasheet* for additional thermal package characteristics.

Table 55. Intel® 850 Chipset and Intel® ICH2 Thermal Design Power

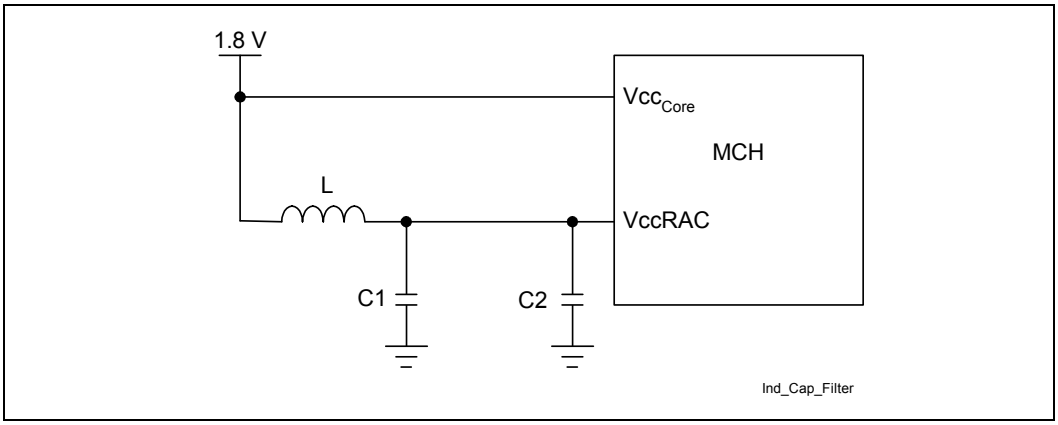
Parameter	Icc Max Sustainable Current (A) S0)
MCH • MCH (UP) Typical Thermal Design Power = 5.8 W • MCH (UP) Maximum Thermal Design Power = 8.0 W	
1.8 V Core	3.2
1.5 V VDDQ AGP I/O	0.37
1.6 V VTT	2.2
ICH2 • Max Thermal Design Power = 1.6 W ±15%	
1.8 V Main Logic	0.30
1.8 V (Stand By) Resume Logic + 1.8 V LAN	0.040
3.3 V Main I/O	0.41
3.3 V (Stand By) Resume Logic	0.062
RTC	.04 (G3)
Processor I/F (1.3 ~ 2.5)	200 uA

NOTE: Remember that values stated for the maximum sustainable current (Icc) of the ICH2 are maximum preliminary measurements, and are subject to change.

12.3 1.8 V RAC Isolation Solution

The MCH requires a low-pass filter on the VccRAC pins to meet clock jitter specifications. The two possible filter solutions may be configured as either an inductor-capacitor (LC) or ferrite bead-capacitor filters. For more details, see Figure 172 and Figure 173. The inductor or ferrite bead must have a minimum current capacity of 500 mA and a maximum DC resistance of 100 mΩ. DC drop is a concern due to the series element between the RAC and 1.8 V supply. The VccRAC pins for the MCH are given in Table 56.

Figure 172. Inductor-Capacitor Filter Circuit

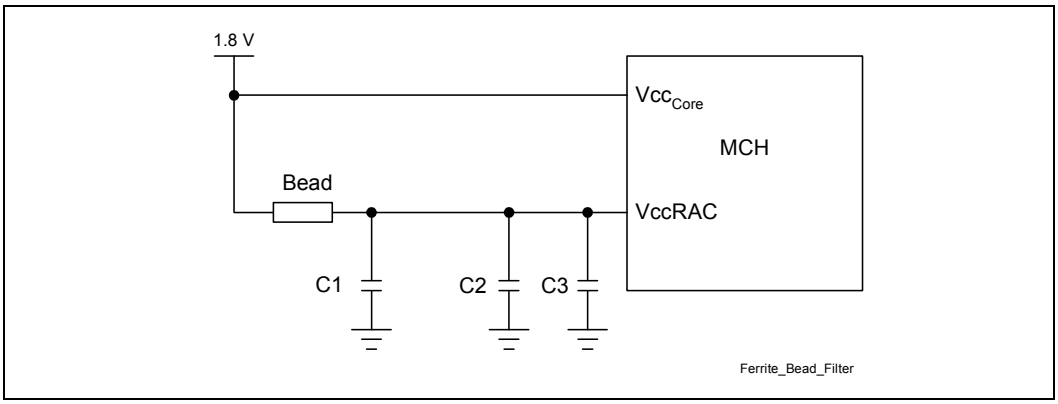


Simulations and validations indicate that L = 3.3 nH and C_1 = 3.3 µF forms an adequate inductor-capacitor filter. The filter must be located within 2-inches the device and the layout of VccRAC connections should follow high-speed design practices.

In addition to the low-pass filter, the RAC requires local decoupling capacitors. These decoupling capacitors should be located close to the RAC pins to control self-induced RAC noise. For the inductor-capacitor filter, two to three 0.1 µF capacitors (C_2) for both RACs should provide adequate decoupling between VccRAC and VSS.

The inductor-capacitor filter and its associated decoupling capacitors can be implemented using 0805 size components.

Figure 173. Ferrite Bead Filter Circuit



As an alternate solution, a 10 Ω (@ 100 MHz) and 10 µF forms an adequate ferrite bead-capacitor filter. The filter must be located within 2-inches the device and the layout of VccRAC connections should follow high-speed design practices.

In addition to the ferrite bead filter, the RAC requires local decoupling capacitors. These decoupling capacitors should be located close to the RAC pins to control self-induced RAC noise. For the ferrite bead filter, use a minimum number of two 0.1 µF capacitors (C_2) per RAC, and a minimum of one 1.0 µF capacitor (C_3) for both RACs should be sufficient. The layout of the capacitor connections should follow high-speed design practices.

The ferrite bead filter and its associated decoupling capacitors can also be implemented using 0805 components except for the 10 µF capacitor, which is a 1206 size component.

Table 56. Intel® MCH 1.8 V RAC Pinout

Intel® MCH 1.8 V RAC Pinout Location	Channel A	Channel B
Ball	T22	C16
	N22	F15
	J22	F14
	J20	C13
	R19	E9
	P19	C9

Figure 174. Customer Reference Board Layout Example

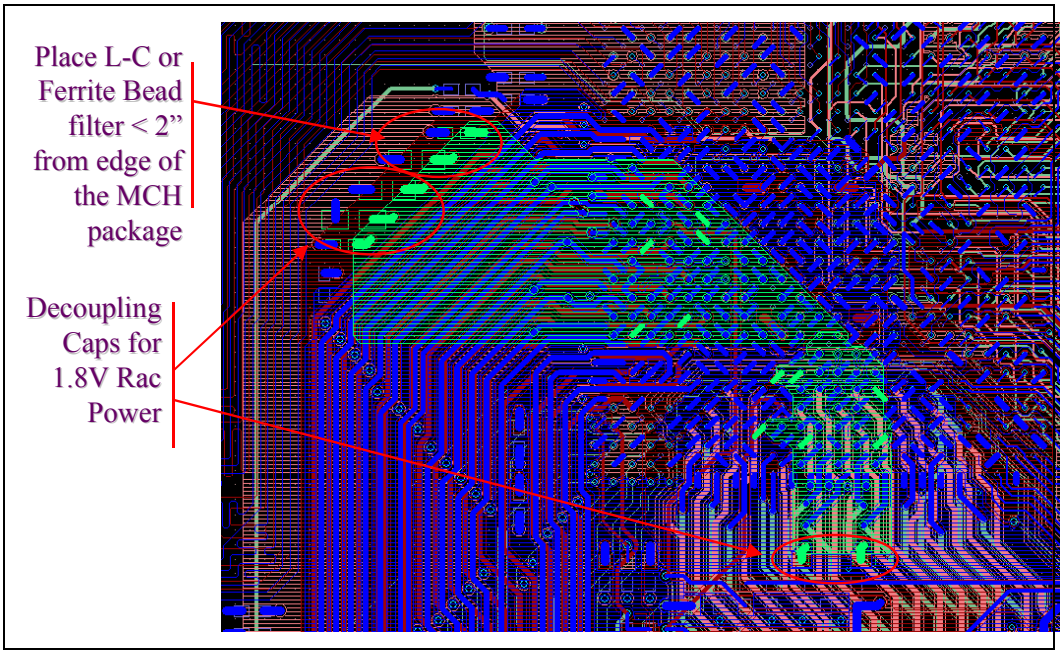


Figure 175. Customer Reference Board Layout Example (Bottom – Layer 6)

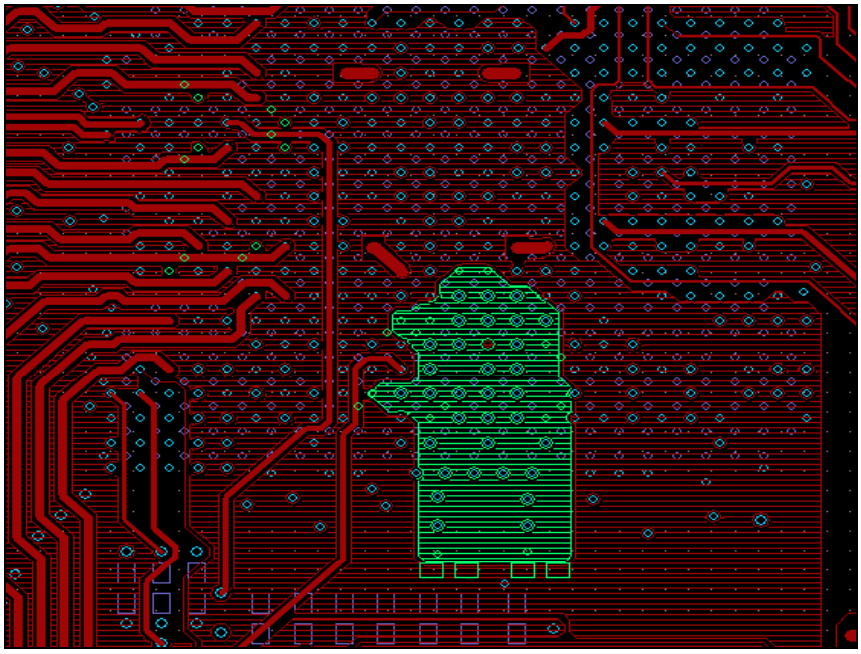
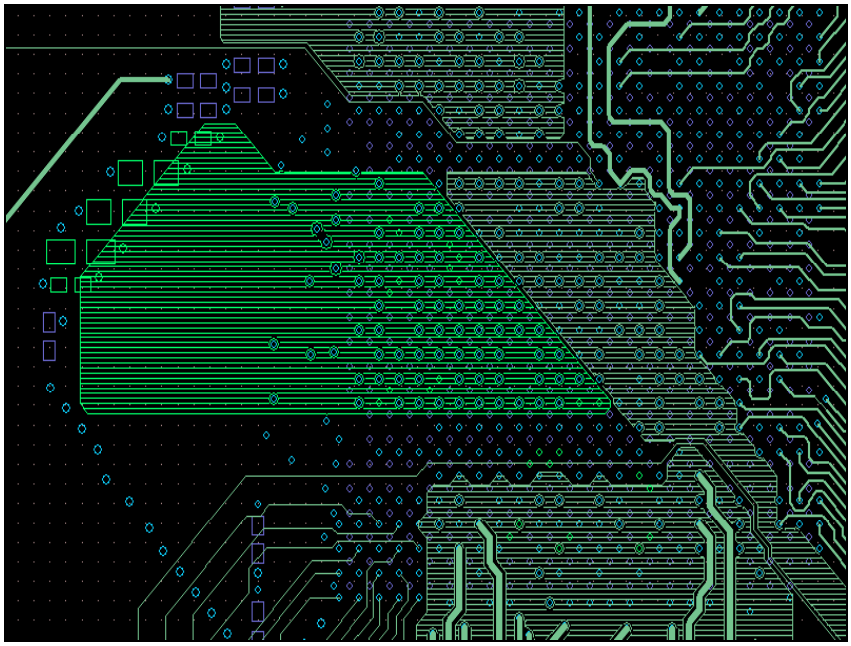


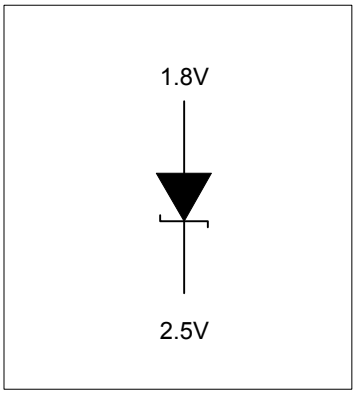
Figure 176. Customer Reference Board Layout Example (Signal 2 – Layer 4)



12.4 Vterm/Vdd Power Sequencing Requirement

Power to the RDRAM device termination resistors (Vterm) must follow the power to the RDRAM device Core. A Schottky diode can be placed between the 1.8 V and 2.5 V to ensure this power-up sequence.

Figure 177. 1.8 V and 2.5 V Power Sequence (Schottky Diode)



12.5 Intel® 850 Chipset Power Sequencing Requirements

The Intel® 850 chipset needs the following power supplies for operation – VCC1_8, VDDQ and VTT.

To avoid forward-biasing the ESD protection-diodes from the IO to Core power supplies, it is necessary that the VCC1_8 power supply ramp up ahead (See Figure 178) of the VDDQ and VTT power supplies. For the same reason, it is necessary to have the VCC1_8 power supply ramp down later than the VDDQ and VTT power supplies. If this cannot be guaranteed, it is important that the VCC1_8 power supply lag (see Figure 179) the I/O supplies by no greater than 1.0 V. There are no dependencies between VDDQ and VTT supplies.

Figure 178. Desired Mode of Power Sequencing

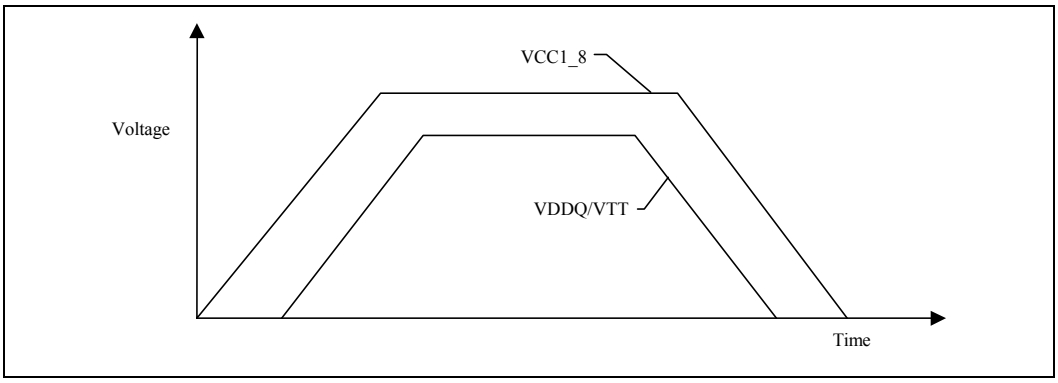
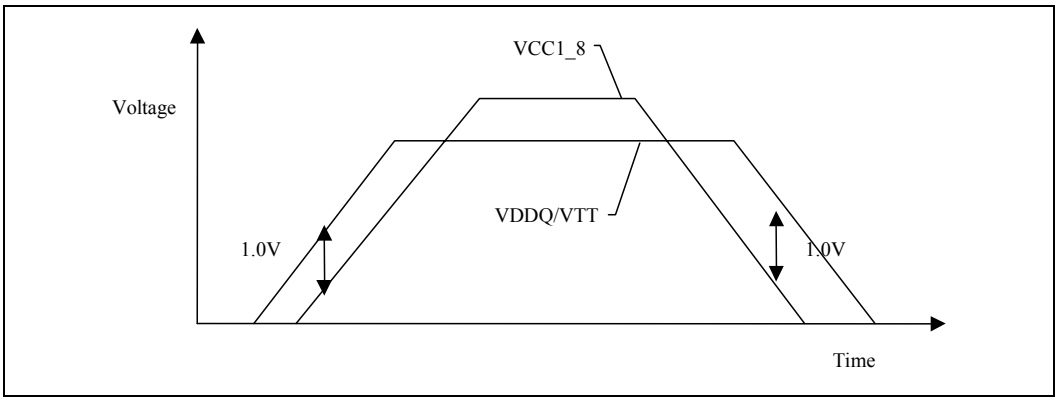


Figure 179. Optional Mode of Power Sequencing



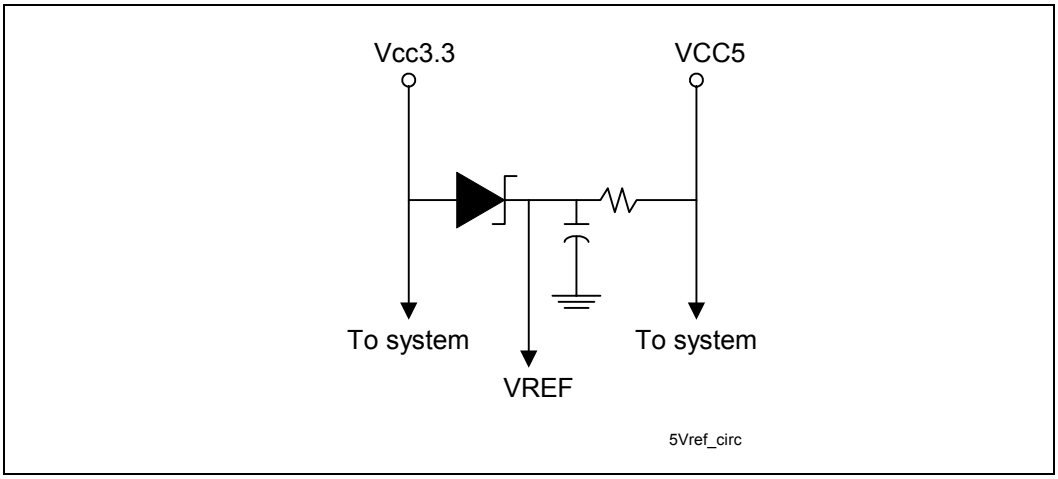
12.6 Intel® ICH2 V5REF and Vcc3.3 Sequencing Requirement

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within .7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 180 shows a sample implementation of how to satisfy the V5REF/3.3 V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend, the only signals that are 5 V tolerant capable are USB OC[3:0]#. If these signals are not needed during suspend, V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX. If OC[3:0]# is needed during suspend and 5 V tolerance is required then V5REF_SUS should be connected to 5V_Always/5V_AUX, but if 5 V tolerance is not needed in suspend, then V5REF_SUS can be connected to either VccSus3_3 or 5 V_Always/5V_AUX rails.

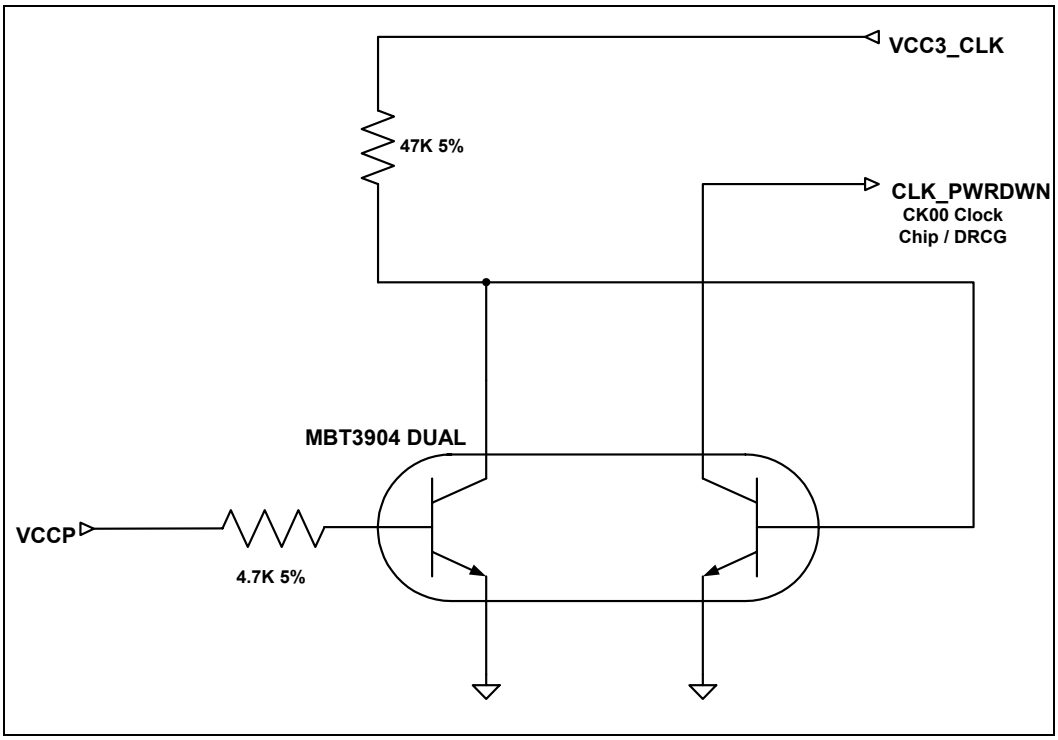
Figure 180. V5REF Sequencing Circuit



12.7 CPU / CK00 Power Sequencing Requirement

To ensure that the correct processor system bus frequency is set, the CPU BSELx pins must be at an operating state before the CK00 clock chip powers up. An example circuit is shown below.

Figure 181. CPU/CK00 Sequencing Circuit



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13 Debug Port Routing Guidelines

In Pentium 4 processor in the 478-pin package based systems, the debug port should be implemented as an on-board debug port.

Refer to the latest revision of the *Pentium® 4 Processor in the 478-pin Package Debug Port Design Guide* for details on the implementation of the debug port.

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14 Debug Tools Specifications

14.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Pentium 4 processor in the 478-pin package systems. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of these systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a system that can make use of an LAI: mechanical and electrical.

14.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor package. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include space normally occupied by the processor heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

14.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

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15 Schematic Review Checklist

15.1 Processor Checklist (All Signals)

All signals of the processor are provided in this section.

Checklist Items	Recommendations	Reason/Impact/Documentation
A[35:3]#	• Connect A[31:3]# to MCH. Leave A[35:32]# as No Connect.	• Chipset does not support extended addressing over 4 GB, leave A[35:32]# unconnected. • AGTL+ source synch I/O signal
A20M#	• Connect to ICH2. No pull-up required.	• Asynch GTL+ Input Signal • Refer to Section 5.4.1.2.
ADS#	• Connect to MCH	• AGTL+ common clock I/O signal
ADSTB[1:0]	• Connect to MCH	• AGTL+ source synch I/O signal
AP[1:0]#	• Leave as No Connect	• Chipset does not support parity protection on the address bus. • AGTL+ common clock I/O signal
BCLK[1:0]	• Connect to CK00 clock. Refer to clock routing guidelines in the latest revision of the design guide. • Connect 33 Ω series resistor on each clock signal. • Connect a “shunt source termination (Rt)” resistor to GND for each signal on processor side of the series resistor. The Rt value should be 49.9 Ω ±1% for 50 Ω MB impedance.	• Rt resistors should be selected to match the characteristic impedance of the board. • System bus clock signal • Refer to Section 4.1of this document.
BINIT#	• Leave as No Connect.	• Chipset does not support this signal. • AGTL+ common clock I/O signal
BNR#	• Connect to MCH	• AGTL+ common clock I/O signal
BPRI#	• Connect to MCH	• AGTL+ common clock input signal

Checklist Items	Recommendations	Reason/Impact/Documentation
BR0#	• Terminate to VCC_CPU with a 51Ω 5% resistor near the processor. Connect to the MCH.	• The Intel 850 chipset contains on-die termination for the BR0# signal. The processor does not contain on-die termination for this particular AGTL+ signal; thus, external termination is required only on the processor end. BR0# termination should equal the resistance value of on die AGTL+ termination resistance (Rtt) value. • AGTL+ common clock I/O signal • Refer to Section 5.4.1.6.
BSEL[1:0]	• Leave as no connect for 82850. Refer to Section 4.2.1 • Connect BSEL0 to CK00 pin SEL100/133 with a 1 kΩ ±5% resistor pull-up to VCC3_CLK for 82850E. Leave BSEL1 as no connect. See Section 4.2.2.	• 82850 – 100 MHz system bus only • 82850E – 100 MHz or 133 MHz system bus
COMP[1:0]	• Terminate to GND with a 51.1Ω ±1% resistor as close as possible to the pin.	• Each COMP pin requires a separate resistor for each pin. • Refer to Section 5.4.1.7
D[63:0]#	• Connect to MCH	• AGTL+ source synch I/O signal
DBI[3:0]	• Connect to MCH	• AGTL+ source synch I/O signal
DBSY#	• Connect to MCH	• AGTL+ common clock I/O signal
DEFER#	• Connect to MCH	• AGTL+ common clock input signal
DP[3:0]#	• Leave as No Connect	• Chipset does not support Enhanced Data Bus Parity. • AGTL+ common clock I/O signal
DRDY#	• Connect to MCH	• AGTL+ common clock I/O signal
DSTBN[3:0]	• Connect to MCH	• AGTL+ source synch I/O signal
DSTBP[3:0]	• Connect to MCH	• AGTL+ source synch I/O signal
FERR#	• Terminate to VCC_CPU with a 62Ω ±5% resistor near the processor. • Connect to ICH2.	• This output signal is not terminated on the processor. Termination is required on the system board. • Asynch GTL+ output signal • Refer to Section 5.4.1.1.
GTLREF[3:0]	• Should be set to 2/3 of VCC_CPU. Processor should have at least 1 dedicated voltage divider for GTLREF signals. Requires a 49.9 Ω ±1% termination resistor to VCC_CPU and a 100 Ω ±1% pull-down resistor to GND as well as additional decoupling capacitors depending on topology.	• Correct settings are critical. This signal controls the signal reference of the AGTL+ input pins. • Refer to Section 5.2.
HIT#	• Connect to MCH	• AGTL+ Common Clock I/O Signal
HITM#	• Connect to MCH	• AGTL+ Common Clock I/O Signal

Checklist Items	Recommendations	Reason/Impact/Documentation
IERR#	• Leave as a No Connect	• Chipset does not support this signal. • Asynch GTL+ output signal.
IGNNE#	• Connect to ICH2. • No pull-up required.	• Termination not required. • Asynch GTL+ input signal. • Refer to Section 5.4.1.2.
INIT#	• Connect to ICH2 and Firmware Hub (FWH). • Voltage translation is required for this signal to meet the input threshold levels of the FWH.	• Termination not required. • Asynch GTL+ input signal. • Refer to Section 5.4.1.3.
LINT[1:0]	• Connect to ICH2. LINT[1] connects to ICH2 NMI and LINT[0] connects to ICH2 INTR. • No pull-up required.	• Asynch GTL+ Input Signal. • Refer to Section 5.4.1.2.
LOCK#	• Connect to MCH	• AGTL+ common clock I/O signal
MCERR#	• Leave as No Connect	• Chipset does not support this signal. • AGTL+ common clock I/O signal
PROCHOT#	• Terminate to VCC_CPU with a 62 Ω ±5% resistor near the processor. • Voltage translation may be required if this signal is connected to external logic.	• Asynch GTL+ output signal • Refer to Section 5.4.1.1.
PWRGOOD	• Terminate to VCC with a 300 Ω ±5% resistor. • Connect to ICH2.	• Asynch GTL+ input signal • Refer to Section 5.4.1.4.
REQ[4:0]#	• Connect to MCH	• AGTL+ source synch I/O signals
Reserved	• Reserved signals must remain as a No Connect.	•
RESET#	• Terminate to VCC_CPU with a 51 Ω ±5% resistor near the processor. • Connect to the MCH.	• AGTL+ common clock input signal
RS[2:0]#	• Connect to MCH	• AGTL+ common clock input signal
RSP#	• Leave as No Connect.	• Chipset does not support this signal. • AGTL+ common clock input signal
SKTOCC#	• Connect to glue logic if pin is used.	• Processor pulls this signal to GND. System board designers may use this pin to determine if the processor is present in the socket.
SLP#	• Connect to ICH2. • No pull-up required.	• Asynch GTL+ input signal • Refer to Section 5.4.1.2.

Checklist Items	Recommendations	Reason/Impact/Documentation
SMI#	• Connect to ICH2. • No pull-up required.	• Asynch GTL+ input signal • Refer to Section 5.4.1.2.
STPCLK#	• Connect to ICH2. • No pull-up required.	• Asynch GTL+ input signal • Refer to Section 5.4.1.2.
TESTHI	Refer to Section 5.4.1.11 for more information.	• Tying any of the TESTHI pins together will prevent the ability to perform boundary scan testing. • Refer to processor datasheet.
THERMTRIP#	• Terminate to VCC_CPU via 62 Ω ±5% resistor. • Voltage translation may be required if this signal is connected to external logic.	• Asynch GTL+ output signal • Refer to Section 5.4.1.1.
TRDY#	• Connect to MCH	• AGTL+ common clock input signal
VCCA	• Connect with isolated power circuitry to VCC_CPU.	• Isolated power for internal processor system bus PLLs. • Refer to Section 11.4.
VCCIOPLL	• Connect with isolated power circuitry to VCC_CPU.	• Isolated power for internal processor system bus PLLs • Refer to Section 11.4.
VCC_SENSE	• Connect to additional glue logic if used. This signal is an output signal.	• Isolated low impedance connection to processor core power (VCC) • Refer to processor datasheet.
VCCVID	• Connect to 1.2V linear regulator	• This voltage powers the processor dynamic VID circuitry.
V_{ID}[4:0]	• Connect to VR or VRM. These are open-drain signals from the processor and require pull-ups to 3.3 V for proper operation. Some VR controllers have internal pull-ups. If the VR controller used does not have 1 kΩ internal pull-ups, 1 kΩ 5% pull-ups to 3.3 V should be placed on the motherboard.	• Refer to the *Intel® Pentium® 4 Processor in the 478-Pin Package VR Down Design Guidelines.*
VSSA	• Connect with isolated power circuitry to VCC_CPU.	• Isolated GND for internal PLLs • Refer to Section 11.4.
V_{SS_SENSE}	• Connect to additional glue logic if used. This signal is an output signal.	• Isolated low impedance connection to core VSS. • Refer to the processor datasheet.
TMS	• Debug port signal. Refer to the latest revision of the *Intel® Pentium® 4 Processor in the 478-pin Package Debug Port Design Guide* for information on the connection and termination of this signal.	• Debug port signal. Proper termination is required for the system to function properly.

Checklist Items	Recommendations	Reason/Impact/Documentation
TRST#	• Debug port signal. Refer to the latest revision of the *Intel® Pentium® 4 Processor in the 478-pin Package Debug Port Design Guide* for information on the connection and termination of this signal.	• Debug port signal. Proper termination is required for the system to function properly.
TCK	• Debug port signal. Refer to the latest revision of the *Intel® Pentium® 4 Processor in the 478-pin Package Debug Port Design Guide* for information on the connection and termination of this signal.	• Debug port signal. Proper termination is required for the system to function properly.
TDI	• Debug port signal. Refer to the latest revision of the *Intel® Pentium® 4 Processor in the 478-pin Package Debug Port Design Guide* for information on the connection and termination of this signal.	• Debug port signal. Proper termination is required for the system to function properly.
TDO	• Debug port signal. Refer to the latest revision of the *Intel® Pentium® 4 Processor in the 478-pin Package Debug Port Design Guide* for information on the connection and termination of this signal.	• Debug port signal.
ITP_CLK[1:0]#	• Debug port signal. Refer to the latest revision of the *Intel® Pentium® 4 Processor in the 478-pin Package Debug Port Design Guide* for information on the connection and termination of this signal.	• Debug port signal.
DBR#	• Debug port signal. Refer to the latest revision of the *Intel® Pentium® 4 Processor in the 478-pin Package Debug Port Design Guide* for information on the connection and termination of this signal.	• Debug port signal.
BPM[5:0]#	• Debug port signal. These signals require 51 Ω 5% termination to VCC_CPU. The termination resistors should be located close to the processor. For systems that incorporate a debug port, 51 Ω 5% termination is required near the debug port as well. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Debug Port Guidelines* for further details.	• Debug port signal. Proper termination is required for the system to function properly.

15.2 CK00 Clock Generator Checklist

Checklist Items	Recommendations	Reason/Impact/Documentation
Ref/MultSel[0:1]	• Use 33 Ω series termination resistor for each signal. • Connect to ICH2 and SIO.	
PCICLK [0:9]	• Use 33 Ω series termination resistor for each signal. • Connect to PCI slots 0 through 4 • Connect to ICH2, FWH, SIO, Glue Chip and Audio Logic Device.	• Refer to Section 4.4.2.1.
3V66 [0:3]	• Use 33 Ω series termination resistor for each signal. • Connect to AGP Connector, MCH, and ICH2.	• Refer to Section 4.4.2.
3VMRef 3VMRef_b	• Use 33 Ω series termination resistor for each signal. • Connect 3VMRef to DRCG1. • Connect 3VMRef_b to DRCG2	• 3VMRef_b is 180° out of phase with 3VMRef.
SEL100/133	• Connect this signal to GND with a 470 Ω ±5% resistor. • Connect this signal to processor pin BSEL0 with a 1 kΩ ±5% resistor pull-up to VCC3_CLK	• This signal needs to be connected to GND for 100 MHz host clock operation only • This connection option allows 100 MHz or 133 MHz host clock operation.
48 MHz /SelA 48 MHz /SelB	• Terminate to GND with 1 kΩ ±5% resistors	• Terminating to GND sets CK00 for 100 MHz or 133 MHz host clock operation
SPREAD#	• Terminate to GND with a 470 Ω ±5% resistor.	• Terminating to GND enables this function
PWRDWN#	• Used to prevent platform from booting with unsupported processors. See Section 4.2 for more information. • Connect to DRCG1 and DRCG2 clock generators.	
CPUCLK/ CPUCLK_B[0:3]	• Connect a 33 Ω ±5% series resistor on each clock signal. Series resistor should be placed on the clock driver side of the shunt source resistor. • Connect a “shunt source termination (Rt)” resistor to GND for each signal after series termination resistor. • Connect differential clock pair to processor, MCH, ITP connector.	• These are differential clocks. • Rt resistors should be selected to match the characteristic impedance of the board. • Refer to Section 4.1
3.3 V(VCC)	• Connect to 3.3 V power plane	
GND	• Connect to GND plane.	

Checklist Items	Recommendations	Reason/Impact/Documentation
XTAL_in XTAL_out	• Connect a 10 pF capacitor from each signal to GND. • Connect to 14.318 MHz crystal oscillator.	• Capacitor values may vary slightly from manufacturer to manufacturer.

15.3 Direct Rambus Clock Generator (DRCG1 and DRCG2) Checklist

Checklist Items	Recommendations	Reason/Impact
VddIR	• Connect to 3.3 V	• Provides the voltage reference for the Refclk clock output from CK00 clock generator • Refer to Section 4.3.1.
Refclk	• Connect Refclk pin of DRCG1 and DRCG2 to 3VMRef and 3VMRef_b outputs from the CK00 clock generator.	
ddP, VddC, VddO,	• These are all 3.3 V voltage pins. Tie directly to VCC3_3 supply. • Place a 0.1 µF capacitor between each pin and the VSS plane for decoupling purposes.	
GndP, GndI, GndC, GndO	• Connect to GND.	• These are all ground pins.
PclkM	• Connect to HCLKOUT on MCH.	• This is a host clock feedback input. • Refer to Section 4.3.2.
SynclkN	• Connect to RCLKOUT on MCH.	• This is a Rambus clock feedback input. • Refer to Section 4.3.2.
VddIPD	• Connect to 1.8 V power plane.	• This is a voltage reference for PclkM and SynclkN signals.
STOPB#	• Terminate to 1.8 V power plane with a 4.7 kΩ resistor.	• This function is not used for Intel 850 chipset-based platform.
PWRDN#	• Terminate to 3.3 V through a 4.7 kΩ resistor. • Connect to CK00 PWRDN# signal.	
S1, S0	• Connect 1 kΩ ±5% series resistors to S0 and S1 and connect signals together. Connect joined signals through a 4.7 kΩ ±5% pull-down resistor to GND and connect a series resistor to a GPIO	• A low voltage (logic “0”) on S1 and S0 places the DRCG* in normal operation mode. The GPIO connection allows software adjustable mode control over CLK and CLKB

Checklist Items	Recommendations	Reason/Impact
Mult[1:0]	• Connect to GPIO.	• These pins determine the internal PLL divider ratio in the DRCG. Connection to GPIO allows software adjustable PLLCLK and REFCLK multipliers. • The Intel 82850 chipset platform supports 400 MHz (PC800) and 300 MHz (PC600) RAMBUS operation only. • The Intel 82850E chipset platform supports 400 MHz (PC800) or 533 MHz (PC1066) RAMBUS operation only.
ClkB/Clk	• Connect a 39 Ω ±5% series resistor near the pins. Connect 51 Ω ±5% parallel resistors after the series resistors through a 0.1 µF capacitor to ground. Connect to RIMM* connector. • These signals should be terminated with 28 Ω ±2% or 27 Ω ±1% resistors to ground through a 0.1 µF capacitor.	• This is the main clock (CTM/CTM#) for the Direct RAMBUS channel. • Refer to Section 4.3.4. • Refer to Section 4.3.3.3.
Global decoupling	• It is recommended that a ferrite filter with 2 capacitors (10 µF and 0.1 µF) be placed near the part for both the 3.3 V planes. Capacitors should be placed on the device side of the Ferrite Bead. Ferrite bead should be 50 Ω at 100 MHz. • Discrete capacitors are recommended for all the aforementioned decoupling. • Cpacks are not recommended.	• This recommendation is to reduce jitter and voltage supply noise for the part. • Cpacks will increase the parasitic inductance of the capacitors, and may require more capacitors than specified above. • Refer to section 4.3.4.

15.4 Intel® 850 Chipset Checklist

Checklist Items	Recommendations	Reason/Impact
HL_STB HL_STB#	• Connect to ICH2	• The length of both hub interface strobe signals must be matched within ±0.1 inches of the HL_STB differential pair. • Refer to Section 8.2.1.
HDVREF[3:0] HAVREF[3:0] CCVREF	• Connect voltage divider to pins. 50 Ω ±1% pull-up to VCC and 100 Ω ±1% pull-down resistor to GND. • Decouple the voltage divider with a 1 µf capacitor. • Keep the voltage divider within 1.5 inches of the MCH V_{REF} ball.	• A single reference divider circuit for all signals is considered sufficient. • Refer to Section 5.5.
HUBREF	• Use a voltage divider circuit with R1=R2=150Ω ±1% • The reference voltage generated by a single HUBREF divider should be bypassed to ground at each component with a 0.01 µF capacitor located close to the component (MCH and ICH2) HUBREF pin. Decouple the voltage divider circuit with a 0.1 µF capacitor placed near the voltage divider circuit.	• Refer to Section 8.2.3.
GRCOMP	• Must be tied to a 40 Ω ±2% or 39 Ω ±1% pull-down resistor to ground.	• Connect within 0.5 inches of the ball. • Refer to Section 7.1.8.
HLR_COMP	• RCOMP Resistor tied to VSS: • Normal: 40 Ω ±2% or 39 Ω ±1% with a trace impedance of 60 Ω ±15%.	• Refer to Section 8.2.4.
HR_COMP	• Use 20.75 Ω ±1% pull-down to VSS	• Refer Section 5.5.
HSWNG [1:0]	• Connect voltage divider to pins. 150 Ω pull-down to GND and a 301 Ω pull-up resistor to V_{TT}. • Decouple the voltage divider with a 1 µf capacitor. • Keep the voltage divider within 1.5 inches of the MCH V_{REF} ball.	• Refer to Section 5.5.

Checklist Items	Recommendations	Reason/Impact
I/O Decoupling requirements	• 4 minimum, 5 preferred 0.1 µf capacitors with 603 packages distributed evenly over the System Bus data lines. • 2 minimum, 3 preferred 0.1 µf capacitors with 603 packages distributed evenly over the system bus address and control lines. • All capacitors placed as close as possible to the MCH package (within 150 mils)	• This is to provide clean power delivery to the system bus I/O ring. • Refer to Section 5.5.1.
1.8 V RAC Power Isolation	• **Option 1 — Low pass filter with inductor:** Place 3.3 nH inductor between V_{CC}RAC and the 1.8 V power plane. Place a 3.3 µf capacitor on MCH side of the inductor. Place 2–3 0.1 µF capacitors near the V_{CC}RAC pins for adequate decoupling between V_{CC}RAC and VSS. Use 0805 size components. • **Option 1 — Low pass filter with Ferrite Bead:** Place 10 Ω (at 100 MHz) between V_{CC}RAC and the 1.8 V power plane. Place a 10 µF capacitor on MCH side of the inductor. Use a minimum of 2 .1 µF capacitors per RAC and a minimum of one 1.0 µF capacitor for both RACs located near the V_{CC}RAC pins. Use 0805 size components except for the 10 µF capacitor, which can be 1206.	• The Intel 850/850E chipset requires a low-pass filter on the V_{CC}RAC pins to meet clock jitter specifications. The low-pass filter isolates V_{CC}RAC from the 1.8 voltage plane that powers the MCH core. • Refer to Section 12.3.
SCK/CMD Circuitry	• This implementation is applicable for RIMM* modules down solution only. Also, this implementation is not necessary if Suspend-to-RAM is not supported in the system. • Transistor needs to be connected to SCK and should be gated with PWROK circuitry. A dummy transistor needs to be connected to the CMD signal to minimize impedance discontinuities. • The transistor should have a Cobo of 4 pF or less.	• This circuitry is needed to avoid the MCH inadvertently taking the RDRAM devices out of power-down due to the CMOS interface being driven during power ramp, the SCK signal should be shunted to ground when the MCH is entering and exiting Suspend-to-RAM. • Refer to Section 6.1.7.

15.5 AGP Checklist

Checklist Items	Recommendations	Reason/Impact
G_FRAME# G_IRDY# G_TRDY# G_DEVSEL# G_STOP# G_SERR# G_PERR# G_RBF# G_PIPE# G_REQ# G_GNT# G_PAR AD_STB[0:1] SB_STB WBF#	• These signals require pull-up resistors to V_{DDQ}. • Acceptable values are between 4 kΩ and 16 kΩ. The recommended value is 8.2 kΩ.	• V_{DDQ} = 1.5 V for 1X, 2X and 4X mode • Pull up to V_{DDQ} ensures that stable values are maintained when agents are not actively driving the bus. • Refer to Section 7.1.9.
AD_STB#[0:1] SB_STB#	• These signals require pull-down resistors. • Acceptable values are between 4 kΩ and 16 kΩ. The recommended value is 8.2 kΩ.	• Pull down to GND ensures that stable values are maintained when agents are not actively driving the bus. • Refer to Section 7.1.9.
INTA# INTB#	• 8.2 kΩ pull-up resistors to 3.3 V • Range is 4 kΩ – 16 kΩ	• These signals should be pulled up only once (for both PCI and AGP). They should be pulled to 3.3 V and MUST NOT be pulled to 5 V. • INTB# is for a two function device and may not be seen with AGP down • Refer to Section 7.1.9 this document.
VREFCG[B66] VREFGC[A66] G_REF[1:0]	• VREFCG should be tied to a resistor divider near the AGP device. • VREFGC should be a no connect. • A 220 Ω – 330 Ω series resistor should be connected from the voltage divider network to the G_REF[1:0] pins on the MCH.	• The V_{REF} divider network should be placed near the AGP interface to achieve the common mode power supply effect. A 0.1 µF decoupling capacitor should be placed near the G_REF[1:0 • Refer to Section 7.1.7.
TYPEDET# [A2]	• Intel 850 chipset only supports 1.5 V add-in card. Therefore, TYPEDET# detection on the motherboard is not required.	• Refer to Section 7.1.6.
PME#	• Connect to PCI PME#	• This is an open drain signal from the AGP connector and does not require pull-up resistor to VCC3_3 if connected to ICH2.
3.3Vaux (B24)	• Connect to $3.3V_{SB}$	• May not be seen with AGP down

Checklist Items	Recommendations	Reason/Impact
Decoupling Capacitors	• Use a 0.01 µF capacitor for each power pin and a bulk 10 µF tantalum capacitor on V_{DDQ} and a 20 µF tantalum capacitor on VCC3_3 plane near the connector.	• This is to ensure that the AGP connector is well decoupled. • Refer to Section 7.1.4.
SBA[7:0]	• No extra Pull-up resistors. Connect to AGP connector.	• In the MCH, weak pull-ups are integrated for SBA[7:0] signals. These signals implement internal pull-ups of a nominal value of 8 kΩ.

15.6 Rambus RIMM* Connector Checklist

Note:

- S3 (Suspend To RAM):
  — RDRAM device support → 2.5 V (ON), 1.8 V (ON), 3.3 V (N/A)
- S5 – 2.5 V (OFF), 1.8 V (OFF), 3.3 V (OFF)

Checklist Items	Recommendations	Reason/Impact
LCTM, LCTM# RCTM, RCTM# LCFM, LCFM# RCFM, RCFM# LROW[2:0] RROW[2:0] LCOL[4:0] RCOL[4:0] RDQA[8:0] LDQA[8:0] RDQB[8:0] LDQB[8:0] CMD SCK	• 0.8 pF – 1.35 pF compensating capacitance is required on each of these RSL connector pins.	• The RIMM* connector pin inductance has been shown to cause an impedance discontinuity on the Rambus channel. This may reduce voltage and timing margin. • Above are examples of calculated numbers. Actual calculated values may vary with board variations. Use CTAB calculations for specific values. • Refer to Section 6.1.2.5.
RSL Signal Termination	• All RSL signals must be terminated to 1.8 V (V_{TERM}) using 27 Ω 1% or 28 Ω 2% tolerance resistors at the end of the channel opposite the MCH.	• Rpacks are OK. • Refer to Section 6.1.3.
RC Termination	• Due to the buffer strengths in the MCH, the high-speed CMOS signals require DC termination. • Terminate with 91 Ω ±2% pull-up and a 39 Ω ±2% pull-down resistor to ensure proper resuming from S3.	• The MCH tri-states SCK during STR entry causing a glitch on SCK. • Refer to Section 6.1.5.
SVDD (A56 and B56)	• Should be tied to 3.3 V for EEPROM (SPD) on RIMM modules. • If the SMBus is tied to $3.3V_{SB}$, then either: —Provide proper isolation on SCL /SDA and pull SVDD to 3.3 V OR —Tie SVDD to $3.3V_{SB}$.	• Ensure proper isolation if some SMBUS devices are powered by $3.3V_{SB}$. • Refer to the RAMBUS datasheets at http://www.rambus.com

Checklist Items	Recommendations	Reason/Impact
SA Pins	• Should be connected to VCC3_3 or GND to set the SMBus address for that RIMM* modules EEPROM. • If the SMBus is tied to $3.3V_{SB}$, then either: — Provide proper isolation on SCL /SDA and pull the HIGH SA pins to 3.3 V OR —Tie the HIGH SA pins to $3.3V_{SB}$.	• This sets the SMBus address. Each device on the SMBus must have an address to distinguish it from another device of the same type. That is, each RIMM* module EEPROM must be strapped to a different address or they will all respond on an access. • Refer to the Rambus datasheets at http://www.rambus.com
SIN & SOUT	Should be daisy-chained between RIMM connectors: • MCH SIO pin connects to 1st RIMM connector SIN (B36) • SOUT (A36) on 1st RIMM connector connects to 2nd RIMM connector SIN (B36) • A 2.2 kΩ–10 kΩ terminating resistor, tied to GND, is required on the last RIMM connector's SOUT pin.	• Refer to Section 6.1.6. • Refer to the Rambus datasheets at http://www.rambus.com
SWE (A57)	• If an OEM needs to write to the SPD devices, it is recommended that this signal be tied to a GPO pin from either the ICH2 or the SIO. • If an OEM does not need to write to the SPD devices, it is recommended that this signal be tied to 3.3 V via a weak pull-up resistor (4.7 kΩ).	• If SWE = 1, write protected. • If SWE = 0, not write protected. • These signals must be driven; do not leave floating. • Refer to the RAMBUS datasheets at http://www.rambus.com
RESET	• For the 168-pin RIMM connector, this is a reserved pin.	• The connector pad is reserved for future use for the 168-pin RIMM connector. • Refer to the RAMBUS datasheets at http://www.rambus.com
V_{DD}	• This is connected to 2.5 V (or $2.5V_{SB}$) • It is REQUIRED that the voltage regulator to the RDRAM* devices (2.5 V RDRAM device Core) is turned OFF in S5. This can be accomplished by connecting the SLP_S5# signal to the 2.5 V RDRAM Core voltage regulator.	• It supplies the core voltage for the RDRAM* technology and interface logic.
V_{CMOS}	• PC600/800/1066: • This is connected to 1.8 V for RDRAM technology • V_{CMOS} must be OFF in S5. • V_{CMOS} can be generated with a voltage divider consisting of a 36 Ω pull-up resistor to VCC2_5 and 100 Ω resistor to GND.	• S5 is a suspend state and power is removed from some components on the motherboard. Therefore, V_{CMOS} should be off while in suspend state. • Refer to Section 6.1.5.

Checklist Items	Recommendations	Reason/Impact
V_{CMOS} decoupling	• PC1066: Minimum of 2 x 0.1 µF capacitors, one near each RIMM input	• PC1066 requirement
2.5 V (V_{DD}) decoupling	• Low frequency decoupling: • This needs to be done on the motherboard with bulk capacitors. • Linear regulator design: 8x 100 µF • Switching regulator: 5x 47µF or 6x 20 µF • PC1066: minimum of 2 x 1000 µF, 2 x 510 µF and 8 x 10 µF MLC capacitors.	• These are EXAMPLES. The exact decoupling requirements are dependent on the voltage regulator design. Refer to the RDRAM device specification for the power delivery requirements.
1.8 V (V_{TERM}) decoupling	• PC600/PC800 High frequency decoupling: —One 0.1 µF ceramic capacitor per 2 RSL signals. These should be placed near the termination resistor pack. • PC600/PC800 Low frequency decoupling: —2 x 100 µF tantalum capacitors. • PC1066 High frequency decoupling: —One 0.1 µF ceramic capacitor per 2 RSL signals (minimum of 13 x 0.1 µF capacitors). These should be placed near the termination resistor pack. For margin improvement, this can be increased to two 0.1 µF capacitors per 2 RSL signals. —2 x 10 µF MLC • PC1066 Low frequency decoupling: —2 x 100 µF tantalum capacitors	• RSL termination voltage decoupling is required on the motherboard. Both high and low frequency decoupling needs to be added on the motherboard. • These are EXAMPLES. The exact decoupling requirements are dependent on the voltage regulator design. Refer to the RDRAM device specification for the power delivery requirements. • Refer to Section 6.1.3.

Checklist Items	Recommendations	Reason/Impact
1.4 V (RAMREF) decoupling (300/400 MHz RDRAM technology) 1.35 V (RAMREF) decoupling (533 MHz RDRAM technology)	This plane must be decoupled in the following manner: • Each RIMM connector: Locally – A value of 0.1 µF is required for local decoupling. • RAMREF Generation Circuit: At resistor divider – The RAMREF generation circuitry should be placed near the MCH. A 75 Ω ±2% pull-up resistor and 300 Ω ±2% pull-down resistor is required for proper reference voltage (1.4V) in 300/400 MHz RDRAM* technology systems. An 84.5 Ω ±2% pull-up resistor and 255 Ω ±2% pull-down resistor is required for proper reference voltage (1.35V) in 533 MHz RDRAM* technology systems. • MCH: Locally – A value of 0.1 µF is required for local decoupling and a 100 Ω series resistor is required near the MCH, but before the voltage divider circuit.	• Refer to Section 6.1.4.

15.7 Intel® ICH2 Checklist

15.7.1 PCI Interface

Checklist Items	Recommendations	Reason/Impact
FYI	• Inputs to the ICH2 must not be left floating.	• Many GPIO signals are fixed inputs that must be pulled up to different sources. See Section 15.7.7 for recommendations
PERR# SERR# PLOCK# STOP# DEVSEL# TRDY# IRDY# FRAME# REQ#[0:4] GPIO[0:1] THRM#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3_3 or a 2.7 kΩ pull-up resistor to VCC5.	• See PCI 2.2 Component Specification Pull-up recommendations for VCC3_3 and VCC5.
PCIRST#	• The PCIRST# signal should be buffered to form the IDERST# signal • 33 Ω series resistor to IDE connectors.	• Improves signal integrity
PCIGNT#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented, they must be pulled up to VCC3_3.	• These signals are actively driven by the ICH2
PME#	• No extra pull-up resistors	• These signals have integrated pull-ups of 9 kΩ ±3 kΩ.
SERIRQ	• External weak (8.2 kΩ) pull-up resistor to VCC3_3 is recommended.	• Open drain signal
GNT[A]# /GPIO[16], GNT[B]/ GNT[5]#/ GPIO[17]	• No extra pull-up needed	• These signals have integrated pull-ups of 24 kΩ. • GNT[A] has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function.
GPIx	• Connect GPI from processor pin BSEL0/CK00 pin SEL100/133 to ICH2 or SIO	• Used to forward system bus frequency to BIOS for 100 MHz or 133 MHz system bus operation
GPOx	• Route two GPO’s from ICH2 or SIO to RDRAM Device Clock Generator pins Mult0, Mult1	• Allows BIOS to set the 4:3 Host-to-RDRAM devicefrequency ratio for 133 MHz system bus operation

15.7.2 Hub Interface

Checklist Items	Recommendations	Reason/Impact
HL[11]	• No pull-up resistor required	• Use a no-stuff or a test point to put the ICH2 into NAND chain mode testing
HL_COMP	• Tie the COMP pin to a 40 Ω 1% or 2% (or 39 Ω 1%) pull-up resistor (to VCC1_8) via a 10-mil wide, very short (~0.5 inch) trace.	• ZCOMP No longer supported.

15.7.3 LAN* Interface

Checklist Items	Recommendations	Reason/Impact
LAN_CLK	• Connect to LAN_CLK on platform LAN connect device.	
LAN_RXD[2:0]	• Connect to LAN_RXD on platform LAN connect device.	• ICH2 contains integrated 9 kΩ pull-up resistors on interface
LAN_TXD[2:0] LAN_RSTSYNC	• Connect to LAN_TXD on platform LAN connect device.	•
	• LAN connect interface can be left NC if not used.	• Input buffers internally terminated
	• In the event of EMI problems during emissions testing (FCC Classifications) you may need to place a decoupling capacitor (~470 pF) on each of the 4 LED pins.	• Reduces emissions attributed to LAN subsystem.

15.7.4 EEPROM Interface

Checklist Items	Recommendations	Reason/Impact
EE_DOUT	• Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM or CNR Connector.	• Connected to EEPROM data input signal • (Input from EEPROM perspective and output from ICH2 perspective)
EE_DIN	• No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector.	• ICH2 contains integrated pull-up resistor for this signal. • Connected to EEPROM data output signal • (Output from EEPROM perspective and input from ICH2 perspective)

15.7.5 FWH/LPC Interface

Checklist Items	Recommendations	Reason/Impact
FWH[3:0]/ LAD[3:0] LDRQ[1:0]	• No extra pull-ups required. Connect straight to FWH/LPC.	• ICH2 integrates 24 kΩ pull-up resistors on these signal lines.

15.7.6 Interrupt Interface

Checklist Items	Recommendations	Reason/Impact
PIRQ#[D:A]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3.	• In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section of this document. Each PIRQx# line has a separate Route Control Register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: - PIRQ[A]# is connected to IRQ16, - PIRQ[B]# to IRQ17, - PIRQ[C]# to IRQ18, - PIRQ[D]# to IRQ19. This frees the ISA interrupts.
PIRQ#[G:F]/ GPIO[4:3]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3.	• In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section of this document. Each PIRQx# line has a separate Route Control Register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: - PIRQ[E]# is connected to IRQ20, - PIRQ[F]# to IRQ21, - PIRQ[G]# to IRQ22, - PIRQ[H]# to IRQ23. This frees the ISA interrupts.
PIRQ#[H] PIRQ#[E]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3.	• Since PIRQ[H]# and PIRQ[E]# are used internally for LAN and USB controllers, they cannot be used as GPIO(s) pin.

Checklist Items	Recommendations	Reason/Impact
APIC	**Pentium 4 processor based systems:** • These processors do not have APIC pins so all platforms using this processor should both tie APICCLK to ground and tie APICD[1:0] to ground via a 1 kΩ–10 kΩ pull-down resistor. **Non-Pentium® 4 processor based systems:** If the APIC is used: • 150 Ω pull-up resistors on APICD[1:0] • Connect APICCLK to CK133 with a 20–33 Ω series termination resistor. If the APIC is not used on UP systems: • The APICCLK can either be tied to GND or connected to CK133, but not left floating. • Pull APICD[1:0] to GND through 10 kΩ pull-down resistors.	**If the APIC is not used on UP systems:** • Use pull downs for each APIC signal. Do not share resistor to pull signals up.

15.7.7 GPIO

Checklist Items	Recommendations	Reason/Impact
GPIO Pins	**GPIO[0:7]:** • These pins are in the Main Power Well. Pull-ups must use the VCC3_3 plane. • Unused **core** well inputs must either be pulled up to VCC3_3 or be pulled down. • GPIO[1:0] can be used as REQ[A:B]#. • GPIO[1] can also used as PCI REQ[5]#. • These signals are 5 V tolerant **GPIO[8, 11:13]:** • These pins are in the resume power well. Pull-ups must use the VccSUS3_3 plane. • Unused **resume** well inputs must be pulled up to VccSUS3_3. • These are the only GPIs that can be used as ACPI compliant wake events. • These signals are not 5 V tolerant **GPIO[16:23]:** • Fixed as output only. Can be left NC. • In main power well. • GPIO22 is open drain. **GPIO[24,25,27,28]:** • I/O pins. Can be left as No Connect. • From resume power well.	• Ensure ALL unconnected signals are OUTPUTS ONLY! • The GPIO signals listed in the Recommendations column are the only GPI signals in the resume well with associated status bits in the GPE1_STS register.

15.7.8 USB

Checklist Items	Recommendations	Reason/Impact
USBP[3:0]P USBP[3:0]N	• See Section 9.4 for circuitry needed on each differential Pair.	

15.7.9 Power Management

Checklist Items	Recommendations	Reason/Impact
THRM#	• Should not be used for this platform. A pull-up is required on this signal.	• Input to ICH2 cannot float. THRM# polarity bit defaults THRM# to active low, so pull up.
SLP_S3# SLP_S5#	• No pull-up/pull-down resistors needed. Signals driven by ICH2.	• Signal driven by ICH2
PWROK	• This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC3_3 and VCC1_8 have reached their nominal voltages	• Timing requirement
PWRBTN#	• No extra pull-up resistors	• These signals have integrated pull-ups of 9 kΩ ±3 kΩ.
RI#	• RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to resume well	• If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns, the RI_STS bit will be set and the system will interpret that as a wake event.
RSMRST#	• This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSUS3_3 and VccSUS1_8 have reached their nominal voltages. Can be tied to RSMPWROK on desktop platforms.	• Timing requirement • Power-well Isolation

15.7.10 Processor Signals

Checklist Items	Recommendations	Reason/Impact
A20M#, CPUSLP#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK#	• Internal circuitry has been added to the ICH2, external pull-up resistors are not needed.	• Push/pull buffers now drive the output signals.
FERR#	• Terminate to VCC with a 62 Ω ±5% resistor near the processor.	
RCIN# A20GATE	• Pull up signals to VCC3_3 through a 10 kΩ resistor.	• Typically, driven by Open Drain external microcontroller
CPUPWRGD	• Connect to the processor's CPUPWRGD input. Requires weak external pull-up resistor.	• Refer to processor documentation of the processor that platform utilizes for specific values.

15.7.11 System Management

Checklist Items	Recommendations	Reason/Impact
SMBDATA SMBCLK	• Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)	• Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ.
SMBALERT#/ GPIO[11]	• See GPIO section if SMBALERT# not implemented	
SMLINK[1:0]	• Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)	• Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ.
INTRUDER#	• Pull signal to V_{CC}RTC (V_{BAT}) if not needed	• Signal in V_{CC}RTC (V_{BAT}) well

15.7.12 RTC

Checklist Items	Recommendations	Reason/Impact
VBIAS	• The VBIAS pin of the ICH2 is connected to a 0.047 µF capacitor. See Section 9.8.7	• For noise immunity on VBIAS signal
RTCX1 RTCX2	• Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor and use 12 pF decoupling capacitors at each signal. • RTCX1 can optionally be driven by an external oscillator instead of a crystal. These signals are 1.8 V only, and must not be driven by a 3.3 V source.	• The ICH2 implements a new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in Section 9.7.1 will be required to maintain the accuracy of the RTC. The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in V_{CCRTC} and V_{BIAS}. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.
SUSCLK	• Route to Test Point if SUSCLK is unused	• To assist in RTC circuit debug

15.7.13 Intel® AC'97

Checklist Items	Recommendations	Reason/Impact
AC_SDOUT	• Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation.	• This pin has a weak internal pull-down. To properly detect a safe_mode condition a strong pull-up will be required to over-ride this internal pull-down.
AC_SDIN[1], AC_SDIN[0]	• Requires pads for weak 10 kΩ pull-downs. Stuff resistor for unused AC_SDIN signal or AC_SDIN signal going to the CNR connector. • If there is no codec on the system board, then both AC_SDIN[1:0] should be pulled down externally with resisters to ground.	• AC_SDIN[1:0] are inputs to an internal OR gate. If a pin is left floating, the output of the OR gate will be erroneous.
AC_BITCLK,	• No extra pull-down resistors required.	• When nothing is connected to the link, BIOS must set a shut-off bit for the internal keeper resistors to be enabled. At that point, you do not need pull-ups/pull-downs on any of the link signals.
AC_SYNC	• No extra pull-down resistors required.	• Some implementations add termination for signal integrity. Platform specific.

15.7.14 Miscellaneous Signals

Checklist Items	Recommendations	Reason/Impact
SPKR	• No extra pull-up resistors • Effective Impedance due speaker and codec circuitry must be greater than 50 kΩ or a means to isolate the resistive load from the signal while PWROK is low be found.	• Has integrated pull-up of between 18 kΩ and 42 kΩ. The integrated pull-up is only enabled at boot/reset for strapping functions; at all other times, the pull-up is disabled. • A low effective impedance may cause the TCO Timer Reboot function to be erroneously disabled.
TP[0]	• Requires external pull-up resistor to VccSUS3_3	• This signal is used for BATLOW in Mobile. • Not required for desktop.
FS[0]	• Route to a test point.	• ICH2 contains an integrated pull-up for this signal. Test point used for manufacturing appears in XOR tree.

15.7.15 Power

Checklist Items	Recommendations	Reason/Impact
V_CPU_IO[1:0]	• The power pins should be connected to the proper power plane for the processor's asynchronous AGTL+ signals. Use one 0.1 µF decoupling capacitor.	• Used to pull up all processor interface signals.
VccRTC	• No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safemode strapping for Clear CMOS	
Vcc3_3	• Requires six 0.1 µF decoupling capacitors.	
VccSus3_3	• Requires one 0.1 µF decoupling capacitor.	
Vcc1_8	• Requires two 0.1 µF decoupling capacitors.	
VccSus1_8	• Requires one 0.1 µF decoupling capacitor.	
V5REF_SUS	• Requires one 0.1 µF decoupling capacitor. • V5REF_SUS only affects 5 V tolerance for USB OC[3:0]# pins and can be connected to VccSUS3.3 or 5V_Always/5V_AUX if 5 V tolerance on OC[3:0]# is not required. If 5 V tolerance on OC[3:0]# is needed then V5REF_SUS USB must be connected to 5V_Always/5V_AUX which remains powered during S5.	
V5REF	• V5REF is the reference voltage for 5 V tolerant inputs in the ICH2. Tie to pins VREF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.	• Refer to Section 12.6 for an example circuit schematic that may be used to ensure the proper V5REF sequencing.

15.7.16 IDE Interface

Checklist Items	Recommendations	Reason/Impact
PDD[15:0], SDD[15:0]	• No extra series termination resistors or other pull-ups/pull-downs are required. • PDD7/SDD7 does not require a 10 kΩ pull-down resistor. • Refer to ATA ATAPI-4 specification.	• These signals have integrated series resistors. • Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	• No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	• These signals have integrated series resistors. • Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.
PDREQ SDREQ	• No extra series termination resistors. • No pull-down resistors needed.	• These signals have integrated series resistors in the ICH2. • These signals have integrated pull-down resistors in the ICH2.
PIORDY SIORDY	• No extra series termination resistors. • Pull-up to VCC3_3 via a 4.7 kΩ resistor.	• These signals have integrated series resistors in the ICH2.
IRQ14, IRQ15	• Recommend 8.2 kΩ–10 kΩ pull-up resistors to VCC3_3. • No extra series termination resistors.	• Open drain outputs from drive.
IDERST#	• The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.	
Cable Detect:	• **Host Side/Device Side Detection** —Connect IDE pin PDIAG/CBLID to an ICH2 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. • **Device Side Detection** —Connect a 0.047 µF capacitor from IDE pin PDIAG/CBLID to GND. No ICH2 connection.	• The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. • **NOTE:** All ATA66/ATA100 drives will have the capability to detect cables

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16 Layout Review Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an Intel 850 chipset. The items contained within this checklist attempt to address important connections to these devices and any critical supporting circuitry. This is not a complete list and does not guarantee that a design will function properly. Beyond the items contained in the following text, refer to the most recent version of the design guide for more detailed instructions on designing a motherboard.

16.1 Processor and System Bus

16.1.1 AGTL+ Signals

This section covers the address, Data, DSTBn/p#, ADSTBn/p# and common clock signals. Refer to the processor datasheet for a system bus list, signal types and definitions.

√	Recommendations	Reason/Impact/Documentation
	• Trace width recommendation is 7 mils with 13 mil edge-to-edge spacing for all signals. Trace spacing can be approximately 5 mils within pin field.	• Refer to Section 5.3.
	• Processor clock differential pairs should have a minimum of 20mil spacing from other signals.	
	• Data signal (D[63:0], and DBI[3:0]#) length should be 2 inches – 10 inches pin-to-pin. Data signals of the same source synchronous group should be routed to the same pad-to-pad length ±100 mils. Length must be added to the motherboard to compensate for package length differences.	• The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. • Refer to Chapter 2.
	• A strobe and its complement (DSTBP[3:0]# and DSTBN[3:0]#) should be routed within ±25 mils of the same pad-to-pad length	• The impact of this recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. It is recommended to simulate skew in order to determine the length that best centers the strobe for a given system. • Refer to Chapter 2.

√	Recommendations	Reason/Impact/Documentation
	• Address signal (A[35:3]# and REQ[4:0]#) length should be 2 inches – 10 inches pin-to-pin. Address signals of the same source synchronous group should be routed to the same pad-to-pad length ±200 mils. Length must be added to the motherboard to compensate for package length differences.	• The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. • Refer to Chapter 2.
	• ADSTB[1:0]# length should be 2 inches – 10 inches pin-to-pin. Address signals of the same source synchronous group should be routed to the same pad-to-pad length ±200 mils. Length must be added to the motherboard to compensate for package length differences.	• The impact of this routing recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. • Refer to Chapter 2.
	All common clock AGTL+ signals (See below) routed 6 inches – 10 inches (pin-to-pin). No length compensation is necessary. BPRI# DEFER# RESET# RS[2:0]# RSP# TRDY# AP[1:0]# ADS# BINIT# BNR# BPM[5:0]# BR0# DBSY# DP[3:0]# DRDY# HIT# HITM# LOCK# MCERR#	• Refer to Chapter 2.
	• All signals impedance's should equal 50 Ω ±15%	• Refer to Chapter 2.

16.1.2 Asynchronous GTL+ and Other Signals

√	Recommendations	Reason/Impact/Documentation
	• FERR# and PROCHOT connects with the "T" topology. Processor to T-junction should be 1 inch–12 inches. Connection to the ICH2 should be made with no stub. T- junction to pull-up should be 3 inches max. A 7 mil spacing is required. Trace impedance should be 60 Ω.	• Refer to Section 5.4.1
	• A20M#, IGNNE#, INIT#, LINT[1:0], SLP#,SMI# and STPCLK# connect in a point-to-point topology. Trace length should be 12 inches max. A 7 mil spacing required. Trace impedance should be 60 Ω.	• Refer to Section 5.4.1
	• THERMTRIP# connects in a "T" topology. Processor to T-junction should be 1 inch–12 inches max. Connection to the ICH2 should be made with no stub. T junction to pull-up resistor should be 3 inches max. Trace impedance should be 60 Ω. Trace spacing should be 7 mils.	• Refer to Section 5.4.1
	• PWRGOOD connected in a "T" topology. Pull-up resistor to T-junction should be 3 inches max. T-junction to processor should be 1.1 inches max. T-junction to ICH2 should be 1–12 inches Trace impedance should be 60 Ω. Trace spacing should be 7 mils.	• Refer to Section 5.4.1
	• THERMDA/THERMDC should connect to remote sensor within 4-8 inches as long as worst-case noise sources (e.g., the clock generator, data and address signals) are avoided. A 10 mil wide trace recommended. Shielded twisted pair recommended for long distance remote sensor.	• Refer to Section 5.4.1
	• VCCIOPLL, VCCA, VSSA circuitry should be routed away from noisy signals or high free signals. Keep traces as short as possible.	• Refer to Section 5.5.
	• Place 51.1 Ω ±1% resistors as close to COMP[1:0] as possible	• Refer to Section 5.4.1

16.1.3 Processor Keep-Out Zones

√	Recommendations	Reason/Impact/Documentation
	• Refer to Chapter 10.	

16.1.4 Processor Decoupling

√	Recommendations	Reason/Impact/Documentation
	• Place ten 560 µF OS-CON capacitors as close to the processor power and ground pins as the heatsink keepout area will allow. Refer to Chapter 11 for more detailed placement guidelines.	• These capacitors are needed to meet the processor voltage transient specifications.
	• Place 30 1206 package 10 µF capacitors as close to processor ground and power pins as possible. Refer to Chapter 11 for more detailed placement guidelines.	• These high frequency decoupling capacitors are needed to meet voltage transients. • Refer to Chapter 11.
	• All capacitors should be placed as close to the processor package as the processor keep-out zone allows.	• Refer to Chapter 11.

16.1.5 Intel® 82850 MCH Decoupling

√	Recommendations	Reason/Impact/Documentation
	• 4–5 0.1 µF capacitors with 603 packages distributed evenly over the system bus data lines. Place as close as possible (within 150 mils) to the chipset package.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane (microstrip). • Refer to Section 5.5.1
	• V_{CC}RAC isolation: Low pass filter circuit should be located within 2 inches of the MCH and the layout of V_{CC}RAC connections should follow high-speed design practices. Decoupling capacitors should be placed as close to the RAC pins as possible to control self-induced RAC noise.	• Proper routing of V_{CC}RAC isolation ensures RAMBUS clock jitter specifications are met. • Refer to Section 12.3.
	• 2–3 0.1 µF capacitors with 603 packages distributed evenly over the system bus address and control lines. Place as close as possible (within 150 mils) to the chipset package.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane. These recommendations are only used for designs containing microstrip configurations. • Refer to Section 5.5.1

16.1.6 AGTL+ (V_{REF} HDVREF [3:0], HAVREF [1:0] and CCVREF)

√	Recommendations	Reason/Impact/Documentation
	• Processor must have at least one dedicated voltage divider. There are four GTLREF signals on the processor. Keep voltage divider within 1.5 inches of the first V_{REF} pin.	• Refer to Section 5.3.
	• 82850 MCH requires one dedicated voltage divider. Voltage divider must be within 1.5 inches of MCH V_{REF} ball.	• Refer to Section 5.5.
	• Decouple each voltage divider with a 1 µF capacitor and each V_{REF} pin with a 220 pF capacitor as close to the pin as possible.	• This recommendation provides a low impedance line without the cost of additional plane or island. • Refer to Section 5.3.
	• When routing V_{REF} use a ~12 mil line trace width.	• This recommendation provides a low impedance line without the cost of additional plane or island. • Refer to Section 5.2.
	• Keep other signals 10 mils away from V_{REF} signal.	• V_{REF} signal must be a clean as possible from noise. • Refer to Section 5.3.

16.2 CK00 Routing Guidelines

16.2.1 CK00 Clocking

√	Recommendations	Reason/Impact/Documentation
	• 20 mil spacing required around all 100 MHz differential clocks	• Refer to Section 4.1.
	• Differential clocks should be routed on same layer. If via is required, then dummy vias need to be placed on other differential clock signals.	• This recommendation is to minimize clock skew due to clock pair to clock pair inconsistencies. • Refer to Section 4.1.
	• Route 100 MHz differential clocks to all agents on the same physical layer.	• Constraining all bus clocks to one physical layer minimizes the impact on skew due to variations in Er (dielectric constant) and impedance due to physical tolerances of circuit board material. Routing on internal layers reduces impedance variations and Er. • Refer to Section 4.1.
	• Connect individual differential clock signal from the CK00 to the MCH, ITP port, and the processor. • CK00 to series resistor should be 0.5 inches max. • Series resistor to termination resistor node should be 0.2 inches max. Termination resistor node to actual termination resistor should be 0.2 inches max. Termination resistor node to processor socket should be 12 inches max for Host_CPU and Host_ITP clocks. • Termination resistor node to MCH should be 12 inches for Host_MCH clocks. Add 0.600 inches ± for length matching to Host_MCH clock to compensate for processor socket and package delay.	• Refer to Section 4.1
	• Traces need to be 50 Ω ±15% single-ended and 100 Ω differential.	• Refer to Section 4.1.
	• Trace width for clocks is 7 mils and spacing between each end of the differential clock should be 7 mils. Uniform spacing should be maintained through the entire length of the trace.	• Degradation in noise rejection will occur if spacing is not uniform. • Refer to Section 4.1
	• All host clocks must be ground referenced.	• This ensures that proper current return path is available. • Refer to Section 4.1

√	Recommendations	Reason/Impact/Documentation
	• Connect individual 33 MHz clock signals to ICH2, FWH, and SIO. Trace length from CK00 chip to series resistor should be 0–0.5 inches and from series resistor to receiver should be Z + (4 – 6 inches). Route singles on a single layer. • Z = 5 inches to 9 inches	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships, located in Section 4.4.1 of this document, between clock signals should be observed. • Refer to Section 4.4 and Section 4.4.2.1.
	• Connect individual PCI 33 MHz clock signals to PCI slots. Trace length from CK00 chip to series resistor should be 0 – 0.5 inches and from series resistor to receiver should be Z + (2 – 4 inches). Route signals on a single layer. • Z = 5 inches to 9 inches	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships, located in Section 4.4.1 of this document, between clock signals should be observed. • Refer to Section 4.4 and Section 4.4.2.1.
	• Connect individual 66 MHz clock signals to ICH2 and MCH. • Trace length from CK00 to series resistor should be 0 – 0.5 inches and from series resistor to receiver should be Z + (4 – 5 inches). Route signals on a single layer. • Z = 5 inches to 9 inches.	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships, located in Section 4.4.1 of this document, between clock signals should be observed. • Refer to Section 4.4 and Section 4.4.2.
	• Connect 66 MHz clock signal to AGP connector. • Trace length from the CK00 to series resistor should be 0 – 0.5 inches and from series resistor to receiver should be equal to Z (5 –9 inches). Route signals on a single layer.	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships, located in Section 4.4.1 of this document, between clock signals should be observed. • Refer to Section 4.4 and Section 4.4.2.

16.3 RAMBUS Technology Routing Guidelines

16.3.1 RSL Signals

√	Recommendations	Reason/Impact
	• MCH to 1st RIMM* connector of Channel A or 1st RIMM connector of Channel B 1 inch–6 inches	• Refer to Section 6.1.1.
	• RIMM connector to RIMM connector of the same channel 0.4 to 1 inch.	• Refer to Section 6.1.1.
	• RIMM connector to Termination less than 2 inches. • The trace length between the last RIMM connector and the termination resistors should be less than 2 inches.	• Length matching in this section is not required. • Refer to Section 6.1.3.
	• RSL traces 18 mils trace width, 6-mil space, and 10-mil ground flood, 6-mil space.	• Refer to Section 6.1.1.
	• All signals must be length matched within ±10 mils of the Nominal RSL length as described in this design guide. Ensure that signals with a dummy via are compensated correctly.	• Refer to Section 6.1.1.
	• ALL RSL signals must have 1 via near the MCH BGA pad. Signals routed on the secondary side of the MB will have a “real via” while signals routed on the top layer will have a “dummy via”. Additionally, all signals with a dummy via must have an additional trace length of 25 mils.	• Refer to Section 6.1.2.2 for further explanation and examples.
	• Signals must “alternate” layers.	• Refer to Section 6.1.2.4 of this document.
	• At least 10 mils ground flood isolation required around ALL RSL signals (ground isolation must be exactly 6 mils from RSL signals). Ground flood recommended for isolation. This ground flood should be as close to the MCH (and the 1st RIMM connector) as possible. If possible, connect the flood to the ground balls/pins on the MCH/connector.	• To control cross talk and odd/even mode velocity deltas. • Refer to Section 6.1.1
	• When RSL traces neckdown to exit the MCH BGA, the minimum width is 15 mils and the neckdown is no longer than 25 mils in length.	• To minimize impedance discontinuities
	• Uniform ground isolation flood is exactly 6 mils from the RSL signals at all times.	• Refer to Section 6.1.1.
	• RSL traces Do NOT neckdown when routing into the RIMM connector.	• To minimize impedance discontinuities
	• If tight serpentining is necessary, 10-mil ground isolation MUST be between serpentine segments	• A RSL signal CAN NOT serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines.

√	Recommendations	Reason/Impact
	• ALL RSL, CMD/SCK and CTM/CTM#/CFM/CFM# signals have CTABs on each RIMM connector pin.	• Compensation for the inductance of the connector. Voltage and timing margins may be reduced with CTABs. • Refer to Section 6.1.2.5.
	• CTABs must not cross (or be on top of) power plane splits. They must be ENTIRELY referenced to ground.	• Refer to Section 6.1.2.5.
	• All RSL signals are routed adjacent to a ground reference plane.	• This includes all signals from the 2nd RIMM connector to the termination. If signals are routed referenced to ground from the 2nd RIMM connector to the termination, the ground reference plane MUST extend under these signals AND include the groundside of the V_{TERM} decoupling capacitors.
	• The traces for CMD and SCK must have a neck down from 18-mil traces to 5-mil traces for 175-mils on either side of the SCK/CMD attach point.	• To minimize impedance discontinuities. Refer to Section 6.1.7.
	• Voltage divider network go reference voltage generation should be within 1.5 inches of the MCH V_{REF} ball.	• Refer to Section 5.5.
	• RSL traces do not cross power plane splits. RSL signals must also not be routed *next to* a power plane split	• To maintain signal integrity.

16.3.2 Ground Isolation

√	Recommendations	Reason/Impact
	• Via to ground every ½ inches around edge of isolation island, between RIMM connectors and between RSL signals (from MCH to 1St RIMM connector)	In channel Ideal: 5 inches Acceptable: 0 inches At end Ideal: 25 inches Acceptable: 5 inches * If 3/4 inch end of ground plane: shorten ground plane by 1/4 inch to meet ½ inch recommendation.
	• Via between every signal within 100 mils of the MCH edge and the RIMM connector edge.	
	• No unconnected ground floods	• To avoid discontinuity in ground planes.
	• Ground isolation fills between serpentines	• To avoid cross talk.
	• Ground isolation not broken by C-tabs	• To avoid discontinuity in the ground plane. • Refer to Section 6.1.2.5.
	• Ground isolation connects to the ground pins in the middle of the RIMM connector.	
	• Ground isolation vias connect on all layers and should NOT have thermal relieves.	
	• Ground pins in RIMM connector should connect on all layers.	

16.3.3 V_{term} Layout

√	Recommendations	Reason/Impact
	• Solid V_{TERM} island is on top routing layer; do not split this plane	
	• Ground island (for ground side of V_{TERM} capacitors) is on top routing layer	
	• Termination resistors connect directly to the V_{TERM} island on the top routing layer (without vias)	• Resistor packs are acceptable; however, discrete resistors are recommended for increase margin and control. • Refer to Section 6.1.3.
	• Decoupling capacitors connect to top layer V_{TERM} island and top routing layer ground island directly.	
	• Use at least 2 vias per decoupling capacitor in the top layer ground island.	
	• Use 2x100 µF Tantalum capacitors to decouple V_{TERM}.	• Refer to Section 6.1.3.
	• Hi-frequency decoupling capacitors must be spread-out across the termination island so that all termination resistors are near high frequency capacitors.	• Refer to Section 6.1.3.
	• 100 µF Tantalum capacitor should be at each end of the V_{TERM} island.	• Refer to Section 6.1.3.
	• 100 µF Tantalum capacitors must be connected to the V_{TERM} island directly	• Refer to Section 6.1.3.
	• 100 µF Tantalum capacitors must have at least 2 vias/capacitor to ground.	
	• V_{TERM} island should be at least 50 mils wide	• Refer to Section 6.1.3

16.3.4 Rambus DRCG* Clock Routing Recommendation

√	Recommendations	Reason/Impact/Documentation
	• 3VMRef trace routed from CK00 must be 6 mils wide and separated by 6 mil space on both sides. A 6 mil wide ground isolation trace should be placed after 6 mil space. Max trace length is 8 inches.	• This recommendation is for microstrip applications. • Refer to Section 4.3.1.
	• VddiR pin on DRCG* can be connected to 3.3 V plane near the DRCG if the plane extends near the DRCG. However, if a 3.3 V trace must be used, it should originate at the clock synthesizer and routed 6 mil wide with 6 mil spacing with 6 mil wide ground trace following.	• Refer to Section 4.3.1.
	• Rclkout and Hclkout from MCH must be routed to Synclkn and Pclkm on the DRCG. Signals must be routed together about 12 mils apart with 6 mil wide traces. A 6 mil wide ground trace located on each side of the pair. A 6 mil spacing between the ground trace and Rclkout and Hclkout signals. Max trace length is 6 inches and must be length matched within 50 mils	• If signals must switch layers then they should switch layers together. • Refer to Section 4.3.2.
	• VddiPD pin on DRCG can be connected to 1.8 V plane near the DRCG if the plane extends near the DRCG. However, if a 1.8 V trace must be used, it should originate at the CK00 clock synthesizer and routed 5 mil wide with 6 mil spacing with 6 mil-wide ground trace.	• Refer to Section 4.3.2.
	• Series resistors (39 Ω) should be mounted very near CTM/CTM# pins. Parallel resistors (51 Ω) should be very near series resistors.	• Refer to Section 4.3.5.
	• CFM pair trace length: —MCH-to-1st RIMM connector 1 inch-6 inches — RIMM* connector-to-RIMM connector 0.4 inch –1.0 inches. —2nd RIMM connector-to-Termination 0–2 inches	• Refer to Section 4.3.3.1.
	• CTM pair trace length: —DRCG-to-2nd RIMM connector 0–6 inches —RIMM connector-to-RIMM* connector 0.4–1.0 inches —1st RIMM connector-to-MCH 1 inch–6 inches	• Refer to Section 4.3.3.1.

√	Recommendations	Reason/Impact/Documentation
	• CTM and CFM pairs routed differentially should be routed: —22 mil ground trace —6 mil spacing —14 mil trace width (clock) —6 mil spacing —14 mil trace width (clock#) —6 mil spacing —22 mil ground trace.	• Refer to Section 4.3.3.1
	• If CTM and CFM pairs routed single-ended, route: —10 mil ground trace —6 mil spacing —18 mil wide clock trace —6 mil wide spacing —10 mil ground trace.	• Refer to Section 4.3.3.1.
	• CFM and CTM pairs must be ground referenced at all time.	• This recommendation ensures a proper return current path. • Refer to Section 4.3.3.2.
	• CFM and CTM pairs must have additional 0.021 inches of trace for every 1 inch of RSL trace.	• This added length is to compensate for the clocks faster velocity. • Refer to Section 4.3.3.2
	• Ensure that each clock pair is length matched within ±2 mils of the RSL channel length. Exact matching is preferred.	• Refer to Section 4.3.3.1.
	• Vias are placed in ground isolation traces and ground reference every 1 inch.	• Refer to Section 4.3.3.1.
	• When CTM/CTM# serpentine together, they MUST maintain EXACTLY mils spacing	

16.3.5 Rambus DRCG* Layout (Clean Power Supply)

√	Recommendations	Reason/Impact
	• 3.3 V DRCG* power flood on the top layer. This should connect to each high frequency (0.1 µF) capacitors are near the DRCG power pins. One capacitor next to each power pin.	• Refer to Section 4.3.5.
	• 10 µF bulk *tantalum* capacitor near DRCG connected directly to the 3.3 V DRC* power flood on the top layer	• Refer to Section 4.3.5.
	• Ferrite bead isolating DRCG power flood from 3.3 V main power.	• Refer to Section 4.3.4.

16.3.6 Rambus DRCG* (CTM/CTM# Output Network Layout)

√	Recommendations	Reason/Impact
	• Series resistors (39 Ω) should be mounted very near CTM/CTM# pins. Parallel resistors (51 Ω) should be very near series resistors.	• Refer to Section 4.3.5.
	• CTM/CTM# should be 18 mils wide from the CTM/CTM# pins to the resistors	• Refer to Section 4.3.3.1.
	• CTM/CTM# should be 14 on 6 routed differential as soon as possible after the resistor network. When not 14 on 6, the clocks should be 18 mils wide	
	• Ensure CTM/CTM# are **ground referenced** and the ground reference is connected to the ground plane every ½ inch to 1 inch with vias.	
	• Ensure CTM/CTM# are **ground isolated** and the ground isolation is connected to the ground plane every ½ inch to 1 inch with vias.	

16.3.7 RAMREF Routing

√	Recommendations	Reason/Impact
	• Ensure 1 x 0.1 µF capacitor on V_{REF} at each RIMM connector	• Refer to Section 6.1.4.
	• Use 10-mil wide trace.	• Refer to Section 6.1.4.
	• Do not route V_{REF} near high-speed signals	
	• V_{REF} minimum trace spacing should be 25 mils.	• To reduce crosstalk and maintain signal integrity.

16.4 AGP Guidelines

16.4.1 All 1X Signals

The 1X signals are: CLK, RBF#, WBF#, ST [2:0], PIPE, REQ#, GNT#, PAR, FRAME#, IRDY#, TRDY, STOP# and DEVSEL#.

√	Recommendations	Reason/Impact
	• Max trace length 7.5 inches	• Refer to Section 7.1.1.
	• 5mil trace width, 5 mil trace separation	• Refer to Section 7.1.1.
	• No trace matching requirements for 1X signals.	• Refer to Section 7.1.1.

16.4.2 2X/4X Signals

The 2X/4X signals are: AD[31:0], C/BE[3:0]#, ADSTB[1:0]#, SBA[7:0], SB_STB, SB_STB#

16.4.2.1 AGP Less Than 6 Inches

√	Recommendations	Reason/Impact
	• 5 mil trace width 15 mil separation between data to data for 60 Ω ±10%; for 60 Ω ±15%, its 20 mils	• Refer to Section 7.1.2.1.
	• 5 mil trace width 20 mil separation between data (and all other signals) to strobes for 60 Ω ±10% and 60 Ω ±15%	• Refer to Section 7.1.2.1.
	• 5 mil trace width 15 mil separation between strobe-to-strobe for 60 Ω ±10%; for 60 Ω ±%, its 20 mils	• Refer to Section 7.1.2.1.
	• If AGP Interface is <6 inches long, then DATA and C/BE#s need to be length matched within ±.25 inches of strobes.	• Refer to Section 7.1.2.1.
	• Strobe pairs must be length matched ±0.1 inches	• Refer to Section 7.1.2.1.
	• Route AD [15:0], C/BE [1:0]#, AD_STB0, and AD_STB0# together. (Good recommendation, but not in AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline. • Refer to Section 7.1.2.1.
	• Route AD [31:16], C/BE [3:2]#, AD_STB1, and AD_STB1# together. (Good recommendation, but not in AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline. • Refer to Section 7.1.2.1.
	• Route SBA [7:0], SB_STB, SB_STB# together. (Good recommendation, but not in AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline. • Refer to Section 7.1.2.1.
	• Recommended that all strobes be ground referenced as well as TRDY#, IRDY#, GNT#.	• Refer to Section 7.1.5.
	• Recommended that ½ the AGP signals are ground referenced.	• Refer to Section 7.1.5.
	• For signals that require pull-up or pull-down resistors, keep stub less than 0.5 inches for 1X signals and 0.01 inches for 2X/4X signals.	• This is to minimize signal reflections from the stub. • Refer to Section 7.1.9.
	• Pour a Ground flood under the V_{DDQ} plane	• Optimizes the mutual inductance between two planes. • Refer to Section 7.1.4.

16.4.2.2 AGP Interface Greater Than 6 Inches and Less Than 7.25 Inches

√	Recommendations	Reason/Impact
	• Board impedance must be 60 Ω ±10%	• Refer to Section 7.1.2.2.
	• 5 mil trace width 20 mil separation between data to data	• Refer to Section 7.1.2.2.
	• 5 mil trace width 20 mil separation between data (and all other signals) to strobes	• Refer to Section 7.1.2.2.
	• 5 mil trace width 20 mil separation between strobe to strobe	• Refer to Section 7.1.2.2.
	• DATA and C/BE#s need to be length matched within ±0.125 inches of strobes.	• Refer to Section 7.1.2.2.
	• Strobe pairs must be length matched ±0.1 inches	• Refer to Section 7.1.2.1.
	• Route AD[15:0], C/BE[1:0]#, AD_STB0, and AD_STB0# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline.
	• Route AD [31:16], C/BE [3:2]#, AD_STB1, and AD_STB1# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline.
	• Route SBA[7:0], SB_STB, SB_STB# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline.
	• Recommended that all strobes be ground referenced as well as TRDY#, IRDY#, GNT#.	• Refer to Section 7.1.5.
	• Recommended that ½ the AGP signals are ground referenced.	• Refer to Section 7.1.5.
	• For signals that require pull-up or pull-down resistors, keep stub less than 0.5 inches for 1X signals and less than 0.01 inches for 2X/4X signals.	• This is to minimize signal reflections from the stub. • Refer to Section 7.1.9.
	• Pour a VSS flood under V_{DDQ} plane	• Optimizes the mutual inductance between two planes. • Refer to Section 7.1.9.

16.4.3 Intel® MCH AGP Decoupling

√	Recommendations	Reason/Impact
	• Min of 6 0.01 µF capacitors spread evenly around the MCH AGP interface.	• It is recommended that a low ESL ceramic capacitor, such as a 0603 body type, X7R dielectric. • Refer to Section 7.1.4.
	• Must be within 0.15 inches from package	• Refer to Section 7.1.4.
	• Pour a VSS flood under V_{DDQ} plane to decouple AGP.	• To help lower inductive path from the decoupling capacitor. • Refer to Section 7.1.4.

16.4.4 AGP Connector Decoupling

√	Recommendations	Reason/Impact
	• One 0.01 µF capacitor next to each power pin on connector, VCC1_5, V_{DDQ}, +5, +12, 3.3VAUX.	• Refer to Section 7.1.11.
	• For Bulk decoupling, need one 10 µF tantalum capacitor to V_{DDQ} and a 20 µF tantalum capacitor on VCC3_3 plane near connector.	• Refer to Section 7.1.11.

16.5 8 Bit Hub Interface

√	Recommendations	Reason/Impact
	• Board impedance needs to be 60 Ω ±15%	• Refer to Section 8.2.
	• Traces need to be routed 5 mils wide with 20 mils spacing	• Refer to Section 8.2.
	• To breakout of the MCH and ICH2 package the hub interface signals can be routed 5 on 5. Signals need to be separated to 5 on 20 within 300 mils of the package.	• Refer to Section 8.2.
	• Max trace length is 6 inches long.	• Refer to Section 8.2.
	• Data signals must be matched within ±0.1 inches of the HL_STB diff pair.	• Refer to Section 8.2.2.
	• Each strobe signal needs to be the same length.	• Refer to Section 8.2.2.
	• HUBREF divider should be placed no more than 3.5 inches of away from MCH or ICH2. If so then need separate resistor divider placed locally.	• Refer to Section 8.2.3.

16.5.1 Hub Decoupling

√	Recommendations	Reason/Impact
	• Two 0.1 µF capacitors per each component (MCH and ICH2) spread over the Hub Interface.	• Refer to Section 8.2.5.
	• Place within 150 mils of each package.	• Refer to Section 8.2.5.

16.6 IDE Interface

√	Recommendations	Reason/Impact
	• 5 mil wide and 7 mil spaces	• Refer to Section 9.1.
	• Max trace length is 8 inches long	• Refer to Section 9.1.
	• Shortest trace length must be 0.5 inches shorter than the longest trace length.	• Refer to Section 9.1.

16.7 CNR

√	Recommendations	Reason/Impact
	• 4.5 inches min to 8.5 inches max trace length for LAN* Connect signals	• Refer to Section 9.2.
	• 60 Ω ±15%	• Refer to Section 9.2.
	• Maximum mismatch between length of clock trace and length of any data trace is 0.5 inches	• Refer to Section 9.2.

16.8 Intel® AC'97

√	Recommendations	Reason/Impact
	• Z_O AC97 = 60 Ω ± 15%	• Refer to Section 9.3.
	• 5 mil trace width, 5 mil spacing between traces	• Refer to Section 9.3.
	• Max Trace Length ICH2/Codec/CNR = 12 inches	• Refer to Section 9.3.

16.9 USB

√	Recommendations	Reason/Impact
	• Characteristic impedance of individual signal lines P+, P- Zo = 45 Ω (90 Ω Differential)	• Refer to Section 9.4.
	• Stack-up: 9 mils wide, 25 mil spacing between Differential pairs	• Refer to Section 9.4.
	• Trace Characteristics: — Line Delay = 160.2 ps —Capacitance = 3.5 pF —Inductance = 7.3 nH —Res @ 20o C = 53.9 mΩ	• Refer to Section 9.4.
	• 15 Ω series resistor to be placed < 1 inch from ICH2	• This is required for source termination of the reflected signal. • Refer to Section 9.4.
	• 47 pF parallel capacitors should be placed as close to the ICH2 as possible	• Refer to Section 9.4.
	• 15 kΩ ± 5% pull-down resistors should be placed as close to the ICH2 as possible.	• Refer to Section 9.4.
	• Optional 47 pF capacitor placed close to the USB connector as possible to the USB data lines	• This capacitor can be used for signal quality (rise/fall) times and to help minimize EMI radiation • Refer to Section 9.4 of this document.
	• Stub length due to 15 kΩ pull-downs should be as short as possible.	• Refer to Section 9.4.

16.10 Intel® ICH2 Decoupling

√	Recommendations	Reason/Impact
	• 3.3 V Core—six 0.1 µF capacitors	• Refer to Section 9.12.
	• 3.3 V Stand By –one 0.1 µF capacitor	• Refer to Section 9.12.
	• Processor I/F ($Vcc_{\_Core}$) –one 0.1µF capacitor	• Refer to Section 9.12.
	• 1.8 V Core–two 0.1 µF capacitors, already included in Hub decoupling	• Refer to Section 9.12.
	• Place Decoupling capacitors as close to the ICH2 as possible (~ 400 mils)	• Refer to Section 9.12.

16.11 RTC

√	Recommendations	Reason/Impact
	• RTC LEAD length ≤ 0.25 inches Max	• Refer to Section 9.8.3.
	• Minimize capacitance between Xin and Xout	• Refer to Section 9.8.3.
	• Put GND plane underneath crystal components	• Refer to Section 9.8.3.
	• Do not route switching signals under the external components (unless on other side of board)	• Refer to Section 9.8.3.

16.12 LAN* Connect Interface

√	Recommendations	Reason/Impact
	• Stack-up: 5 mils wide, 10 mil spacing	
	• Z_O = 60 Ω ±15%	• Signal integrity requirement.
	• LAN Max Trace Length ICH2 to CNR: L = 3 inches to 9 inches (0.5 inches to 3 inches on card)	• To meet timing requirements.
	• Stubs due to R-pak CNR/LOM stuffing option should not be present.	• To minimize inductance.
	• Maximum Trace Lengths: ICH2 to 82562EH/ET/EM : L = 4.5 inches to 8.5 inches	• To meet timing requirements.
	• Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches	• To meet timing and signal quality requirements.
	• Maintain constant symmetry and spacing between the traces within a differential pair.	• To meet timing and signal quality requirements.
	• Keep the total length of each differential pair under 4 inches.	• Issues found with traces longer than 4 inches : IEEE phy conformance failures, excessive EMI and or degraded receive BER.
	• Do not route the transmit differential traces closer than 70 mils to the receive differential traces.	• To minimize cross-talk.
	• Distance between differential traces and any other signal line is 70 mils.	• To minimize cross-talk.
	• Keep Max separation between differential pairs to 7 mils.	• To meet timing and signal quality requirements.
	• Differential trace impedance should be controlled to be ~100 ohms.	• To meet timing and signal quality requirements.
	• For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two 45 degree bends.	• To meet timing and signal quality requirements.

√	Recommendations	Reason/Impact
	• Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	• This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
	• Do not route traces and vias under crystals or oscillators.	• This will prevent coupling to or from the clock.
	• Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	• To control trace EMI radiation.
	• Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	• Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.
	• Vias to decoupling capacitors should be sufficiently large in diameter.	• To decrease series inductance.
	• Avoid routing high-speed LAN* or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.	• To minimize crosstalk.
	• Isolate I/O signals from high-speed signals.	• To minimize crosstalk.
	• Place the 82562ET/EM part more than 1.5 inches away from any board edge.	• This minimizes the potential for EMI radiation problems.
	• Verify proper EEPROM size: —82562ET – 64 word —82562EM – 256 word	• The 82562EM requires a larger EEPROM to store the alert envelope and other configuration information.
	• Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the 82562ET/EM.	• Research and development has shown that this is a robust design recommendation.
	• Place decoupling capacitors (0.1 µF) as close to the 82562ET/EM as possible.	
	• RBIAS10 and RBIAS100 resistors should be 1% values	• These are biasing resistors that require 1% accuracy. Note that the values shown on the reference schematic are recommended starting values. Fine tuning (via IEEE conformance testing) is required for every new design.

16.13 Miscellaneous

√	Recommendations	Reason/Impact
	• 1.8 V Stand By: one 0.1 µF capacitor	• Refer to Section 9.12.
	• 5 V Reference: two 0.1 µF capacitors	• Refer to Section 9.12.
	• 5 V Reference Stand By: one 0.1 µF capacitor	• Refer to Section 9.12.

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Appendix A: Reference Schematics

The following pages contain reference schematics for both 4 layer and 6 layer 82850 platforms.

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CR-1

INTEL(R) PENTIUM 4 PROCESSOR IN THE 478 PIN PACKAGE PROCESSOR AND INTEL(R) 850 CHIPSET CUSTOMER REFERENCE SCHEMATIC

PAGE #	COMPONENT/FUNCTION
1	COVER PAGE
2	TABLES: BLOCK DIAGRAM
3	TABLES: RESET MAP
4	TABLES: CLOCK DISTRIBUTION
5	TABLES: GPIO/IDSEL MAPPING
6	CORE: CK_SKS (MAIN CLOCK GENERATOR)
7	CORE: DMCG RAMBUS CLOCK GEN
8-9	CORE: CPU CONNECTOR & DECOUPLING
10	CORE: CPU PULL-UPS & PULL-DOWNS
11-12	CORE: 82850 (TEHAMA)
13	CORE: 82850 DECOUPLING & REFERENCE VOLTAGES
14	CORE: AGP SLOT & AGP PULL-UPS/PULL-DOWNS
15-18	CORE: RIMM CONNECTORS (4) & RTERM DISCRETES
19-20	ICH2: 82801A I/O CONTROLLER HUB
21	ICH2: ICH2 PULL-UP/PULL-DOWNS
22	ICH2: GPIO REMAP
23	ICH2: LAN LINK
24	ICH2: IDE PRIMARY & SECONDARY
25	ICH2: USB BACK PANEL
26	ICH2: USB JUMPER BLOCK
27	ICH2: USB FRONT PANEL
28-32	ICH2: PCI SLOTS 5 - 1
33	ICH2: PCI PULL-UPS; PC/PCI HEADER
34	CNR CONNECTOR & POWER
35	USB2.0: QFP MODEL
36	USB2.0: BGA MODEL
37	LAN: KINNERETH & KINNERETH+
38	AUDIO: ADI1885 CODEC
39	AUDIO: CODEC FILTERING CAPS
40	AUDIO: ATAPI HEADERS
41	AUDIO: MIC-IN
42	AUDIO: MAIN OUTPUT AMP (SSM2250)
43	AUDIO: TRANSIENT CONTROL
44	AUDIO: VREG
45	SIO: LPC47M102
46	SIO: FLOPPY
47	SIO: KEYBOARD & MOUSE PORTS (PS/2)
48	SIO: PARALLEL PORT
49	SIO: COM1 & COM2; RI HEADER
50	FWH

PAGE #	COMPONENT/FUNCTION
51	GLUE4
52	HECETA4
53	PC SPEAKER
54	FRONT PANEL HEADER
55	ALTERNATE HEADERS
56	FAN: ADM1031 THERMAL/FAN CONTROL
57	FAN: FAN HEADERS (4)
58	SMBUS ISOLATION
59	DIAG LEDS
60	BLANK PAGE
61	VREG: POWER CONNECTOR
62	VREG: BATTERY
63	VREG: PCI VAUX; STR STBY GENERATION
64	VREG: 2.5V RIMM
65	VREG: 2.5V RIMM DECOUPLING
66	VREG: WAKE USB & PS/2
67	VREG: 12/3.3/1.8V STBY GENERATION
68	VREG: RIMM 1.8V CMOS
69	VREG: AGP (1.5V)/1.8V CORE/ 1.8V VTERM
70	VREG: AGP DECOUPLING
71	VREG: 1.8V CORE DECOUPLING
72	VREG: 1.8V VTERM DECOUPLING
73	VREG: CPU MAIN REGULATOR (VCCP)
74	VREG: CPU INPUT/OUTPUT CAPS
75	VREG: GENERIC BOARD DECOUPLING
76	IMPEDANCE COUPONS, TEST CAP SITES & LABELS
77	BACKSIDE CAP SITES (805)
78	DEBUG: SWITCHES AND MISC DEBUG
79	DEBUG: ITP CONN AND MISC DEBUG

6-LAYER DESIGN REV 1.0

POWER SYMBOLS USED:

VCC3
VCC
+12V
-12V
-5V (PAGE 65, POWER-CONN)

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT (PBA) ENG. PARTS LIST FOR ITEMS SHOWN AS OPTIONAL IN THIS SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC= +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
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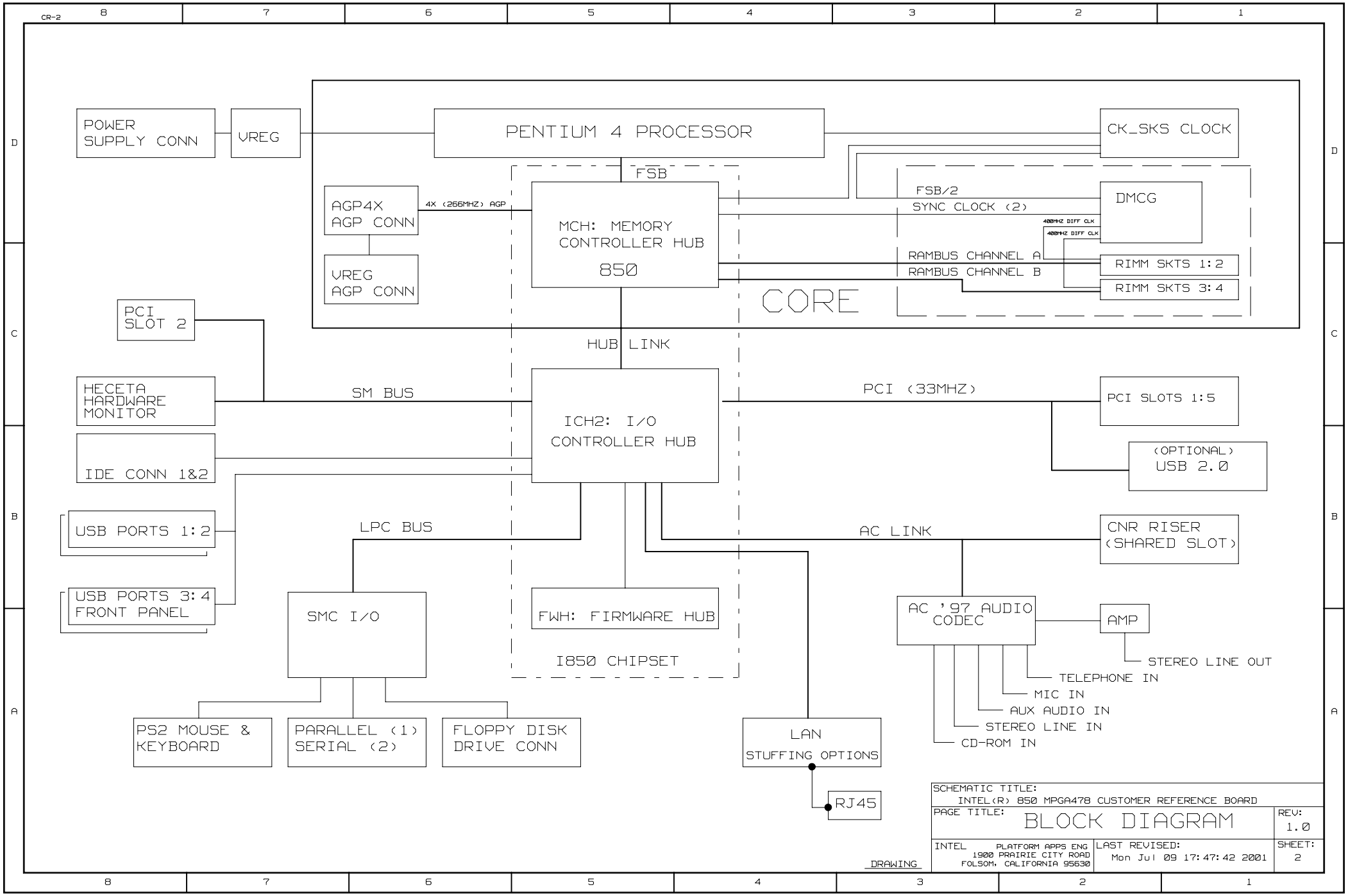
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CK_SKS CLOCK
FSB
AGP4X AGP CONN
4X (266MHZ) AGP
MCH: MEMORY CONTROLLER HUB 850
FSB/2
SYNC CLOCK (2)
DMCG
400MHZ DIFF CLK
400MHZ DIFF CLK
RAMBUS CHANNEL A
RAMBUS CHANNEL B
RIMM SKTS 1:2
RIMM SKTS 3:4
VREG AGP CONN
CORE
PCI SLOT 2
HUB LINK
HECETA HARDWARE MONITOR
SM BUS
ICH2: I/O CONTROLLER HUB
PCI (33MHZ)
PCI SLOTS 1:5
IDE CONN 1&2
(OPTIONAL) USB 2.0
USB PORTS 1:2
LPC BUS
AC LINK
CNR RISER (SHARED SLOT)
USB PORTS 3:4 FRONT PANEL
SMC I/O
FWH: FIRMWARE HUB
AC '97 AUDIO CODEC
AMP
STEREO LINE OUT
I850 CHIPSET
TELEPHONE IN
MIC IN
AUX AUDIO IN
STEREO LINE IN
CD-ROM IN
PS2 MOUSE & KEYBOARD
PARALLEL (1) SERIAL (2)
FLOPPY DISK DRIVE CONN
LAN STUFFING OPTIONS
RJ45
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
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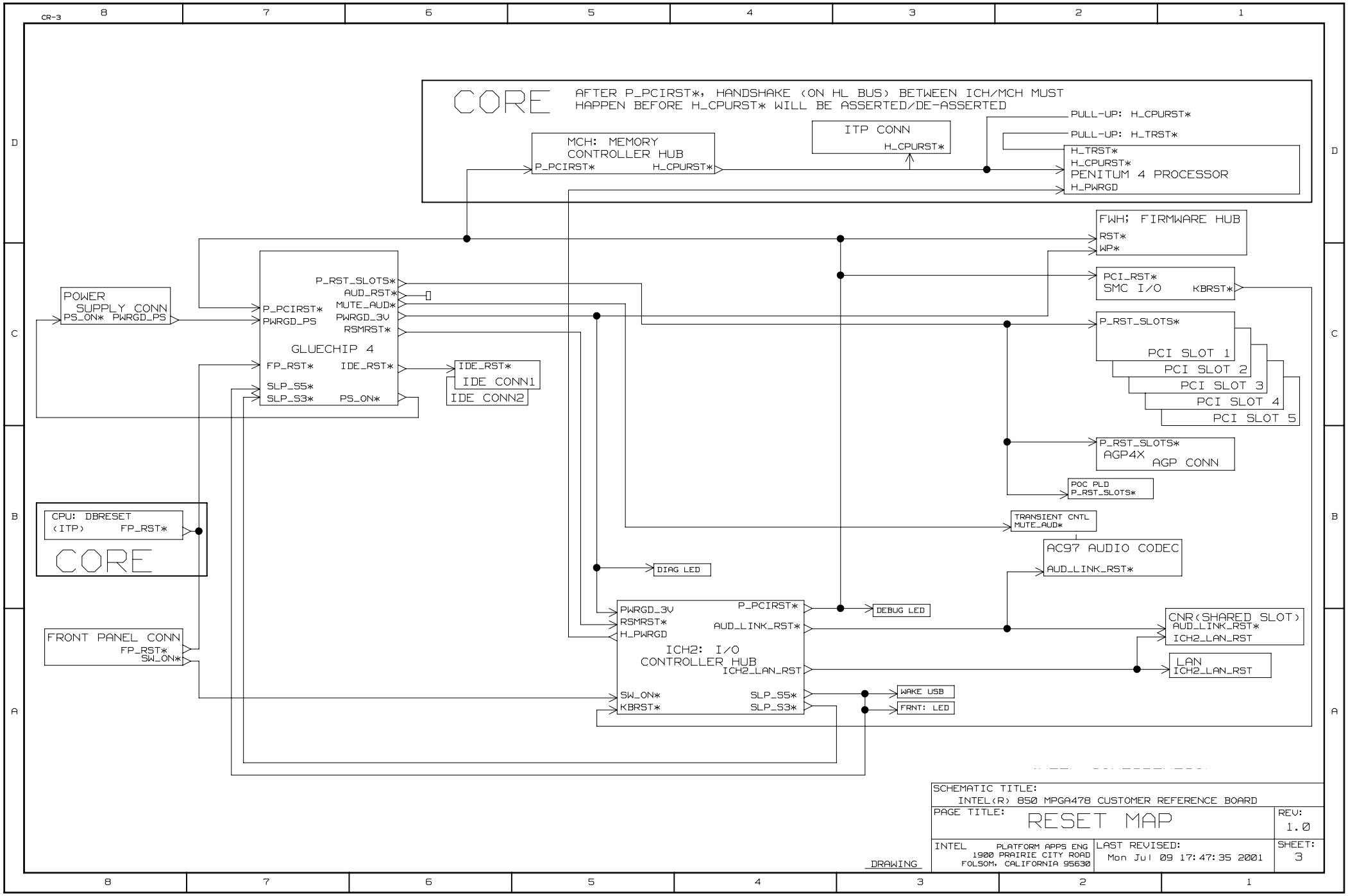
CR-3
CORE
AFTER P_PCIRST*, HANDSHAKE (ON HL BUS) BETWEEN ICH/MCH MUST HAPPEN BEFORE H_CPURST* WILL BE ASSERTED/DE-ASSERTED
PULL-UP: H_CPURST*
PULL-UP: H_TRST*
ITP CONN
H_CPURST*
MCH: MEMORY CONTROLLER HUB
P_PCIRST*
H_CPURST*
H_TRST*
H_CPURST*
PENITUM 4 PROCESSOR
H_PWRGD
FWH: FIRMWARE HUB
RST*
WP*
PCI_RST*
SMC I/O
KBRST*
POWER SUPPLY CONN
PS_ON*
PWRGD_PS
P_PCIRST*
PWRGD_PS
P_RST_SLOTS*
AUD_RST*
MUTE_AUD*
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IDE CONN2
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PCI SLOT 2
PCI SLOT 3
PCI SLOT 4
PCI SLOT 5
P_RST_SLOTS*
AGP4X
AGP CONN
POC PLD
P_RST_SLOTS*
CPU: DBRESET
(ITP)
FP_RST*
CORE
TRANSIENT CNTL
MUTE_AUD*
AC97 AUDIO CODEC
AUD_LINK_RST*
DIAG LED
PWRGD_3V
RSMRST*
H_PWRGD
P_PCIRST*
AUD_LINK_RST*
ICH2: I/O CONTROLLER HUB
ICH2_LAN_RST
SW_ON*
KBRST*
SLP_S5*
SLP_S3*
DEBUG LED
CNR(SHARED SLOT)
AUD_LINK_RST*
ICH2_LAN_RST
LAN
ICH2_LAN_RST
WAKE USB
FRNT: LED
FRONT PANEL CONN
FP_RST*
SW_ON*
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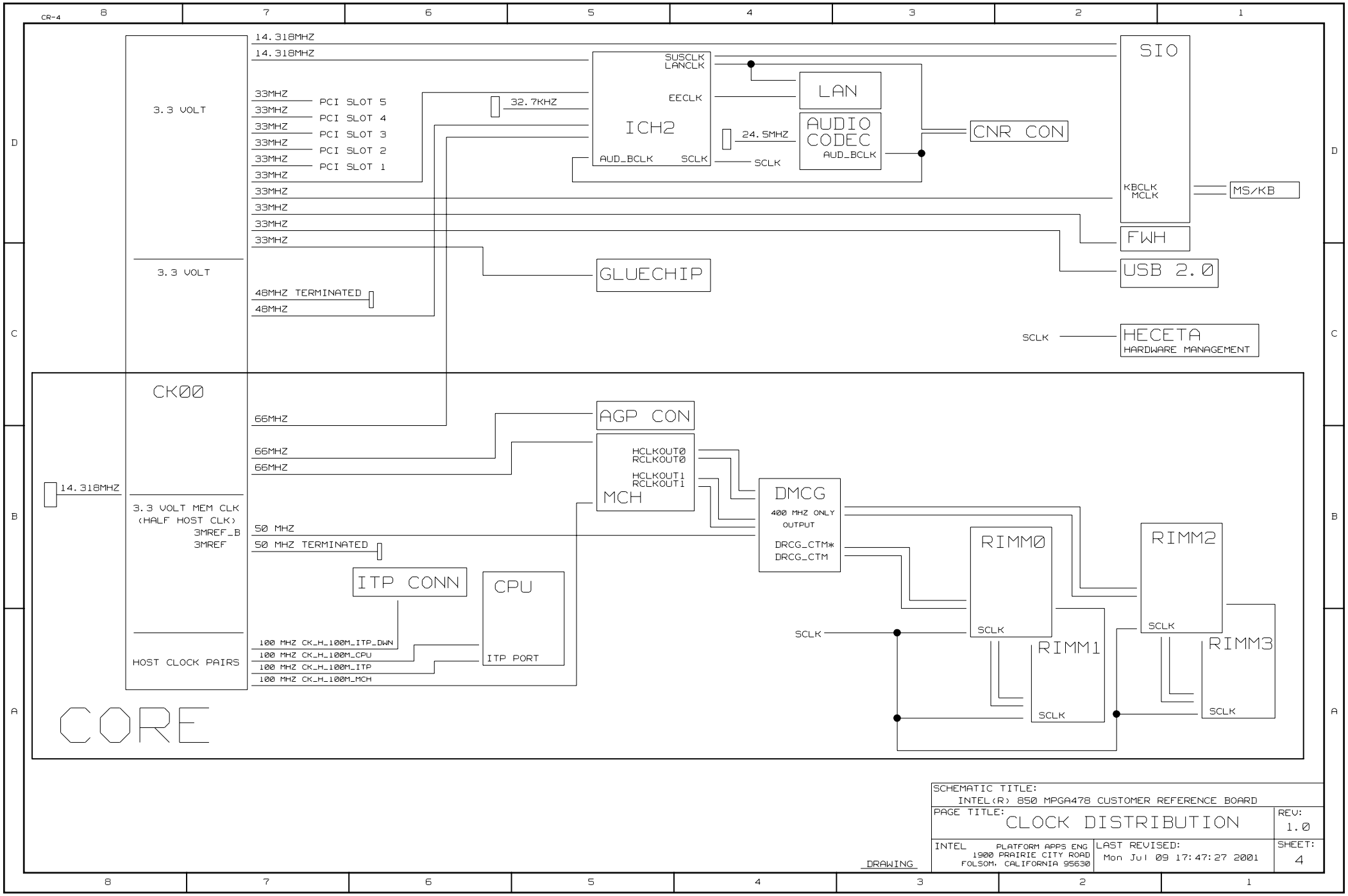
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33MHZ
PCI SLOT 5
PCI SLOT 4
PCI SLOT 3
PCI SLOT 2
PCI SLOT 1
32.7KHZ
SUSCLK
LANCLK
EECLK
ICH2
AUD_BCLK
SCLK
24.5MHZ
LAN
AUDIO CODEC
AUD_BCLK
CNR CON
SIO
KBCLK
MCLK
MS/KB
FWH
USB 2.0
GLUECHIP
3.3 VOLT
48MHZ TERMINATED
48MHZ
SCLK
HECETA
HARDWARE MANAGEMENT
CK00
66MHZ
AGP CON
HCLKOUT0
RCLKOUT0
HCLKOUT1
RCLKOUT1
MCH
14.318MHZ
3.3 VOLT MEM CLK
(HALF HOST CLK)
3MREF_B
3MREF
50 MHZ
50 MHZ TERMINATED
DMCG
400 MHZ ONLY
OUTPUT
DRCG_CTM*
DRCG_CTM
RIMM0
RIMM2
RIMM1
RIMM3
ITP CONN
CPU
ITP PORT
100 MHZ CK_H_100M_ITP_DWN
100 MHZ CK_H_100M_CPU
100 MHZ CK_H_100M_ITP
100 MHZ CK_H_100M_MCH
HOST CLOCK PAIRS
CORE
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
CLOCK DISTRIBUTION
REV:
1.0
INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Mon Jul 09 17:47:27 2001
SHEET:
4
DRAWING

CR-5

UPDATED 12/05/00

	PIN NAME	WELL	USAGE	DURING RESET	S3/S5	NOTES
ICH	GPIO[0]	MAIN	P_PCIREQA*	---	---	P/U ON PAGE 34, 2.7K TO VCC5
	GPIO[1]	MAIN	P_REQ5*	---	---	USB2.0 REQ
	GPI[2]	MAIN	P_INTE*	---	---	USED BY INTERNAL LAN DEVICE
	GPI[3]	MAIN	P_INTF*	---	---	SWIZZLED INTO PCI SLOTS
	GPI[4]	MAIN	P_INTG*	---	---	SWIZZLED INTO PCI SLOTS
	GPI[5]	MAIN	P_INTH*	---	---	USED BY INTERNAL USB CONTROLLER #2;USB2.0 INTA, SWIZZLED INTO PCI SLOTS
	GPI[6]	MAIN	GPIO_DMA66_DETECT_PRI	---	---	MATCHES EASTON
	GPI[7]	MAIN	GPIO_DMA66_DETECT_SEC	---	---	MATCHES EASTON
	GPI[8]	RESUME	SMI INPUT	---	---	WIRED-OR WITH USB2.0; PULLUP TO 10K 3.3VSB PG 48
	GPI[11]	RESUME	SMB_ALERT_PU	---	---	10K P/U PG 22
	GPI[12]	RESUME	SIO_GP42_IOPME*	---	---	10K P/U TO 3.3VSB PG 48
	GPI[13]	RESUME	CDC_DWN_ENAB*	---	---	10K P/U TO 3.3VSB PG23 (NOT USED); 10K P/D SITE PG 35
	GPO[16]	MAIN	P_PCIGNTA*	HI-Z	OFF	PC/PCI HEADER PG 34; 10K EMPTY SITE PG 34
	GPO[17]	MAIN	P_GNT5*	HIGH	OFF	USED BY USB2.0 OR ES1373 PCI GNT
	GPO[18]	MAIN	ICH2_GPO18_FAN	HIGH	OFF	3RD FAN CONTROL OUTPUT FROM ICH2
	GPO[19]	MAIN	GPIO_DIAGLED_DATA	HIGH	OFF	
	GPO[20]	MAIN	GPIO_MEM_SPD_WE*	HIGH	OFF	DISABLED BY DEFAULT PG 16
	GPO[21]	MAIN	NOT USED	HIGH	OFF	DRCG LOW POWER-UP REQUIRES GPO TO DEFAULT HIGH (CAN'T USE FOR DMCG)
	GPO[22]	MAIN	GPIO_NO_POP*	HI-Z	OFF	O/D OUTPUT; P/U ON PAGE 55
	GPO[23]	MAIN	GPIO_DIAGLED_STB	LOW	OFF	
	GPIO[24]	RESUME	GPIO_AUD_EN (OUTPUT)	LOW	OFF	USED TO HOLD AUDIO CONTROLLERS IN RESET TO DISABLE
	GPIO[25]	RESUME	GPIO_GRN_BLNK (OUTPUT)	HIGH	DEFINED	GPIO 25, 27, 28 ARE BLINK CAPABLE
	GPIO[27]	RESUME	GPIO_YLW_BLNK (OUTPUT)	HI-Z	DEFINED	GPIO 25, 27, 28 ARE BLINK CAPABLE
	GPIO[28]	RESUME	GPIO_LAN_DISABLE/EMAIL_LED(OUTPUT)	HI-Z	DEFINED	GPIO 25, 27, 28 ARE BLINK CAPABLE
FWH	GPI4		CONFIG JUMPER	INPUT	DEFINED	CONFIG JUMPER
	GPI3		MANUF MODE	INPUT	DEFINED	MANUF MODE
	GPI2		HI/LOW BIOS CONFIG	INPUT	DEFINED	HI/LOW BIOS CONFIG
	GPI1		HI/LOW BIOS CONFIG	INPUT	DEFINED	HI/LOW BIOS CONFIG
	GPI0		HI/LOW BIOS CONFIG	INPUT	DEFINED	HI/LOW BIOS CONFIG
SIO	GPI5		AGP_PRO_PRSNT2	INPUT	DEFINED	FOR AGPPRO50 CARD DETECTIONS
	GPI6		AGP_PRO_PRSNT1	INPUT	DEFINED	FOR AGPPRO50 CARD DETECTIONS
	GPO22		GPIO_RMB_FREQ0	INPUT	DEFINED	USED TO SETUP DMCG FREQUENCY 300/400
	GPO61		GPIO_RMB_FREQ1	INPUT	DEFINED	USED TO SETUP DMCG FREQUENCY 300/400
	GP027/IOSMI*		IO_SMI*	INPUT	DEFINED	SENDS IO SMI REQUEST TO ICH2
	GPO60		100*/133 SELECT	INPUT	DEFINED	100*/133 SELECT

IRQ ROUTING TABLE
MATCHES EASTON FAB B

	AGP	SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	AC97,MODEM,SMBUS	USB #1	LAN	USB #2	USB 2.0
P_INTA*	IRQA										
P_INTB*	IRQB	IRQD	IRQC	IRQB	IRQA	IRQD	X				
P_INTC*											IRQB
P_INTD*								X			IRQA
P_INTE*									X		
P_INTF*		IRQA	IRQD	IRQC	IRQB	IRQA					
P_INTG*		IRQB	IRQA	IRQD	IRQC	IRQB					
P_INTH*		IRQC	IRQB	IRQA	IRQD	IRQC				X	IRQC
REQ/GNT		0	1	2	3	4					5
IDSEL		25	26	27	28	29					17
					OPT 19						

DRAWING

SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD

PAGE TITLE:
GPIO, IRQ, IDSEL MAPS

REV: 1.0

INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

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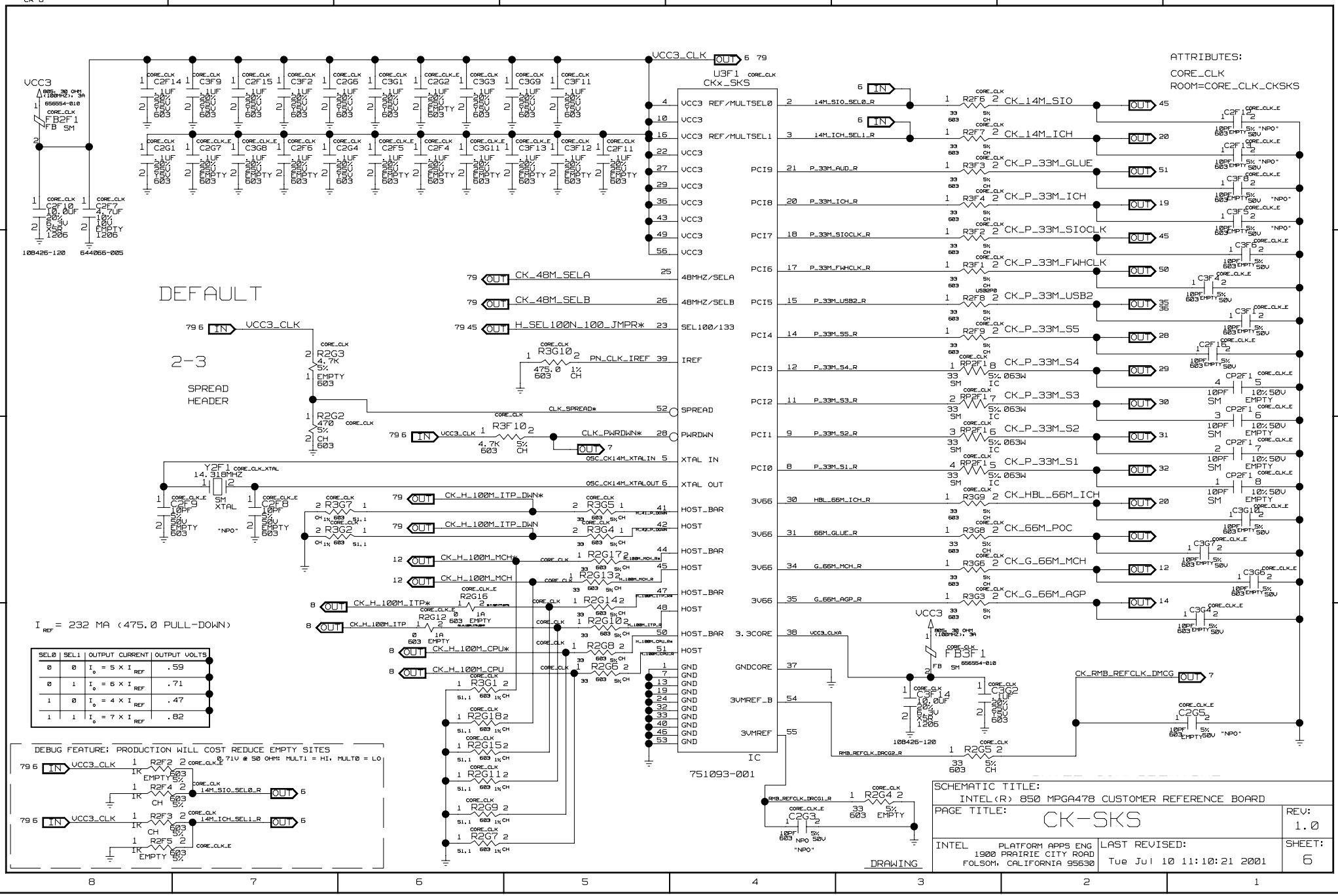
SHEET: 5


CR-6
ATTRIBUTES:
CORE_CLK
ROOM=CORE_CLK_CKSKS
U3F1
CKx_SKS
751093-001
IC
DEFAULT
2-3
SPREAD
HEADER
VCC3_CLK
CK_48M_SELA
CK_48M_SELB
H_SEL100N_100_JMPR*
PN_CLK_IREF
CLK_SPREAD*
CLK_PWRDWN*
OSC_CK14M_XTALIN
OSC_CK14M_XTALOUT
CK_H_100M_ITP_DWN*
CK_H_100M_ITP_DWN
CK_H_100M_MCH*
CK_H_100M_MCH
CK_H_100M_ITP*
CK_H_100M_ITP
CK_H_100M_CPU*
CK_H_100M_CPU
CK_14M_SIO
CK_14M_ICH
CK_P_33M_GLUE
CK_P_33M_ICH
CK_P_33M_SIOCLK
CK_P_33M_FWHCLK
CK_P_33M_USB2
CK_P_33M_S5
CK_P_33M_S4
CK_P_33M_S3
CK_P_33M_S2
CK_P_33M_S1
CK_HBL_66M_ICH
CK_66M_POC
CK_G_66M_MCH
CK_G_66M_AGP
CK_RMB_REFCLK_DMCG
I REF = 232 MA (475.0 PULL-DOWN)
SEL0 | SEL1 | OUTPUT CURRENT | OUTPUT VOLTS
0 | 0 | I o = 5 X I REF | .59
0 | 1 | I o = 6 X I REF | .71
1 | 0 | I o = 4 X I REF | .47
1 | 1 | I o = 7 X I REF | .82
DEBUG FEATURE: PRODUCTION WILL COST REDUCE EMPTY SITES
0.71V @ 50 OHM: MULT1 = HI, MULT0 = LO
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
CK-SKS
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
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DRAWING

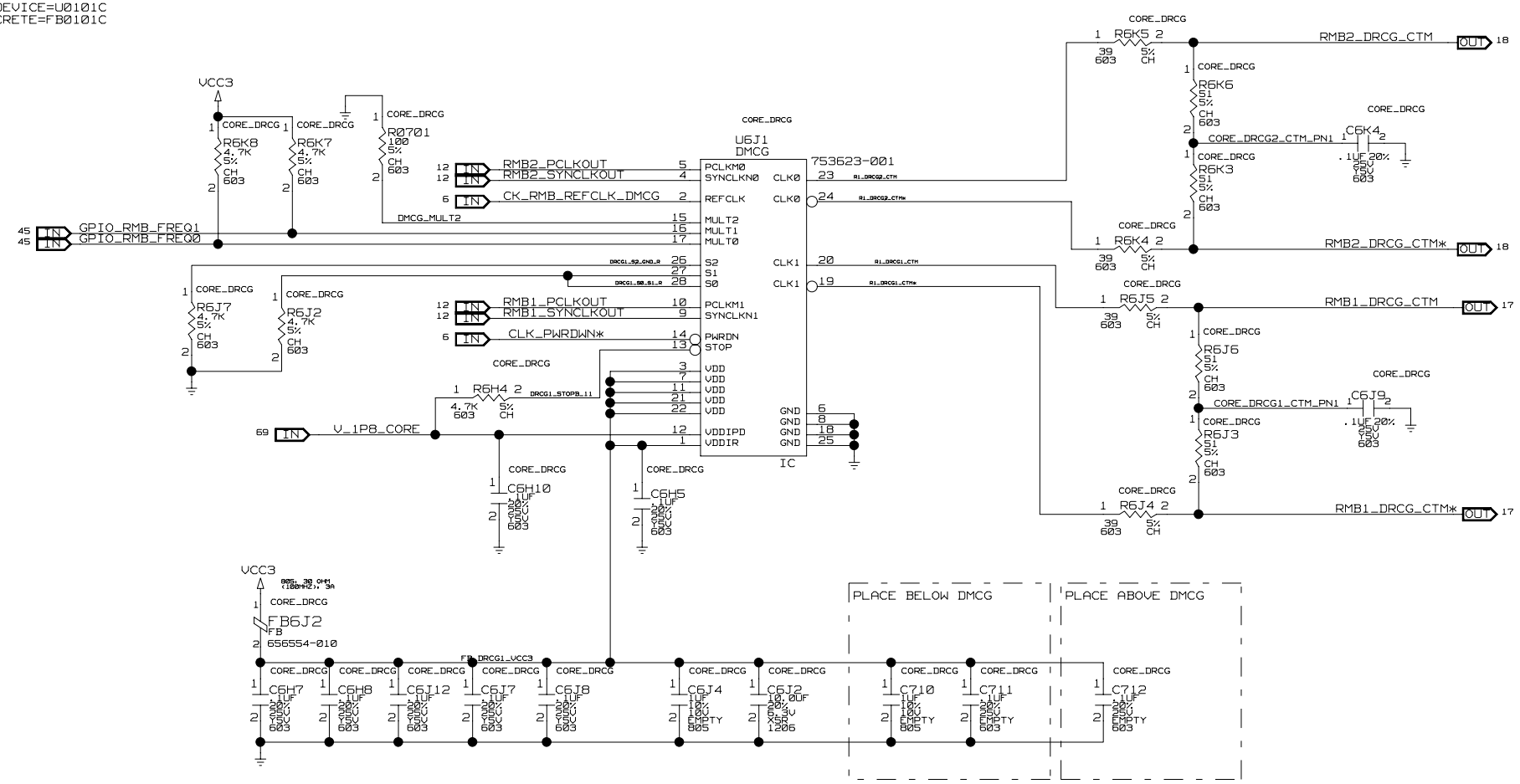
CR-7

LAST_USED:

RESISTOR=R0112C
CAPACITOR=C0113C
NO RES PAK
NO TEST POINT
IC_DEVICE=U0101C
DISCRETE=FB0101C

ATTRIBUTES:

CORE_DRCG



FUNCTION	S0	S1	S2	CLK	CLKB
NORMAL	0	0	0	NORM	NORM
BYPASS	1	0	0	PLLCLK	PLLCLKB
TEST	1	1	0	REFCLK	REFCLKB
OUTPUT TEST (OE)	0	1	X	HI-Z	HI-Z
RESERVED	0	0	1	---	---
RESERVED	1	0	1	---	---
RESERVED	1	1	1	HI-Z	HI-Z

MULT0	MULT1	MULT2	PLLCLK	REFCLK
0	0	0	4	1
0	1	0	6	1
1	1	0	8	1
1	0	0	8	3

REFCLK & PLL MULTIPLIER SELECT TABLE
DATA FROM CY2211 DRCG SPEC, 10/27/98

ROOM=CORE_CLK_DRCG
BOM=CORE_DRCG
BOM=CORE_DRCG_DCPL FOR DEFAULT EMPTY
BOM=CORE_*** FOR CONFIGURATION OPTIONS AS NOTED

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD

PAGE TITLE: DMCG

REV: 1.0

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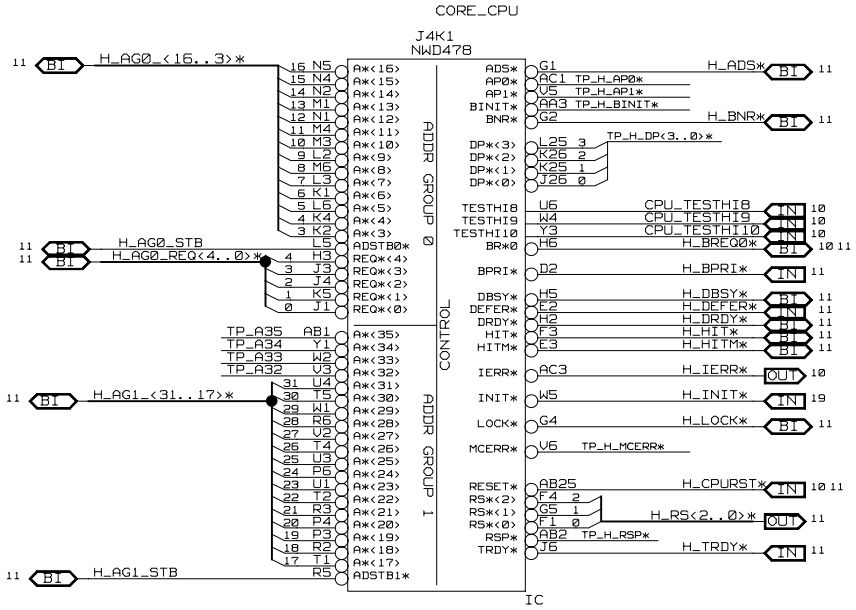
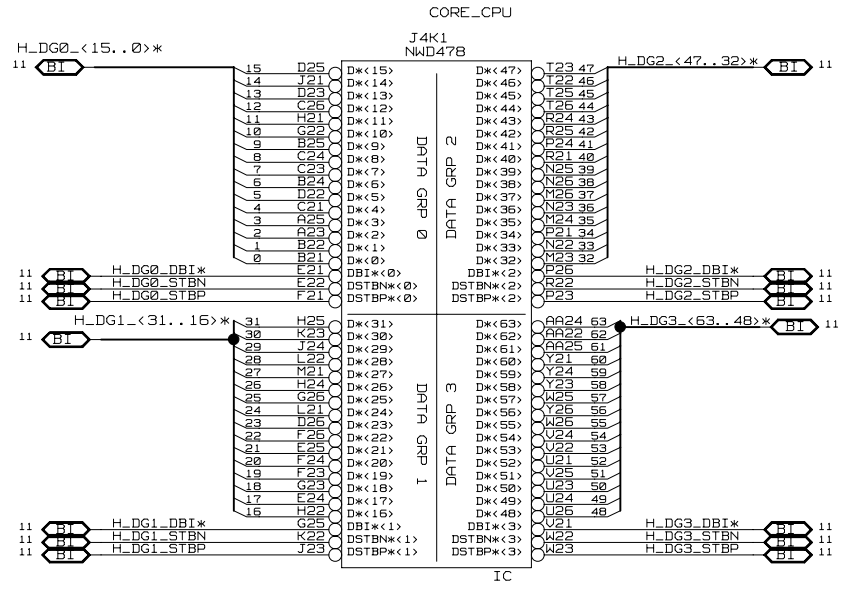
SHEET: 7

CR-8

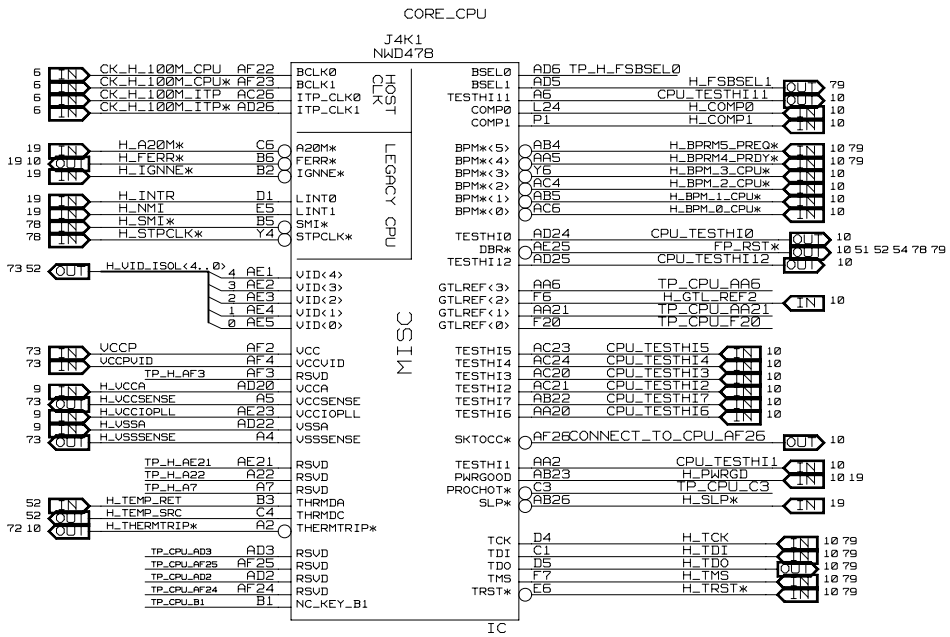
ATTRIBUTES:

CORE_CPU
ROOM=CORE





GND=AF7,AF24,AF22,AF19
GND=AD14,AD12,AD10,AD8,AD4,AD1,AD23,AD21,AE17,AE15,AE13,AE11,AE9,AE25
GND=AB20,AC17,AC15,AC13,AC11,AC9,AC7,AC5,AC2,AC22,AC19,AD18,AD16
GND=AA24,AA1,AA23,AB19,AB18,AB16,AB14,AB12,AB10,AB8,AB6,AB3,AB24,AB21
GND=V4,V1,V23,W6,W3,W24,W21,Y5,Y2,Y22,AA17,AA15,AB13,AA11,AA8,AA26,AA7
VCCP=AD11,AD9,AD7,AD19,AE18,AE16,AE14,AE12,AE10,AE8,AE6,AE20
VCCP=AB15,AB13,AB11,AB9,AB7,AB19,AC18,AC16,AC14,AC12,AC10,AC8,AD17,AD15,AD13
VCCP=F14,F12,F10,F8,E20,D7,F15,F13,F11,F9,F19,AA18,AA16,AA14,AA12,AA10,AA8,AB17
VCCP=B13,B11,B9,B7,B19,C18,C16,C14,C12,C10,C8,C20,D17,D15,D13,D11,D9,D7,D19,E18,E16
VCCP=AF17,AF15,AF13,AF11,AF9,AF7,AF5,AF21,AF19,AF18,AF16,AF14,AF12,AF10,AF8,AF20,B17,B15
GND=W24,Y2,Y5,Y22,Y25,AA1,AA4,AA7,AA9,AA11,AA13,AA15,AA17,AA19,AA23,AA26
GND=K6,N3,N22,N21,P5,P2,P24,P22,R20,R4,R1,R23,T6,T3,T24,T21,U5,U2,U22,U25,V26
GND=G21,H20,H4,H1,H23,J5,J2,J25,J22,K6,K3,K24,K21,L26,L4,L1,L23,M5,M2,M25,M22
GND=F11,F9,F26,F7,F4,E1,E23,E19,F18,F16,F14,F12,F10,F8,F5,F2,F25,F22,G6,G3,G24
GND=C3,C2,C25,C22,C19,D18,D16,D14,D12,D10,D8,D6,D3,D24,D21,D20,E17,E15,E13
GND=A3,A24,A21,A19,B18,B16,B14,B12,B10,B26,B8,B4,B23,B20,C17,C15,C13,C11,C9,C7
GND=AF18,AF16,AF14,AF12,AF10,AF26,AF8,AF6,AF1,AF20,A17,A15,A13,A11,A9,A26



SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: CPU CONNECTOR	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:26 2001
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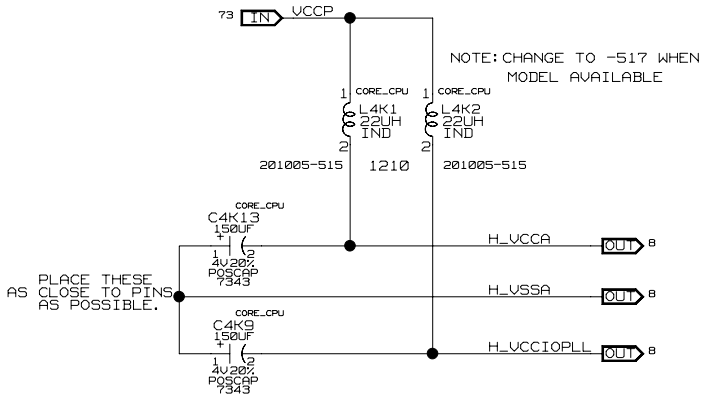
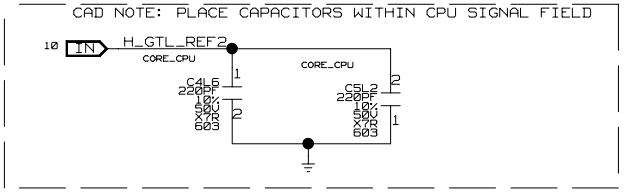
CR-9

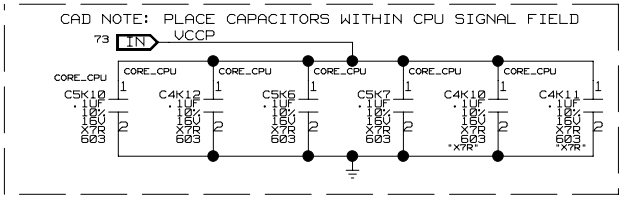
LAST_USED:

NO RESISTOR
CAPACITOR C1000C
NO RES PAK
NO TEST POINT

ATTRIBUTES:
CORE_CPU
ROOM=CORE

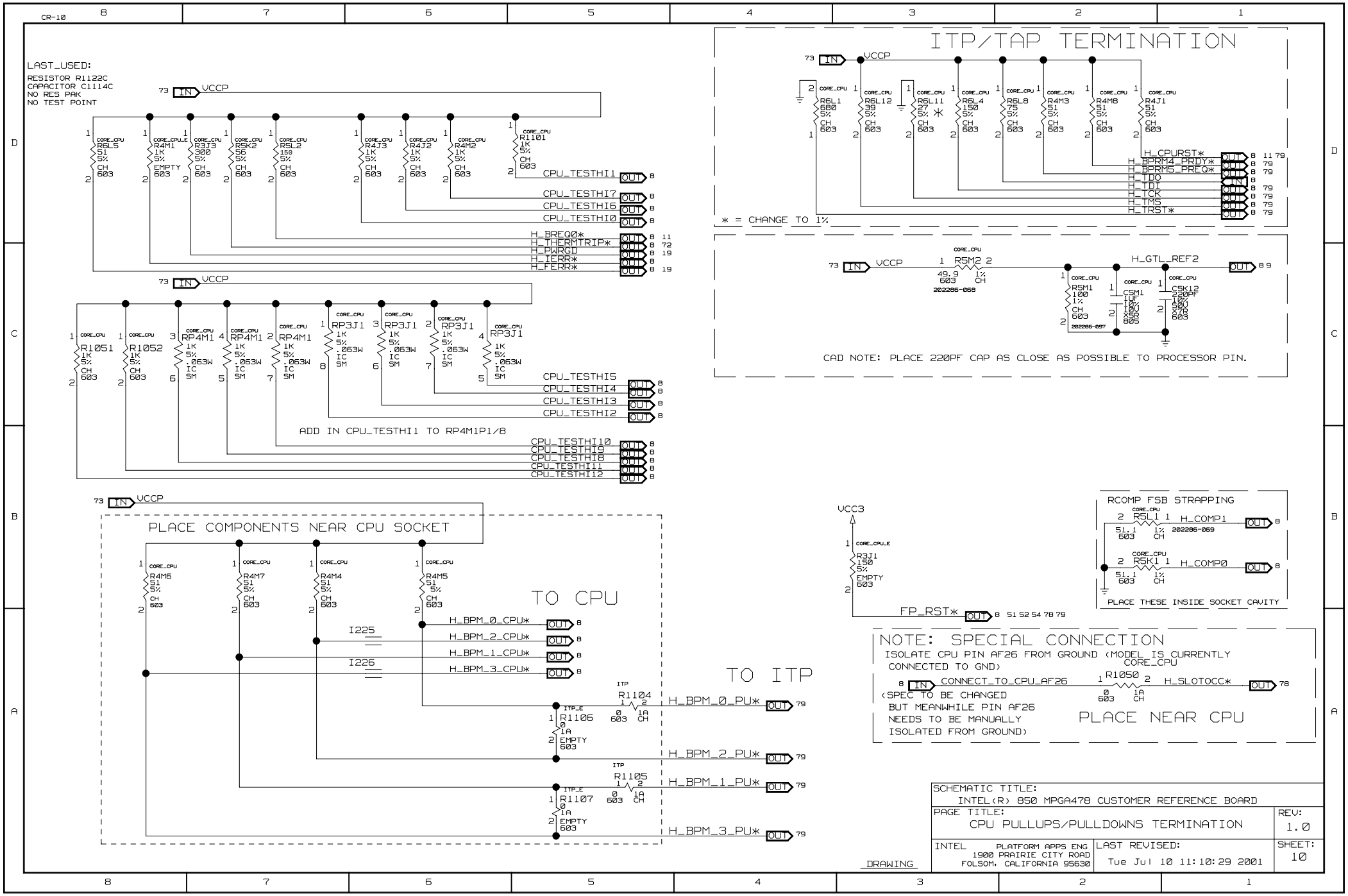






SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU DECOUPLING		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:28 2001	SHEET: 9

DRAWING


CR-10
LAST_USED:
RESISTOR R1122C
CAPACITOR C1114C
NO RES PAK
NO TEST POINT
ITP/TAP TERMINATION
VCCP
CPU_TESTHI1
CPU_TESTHI7
CPU_TESTHI6
CPU_TESTHI0
H_BREQ0*
H_THERMTRIP*
H_PWRGD
H_IERR*
H_FERR*
H_CPURST*
H_BPRM4_PRDY*
H_BPRM5_PREQ*
H_TDO
H_TDI
H_TCK
H_TMS
H_TRST*
* = CHANGE TO 1%
H_GTL_REF2
CAD NOTE: PLACE 220PF CAP AS CLOSE AS POSSIBLE TO PROCESSOR PIN.
CPU_TESTHI5
CPU_TESTHI4
CPU_TESTHI3
CPU_TESTHI2
ADD IN CPU_TESTHI1 TO RP4M1P1/8
CPU_TESTHI10
CPU_TESTHI9
CPU_TESTHI8
CPU_TESTHI11
CPU_TESTHI12
PLACE COMPONENTS NEAR CPU SOCKET
TO CPU
H_BPM_0_CPU*
H_BPM_2_CPU*
H_BPM_1_CPU*
H_BPM_3_CPU*
TO ITP
H_BPM_0_PU*
H_BPM_2_PU*
H_BPM_1_PU*
H_BPM_3_PU*
VCC3
FP_RST*
RCOMP FSB STRAPPING
H_COMP1
H_COMP0
PLACE THESE INSIDE SOCKET CAVITY
NOTE: SPECIAL CONNECTION
ISOLATE CPU PIN AF26 FROM GROUND (MODEL IS CURRENTLY CONNECTED TO GND)
CONNECT_TO_CPU_AF26
H_SLOTOCC*
(SPEC TO BE CHANGED BUT MEANWHILE PIN AF26 NEEDS TO BE MANUALLY ISOLATED FROM GROUND)
PLACE NEAR CPU
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
CPU PULLUPS/PULLDOWNS TERMINATION
REV:
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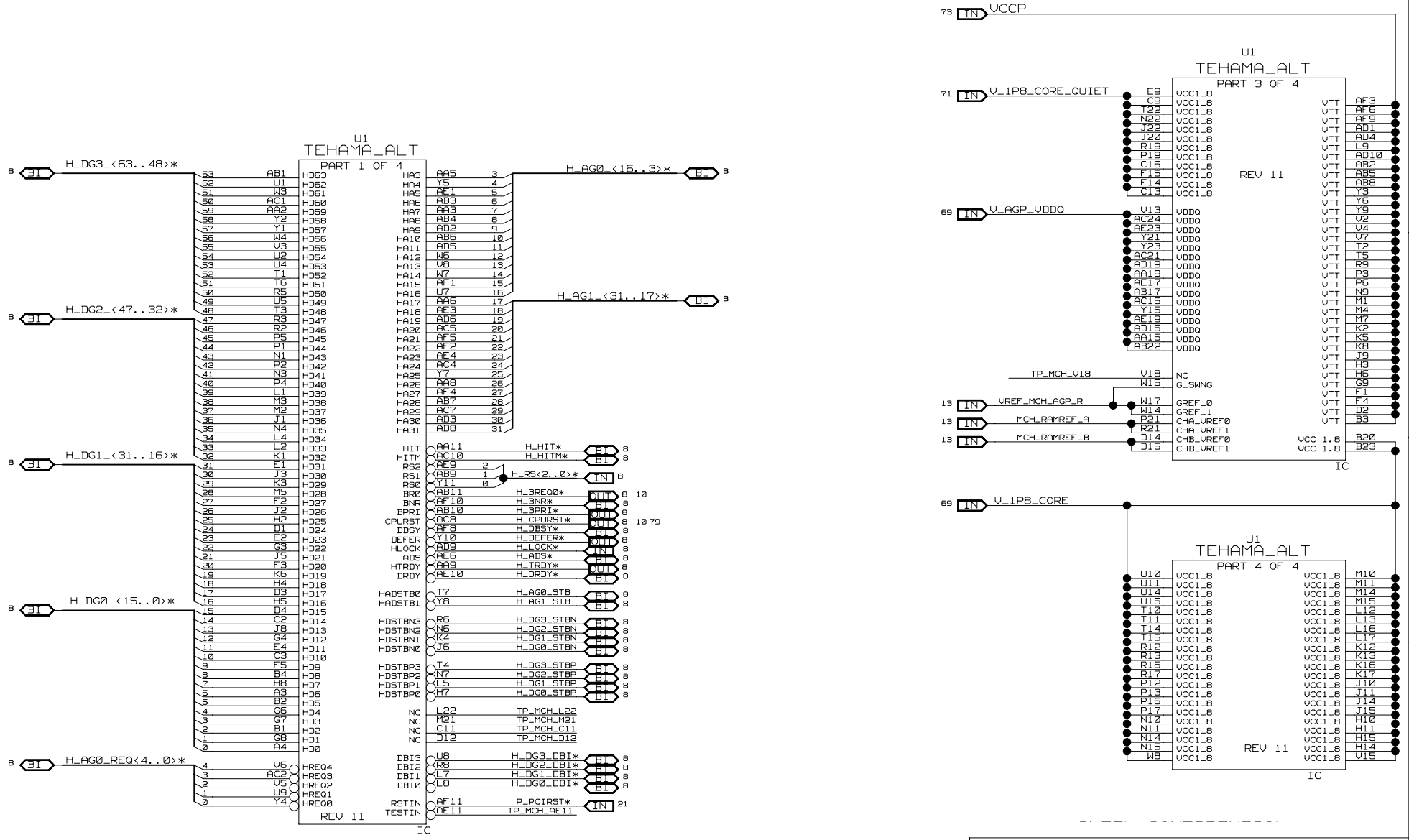
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:10:29 2001
SHEET:
10
DRAWING



SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD

PAGE TITLE: MCH: CHIPSET

REV: 1.0

INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
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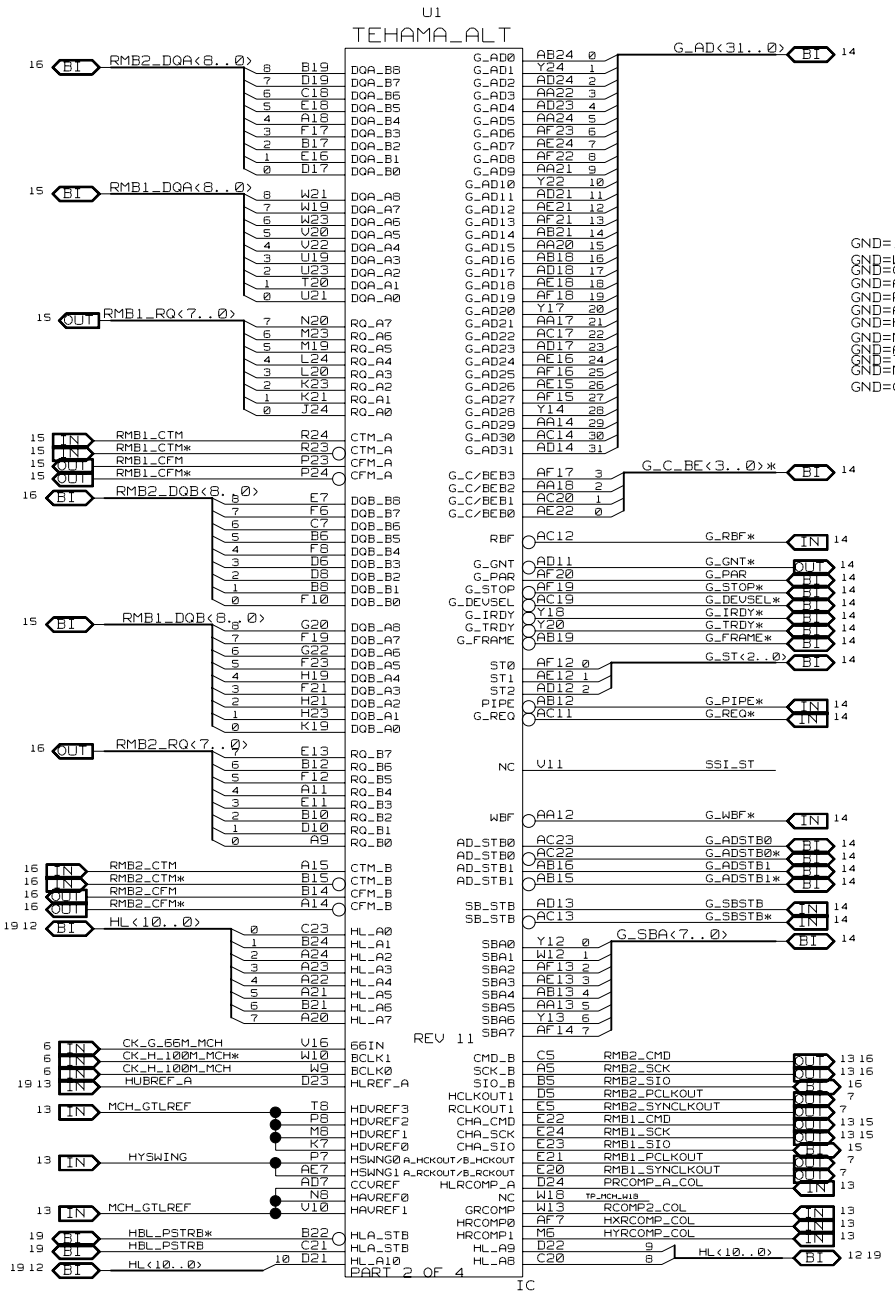
LAST REVISED: Tue Jul 10 11:10:31 2001

SHEET: 11

CHIPSET; PART 1 OF 2

DRAWING

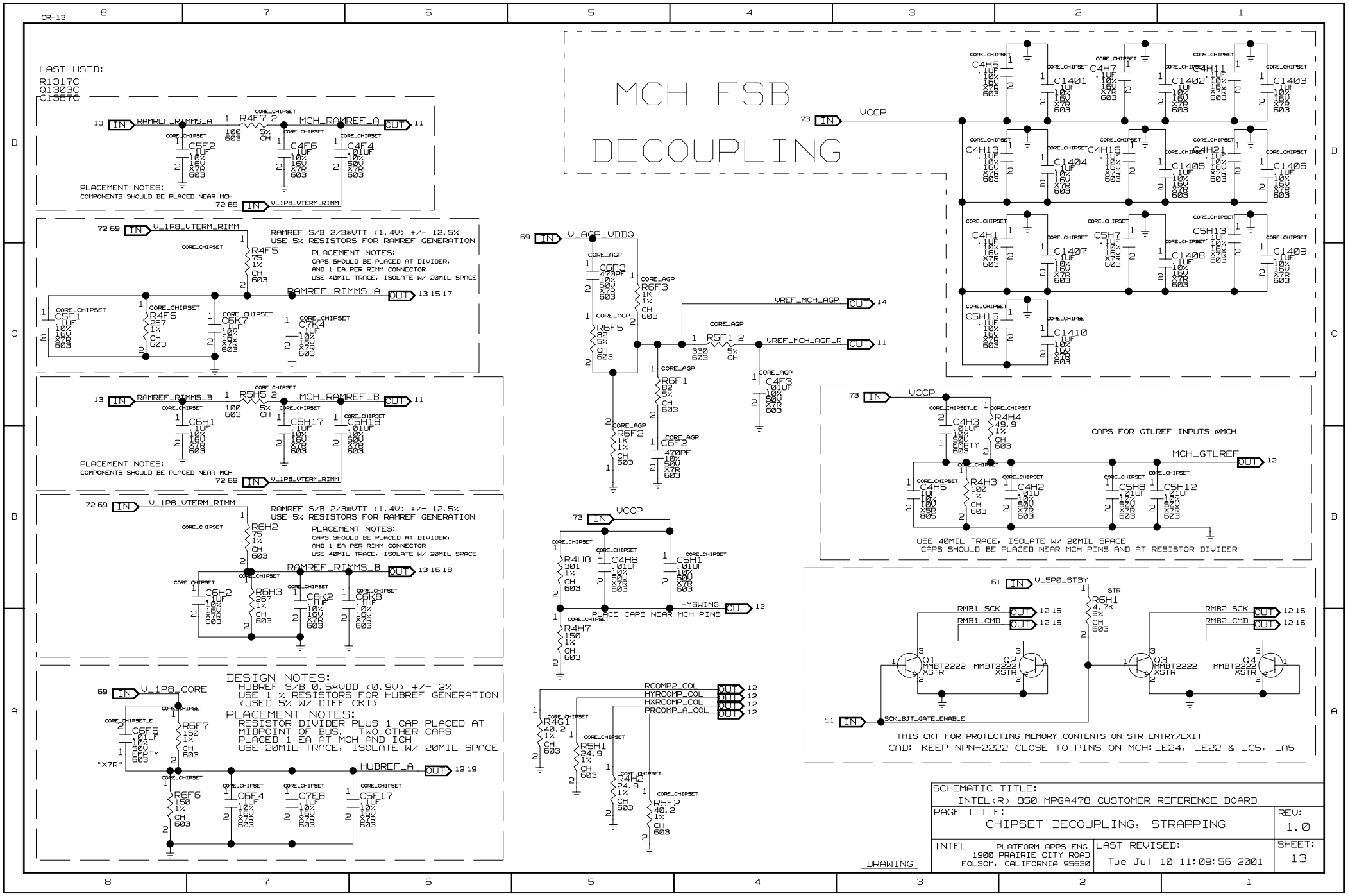


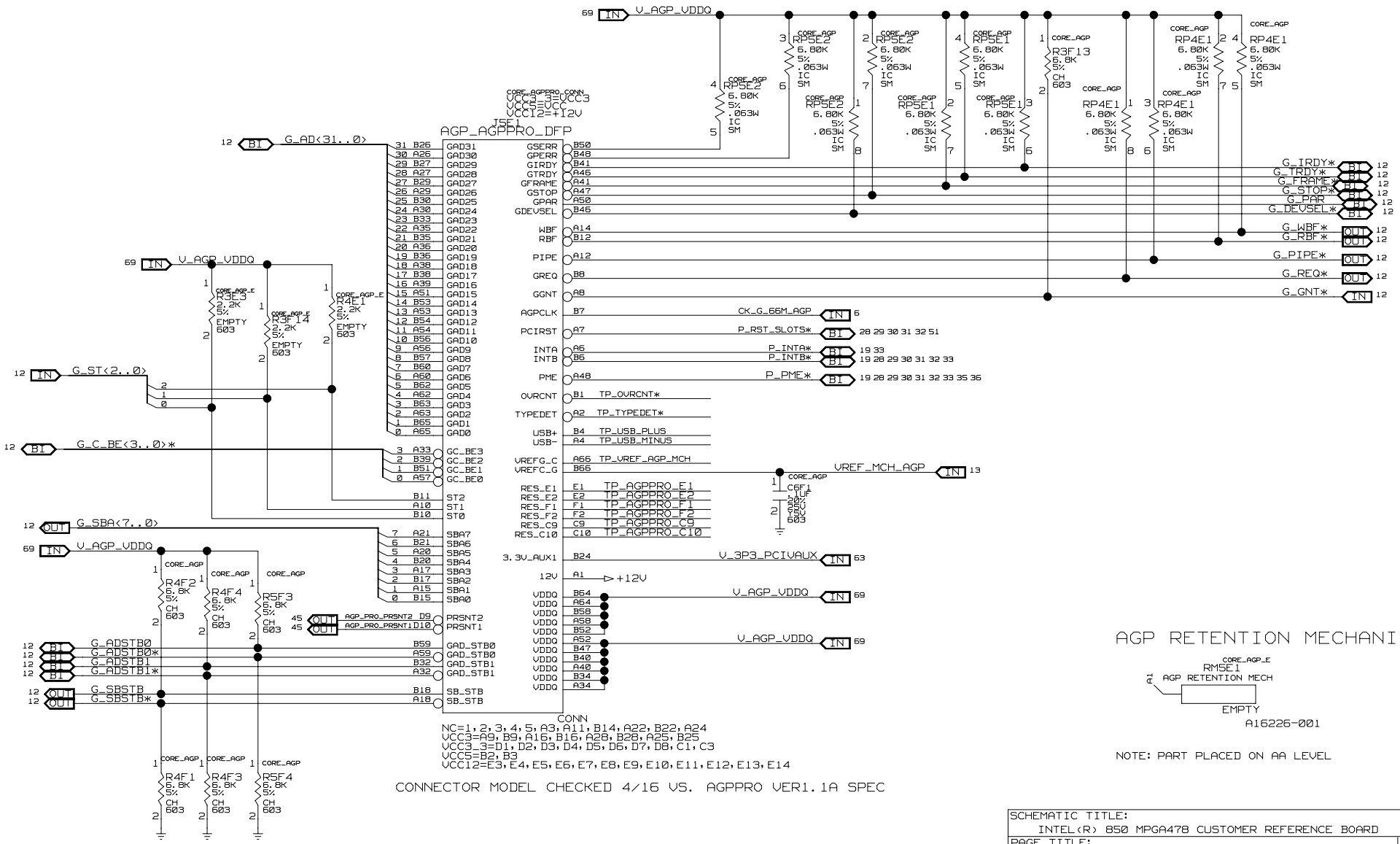
GND=1,2,3,4,V17
GND=W11,V17
GND=C22,C24,D20
GND=AF24,AE14,AE20,AD16,AD22,AC18,AB14,AB20,AB23,AA16,W16,V12,V14
GND=R7,P9,N2,N5,M9,L3,L6,K9,J4,J7,H9,G2,G5,E3,C1,C4,A2
GND=AE2,AE5,AE8,AC3,AC6,AC9,AA1,AA4,AA7,AA10,W2,W5,V9,U3,U6,T9,R1,R4
GND=H12,H13,H16,H17,J12,J13,J16,J17,K10,K11,K14,K15,L10,L11,L14,L15,M12,M13,M16
GND=M17,N12,N13,N16,N17,P10,P11,P14,P15,R10,R11,R14,R15,T12,T13,T16,T17,U12,U13,U16,U17
GND=AD20,AC16,AA23,Y16,A7,Y19,W20,W22,V19,V21,V23,U18,U20,U22,U24,T18,A19
GND=T19,T21,T23,T24,R16,R20,R22,P18,P20,P22,N18,N19,N21,N23,N24,M18,M20,A16,A17
GND=M22,M24,L18,L19,L21,L23,K18,K20,K22,K24,J18,J19,J21,J23,H18,H20,H22,G10..G19
GND=G21,G23,F7,F9,F11,F13,F16,F18,F20,F22,F24,E6,E8,E10,E12,E14,E15,E17,E19,D7,D9,A13

CHIPSET: PART 2 OF 2

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: MCH: CHIPSET		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:33 2001	SHEET: 12

DRAWING

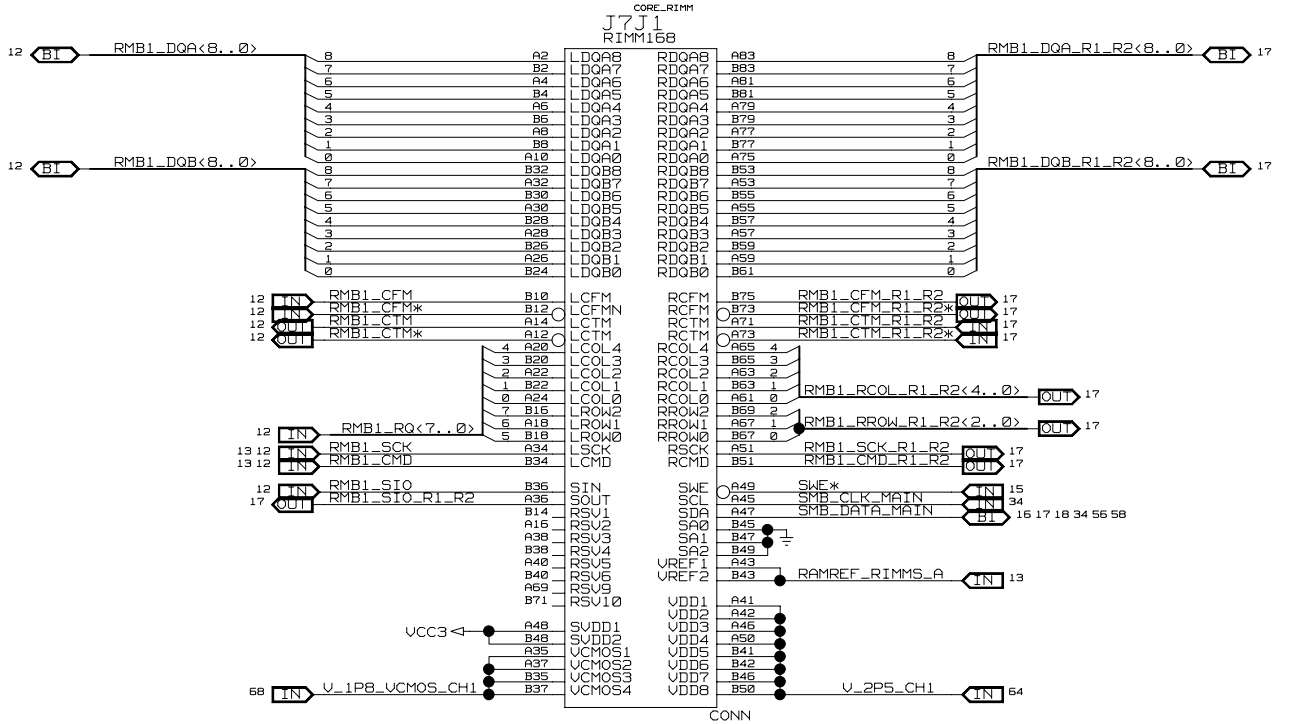

CR-13
LAST USED:
R1317C
Q1303C
C1367C
MCH FSB
DECOUPLING
RAMREF_RIMMS_A
MCH_RAMREF_A
PLACEMENT NOTES:
COMPONENTS SHOULD BE PLACED NEAR MCH
V_1P8_VTERM_RIMM
RAMREF S/B 2/3*VTT (1.4V) +/- 12.5%
USE 5% RESISTORS FOR RAMREF GENERATION
PLACEMENT NOTES:
CAPS SHOULD BE PLACED AT DIVIDER,
AND 1 EA PER RIMM CONNECTOR
USE 40MIL TRACE, ISOLATE W/ 20MIL SPACE
RAMREF_RIMMS_B
MCH_RAMREF_B
V_1P8_CORE
DESIGN NOTES:
HUBREF S/B 0.5*VDD (0.9V) +/- 2%
USE 1 % RESISTORS FOR HUBREF GENERATION
(USED 5% W/ DIFF CKT)
PLACEMENT NOTES:
RESISTOR DIVIDER PLUS 1 CAP PLACED AT
MIDPOINT OF BUS. TWO OTHER CAPS
PLACED 1 EA AT MCH AND ICH
USE 20MIL TRACE, ISOLATE W/ 20MIL SPACE
HUBREF_A
V_AGP_VDDQ
VREF_MCH_AGP
VREF_MCH_AGP_R
VCCP
HYSWING
PLACE CAPS NEAR MCH PINS
RCOMP2_COL
HYRCOMP_COL
HXRCOMP_COL
PRCOMP_A_COL
CAPS FOR GTLREF INPUTS @MCH
MCH_GTLREF
USE 40MIL TRACE, ISOLATE W/ 20MIL SPACE
CAPS SHOULD BE PLACED NEAR MCH PINS AND AT RESISTOR DIVIDER
V_5P0_STBY
RMB1_SCK
RMB1_CMD
RMB2_SCK
RMB2_CMD
SCK_BJT_GATE_ENABLE
THIS CKT FOR PROTECTING MEMORY CONTENTS ON STR ENTRY/EXIT
CAD: KEEP NPN-2222 CLOSE TO PINS ON MCH: _E24, _E22 & _C5, _A5
DRAWING
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
CHIPSET DECOUPLING, STRAPPING
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:09:56 2001
SHEET:
13

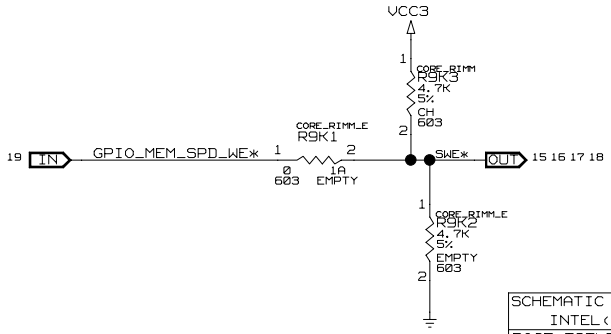

CR-14
V_AGP_VDDQ
G_AD<31..0>
G_ST<2..0>
G_C_BE<3..0>*
G_SBA<7..0>
G_ADSTB0
G_ADSTB0*
G_ADSTB1
G_ADSTB1*
G_SBSTB
G_SBSTB*
CORE_AGPPRO_CONN
VCC3_3=VCC3
VCC5=VCC
VCC12=+12V
J5E1
AGP_AGPPRO_DFP
GAD31 GAD30 GAD29 GAD28 GAD27 GAD26 GAD25 GAD24 GAD23 GAD22 GAD21 GAD20 GAD19 GAD18 GAD17 GAD16 GAD15 GAD14 GAD13 GAD12 GAD11 GAD10 GAD9 GAD8 GAD7 GAD6 GAD5 GAD4 GAD3 GAD2 GAD1 GAD0
GC_BE3 GC_BE2 GC_BE1 GC_BE0
ST2 ST1 ST0
SBA7 SBA6 SBA5 SBA4 SBA3 SBA2 SBA1 SBA0
PRSNT2 PRSNT1
GAD_STB0 GAD_STB0 GAD_STB1 GAD_STB1
SB_STB SB_STB
GSERR GPERR GIRDY GTRDY GFRAME GSTOP GPAR GDEVSEL
WBF RBF
PIPE
GREQ
GGNT
AGPCLK
PCIRST
INTA INTB
PME
OVRCNT
TYPEDET
USB+ USB-
VREFG_C VREFC_G
RES_E1 RES_E2 RES_F1 RES_F2 RES_C9 RES_C10
3.3V_AUX1
12V
VDDQ
CK_G_66M_AGP
P_RST_SLOTS*
P_INTA*
P_INTB*
P_PME*
TP_OVRCNT*
TP_TYPEDET*
TP_USB_PLUS
TP_USB_MINUS
TP_VREF_AGP_MCH
VREF_MCH_AGP
TP_AGPPRO_E1
TP_AGPPRO_E2
TP_AGPPRO_F1
TP_AGPPRO_F2
TP_AGPPRO_C9
TP_AGPPRO_C10
V_3P3_PCIVAUX
+12V
AGP_PRO_PRSNT2 D9
AGP_PRO_PRSNT1 D10
G_IRDY*
G_TRDY*
G_FRAME*
G_STOP*
G_PAR
G_DEVSEL*
G_WBF*
G_RBF*
G_PIPE*
G_REQ*
G_GNT*
CONN
NC=1,2,3,4,5,A3,A11,B14,A22,B22,A24
VCC3=A9,B9,A16,B16,A28,B28,A25,B25
VCC3_3=D1,D2,D3,D4,D5,D6,D7,D8,C1,C3
VCC5=B2,B3
VCC12=E3,E4,E5,E6,E7,E8,E9,E10,E11,E12,E13,E14
CONNECTOR MODEL CHECKED 4/16 VS. AGPPRO VER1.1A SPEC
AGP RETENTION MECHANISM
RM5E1
AGP RETENTION MECH
EMPTY
A16226-001
NOTE: PART PLACED ON AA LEVEL
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
AGP/AGP PRO
REV:
1.0
INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:09:59 2001
SHEET:
14
DRAWING

LAST USED:
R0406C
C0400C

RAMBUS #1, RIMM1

I2C ADDRESS: 000





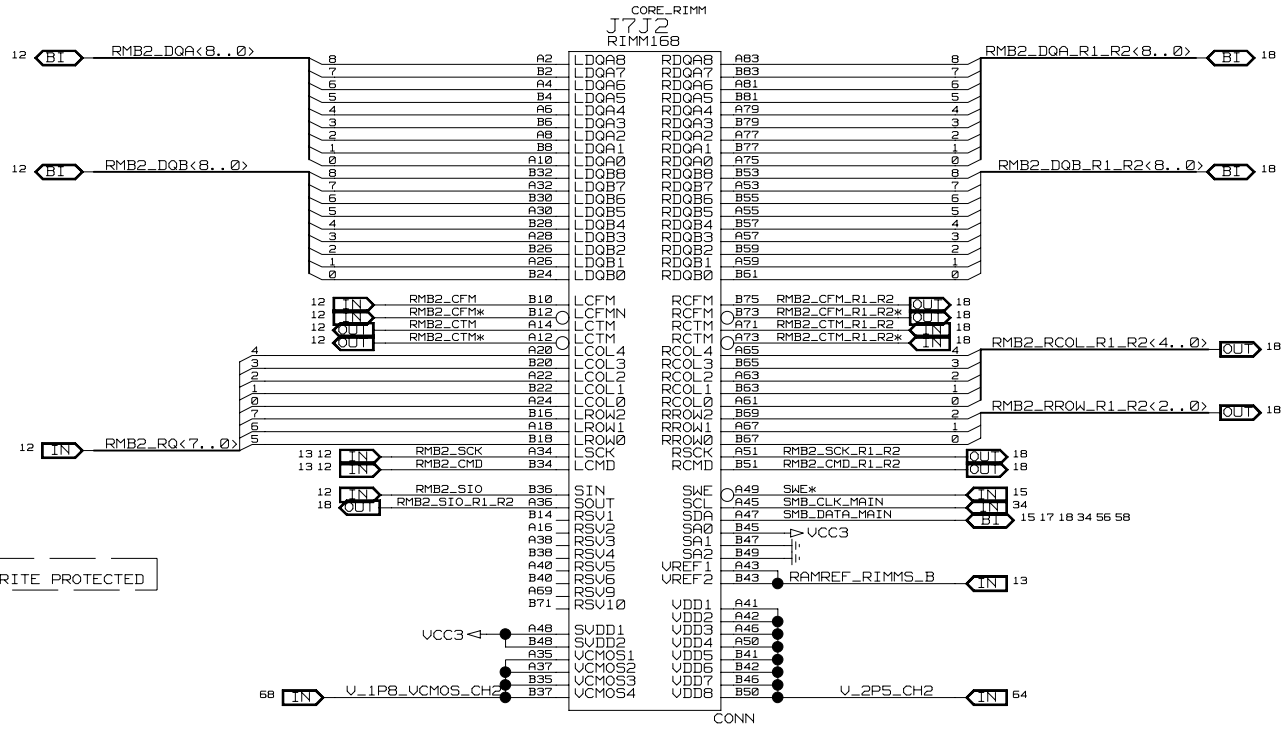
ROOM=CORE_RIMM
BOM=CORE_RIMM

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: RAMBUS		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:36 2001	SHEET: 15

RAMBUS #2, RIMM1

I2C ADDR: 001



DESIGN NOTE:
SWE: 'HIGH' IS WRITE PROTECTED

ROOM=CORE_RIMM
BOM=CORE_RIMM

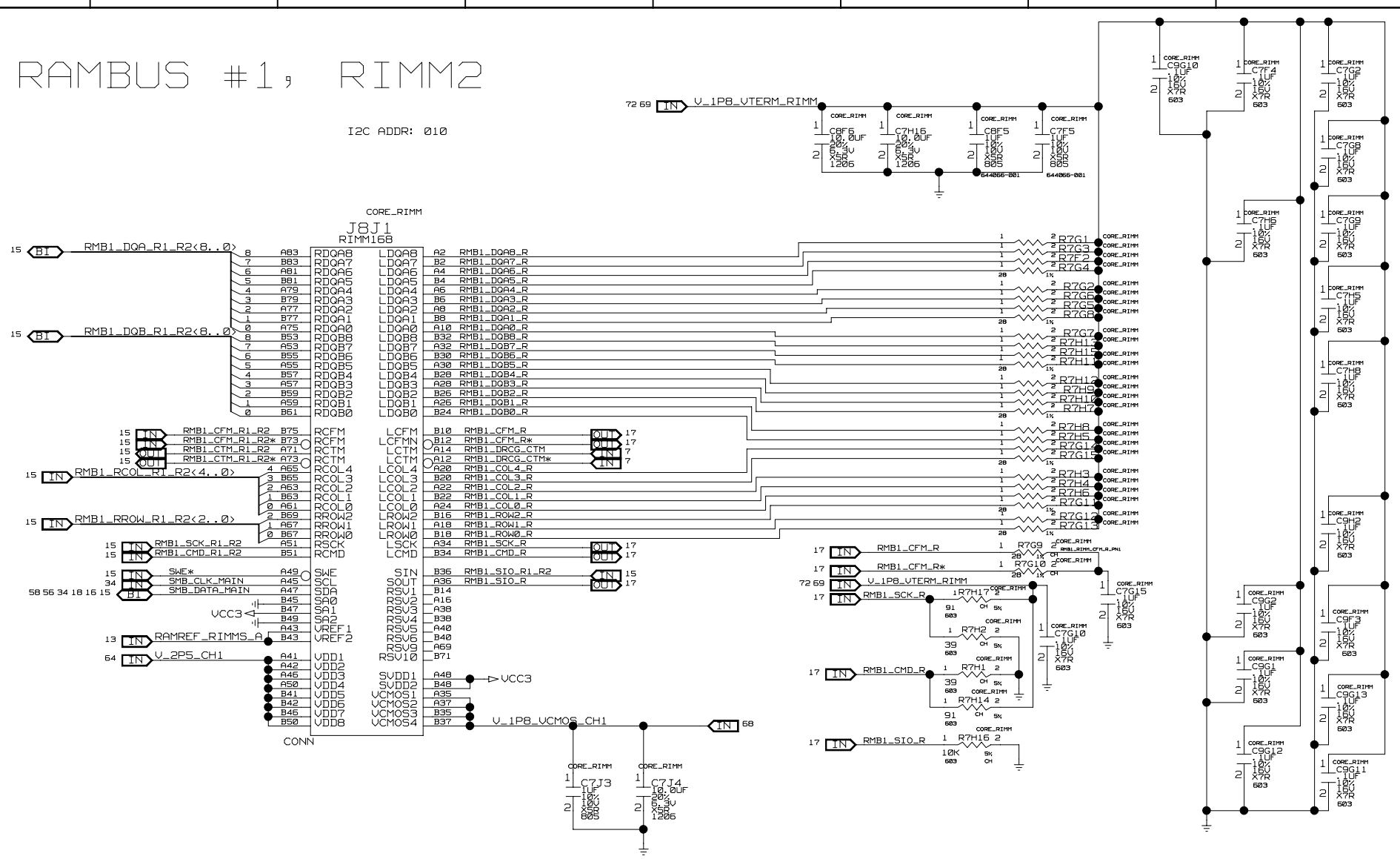
DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: RAMBUS	REV: 1.0
INTEL PLATFORM APPS ENG, 1900 PRAIRIE CITY ROAD, FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:39 2001
	SHEET: 16

LAST USED:
C2013

RAMBUS #1, RIMM2

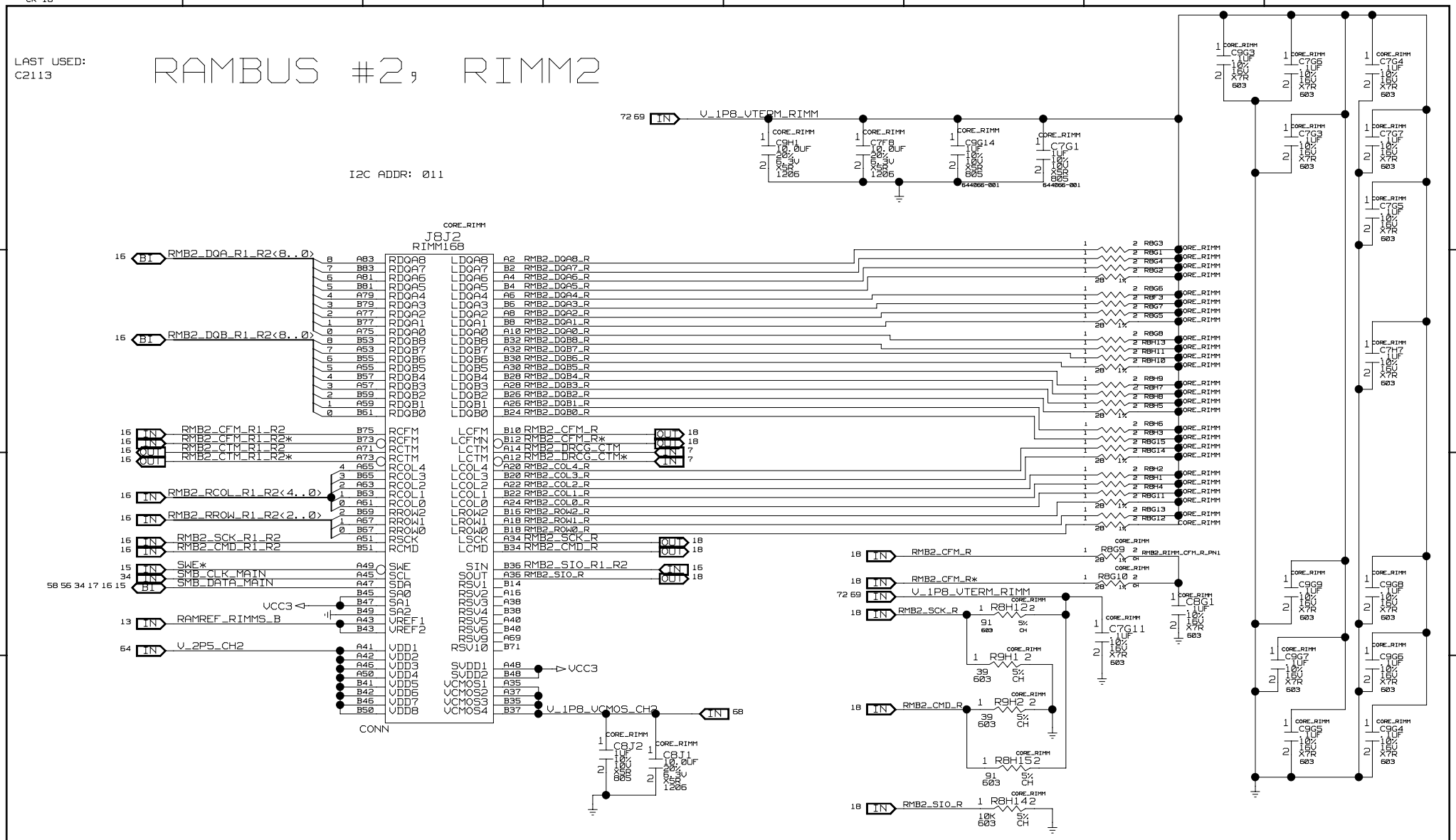
I2C ADDR: 010



ROOM=CORE_RIMM
BOM=CORE
BOM=CORE_DCPL FOR DEFAULT EMPTY

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: RAMBUS CH A TERM	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:40 2001
	SHEET: 17



SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD

PAGE TITLE: RAMBUS CHB TERM

REV: 1.0

INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Jul 10 11:10:42 2001

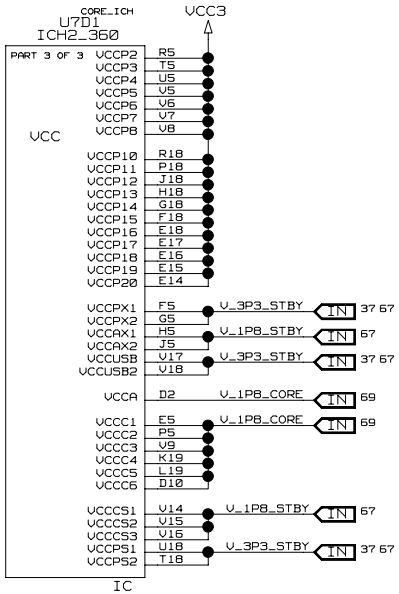
SHEET: 18

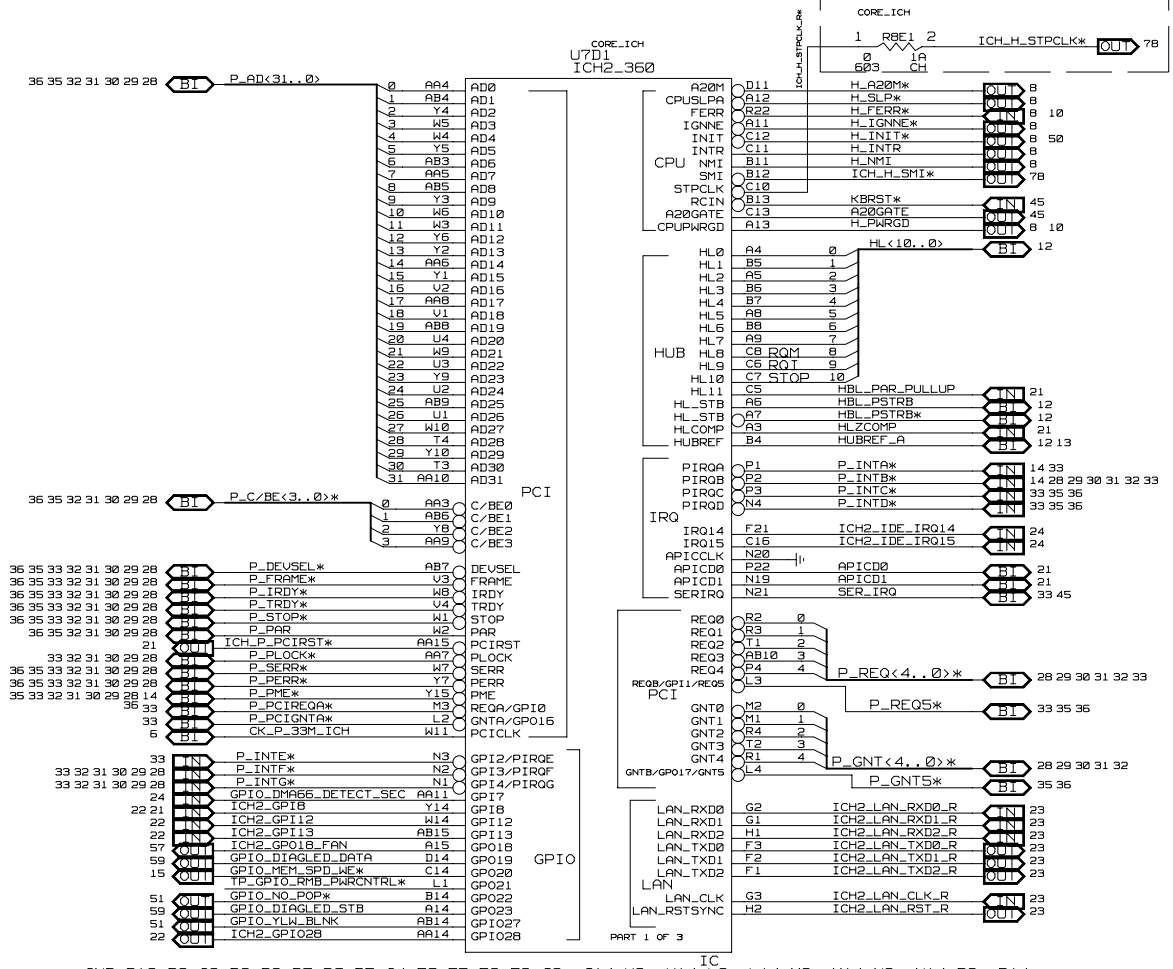
DRAWING

# IDE/HUBLINK
BOM=CORE_ICH
ROOM=CORE_ICH

LAST_USED:
NO RESISTOR
NO CAPACITOR
NO RES PAK
NO TEST POINT

ATTRIBUTES:
CORE_ICH
ROOM=CORE_ICH



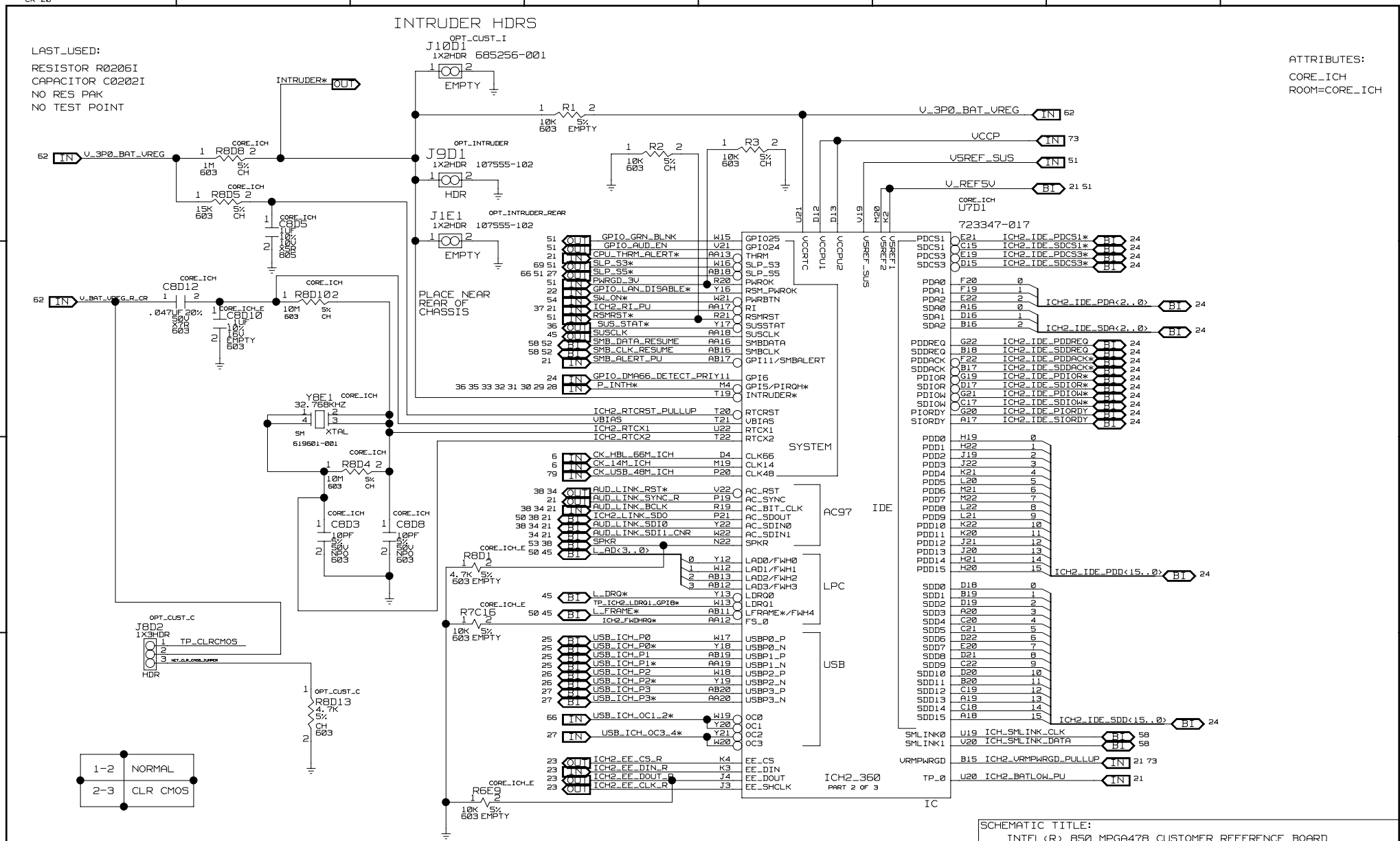


GND=B10, B9, C9, D9, D8, D7, D6, D5, C4, E6, E7, E8, E9, J9..J14, K9..K14, L9..L14, M9..M14, N9..N14, P9..P14
GND=D3, K1, AA1, AA2, AB1, AB2, AA21, AA22, AB21, AB22, A1, A2, A21, A22, B1, B2, B3, B21, B22, C2, C3, A10

[PAGE_TITLE=ICH2_360]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: CPU/AC97/SYS_MGMT		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:44 2001	SHEET: 19



LPC/INTERUPT/USB/PWR_MGMT/SMBUS

[PAGE_TITLE=ICH2_360]

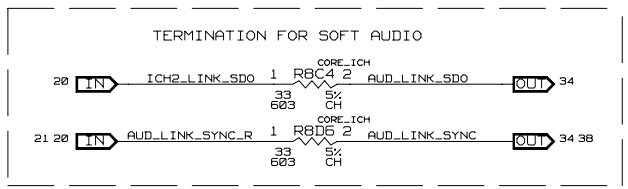
DRAWING

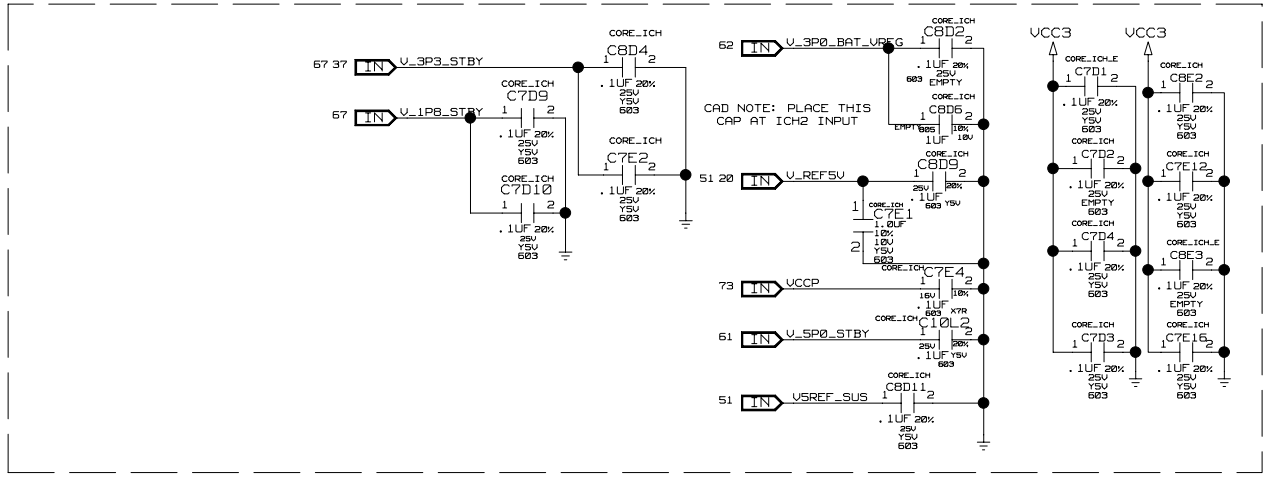
SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI INTERFACE	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:47 2001
	SHEET: 20

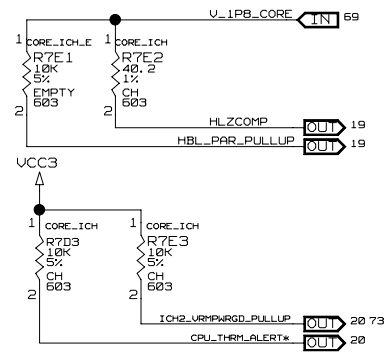
LAST_USED:

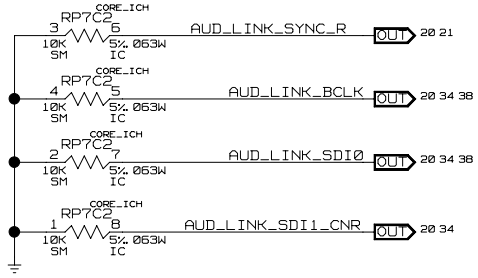
RESISTOR R0309I
CAPACITOR C0307I
NO RES PAK
NO TEST POINT

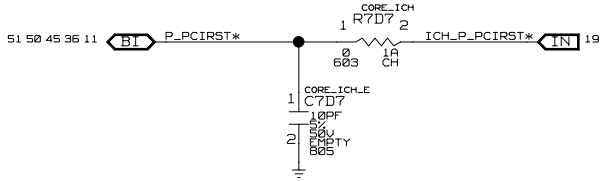
ATTRIBUTES:
CORE_ICH
ROOM=CORE_ICH

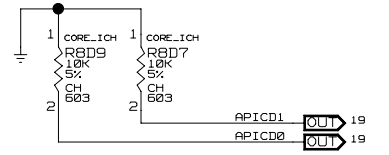


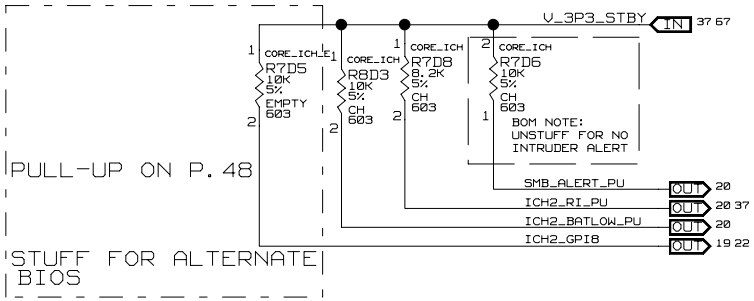












[PAGE_TITLE=ICH2_360]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: ICH2 PULLUPS & DECOUPLING		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:48 2001	SHEET: 21

ICH

ICH_GPO19
EA = DIAGLED_DATA
WTVV = TP

* GPIO27
EA = YLW_BLNK
WTVV = YLW_BLNK

* GPO20
EA = MEM_SPD_WE*
WTVV = GPIO_RMB_SPD_WE*

* GPO21
EA = FLUSH_CACHE*
WTVV = TP

* GPI8
EA = PULL-UP OR DOWN OPTION
WTVV = PULL-UP

* GPO18
EA = GPIO_SMI*
WTVV = TP

ICH_GPO22
EA = MUTE_AUD*
WTVV = TP

ICH_GPI13
EA = CDC_DWN_ENAB*
WTVV = GPIO_PME_SIO_OUT*

ICH_GPI7
EA = GPIO_DMA66_DETECT_SEC
WTVV = PULL-UP

ICH_GPI6
EA = DMA66_DETECT_PRI
WTVV = PULL-UP

ICH_GPIO24
EA = AUD_EN
WTVV = LAN_DISABLE

ICH_GPIO25
EA = GRN_BLNK
WTVV = TP

ICH_GPO23
EA = DIAGLED_STB
WTVV = TP

ICH_GPIO28
EA = LAN_DISABLE
WTVV = GRN_BLNK

ICH_GPI12
EA = IO_PME*
WTVV = GPIO_SMI_OUT*

FWH

* GPI4
EA = CONFIG JMPR
WTVV = CONFIG JMPR

* GPI3
EA = MTM
WTVV = MTM

* GPI2
EA = PULL-UP/DOWN
WTVV = PULL-DOWN

FWH_GPI1
EA = PULL-UP/DOWN
WTVV = DMA66_DETECT_SEC

FWH_GPI0
EA = PULL-UP/DOWN
WTVV = DMA66_DETECT_PRI

SIO

* GP22
EA = TP
WTVV = RMB_FREQ0

* GP60
EA = TP
WTVV = RMB_PWRCNTRL*

* GP61
EA = TP
WTVV = RMB_FREQ1

SIO_GP20
EA = TP
WTVV = AUD_EN

SIO_GP21
EA = TP
WTVV = NO_POP*

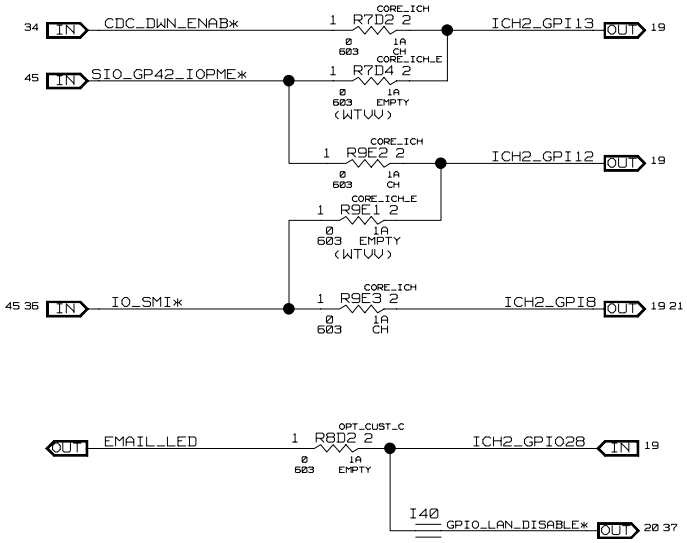
SIO_GP42/IO_PME*
EA = IO_PME*
WTVV = GPIO_PME_SIO_OUT*

SIO_GP27/SMI
EA = H_SMI*
WTVV = GPIO_SMI_OUT*

SIO_GP43
EA = TP
WTVV = TP/DIAG_DATA

SIO_GP26
EA = GAME_MIDI_OUT
WTVV = CDC_DOWN

SIO_GP24
EA = TP
WTVV = SIO_SYS_OPT/DIAG_STB



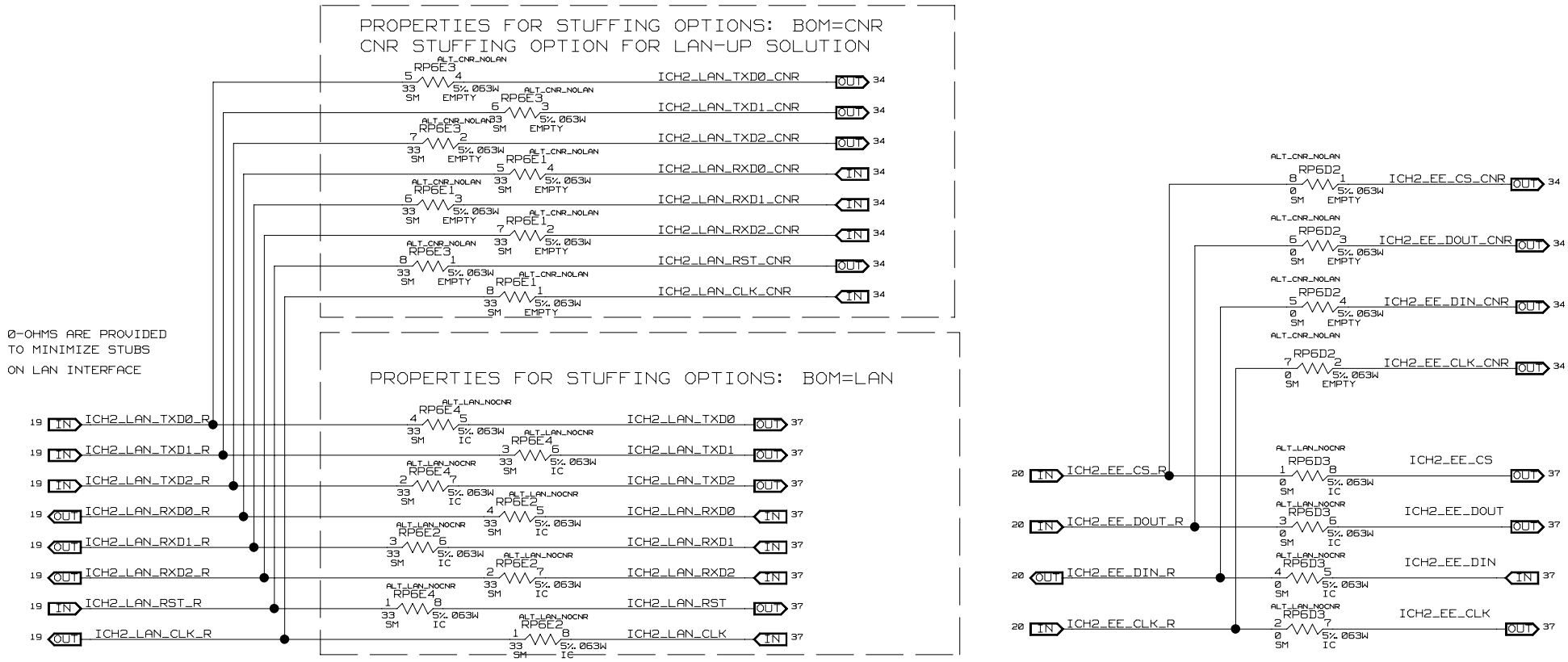
[PAGE_TITLE=ICH2_360]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: GPIO REMAPPING		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:49 2001	SHEET: 22

LAN LINK STUFFING OPTION PAGE

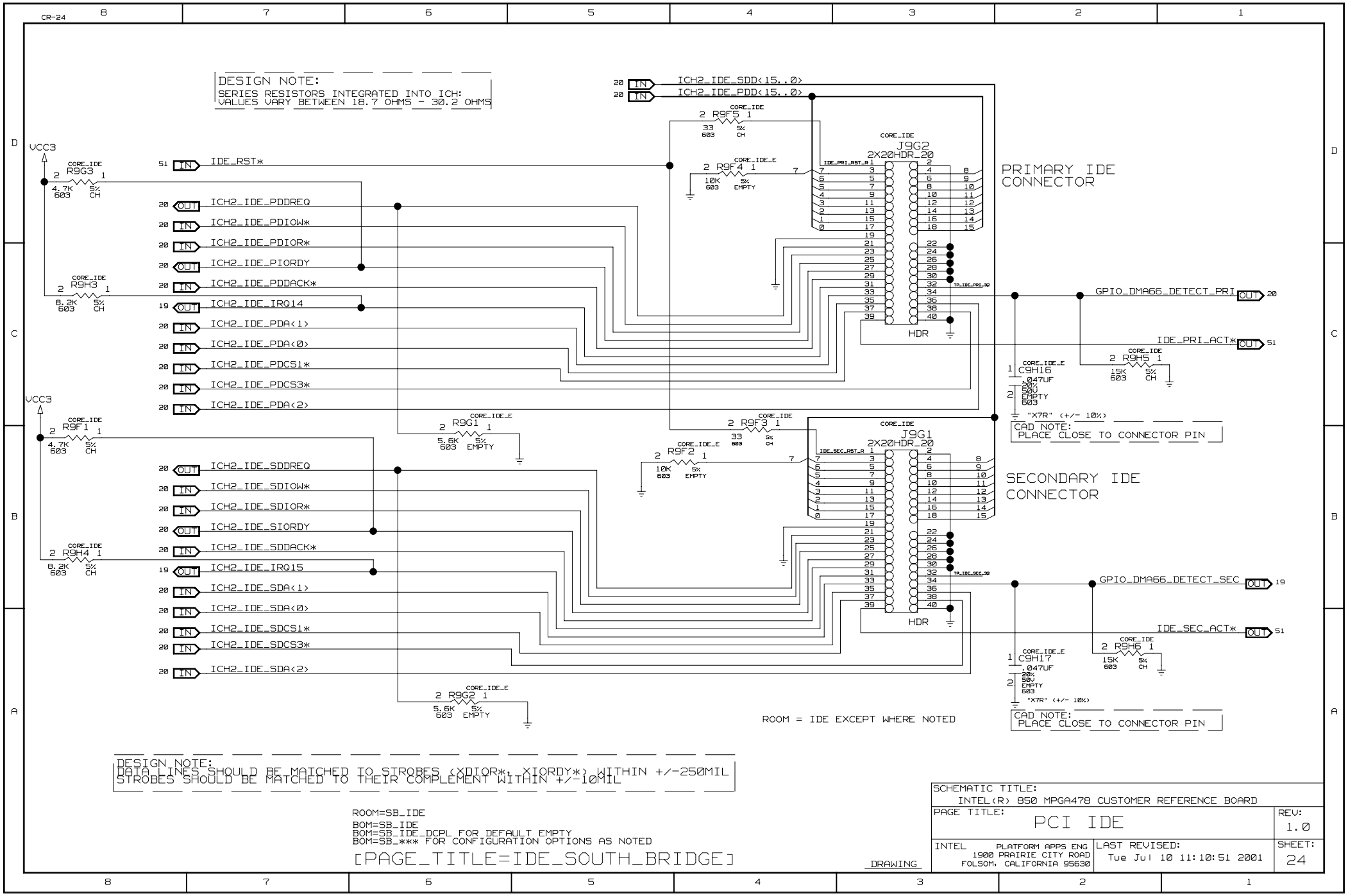
STUFF ONE OR THE OTHER NOT BOTH

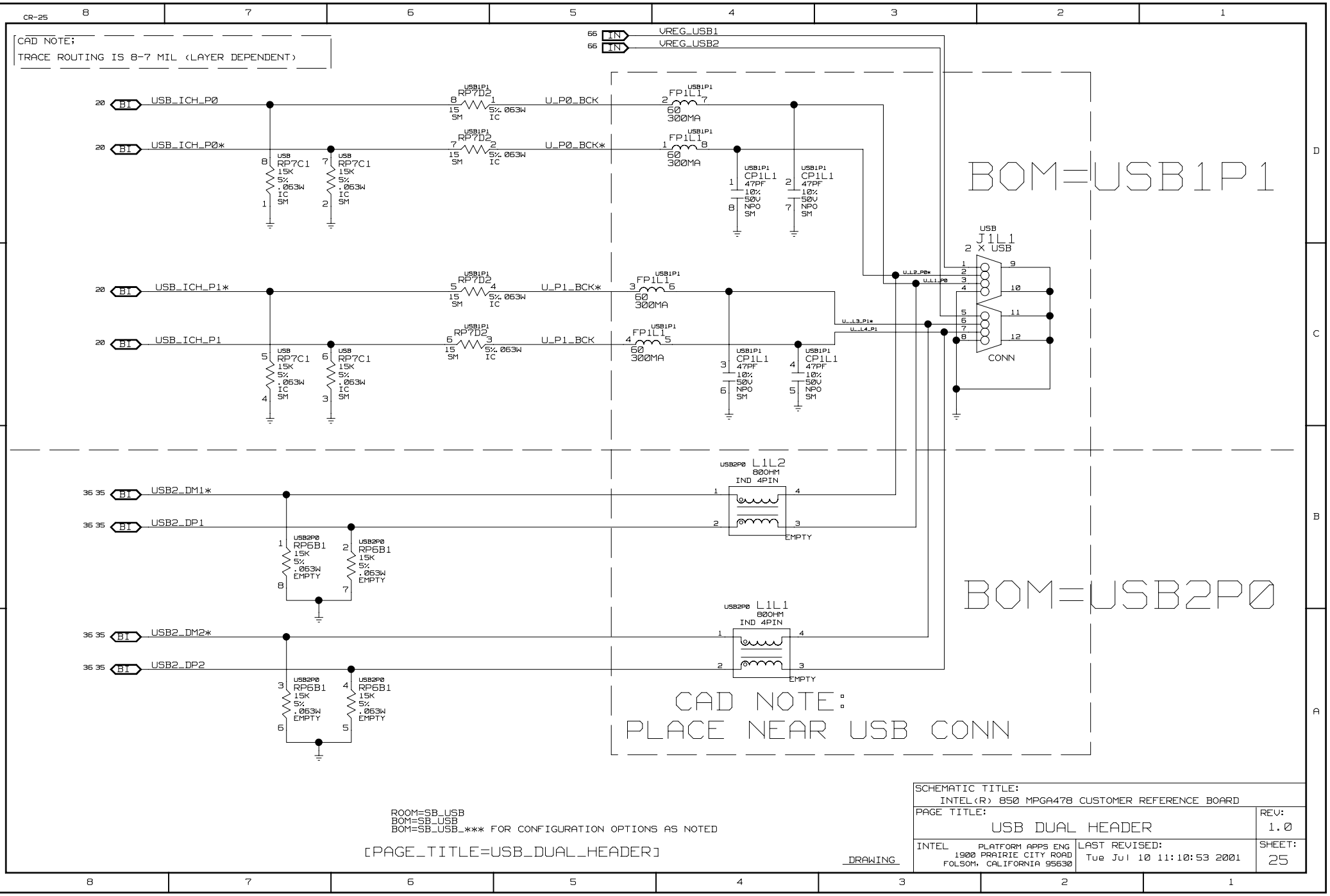


[PAGE_TITLE=ICH2_360]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: LAN LINK STUFFING OPTION		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:50 2001	SHEET: 23


CR-24
DESIGN NOTE:
SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS
ICH2_IDE_SDD<15..0>
ICH2_IDE_PDD<15..0>
R9F5 33 603 5% CH
R9F4 10K 603 5% EMPTY
J9G2 2X20HDR_20
PRIMARY IDE CONNECTOR
HDR
GPIO_DMA66_DETECT_PRI
IDE_PRI_ACT*
C9H16 .047UF 20% 50V EMPTY 603 "X7R" (+/- 10%)
R9H5 15K 603 5% CH
CAD NOTE: PLACE CLOSE TO CONNECTOR PIN
VCC3
R9G3 4.7K 603 5% CH
R9H3 8.2K 603 5% CH
IDE_RST*
ICH2_IDE_PDDREQ
ICH2_IDE_PDIOW*
ICH2_IDE_PDIOR*
ICH2_IDE_PIORDY
ICH2_IDE_PDDACK*
ICH2_IDE_IRQ14
ICH2_IDE_PDA<1>
ICH2_IDE_PDA<0>
ICH2_IDE_PDCS1*
ICH2_IDE_PDCS3*
ICH2_IDE_PDA<2>
R9F1 4.7K 603 5% CH
R9H4 8.2K 603 5% CH
R9G1 5.6K 603 5% EMPTY
R9F3 33 603 5% CH
R9F2 10K 603 5% EMPTY
J9G1 2X20HDR_20
SECONDARY IDE CONNECTOR
GPIO_DMA66_DETECT_SEC
IDE_SEC_ACT*
C9H17 .047UF 20% 50V EMPTY 603 "X7R" (+/- 10%)
R9H6 15K 603 5% CH
ICH2_IDE_SDDREQ
ICH2_IDE_SDIOW*
ICH2_IDE_SDIOR*
ICH2_IDE_SIORDY
ICH2_IDE_SDDACK*
ICH2_IDE_IRQ15
ICH2_IDE_SDA<1>
ICH2_IDE_SDA<0>
ICH2_IDE_SDCS1*
ICH2_IDE_SDCS3*
ICH2_IDE_SDA<2>
R9G2 5.6K 603 5% EMPTY
ROOM = IDE EXCEPT WHERE NOTED
DESIGN NOTE:
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL
ROOM=SB_IDE
BOM=SB_IDE
BOM=SB_IDE_DCPL FOR DEFAULT EMPTY
BOM=SB_*** FOR CONFIGURATION OPTIONS AS NOTED
[PAGE_TITLE=IDE_SOUTH_BRIDGE]
DRAWING
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
PCI IDE
REV: 1.0
INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:10:51 2001
SHEET: 24



ROOM=SB_USB
BOM=SB_USB
BOM=SB_USB_*** FOR CONFIGURATION OPTIONS AS NOTED

[PAGE_TITLE=USB_DUAL_HEADER]

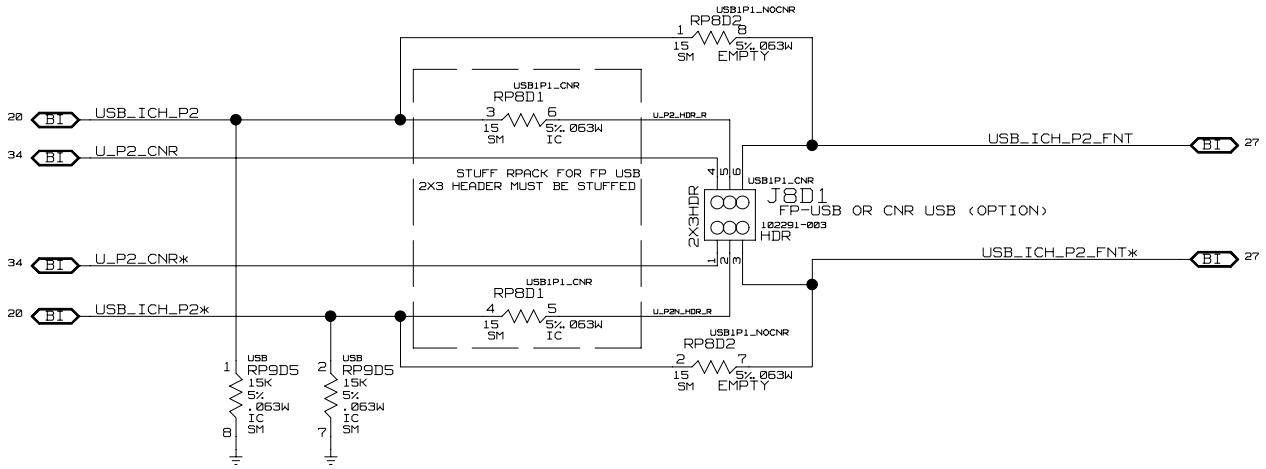
DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: USB DUAL HEADER	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:53 2001
	SHEET: 25

CAD NOTE;
TRACE ROUTING IS 8 MIL, 7 MIL SPACING

JUMPER POSITION	FEATURE
1-2, 4-5	CNR USB
5-6, 2-3	* FRONT PANEL USB
	NO OTHER OPTIONS VALID

* DEFAULT STUFFING

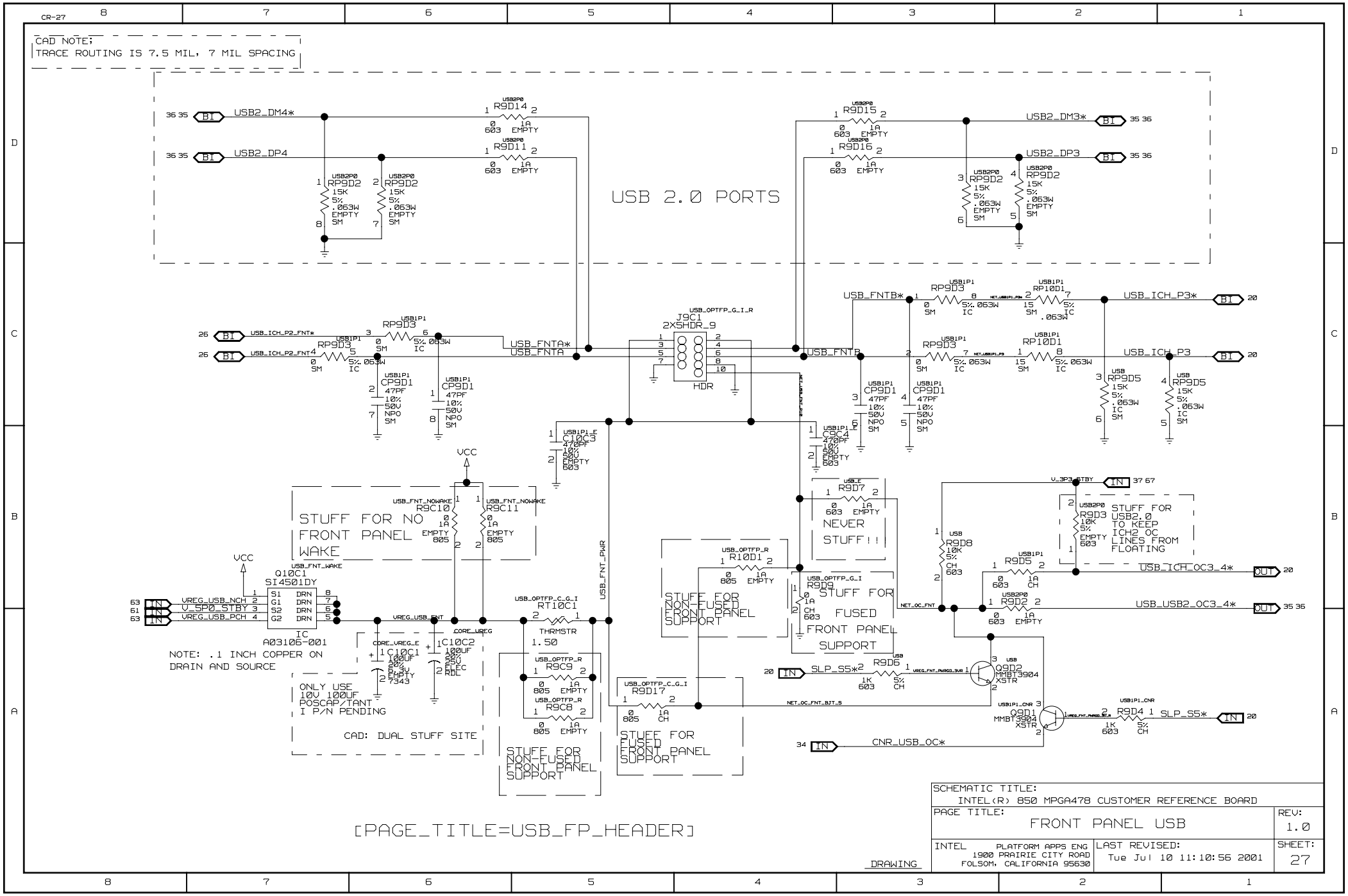


ROOM=SB_USB
BOM=SB_USB
BOM=SB_USB_*** FOR CONFIGURATION OPTIONS AS NOTED

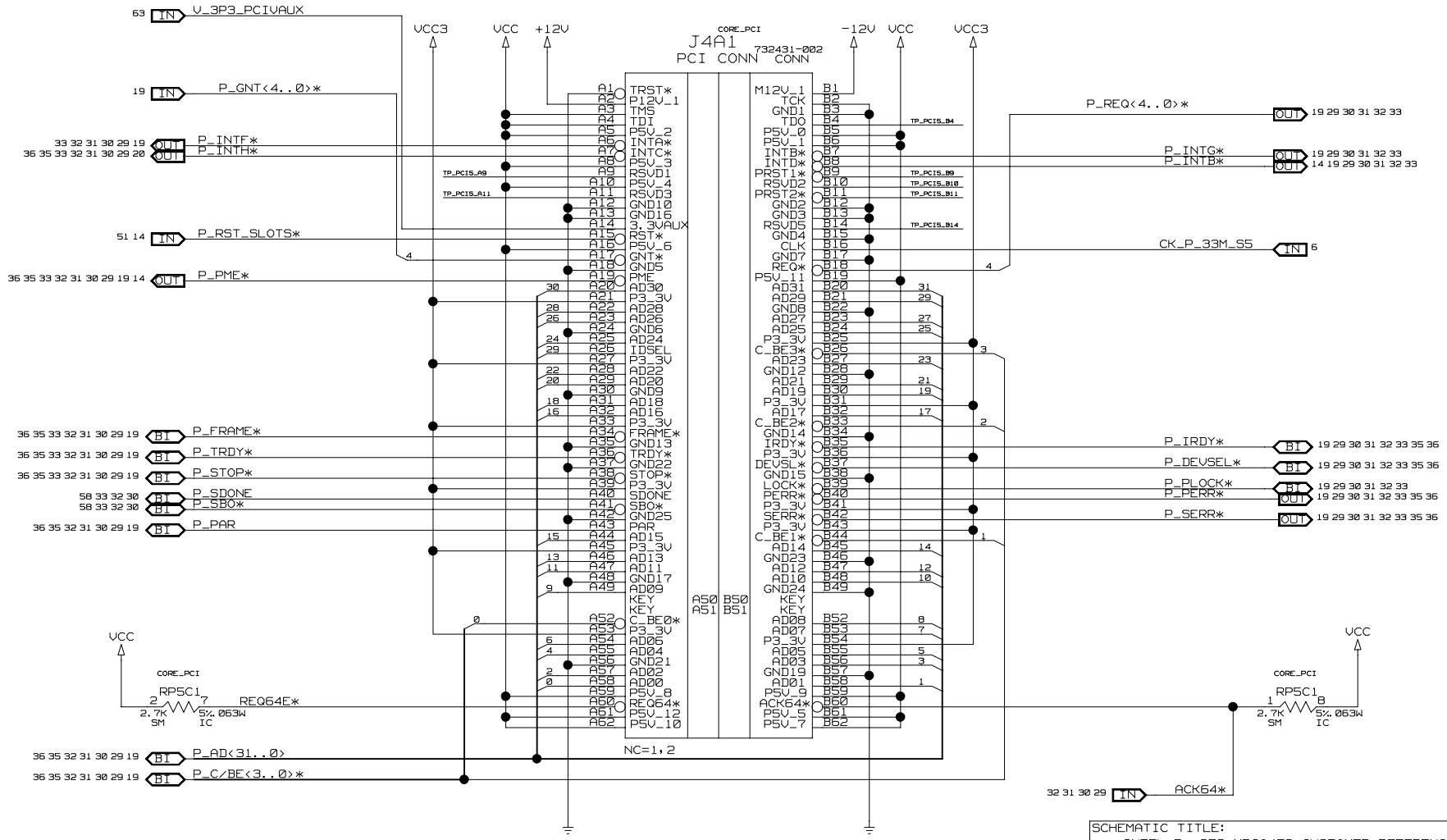
[PAGE_TITLE=USB_FP_HEADER]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: USB1.1 FRONT/CNR JUMPER BLOCK	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:55 2001
	SHEET: 26


CR-27
CAD NOTE;
TRACE ROUTING IS 7.5 MIL, 7 MIL SPACING
USB 2.0 PORTS
USB2_DM4*
USB2_DP4
USB2_DM3*
USB2_DP3
USB_ICH_P2_FNT*
USB_ICH_P2_FNT
USB_FNTA*
USB_FNTA
USB_FNTB*
USB_FNTB
USB_ICH_P3*
USB_ICH_P3
J9C1
2X5HDR_9
HDR
STUFF FOR NO FRONT PANEL WAKE
VCC
Q10C1
SI4501DY
IC
A03106-001
NOTE: .1 INCH COPPER ON DRAIN AND SOURCE
ONLY USE 10V 100UF POSCAP/TANT I P/N PENDING
CAD: DUAL STUFF SITE
STUFF FOR NON-FUSED FRONT PANEL SUPPORT
STUFF FOR FUSED FRONT PANEL SUPPORT
NEVER STUFF!!
STUFF FOR USB2.0 TO KEEP ICH2 OC LINES FROM FLOATING
USB_ICH_OC3_4*
USB_USB2_OC3_4*
SLP_S5*
CNR_USB_OC*
[PAGE_TITLE=USB_FP_HEADER]
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
FRONT PANEL USB
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:10:56 2001
SHEET:
27
DRAWING

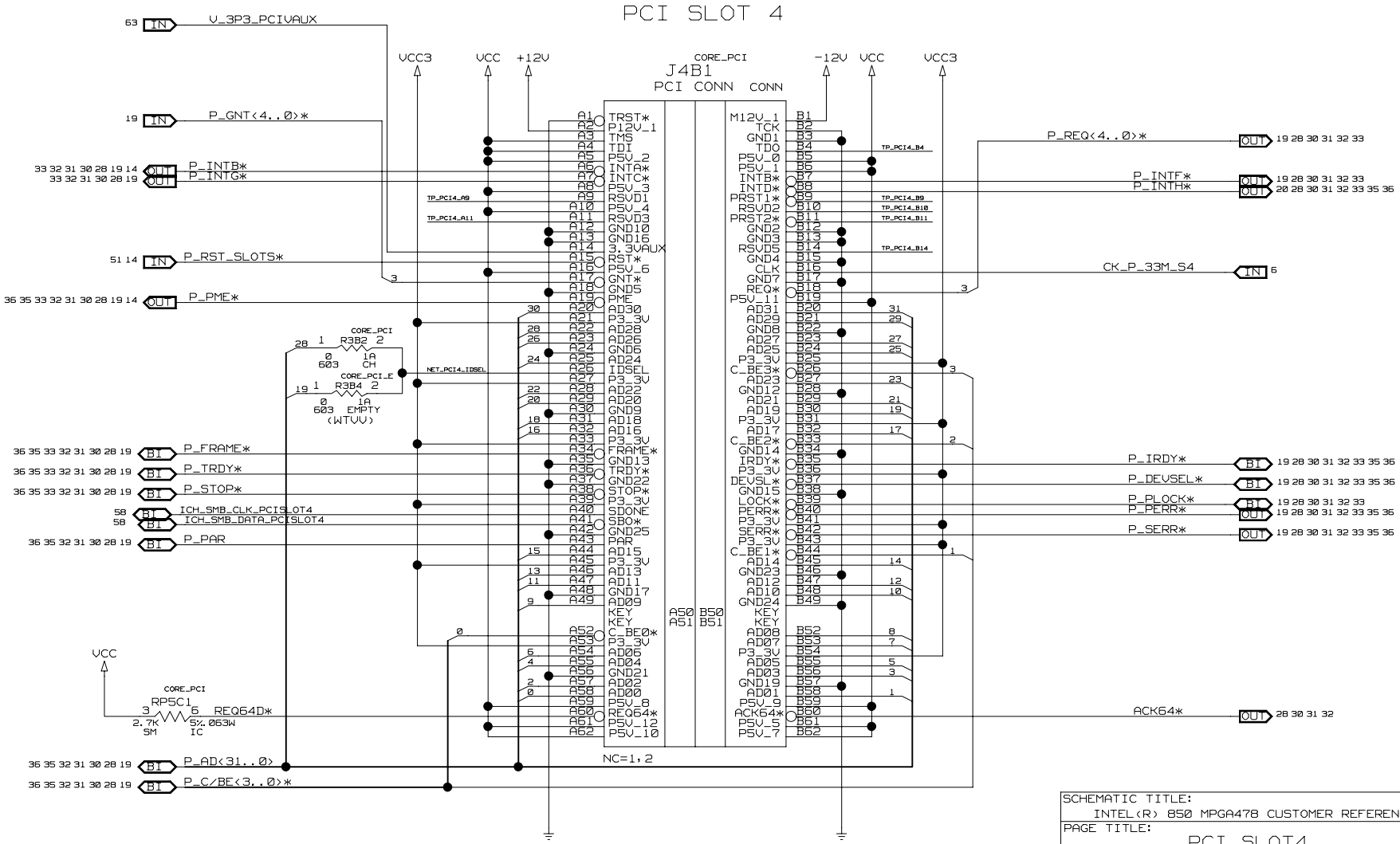
(SHARED WITH CNR)
PCI SLOT 5



[PAGE_TITLE=PCI_SLOT5]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT 5 SHARED WITH CNR		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:58 2001	SHEET: 28



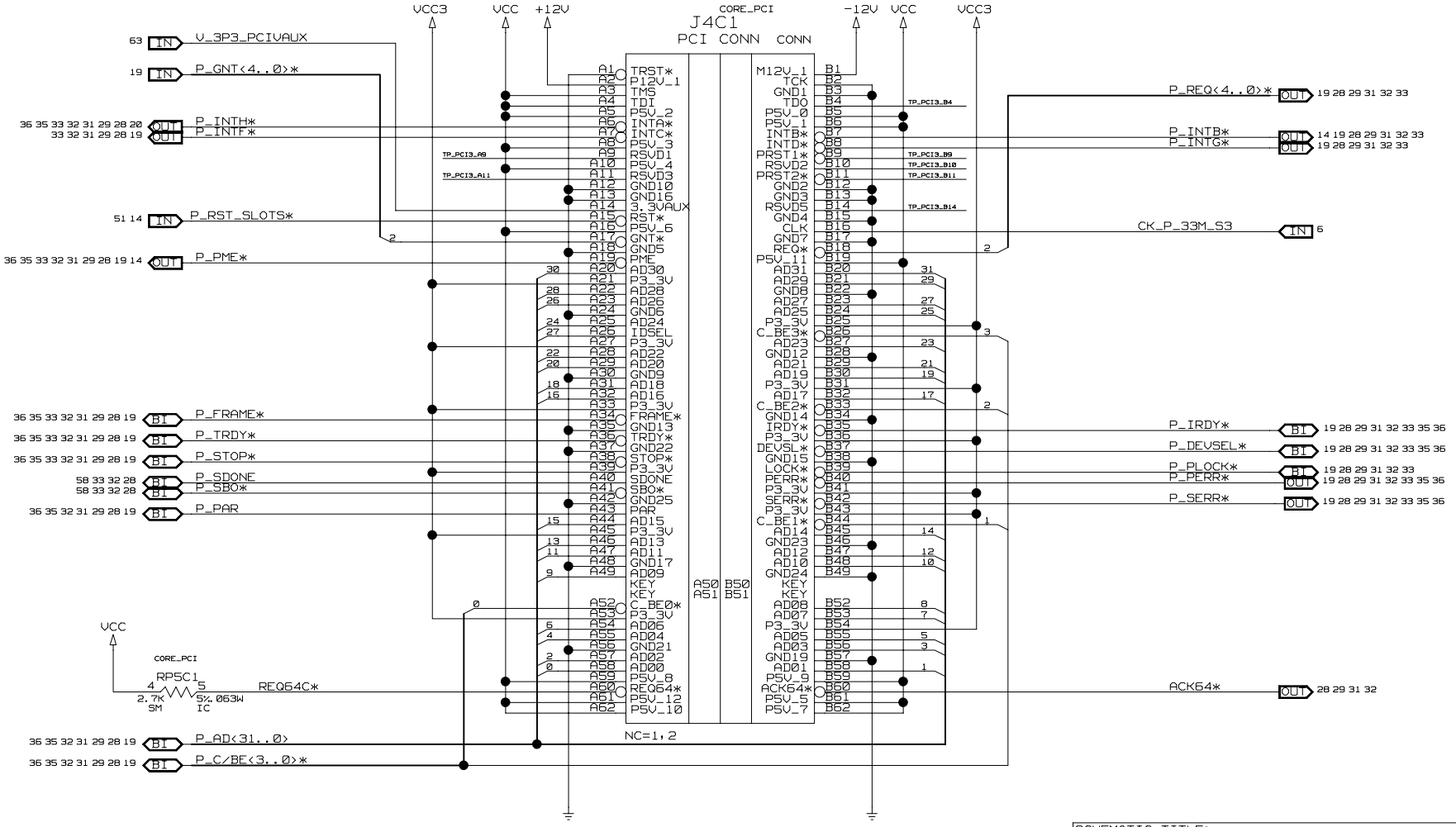
PCI SLOT 4

[PAGE_TITLE=PCI_SLOT4]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: PCI SLOT4	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:59 2001
	SHEET: 29

PCI SLOT 3



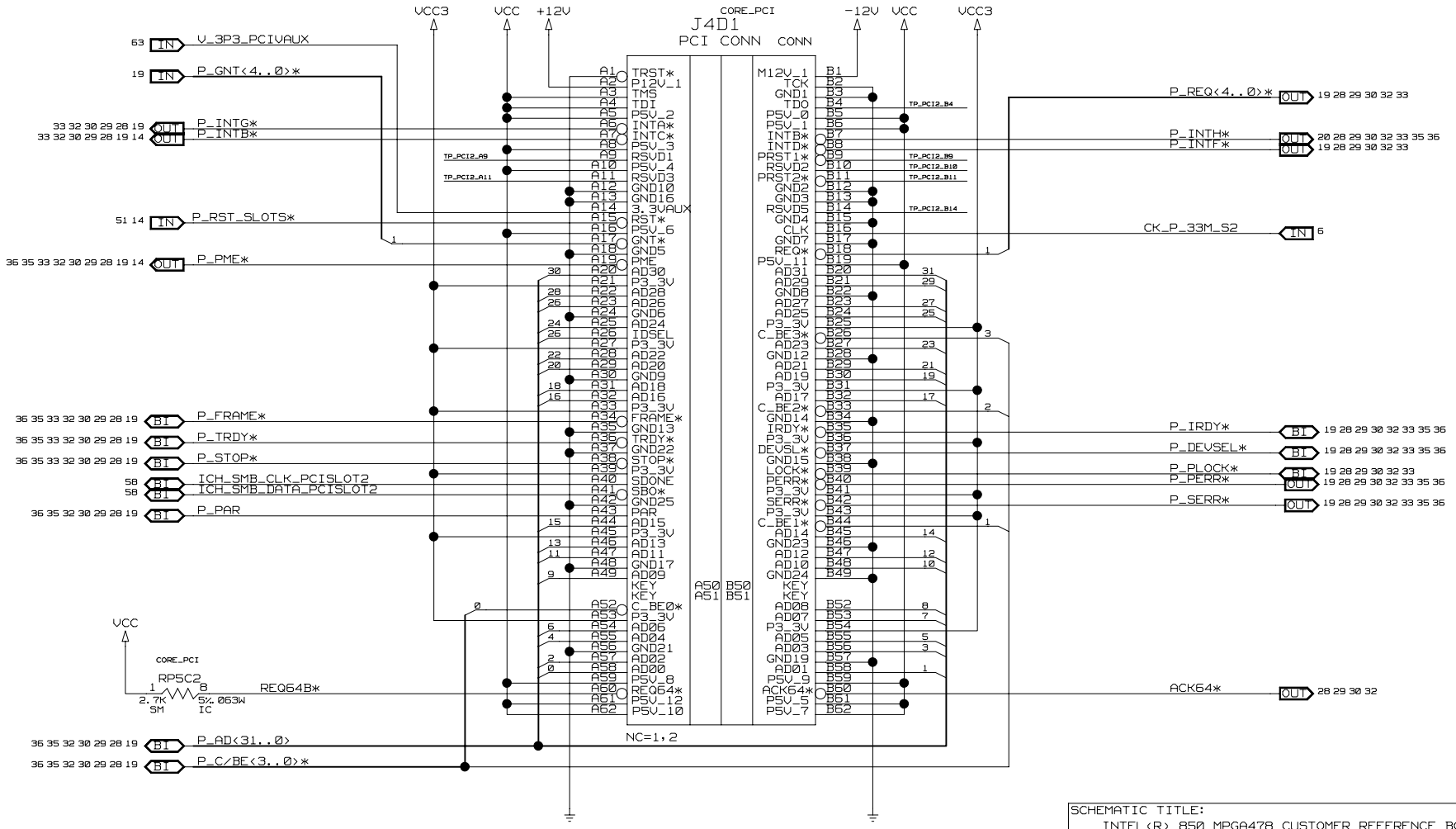
PCI SLOT 3

[PAGE_TITLE=PCI_SLOT3]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT 3		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:00 2001	SHEET: 30

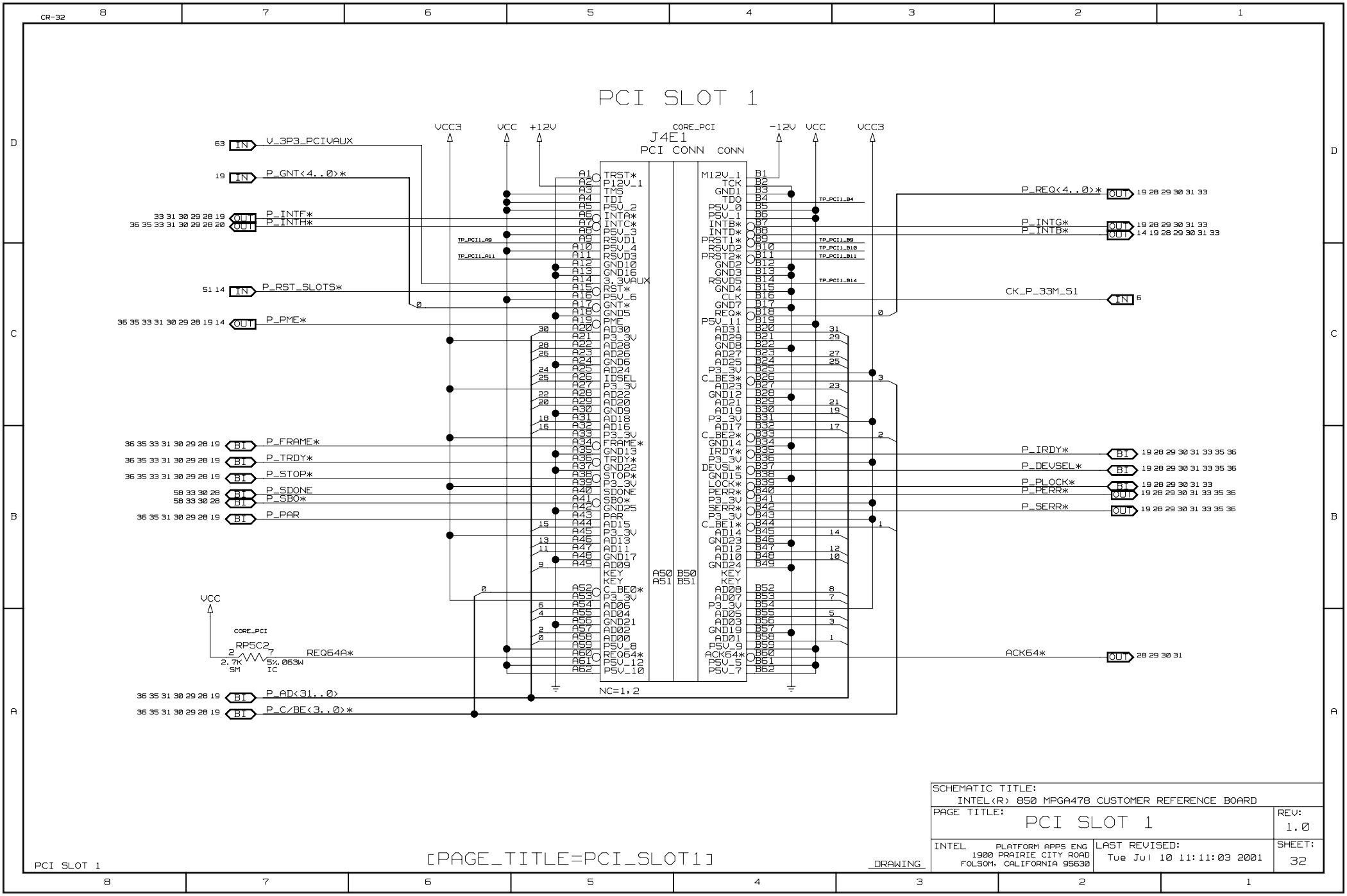
PCI SLOT 2

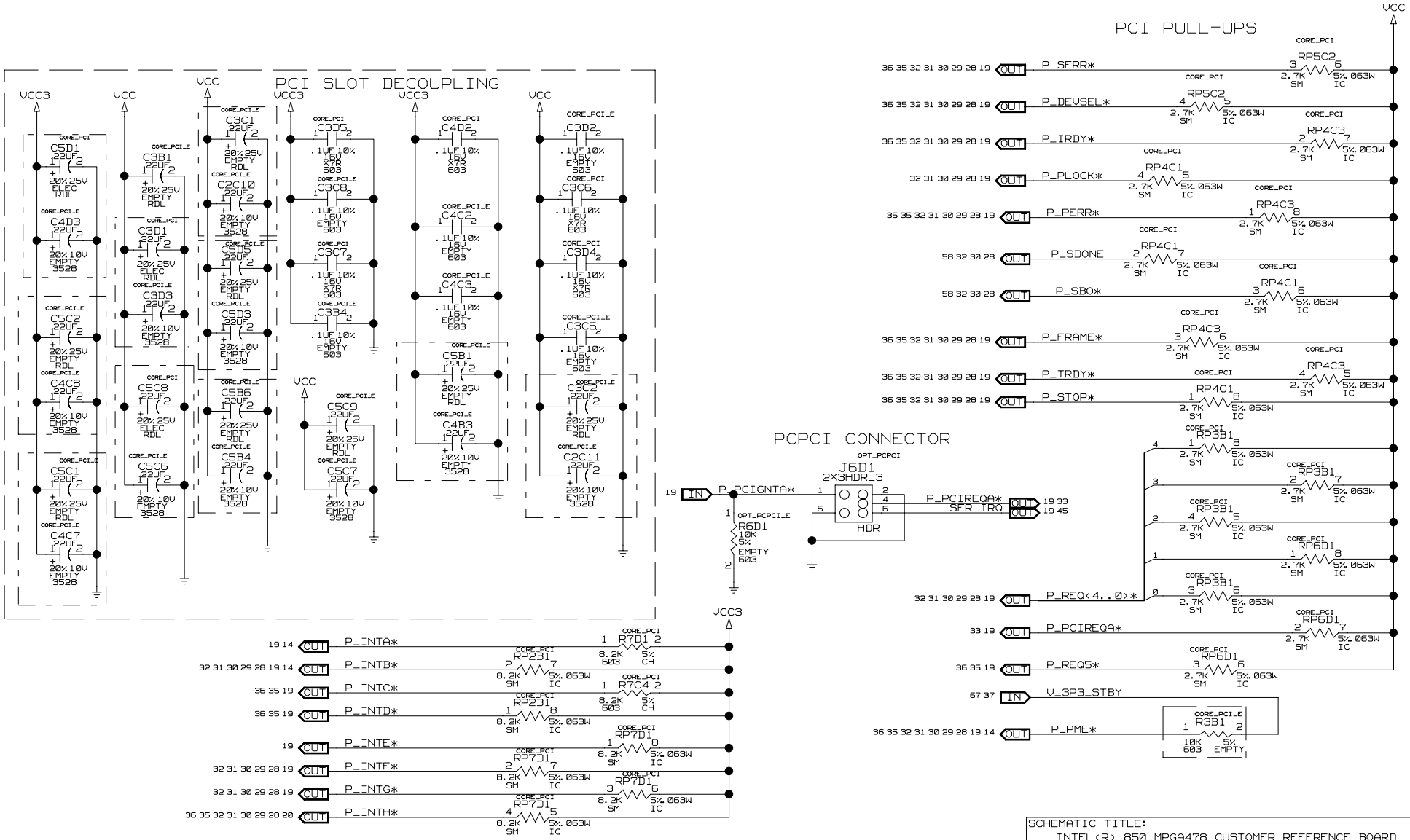


[PAGE_TITLE=PCI_SLOT2]

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: PCI SLOT 2		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:02 2001	SHEET: 31

DRAWING


PCI SLOT 1
CR-32
J4E1
PCI CONN CONN
CORE_PCI
VCC3
VCC
+12V
-12V
V_3P3_PCIVAUX
P_GNT<4..0>*
P_INTF*
P_INTH*
P_RST_SLOTS*
P_PME*
P_FRAME*
P_TRDY*
P_STOP*
P_SDONE
P_SBO*
P_PAR
REQ64A*
P_AD<31..0>
P_C/BE<3..0>*
P_REQ<4..0>*
P_INTG*
P_INTB*
CK_P_33M_S1
P_IRDY*
P_DEVSEL*
P_PLOCK*
P_PERR*
P_SERR*
ACK64*
RP5C2
2.7K SM
5%.063W IC
NC=1,2
[PAGE_TITLE=PCI_SLOT1]
DRAWING
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
PCI SLOT 1
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:03 2001
SHEET:
32



SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD

PAGE TITLE: ICH PCI TERMINATION

REV: 1.0

INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

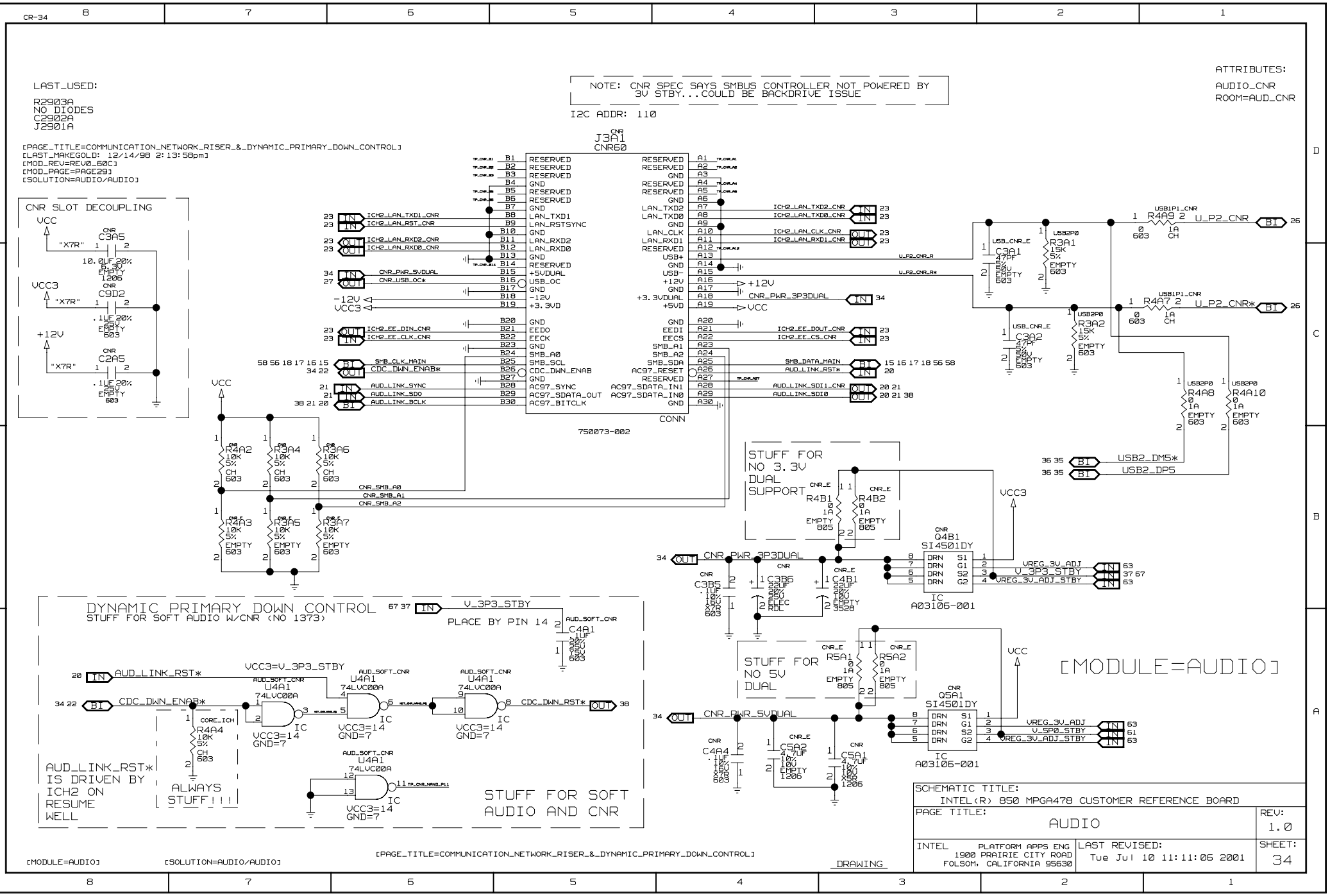
LAST REVISED: Tue Jul 10 11:11:04 2001

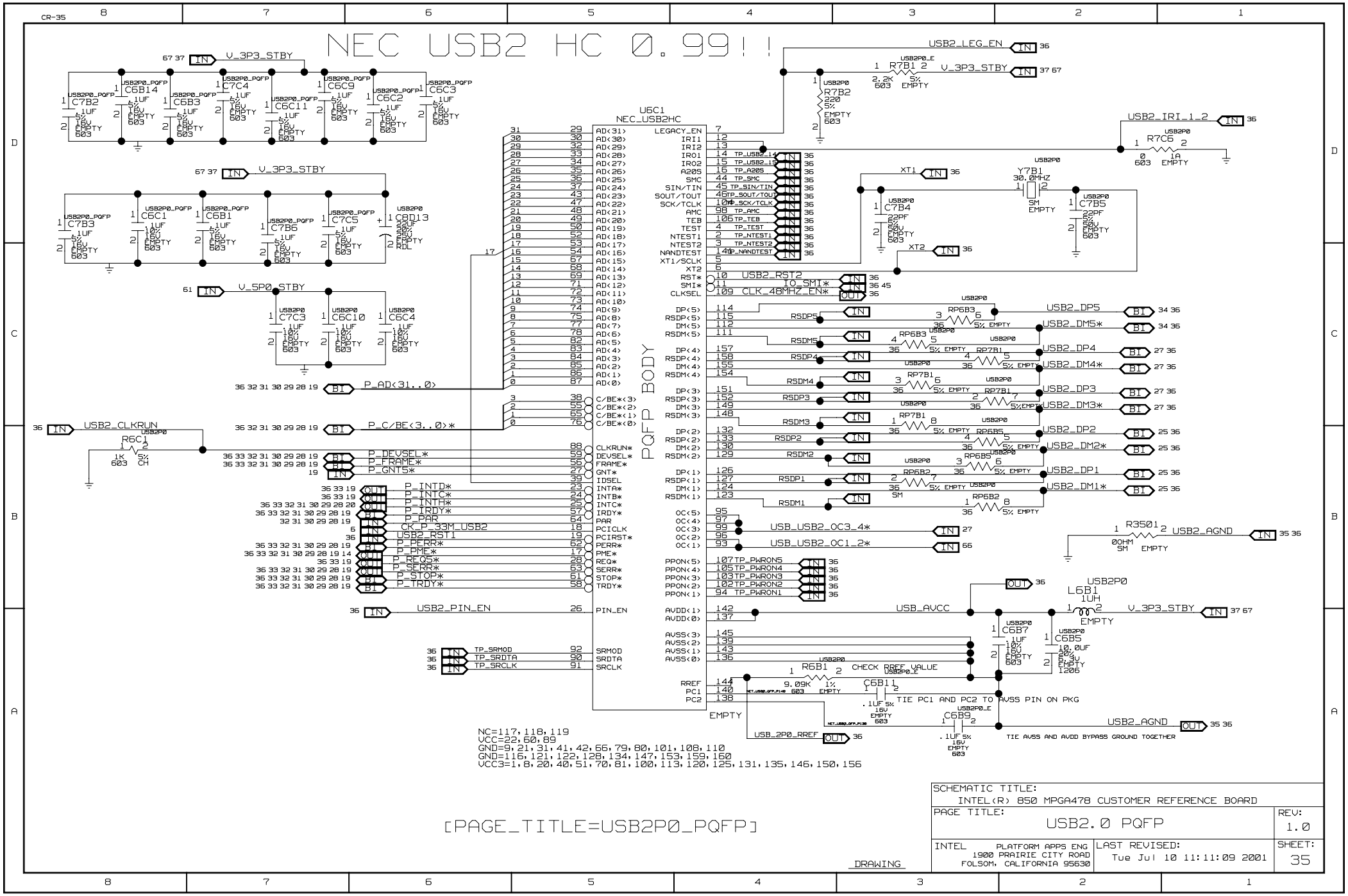
SHEET: 33

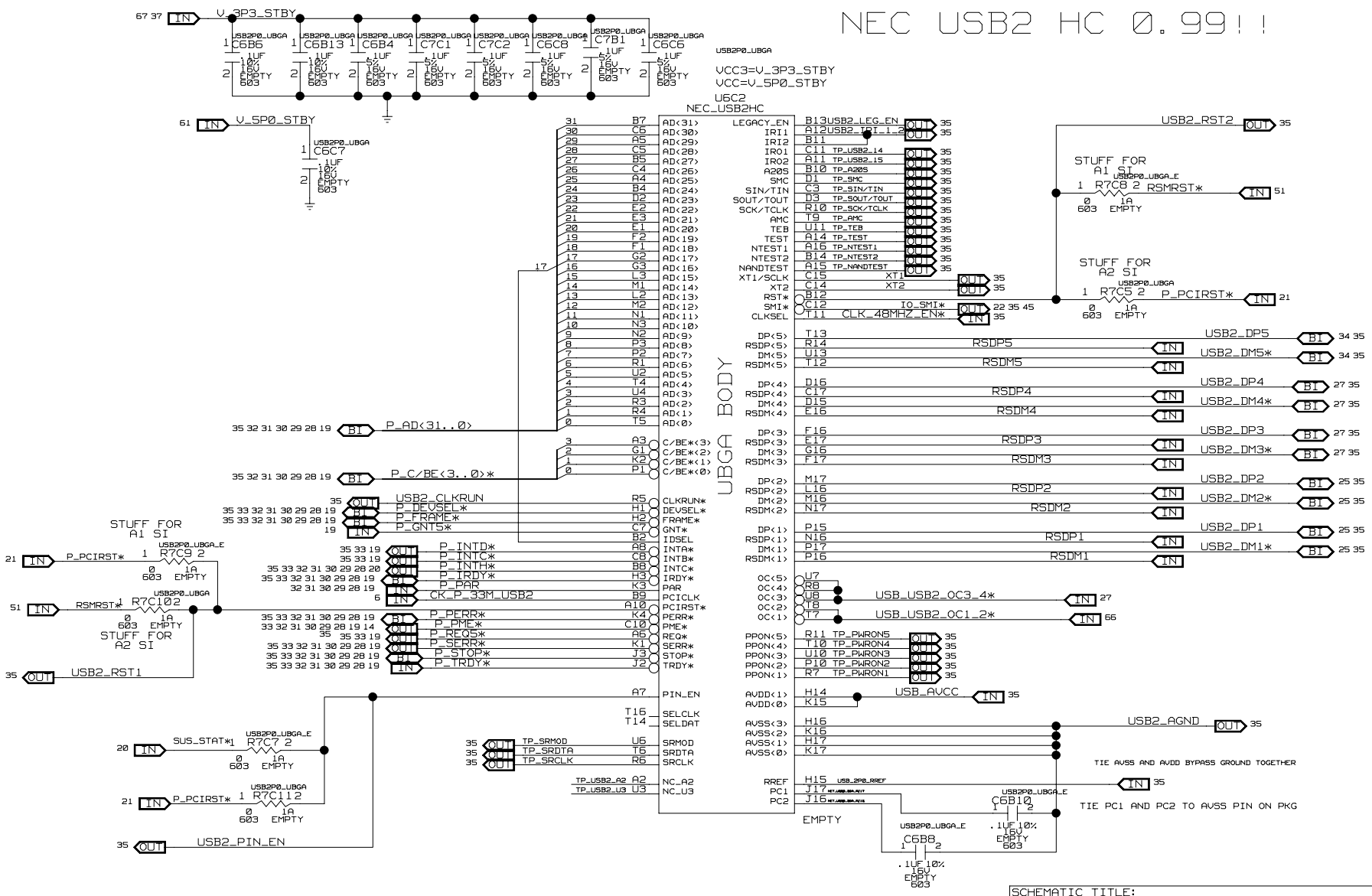
[MODULE=ICH]

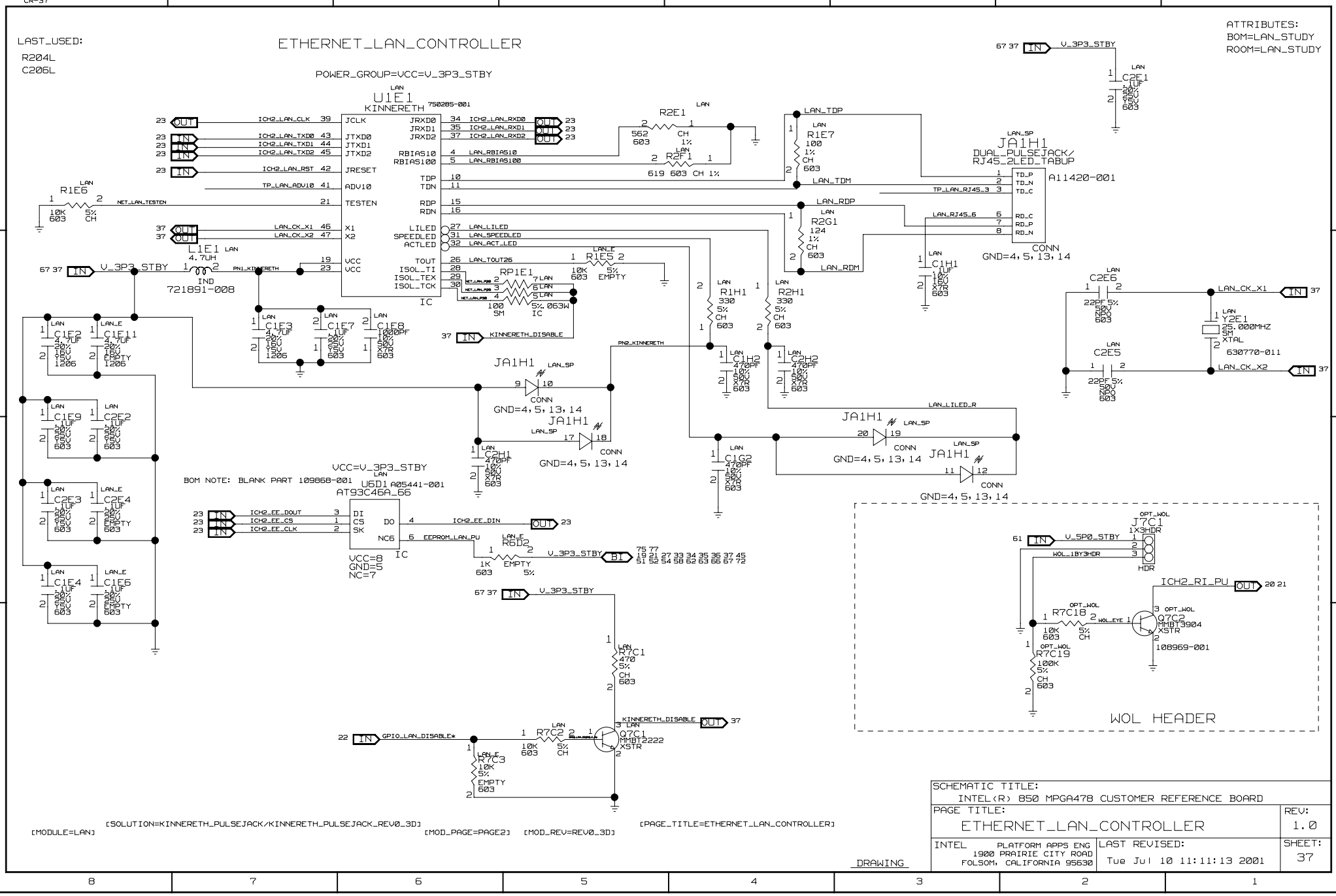
[PAGE_TITLE=ICH_PCI_TERMINATION]

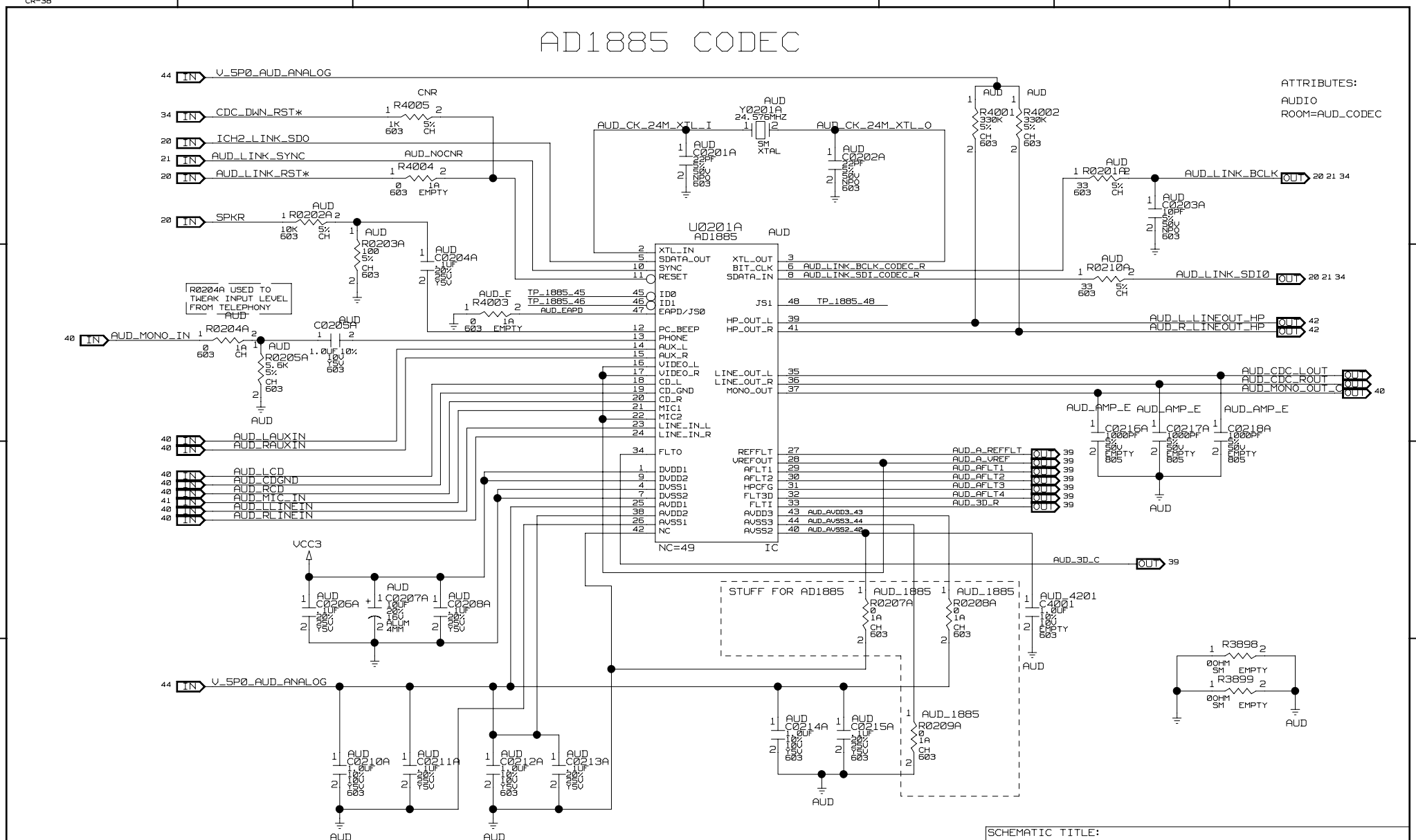
DRAWING


CR-34
LAST_USED:
R2903A
NO DIODES
C2902A
J2901A
[PAGE_TITLE=COMMUNICATION_NETWORK_RISER_&_DYNAMIC_PRIMARY_DOWN_CONTROL]
[LAST_MAKEGOLD: 12/14/98 2:13:58pm]
[MOD_REV=REV0_60C]
[MOD_PAGE=PAGE29]
[SOLUTION=AUDIO/AUDIO]
NOTE: CNR SPEC SAYS SMBUS CONTROLLER NOT POWERED BY 3V STBY...COULD BE BACKDRIVE ISSUE
I2C ADDR: 110
ATTRIBUTES:
AUDIO_CNR
ROOM=AUD_CNR
CNR SLOT DECOUPLING
J3A1
CNR60
750073-002
CONN
STUFF FOR NO 3.3V DUAL SUPPORT
STUFF FOR NO 5V DUAL
DYNAMIC PRIMARY DOWN CONTROL
STUFF FOR SOFT AUDIO W/CNR (NO 1373)
PLACE BY PIN 14
AUD_LINK_RST* IS DRIVEN BY ICH2 ON RESUME WELL
ALWAYS STUFF!!!
STUFF FOR SOFT AUDIO AND CNR
[MODULE=AUDIO]
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
AUDIO
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:06 2001
SHEET:
34
DRAWING


NEC USB2 HC 0.99!!
U6C1
NEC_USB2HC
PQFP BODY
V_3P3_STBY
V_5P0_STBY
USB2_LEG_EN
USB2_IRI_1_2
XT1
XT2
Y7B1
30.0MHZ
USB2_RST2
TO_SMI*
CLK_48MHZ_EN*
P_AD<31..0>
P_C/BE<3..0>*
USB2_CLKRUN
P_DEVSEL*
P_FRAME*
P_GNT5*
P_INTD*
P_INTC*
P_INTH*
P_IRDY*
P_PAR
CK_P_33M_USB2
USB2_RST1
P_PERR*
P_PME*
P_REQ5*
P_SERR*
P_STOP*
P_TRDY*
USB2_PIN_EN
TP_SRMOD
TP_SRDTA
TP_SRCLK
USB2_DP5
USB2_DM5*
USB2_DP4
USB2_DM4*
USB2_DP3
USB2_DM3*
USB2_DP2
USB2_DM2*
USB2_DP1
USB2_DM1*
USB_USB2_OC3_4*
USB_USB2_OC1_2*
USB2_AGND
USB_AVCC
V_3P3_STBY
USB_2P0_RREF
CHECK RREF VALUE
TIE PC1 AND PC2 TO AVSS PIN ON PKG
TIE AVSS AND AVDD BYPASS GROUND TOGETHER
NC=117,118,119
VCC=22,60,89
GND=9,21,31,41,42,66,79,80,101,108,110
GND=116,121,122,128,134,147,153,159,160
VCC3=1,8,20,40,51,70,81,100,113,120,125,131,135,146,150,156
[PAGE_TITLE=USB2P0_PQFP]
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
USB2.0 PQFP
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:09 2001
SHEET:
35
DRAWING


NEC USB2 HC 0.99!!
V_3P3_STBY
V_5P0_STBY
VCC3=V_3P3_STBY
VCC=V_5P0_STBY
U6C2
NEC_USB2HC
UBGA BODY
P_AD<31..0>
P_C/BE<3..0>*
USB2_CLKRUN
P_DEVSEL*
P_FRAME*
P_GNT5*
P_INTD*
P_INTC*
P_INTH*
P_TRDY*
P_PAR
CK_P_33M_USB2
P_PERR*
P_PME*
P_REQ5*
P_SERR*
P_STOP*
P_TRDY*
USB2_RST2
RSMRST*
P_PCIRST*
USB2_DP5
USB2_DM5*
USB2_DP4
USB2_DM4*
USB2_DP3
USB2_DM3*
USB2_DP2
USB2_DM2*
USB2_DP1
USB2_DM1*
USB_USB2_OC3_4*
USB_USB2_OC1_2*
USB_AVCC
USB2_AGND
TIE AVSS AND AVDD BYPASS GROUND TOGETHER
TIE PC1 AND PC2 TO AVSS PIN ON PKG
STUFF FOR A1 SI
STUFF FOR A2 SI
USB2_RST1
USB2_PIN_EN
SUS_STAT*
TP_SRMOD
TP_SRDTA
TP_SRCLK
[PAGE_TITLE=USB2P0_UBGA]
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
USB2.0 UBGA
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:11 2001
SHEET:
36
DRAWING


CR-37
LAST_USED:
R204L
C206L
ETHERNET_LAN_CONTROLLER
POWER_GROUP=VCC=V_3P3_STBY
ATTRIBUTES:
BOM=LAN_STUDY
ROOM=LAN_STUDY
U1E1
KINNERETH
750285-001
IC
JA1H1
DUAL_PULSEJACK/
RJ45_2LED_TABUP
A11420-001
CONN
GND=4,5,13,14
U6D1 A05441-001
AT93C46A_66
VCC=V_3P3_STBY
BOM NOTE: BLANK PART 109868-001
VCC=8
GND=5
NC=7
WOL HEADER
J7C1
1X3HDR
HDR
Q7C2
MMBT3904
XSTR
108969-001
Q7C1
MMBT2222
XSTR
Y2E1
25.000MHZ
SM
XTAL
630770-011
L1E1
4.7UH
IND
721891-008
[SOLUTION=KINNERETH_PULSEJACK/KINNERETH_PULSEJACK_REV0_3D]
[MODULE=LAN]
[MOD_PAGE=PAGE2]
[MOD_REV=REV0_3D]
[PAGE_TITLE=ETHERNET_LAN_CONTROLLER]
DRAWING
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
ETHERNET_LAN_CONTROLLER
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:13 2001
SHEET:
37



SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD

PAGE TITLE: AD1885 CODEC

REV: 1.0

INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Jul 10 11:10:02 2001

SHEET: 38

[PAGE_TITLE=AD1881/AD1885_CODEC_SC4297A/CS4200/CS4201]
[LAST_MAKEGOLD: 6/27/00 1:10:05 AM]
[MOD_PAGE=PAGE2] [MOD_REV=0.66C]

[MODULE=AUDIO] [SOLUTION=AUDIO\AUDIO--372]

DRAWING

CODEC CAPS

LAST_USED:

R4006A
C4026A
U4001A
Y4001A

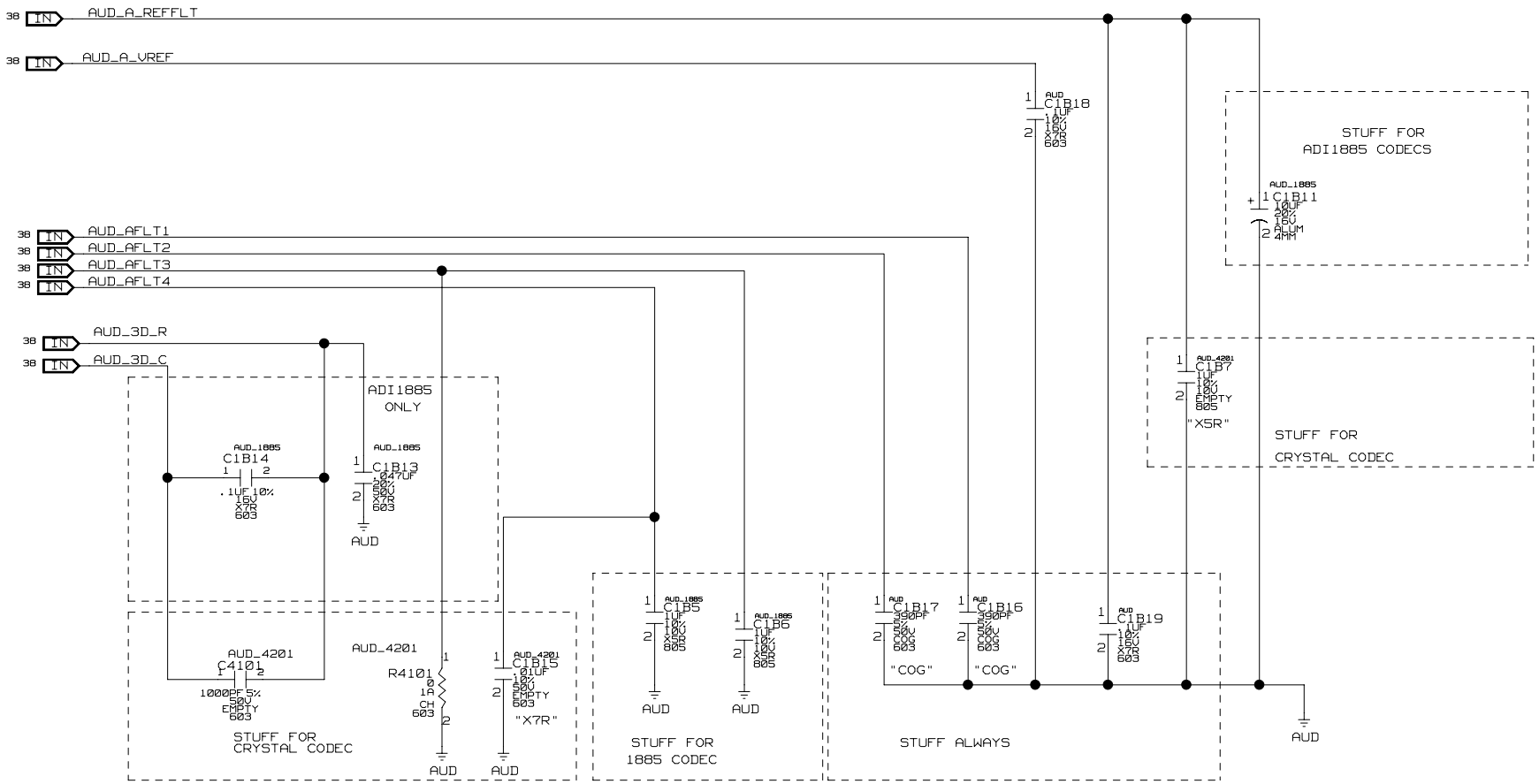
MULTI LAYOUT FOR
4201 & 1885(DEFAULT)

KEEP CAPS AS CLOSE
AS POSSIBLE TO AC97
CODEC.

ATTRIBUTES:

AUDIO
ROOM=AUD_CODEC

AUDIO SUBMODULE 2



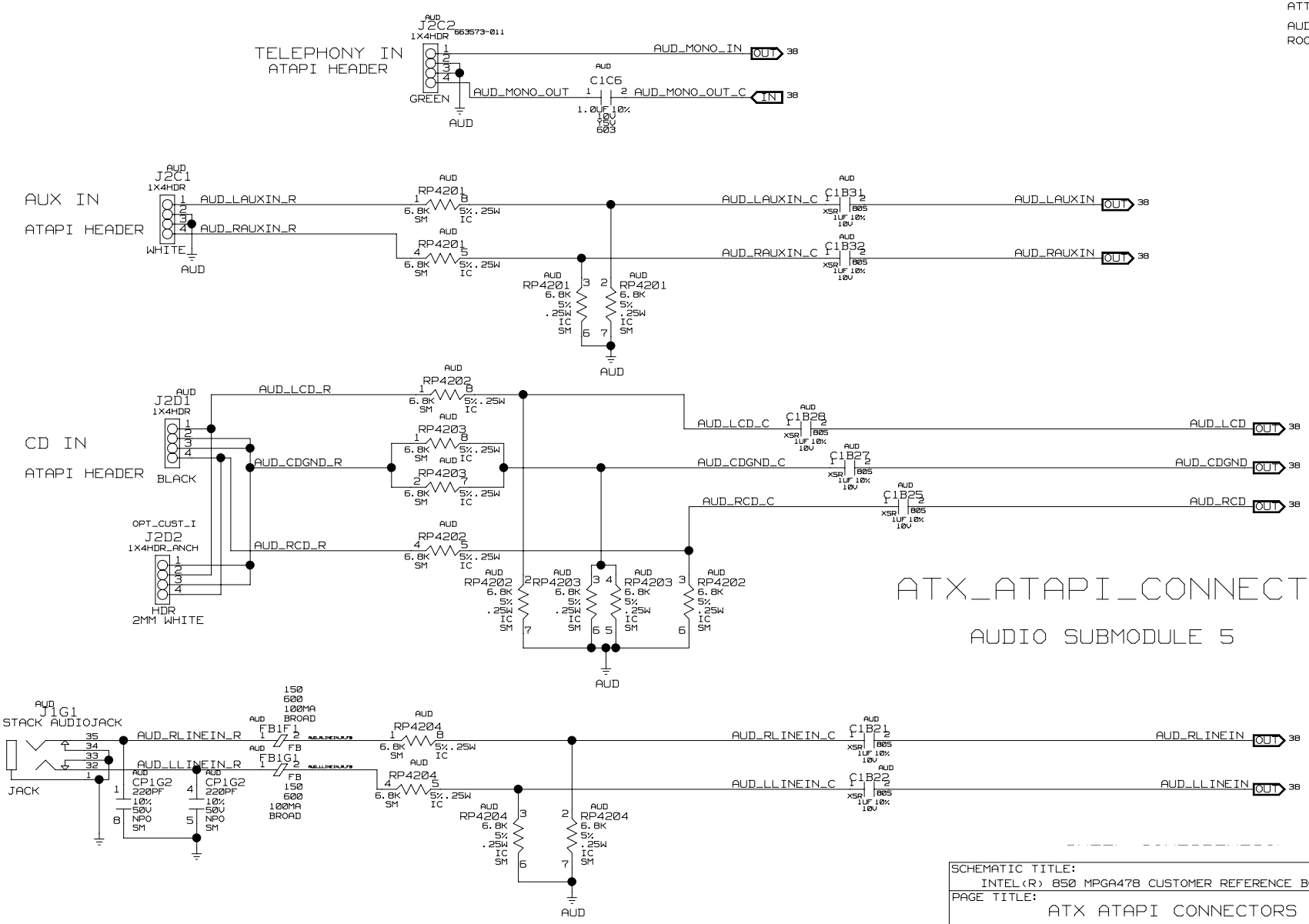
SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: CODEC CAPS		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:15 2001	SHEET: 39

[PAGE_TITLE=CODEC]

DRAWING

LAST_USED:
CP2701A
C2710A
U2701A
RP2701A
J2705A

ATTRIBUTES:
AUDIO
ROOM=AUD_CONNS



SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD

PAGE TITLE: ATX ATAPI CONNECTORS

REV: 1.0

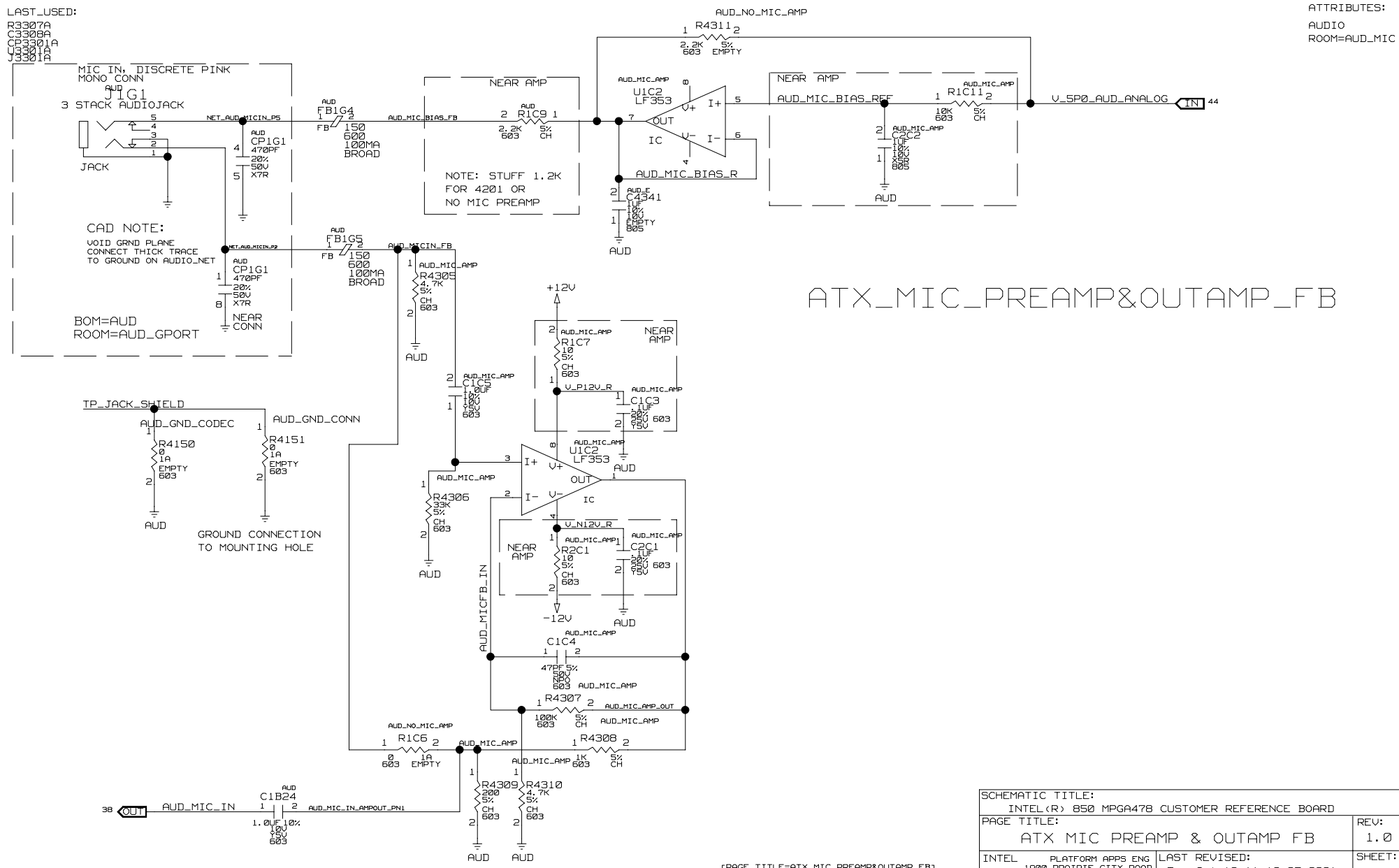
INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Jul 10 11:11:16 2001

SHEET: 40

DRAWING

[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO] [MOD_PAGE=PAGE27] [MOD_REV=REV0_60C] [PAGE_TITLE=ATX_ATAPI_CONNECTORS]

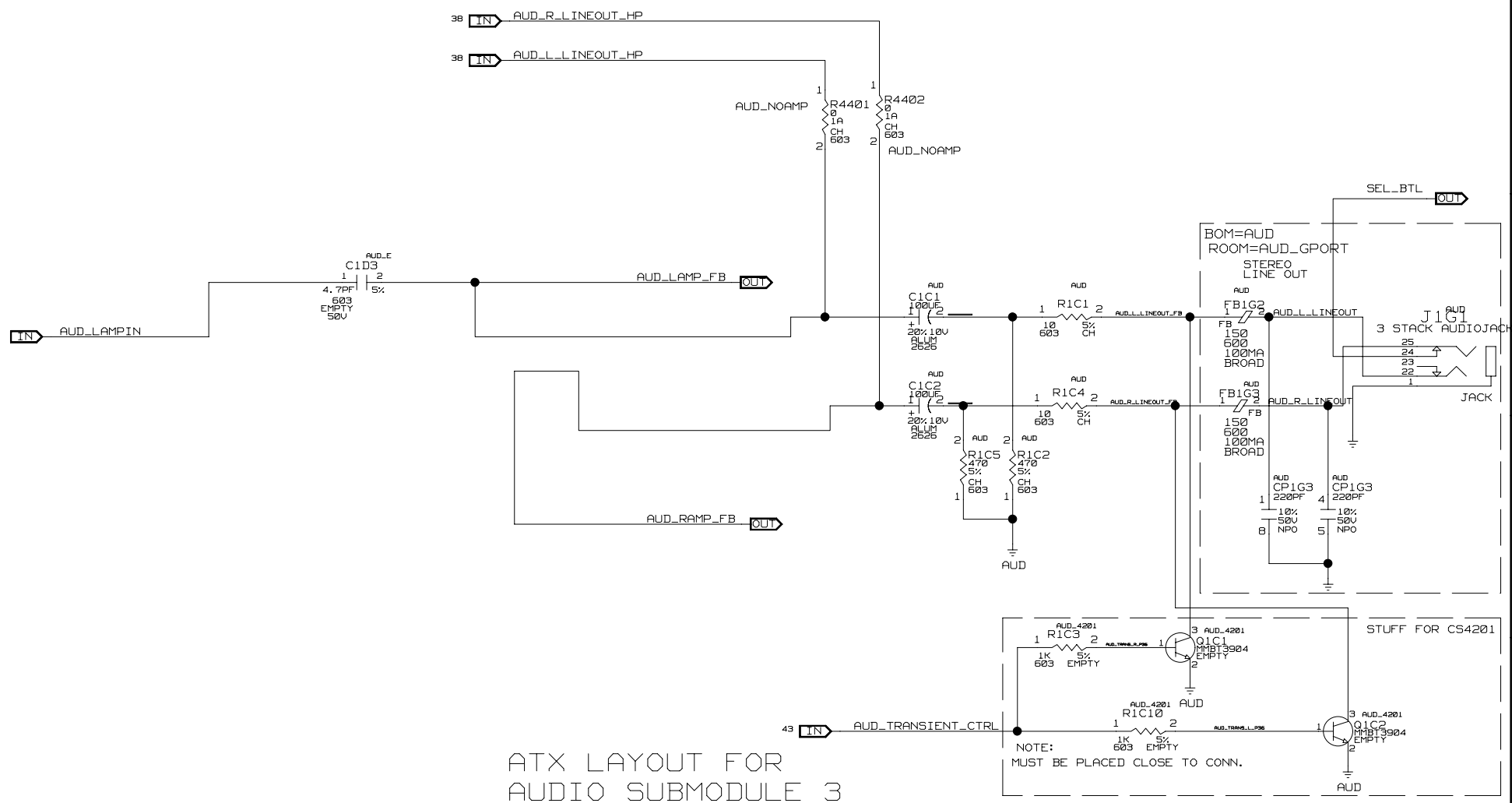

CR-41
LAST_USED:
R3307A
C3308A
CP3301A
CJ301A
J3301A
ATTRIBUTES:
AUDIO
ROOM=AUD_MIC
MIC IN, DISCRETE PINK
MONO CONN
J1G1
3 STACK AUDIOJACK
JACK
CP1G1
470PF
20%
50V
X7R
CAD NOTE:
VOID GRND PLANE
CONNECT THICK TRACE
TO GROUND ON AUDIO_NET
BOM=AUD
ROOM=AUD_GPORT
NEAR CONN
FB1G4
150
600
100MA
BROAD
FB1G5
NEAR AMP
R1C9
2.2K
603
5%
CH
NOTE: STUFF 1.2K
FOR 4201 OR
NO MIC PREAMP
AUD_NO_MIC_AMP
R4311
2.2K
603
5%
EMPTY
U1C2
LF353
OUT
IC
AUD_MIC_BIAS_R
C4341
1UF
10%
10V
EMPTY
805
AUD_MIC_BIAS_REF
R1C11
10K
603
5%
CH
C2C2
1UF
10%
10V
X5R
805
V_5P0_AUD_ANALOG
IN
44
ATX_MIC_PREAMP&OUTAMP_FB
R4305
4.7K
5%
CH
603
+12V
R1C7
10
5%
CH
603
V_P12V_R
C1C3
1UF
20%
25V
Y5V
603
C1C5
1.0UF
10%
10V
Y5V
603
TP_JACK_SHIELD
AUD_GND_CODEC
AUD_GND_CONN
R4150
0
1A
EMPTY
603
R4151
0
1A
EMPTY
603
GROUND CONNECTION
TO MOUNTING HOLE
R4306
33K
5%
CH
603
V_N12V_R
R2C1
10
5%
CH
603
C2C1
1UF
20%
25V
Y5V
603
-12V
AUD_MICFB_IN
C1C4
47PF 5%
50V
NPO
603
R4307
100K
603
5%
CH
AUD_MIC_AMP_OUT
R1C6
0
603
1A
EMPTY
R4308
1K
603
5%
CH
R4309
200
5%
CH
603
R4310
4.7K
5%
CH
603
38
OUT
AUD_MIC_IN
C1B24
1.0UF 10%
10V
Y5V
603
AUD_MIC_IN_AMPOUT_PN1
[MODULE=AUDIO]
[SOLUTION=AUDIO/AUDIO]
[MOD_PAGE=PAGE33]
[MOD_REV=REV0_60C]
[PAGE_TITLE=ATX_MIC_PREAMP&OUTAMP_FB]
DRAWING
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
ATX MIC PREAMP & OUTAMP FB
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:10:07 2001
SHEET:
41

LAST_USED:

U3601A
C3610A
R3611A
CP3601A
J3601A
Q3601A

ATTRIBUTES:

AUDIO
ROOM=AUD_AMP



ATX LAYOUT FOR AUDIO SUBMODULE 3

SSM2250_AMP

[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO] [MOD_PAGE=PAGE36] [MOD_REV=REV0_60C] [PAGE_TITLE=TDA1308/LM4880_AMP]

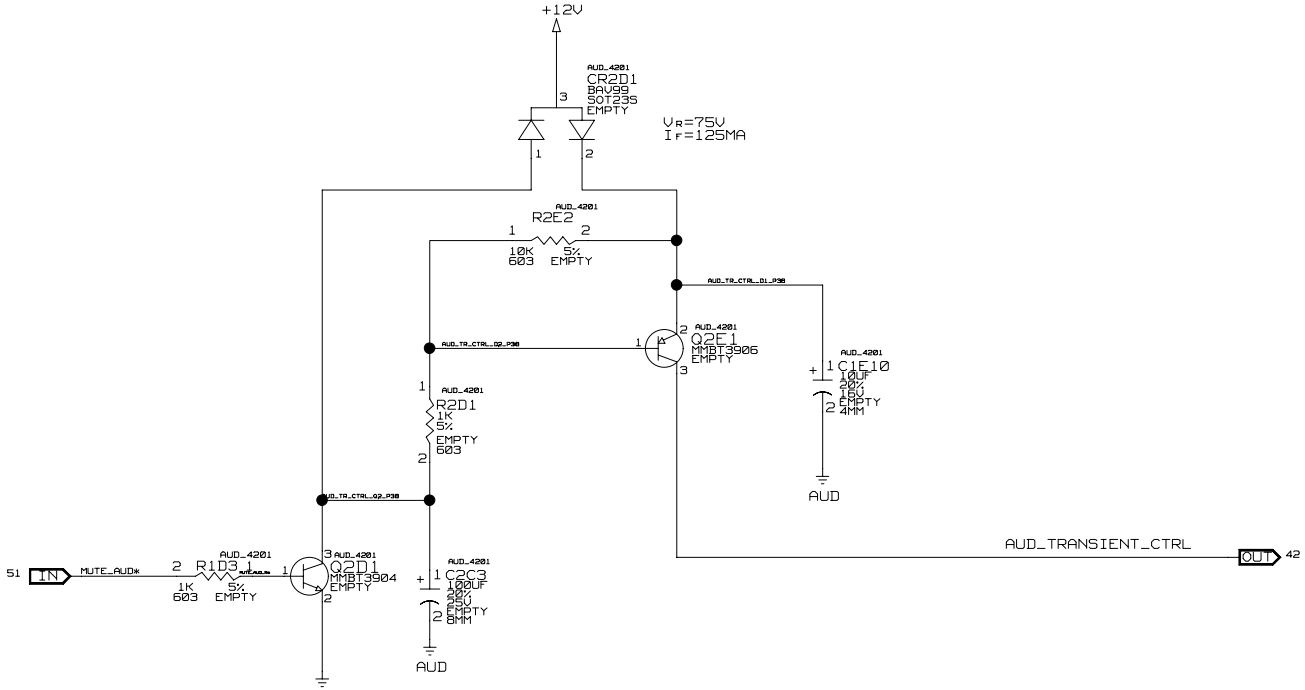
DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: ATX LAYOUT FOR AUDIO SUBMODULE 3		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:17 2001	SHEET: 42

LAST_USED:
R3805A
C3802A
Q3803A
CR3801A

ATTRIBUTES:
AUDIO
ROOM=AUD_AMP

TRANSIENT CONTROL



STUFF PAGE FOR CRYSTAL 4201

[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO] [PAGE_TITLE=TRANSIENT]

DRAWING

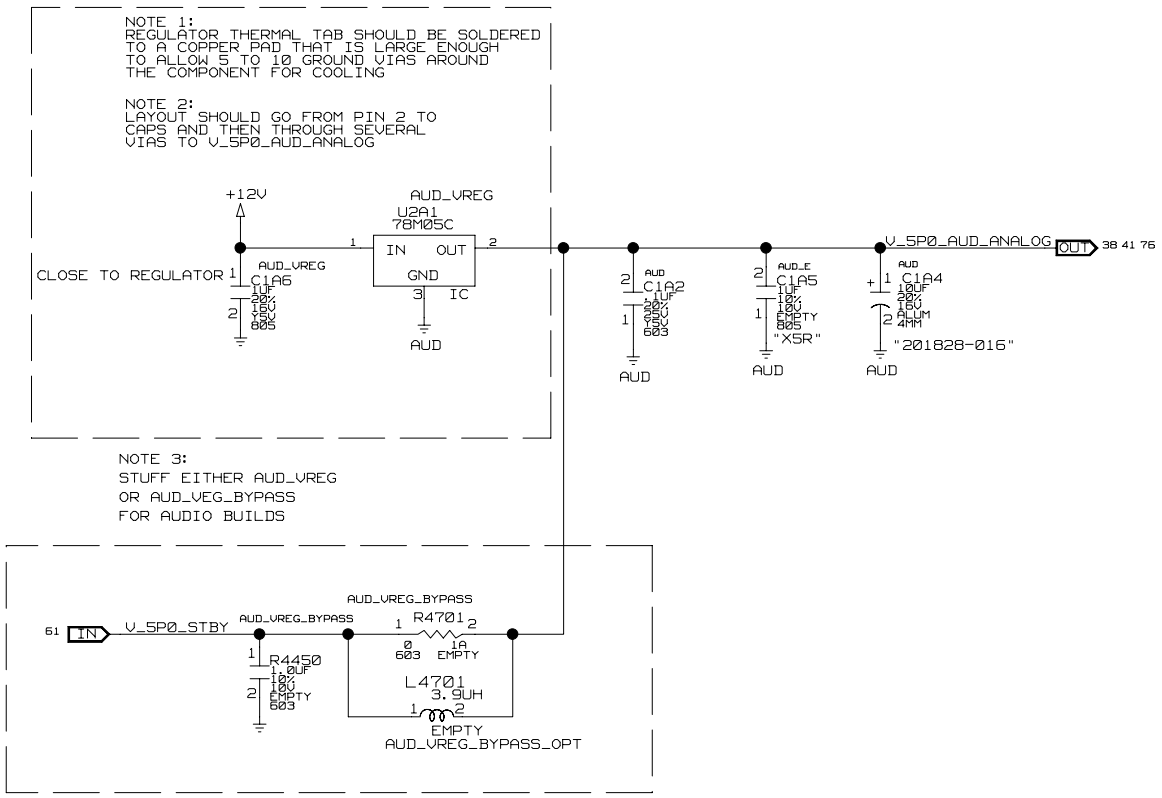
SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: TRANSIENT CONTROL		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:18 2001	SHEET: 43

AUDIO_VREG

[MODULE=AUDIO]

LAST_USED:
U3401A
C3404A

ATTRIBUTES:
AUDIO
ROOM=AUD_VREG

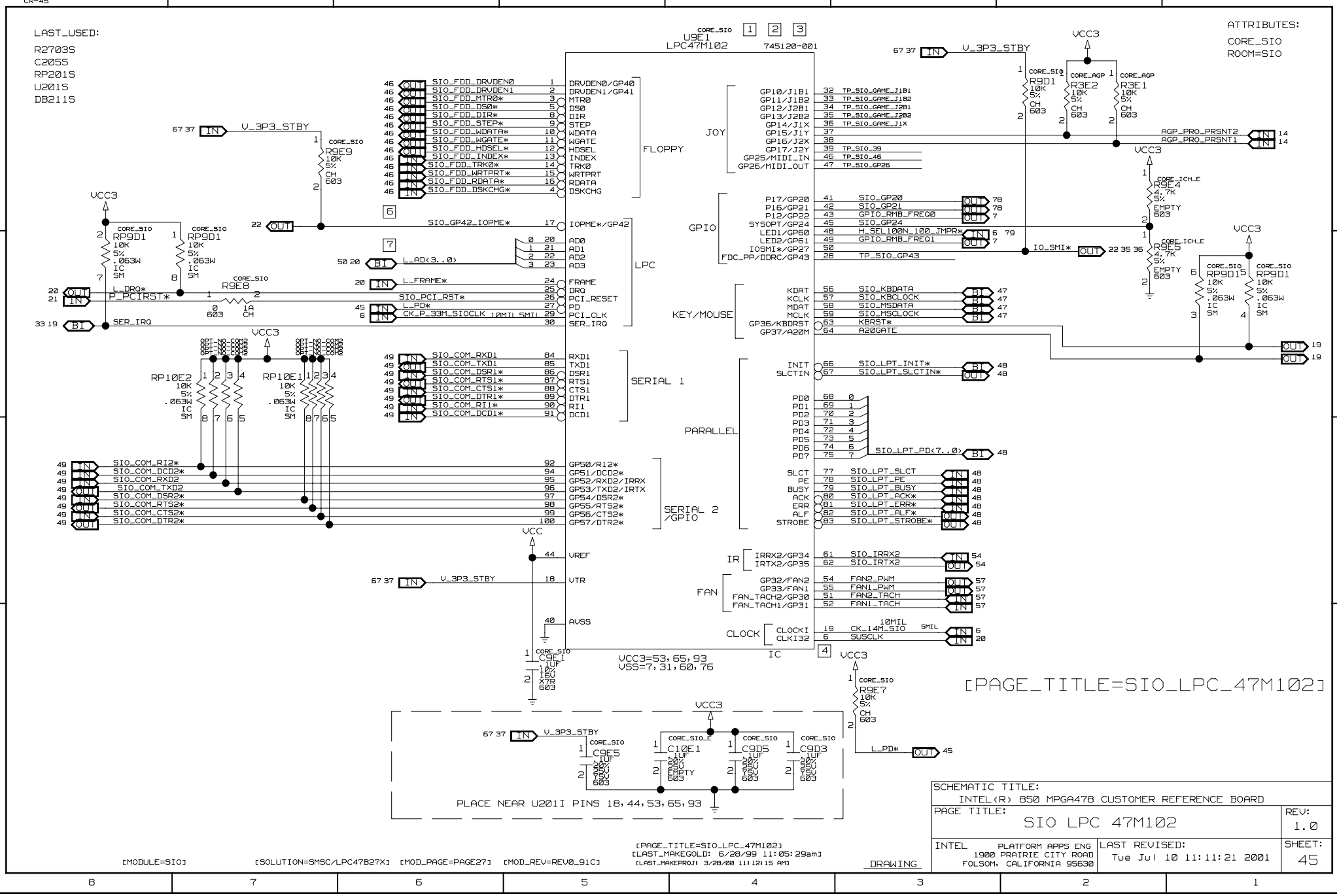


SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: AUDIO VREG	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:19 2001
	SHEET: 44

[SOLUTION=AUDIO/AUDIO]

[PAGE_TITLE=AUDIO_VREG]
[LAST_MAKEGOLD: 6/14/99 9:19:58am]
[MOD_PAGE=PAGE34] [MOD_REV=REV0_60C]

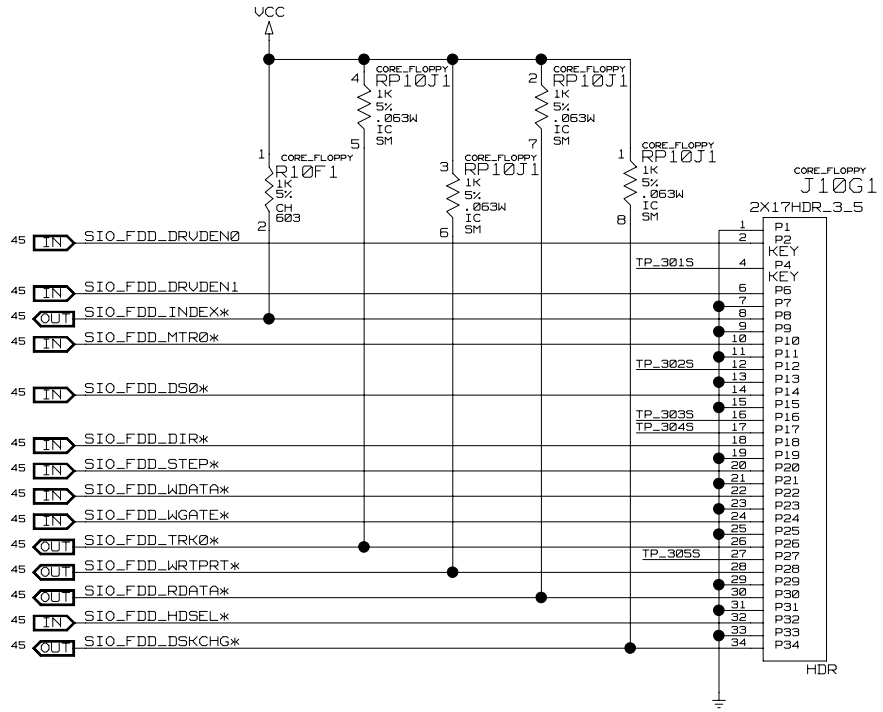
DRAWING


CR-45
LAST_USED:
R2703S
C205S
RP201S
U201S
DB211S
ATTRIBUTES:
CORE_SIO
ROOM=SIO
U9E1
LPC47M102
745120-001
FLOPPY
LPC
GPIO
KEY/MOUSE
SERIAL 1
PARALLEL
SERIAL 2 /GPIO
IR
FAN
CLOCK
IC
JOY
VCC3=53,65,93
VSS=7,31,60,76
PLACE NEAR U201I PINS 18,44,53,65,93
[PAGE_TITLE=SIO_LPC_47M102]
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
SIO LPC 47M102
REV:
1.0
INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:21 2001
SHEET:
45
DRAWING
[MODULE=SIO]
[SOLUTION=SMSC/LPC47B27X]
[MOD_PAGE=PAGE27]
[MOD_REV=REV0_91C]
[PAGE_TITLE=SIO_LPC_47M102]
[LAST_MAKEGOLD: 6/28/99 11:05:29am]
[LAST_MAKEPROJ: 3/28/00 11:12:15 AM]

LAST_USED:
R300S
J301S
RP301S
TP_305S

ATX_FLOPPY

ATTRIBUTES:
CORE_FLOPPY
ROOM=SIO_FLOPPY



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[LAST_MAKEGOLD: 6/28/99 11:05:37am]
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PAGE TITLE: ATX FLOPPY	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:22 2001
	SHEET: 46

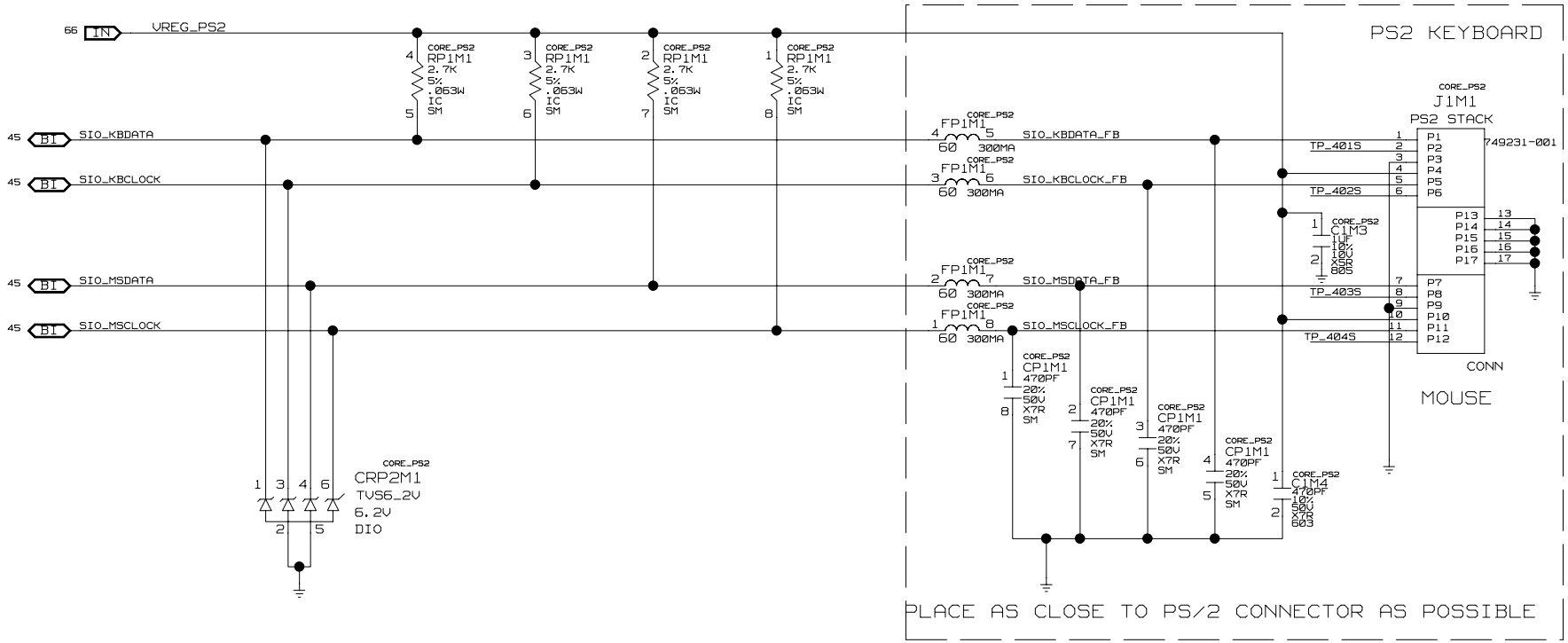
ATX DOUBLE-STACKED PS2_KEYBOARD/MOUSE

LAST_USED:

CR404S
RP401S
TP_404S
CP401S
FP401S
CRP401S
FB401S
RT401S
J401S
C402S

ATTRIBUTES:

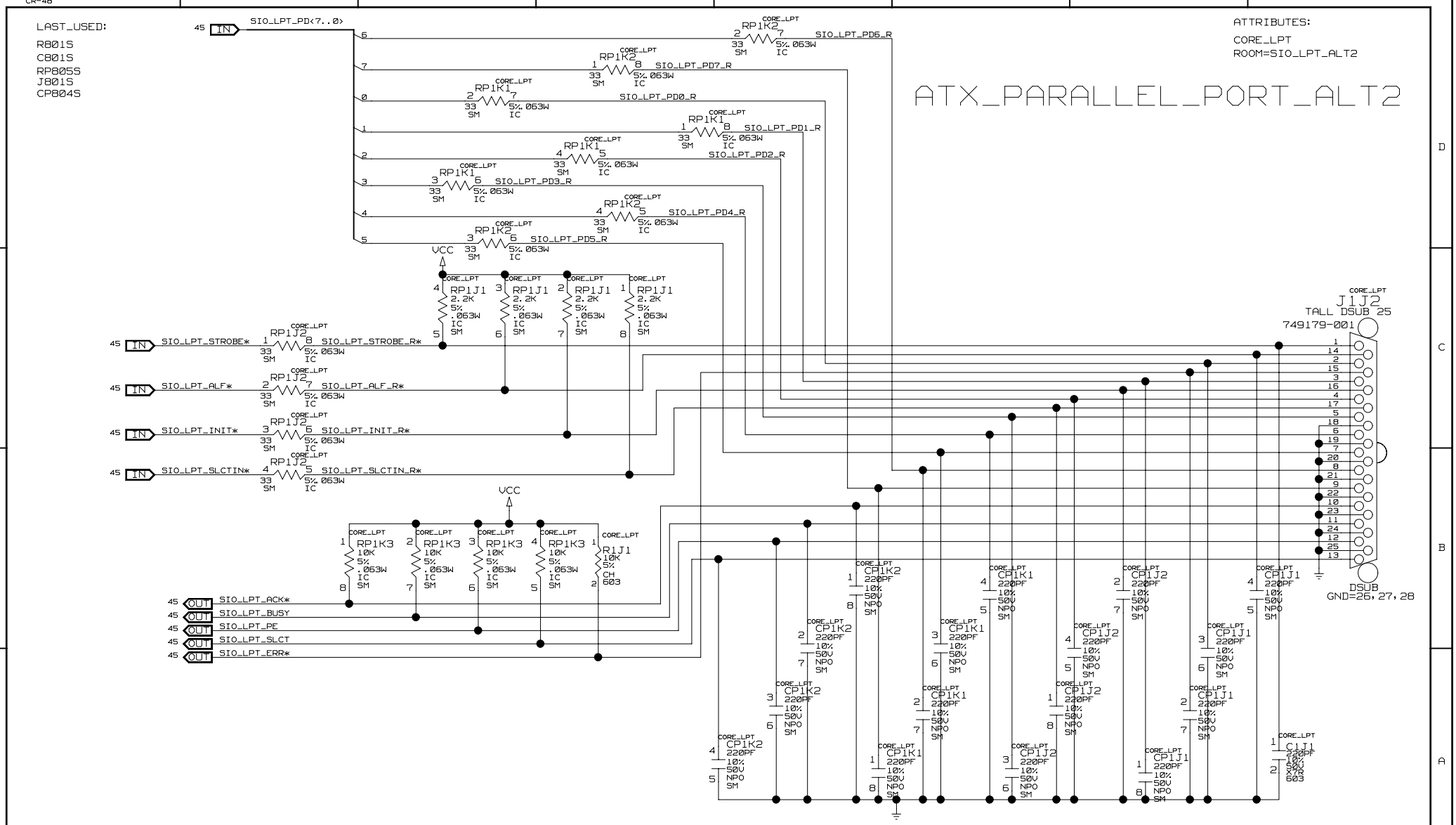
CORE_PS2
ROOM=SIO_PS2KEYMOUSE



[MODULE=SIO] [SOLUTION=SMSC/LPC47B27X] [MOD_PAGE=PAGE4] [MOD_REV=REV0_91C] [PAGE_TITLE=PS2_KEYBOARD/MOUSE] [LAST_MAKEGOLD: 6/28/99 11:05:40am]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: PS2 KETBOARD/MOUSE		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:23 2001	SHEET: 47


CR-4B
LAST_USED:
R801S
C801S
RP805S
J801S
CP804S
ATTRIBUTES:
CORE_LPT
ROOM=SIO_LPT_ALT2
ATX_PARALLEL_PORT_ALT2
SIO_LPT_PD<7..0>
SIO_LPT_PD6_R
SIO_LPT_PD7_R
SIO_LPT_PD0_R
SIO_LPT_PD1_R
SIO_LPT_PD2_R
SIO_LPT_PD3_R
SIO_LPT_PD4_R
SIO_LPT_PD5_R
SIO_LPT_STROBE*
SIO_LPT_STROBE_R*
SIO_LPT_ALF*
SIO_LPT_ALF_R*
SIO_LPT_INIT*
SIO_LPT_INIT_R*
SIO_LPT_SLCTIN*
SIO_LPT_SLCTIN_R*
SIO_LPT_ACK*
SIO_LPT_BUSY
SIO_LPT_PE
SIO_LPT_SLCT
SIO_LPT_ERR*
VCC
J1J2
TALL DSUB 25
749179-001
DSUB
GND=26,27,28
[MOD_REV=REV0_91C]
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[LAST_MAKEGOLD: 6/28/99 11:05:57am]
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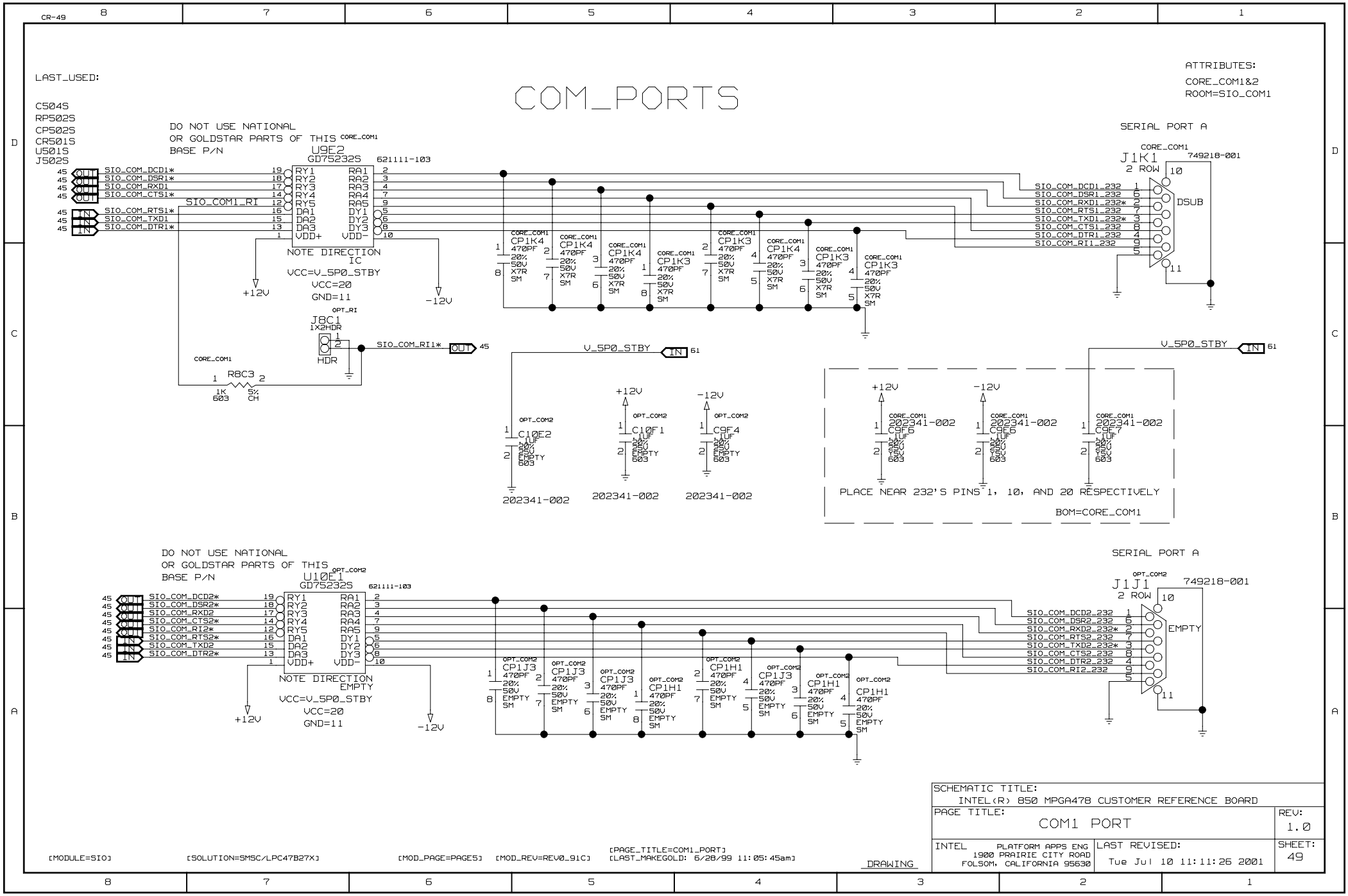
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
ATX PARALLEL PORT ALT2
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:25 2001
SHEET:
48



CR-49
LAST_USED:
C504S
RP502S
CP502S
CR501S
U501S
J502S
COM_PORTS
ATTRIBUTES:
CORE_COM1&2
ROOM=SIO_COM1
DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS
BASE P/N
U9E2
GD75232S
621111-103
NOTE DIRECTION
IC
VCC=V_5P0_STBY
VCC=20
GND=11
SIO_COM1_RI
SIO_COM_DCD1*
SIO_COM_DSR1*
SIO_COM_RXD1
SIO_COM_CTS1*
SIO_COM_RTS1*
SIO_COM_TXD1
SIO_COM_DTR1*
+12V
-12V
J8C1
1X2HDR
HDR
SIO_COM_RI1*
R8C3
1K
603
5%
CH
CP1K4
CP1K3
470PF
20%
50V
X7R
SM
SERIAL PORT A
J1K1
2 ROW
749218-001
DSUB
SIO_COM_DCD1_232
SIO_COM_DSR1_232
SIO_COM_RXD1_232*
SIO_COM_RTS1_232
SIO_COM_TXD1_232*
SIO_COM_CTS1_232
SIO_COM_DTR1_232
SIO_COM_RI1_232
V_5P0_STBY
C10E2
C10F1
C9F4
1UF
20%
25V
Y5V
603
202341-002
C9F6
C9F7
PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY
BOM=CORE_COM1
U10E1
GD75232S
NOTE DIRECTION
EMPTY
VCC=V_5P0_STBY
VCC=20
GND=11
SIO_COM_DCD2*
SIO_COM_DSR2*
SIO_COM_RXD2
SIO_COM_CTS2*
SIO_COM_RI2*
SIO_COM_RTS2*
SIO_COM_TXD2
SIO_COM_DTR2*
CP1J3
CP1H1
SERIAL PORT A
J1J1
2 ROW
749218-001
EMPTY
SIO_COM_DCD2_232
SIO_COM_DSR2_232
SIO_COM_RXD2_232*
SIO_COM_RTS2_232
SIO_COM_TXD2_232*
SIO_COM_CTS2_232
SIO_COM_DTR2_232
SIO_COM_RI2_232
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
COM1 PORT
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:26 2001
SHEET:
49
DRAWING
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[SOLUTION=SMSC/LPC47B27X]
[MOD_PAGE=PAGE5]
[MOD_REV=REV0_91C]
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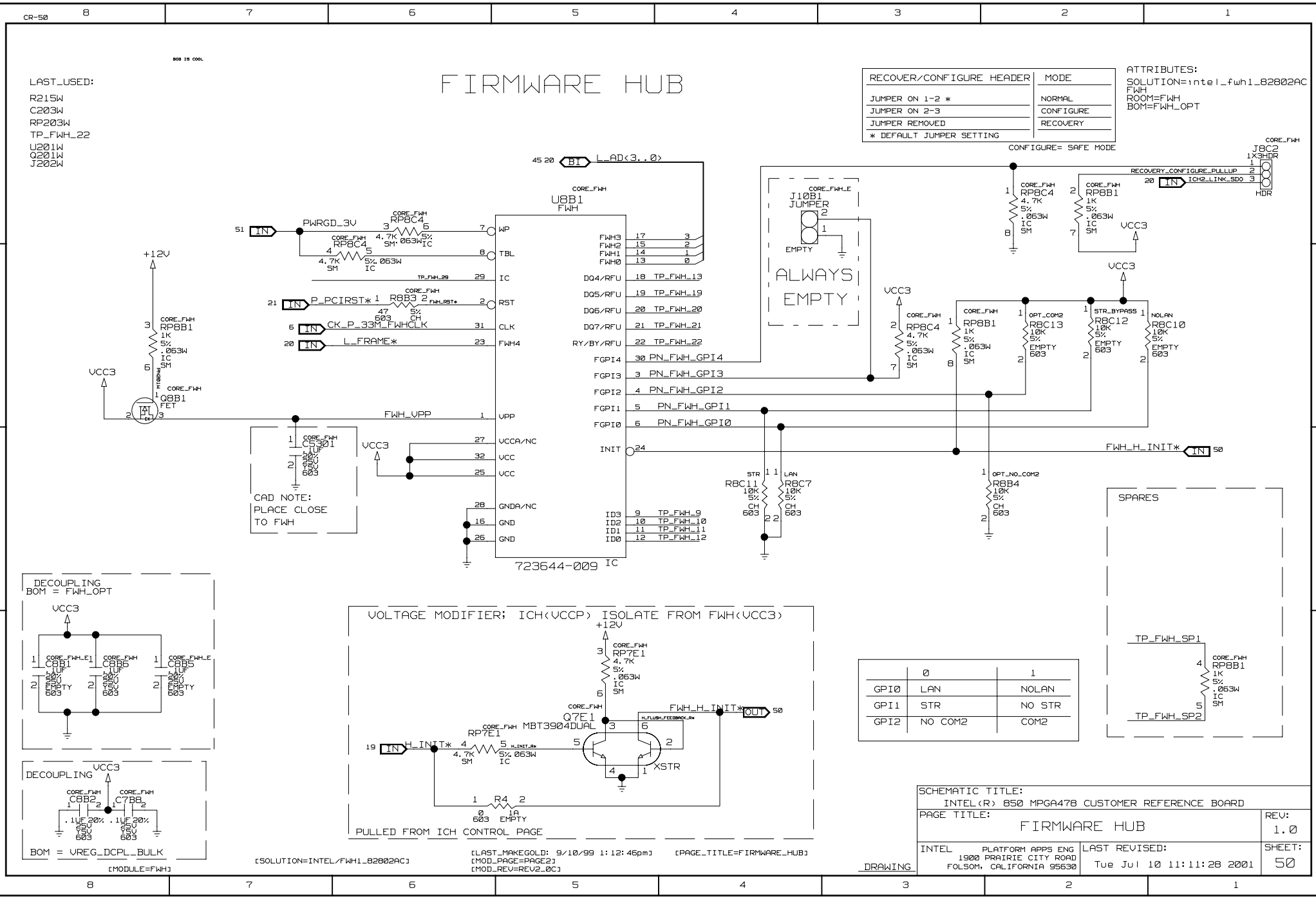
[LAST_MAKEGOLD: 6/28/99 11:05:45am]


CR-50
BOB IS COOL
FIRMWARE HUB
LAST_USED:
R215W
C203W
RP203W
TP_FWH_22
U201W
Q201W
J202W
RECOVER/CONFIGURE HEADER | MODE
JUMPER ON 1-2 * | NORMAL
JUMPER ON 2-3 | CONFIGURE
JUMPER REMOVED | RECOVERY
* DEFAULT JUMPER SETTING
CONFIGURE= SAFE MODE
ATTRIBUTES:
SOLUTION=intel_fwh1_82802AC
FWH
ROOM=FWH
BOM=FWH_OPT
U8B1
FWH
723644-009
IC
L_AD<3..0>
PWRGD_3V
P_PCIRST*
CK_P_33M_FWHCLK
L_FRAME*
FWH_VPP
FWH_H_INIT*
J8C2
1X3HDR
HDR
RECOVERY_CONFIGURE_PULLUP
ICH2_LINK_SDO
J10B1
JUMPER
EMPTY
ALWAYS
EMPTY
PN_FWH_GPI4
PN_FWH_GPI3
PN_FWH_GPI2
PN_FWH_GPI1
PN_FWH_GPI0
TP_FWH_13
TP_FWH_19
TP_FWH_20
TP_FWH_21
TP_FWH_22
TP_FWH_9
TP_FWH_10
TP_FWH_11
TP_FWH_12
Q8B1
FET
CAD NOTE:
PLACE CLOSE
TO FWH
SPARES
TP_FWH_SP1
TP_FWH_SP2
DECOUPLING
BOM = FWH_OPT
DECOUPLING
BOM = VREG_DCPL_BULK
VOLTAGE MODIFIER; ICH(VCCP) ISOLATE FROM FWH(VCC3)
Q7E1
MBT3904DUAL
XSTR
PULLED FROM ICH CONTROL PAGE
GPI0 | LAN | NOLAN
GPI1 | STR | NO STR
GPI2 | NO COM2 | COM2
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
FIRMWARE HUB
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:28 2001
SHEET:
50
DRAWING
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[LAST_MAKEGOLD: 9/10/99 1:12:46pm]
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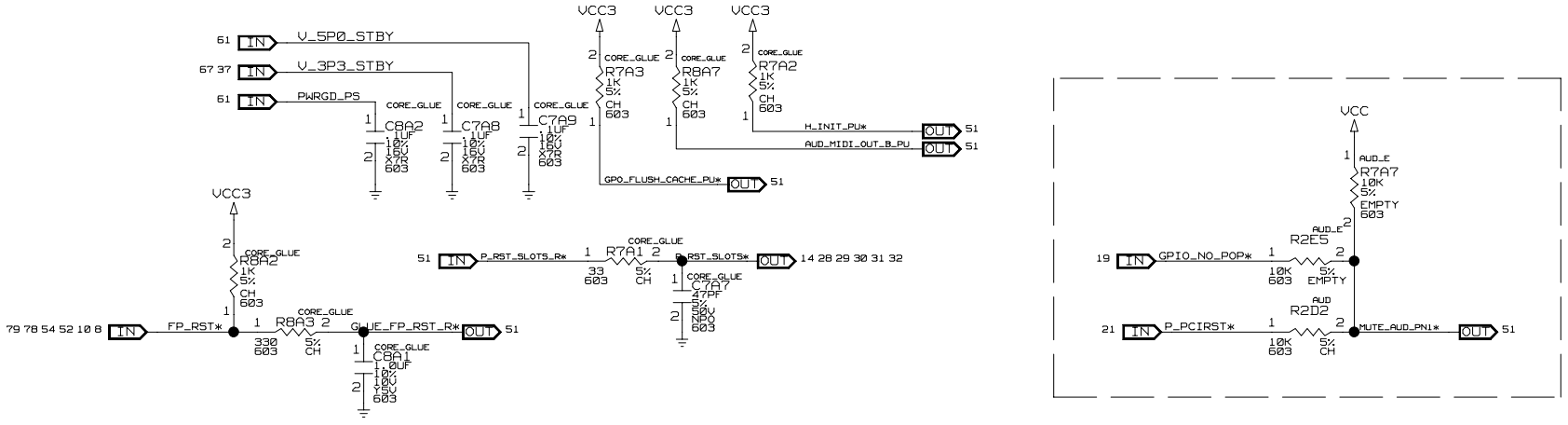
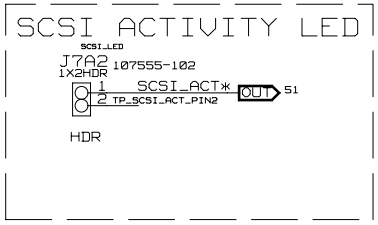
GLUECHIP4

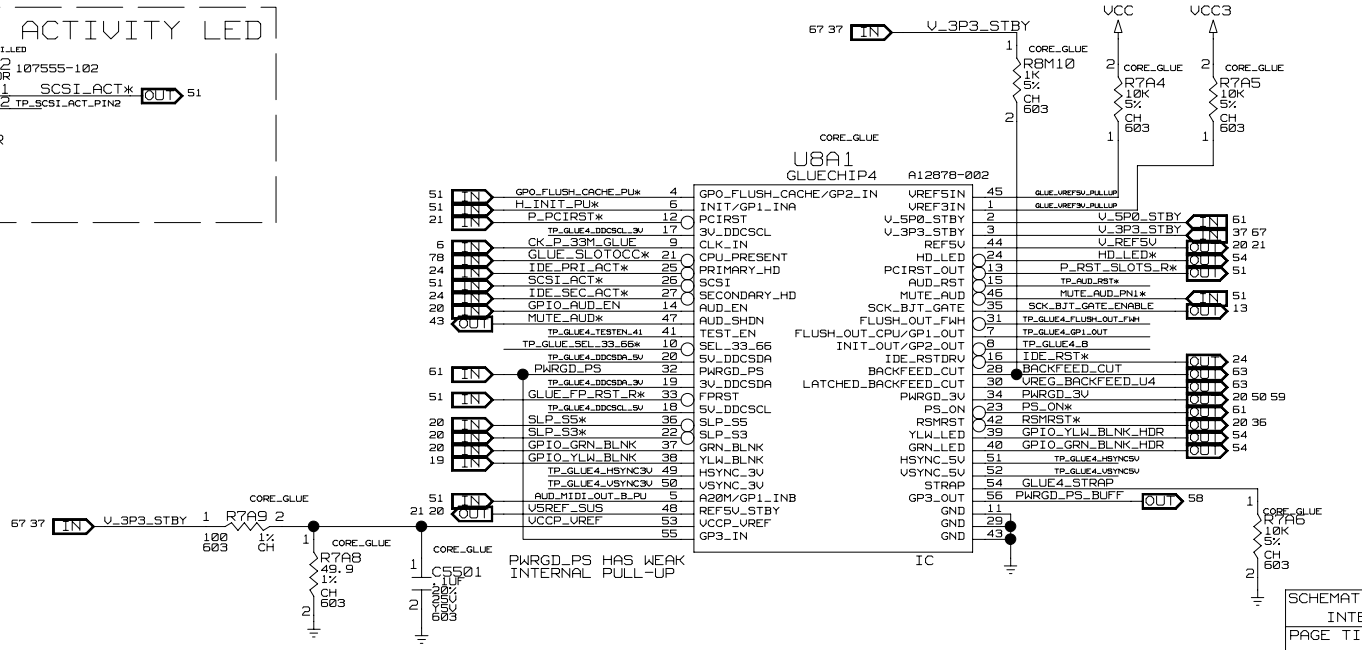


GLUE4 INPUTS

PIN	FUNCTION	TYPE
1	VREF3IN	3I
2	5VSB	PI
3	3VSB	PI
4	GP2_IN	3IU
5	GP1_INB	VCCP REF
6	GP1_INA	VCCP REF
9	CLK_IN	3I
10	SEL_33_66	3IU
12	PCIRST*	3I
14	AUD_EN	3IU
17	3V_DDCSCL	3IOD
18	5V_DDCSCL	5IOD
19	3V_DDCSDA	3IOD
20	5V_DDCSDA	5IOD
21	CPU_PRESENT*	3IU
22	SLP_S3*	3I
25	PRIMARY_HD*	5IU
26	SCSI*	5IU
27	SECONDARY_HD*	5IU
32	PWRGD_PS	5IU
33	FPRST*	5IU
36	SLP_S5*	3I
37	GRN_BLNK	3IU
38	YLW_BLNK	3IU
41	TEST_EN	5ID
45	VREF5IN	5I
46	MUTE_AUD*	3IU
49	HSYNCH_3V	3I
50	VSYNCH_3V	3I
53	VCCP_VREF	AI
54	STRAP	3IU
55	GP3_IN	5I

SCSI ACTIVITY LED





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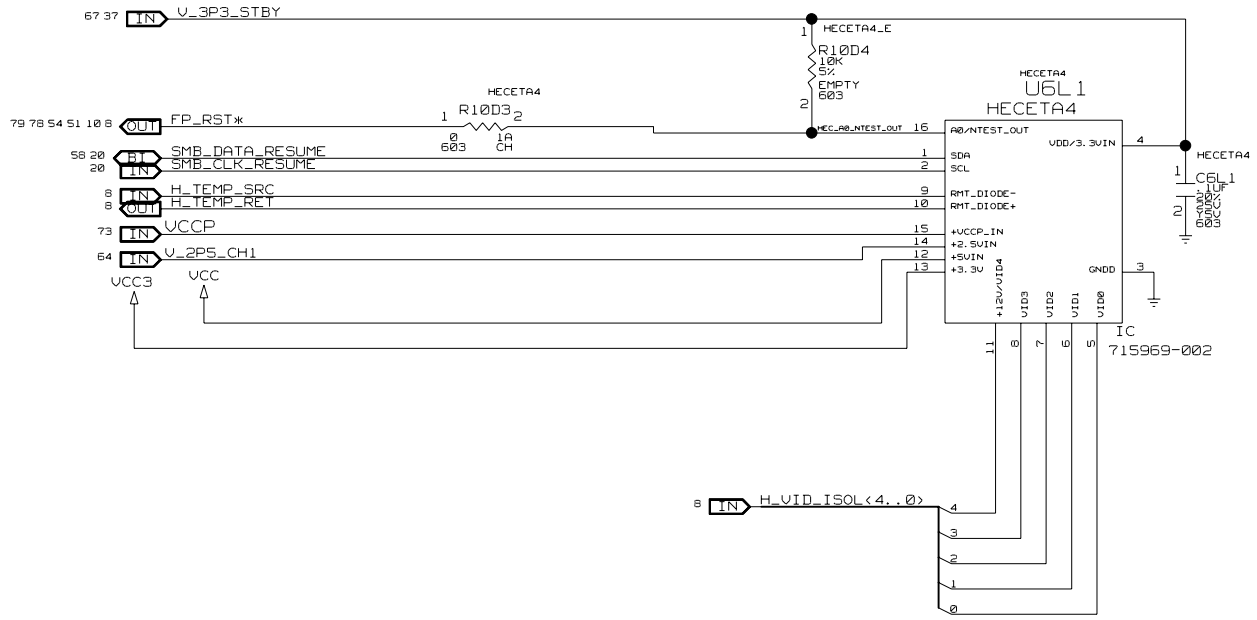
PAGE TITLE: GLUECHIP 4	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:30 2001
	SHEET: 51

CR-52

HARDWARE MANAGEMENT: HECETA



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ROOM=HWM_HECETA4
BOM=HWM_HECETA4

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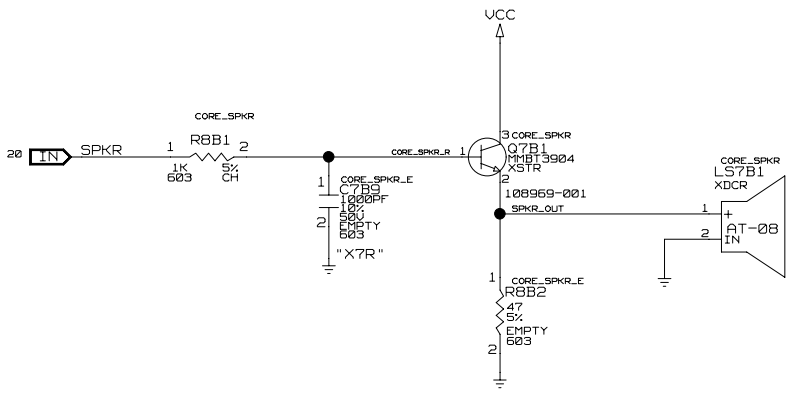
PAGE TITLE: HECETA 4		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:31 2001	SHEET: 52

SPEAKER



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PAGE TITLE: SPEAKER		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:32 2001	SHEET: 53

LAST_USED:
R1105S
C1104S
J1101S

SPARES
RP9D4 CORE_ICH 4 5 220 SM 5% .063W IC
RP9D4 CORE_ICH 3 6 220 SM 5% .063W IC

ATTRIBUTES:
SIO_STDFNTPNL
ROOM=SIO_STDFNTPNL

STD_FRONT_PANEL_HDR

VCC_HDLED_PWR OUT

R10D2 CORE_STDFNTPNL 1 2 10K 603 5% CH — VCC3
R9D12 CORE_ICH 1 2 330 603 5% CH — VCC
UNSTUFF FOR C

51 IN HD_LED*
79 78 52 51 10 8 OUT FP_RST*
45 OUT SIO_IRRX2
45 IN SIO_IRTX2

61 IN V_5P0_STBY
RP9D4 CORE_ICH 2 7 220 SM 5% .063W IC
RP9D4 CORE_ICH 1 8 220 SM 5% .063W IC

J9D2 CORE_STDFNTPNL
2X8HDR_10_14
HDR
VCC

GPIO_GRN_BLNK_HDR IN 51
GPIO_YLW_BLNK_HDR IN 51

VCC

CP9D2 CORE_STDFNTPNL_E 470PF 20% 50V EMPTY SM
CP9D2 CORE_STDFNTPNL_E 470PF 20% 50V EMPTY SM
CP10D1 CORE_STDFNTPNL_E 470PF 20% 50V EMPTY SM
C9B 602431-005 470PF 10% 50V EMPTY 603 "X7R"
CP10D1 CORE_STDFNTPNL_E 470PF 20% 50V EMPTY SM
CP10D1 CORE_STDFNTPNL_E 470PF 20% 50V EMPTY SM
CP10D1 CORE_STDFNTPNL_E 470PF 20% 50V EMPTY SM
CP9D2 CORE_STDFNTPNL_E 470PF 20% 50V EMPTY SM
CP9D2 CORE_STDFNTPNL_E 470PF 20% 50V EMPTY SM

BOM=CORE_STDFNTPNL_E

67 37 IN V_3P3_STBY
R9D10 CORE_ICH 1 2 22K 603 5% CH 202285-081
SW_ON* OUT 20

78 IN SWITCH_ON*
R9D13 CORE_ICH 1 2 33 603 5% CH 202285-013
C9D4 CORE_ICH 1UF 20% 16V 805 202341-007

J8C3 CORE_STDFNTPNL 1X3HDR2 HDR 102276-304
GPIO_GRN_BLNK_HDR IN 51
C8C1 CORE_STDFNTPNL_E 470PF 10% 50V EMPTY 603
GPIO_YLW_BLNK_HDR IN 51
C8C2 CORE_STDFNTPNL_E 470PF 10% 50V EMPTY 603

[MODULE=SIO] [SOLUTION=SMSC/LPC47B27X] [MOD_PAGE=PAGE11] [MOD_REV=REV0_91C]
[PAGE_TITLE=STD_FRONT_PANEL_HDR]
[LAST_MAKEGOLD: 6/28/99 11:04:37am]

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PAGE TITLE: STD FRONT PANEL HDR	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:33 2001
	SHEET: 54

CR-55

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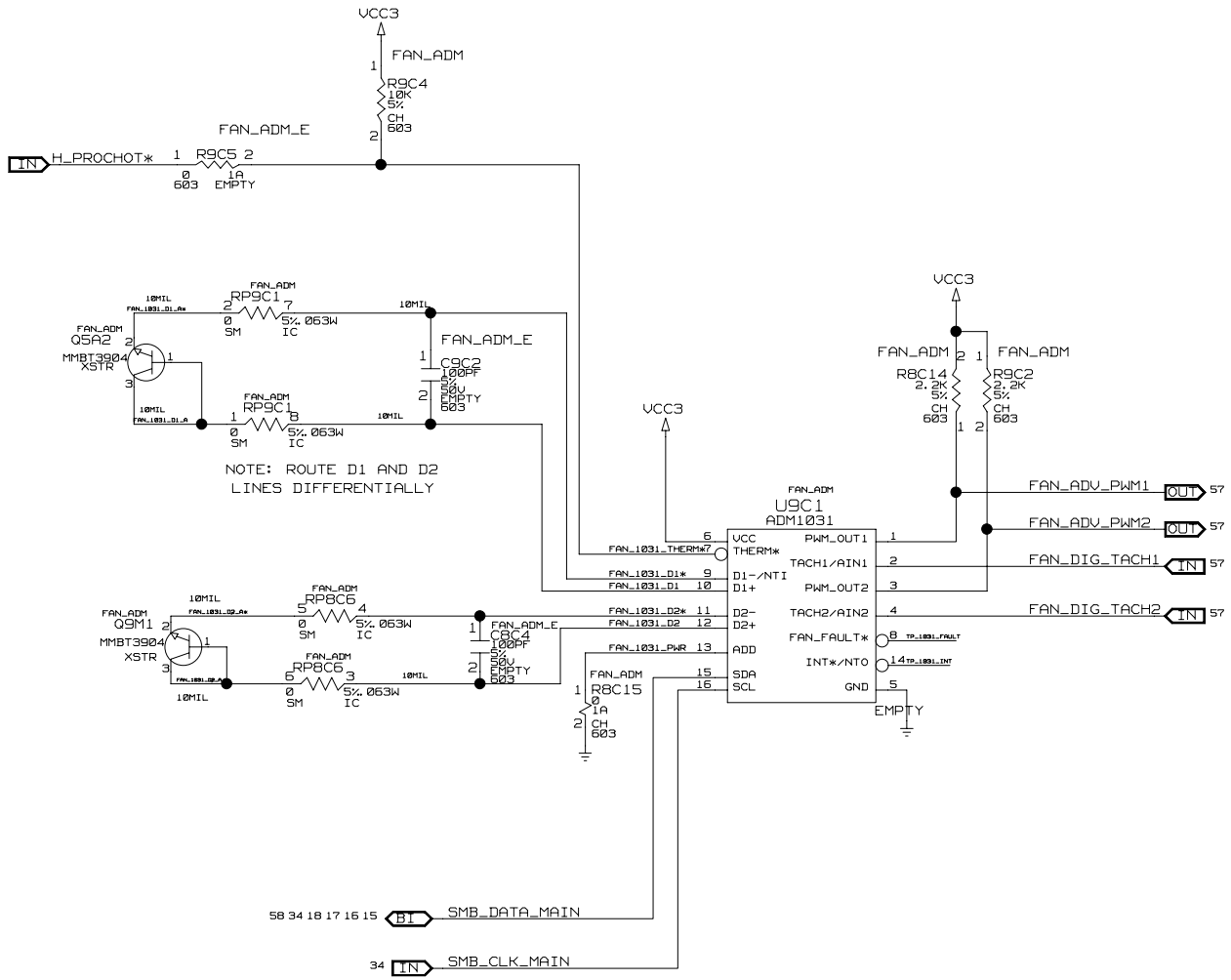
PAGE TITLE:		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Mon Jul 09 17:39:28 2001	SHEET: 55

LAST USED:
C406L

ATTRIBUTES:



[PAGE_TITLE=FAN_CONTRO]

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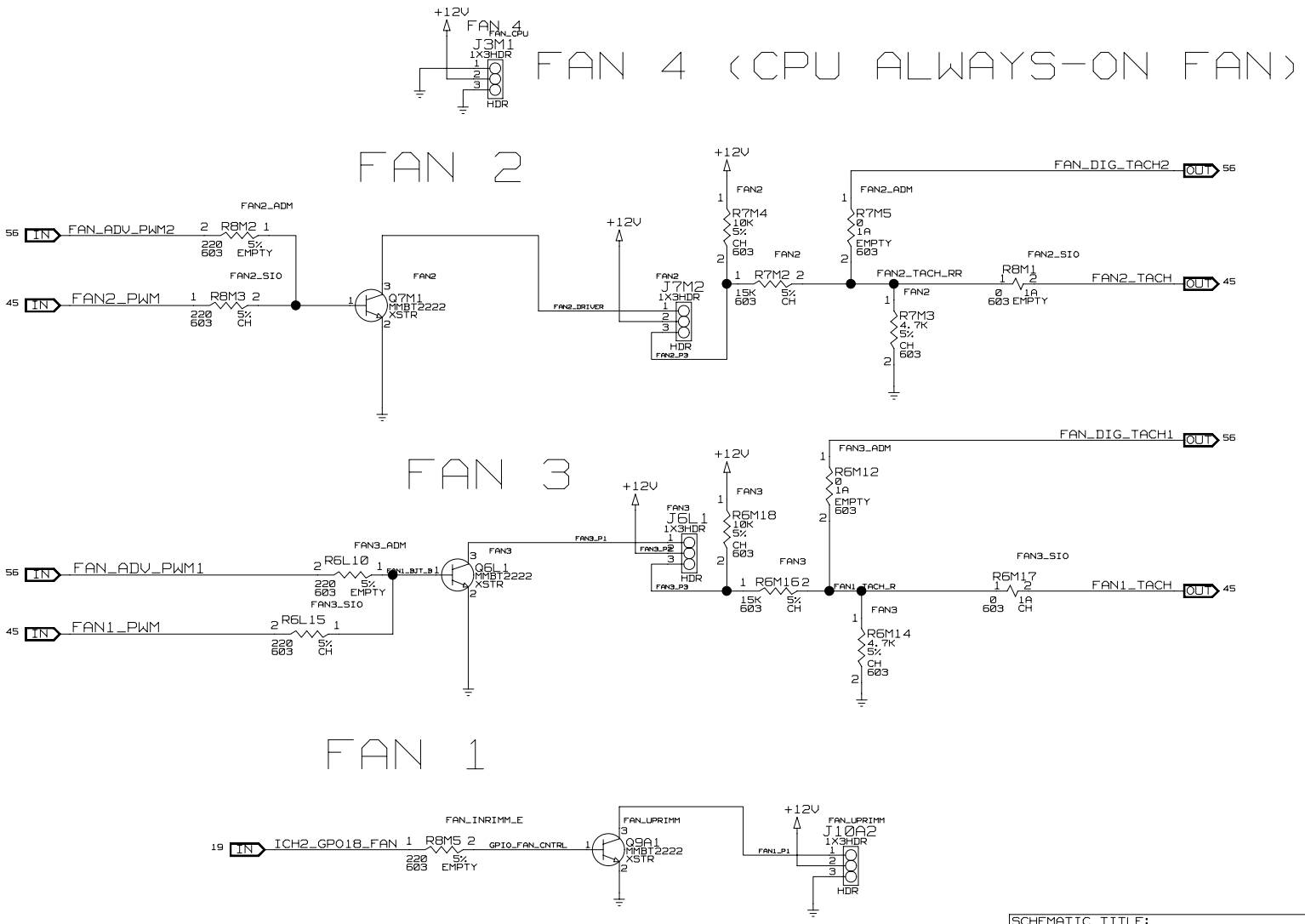
PAGE TITLE: FAN CONTROL		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:35 2001	SHEET: 56



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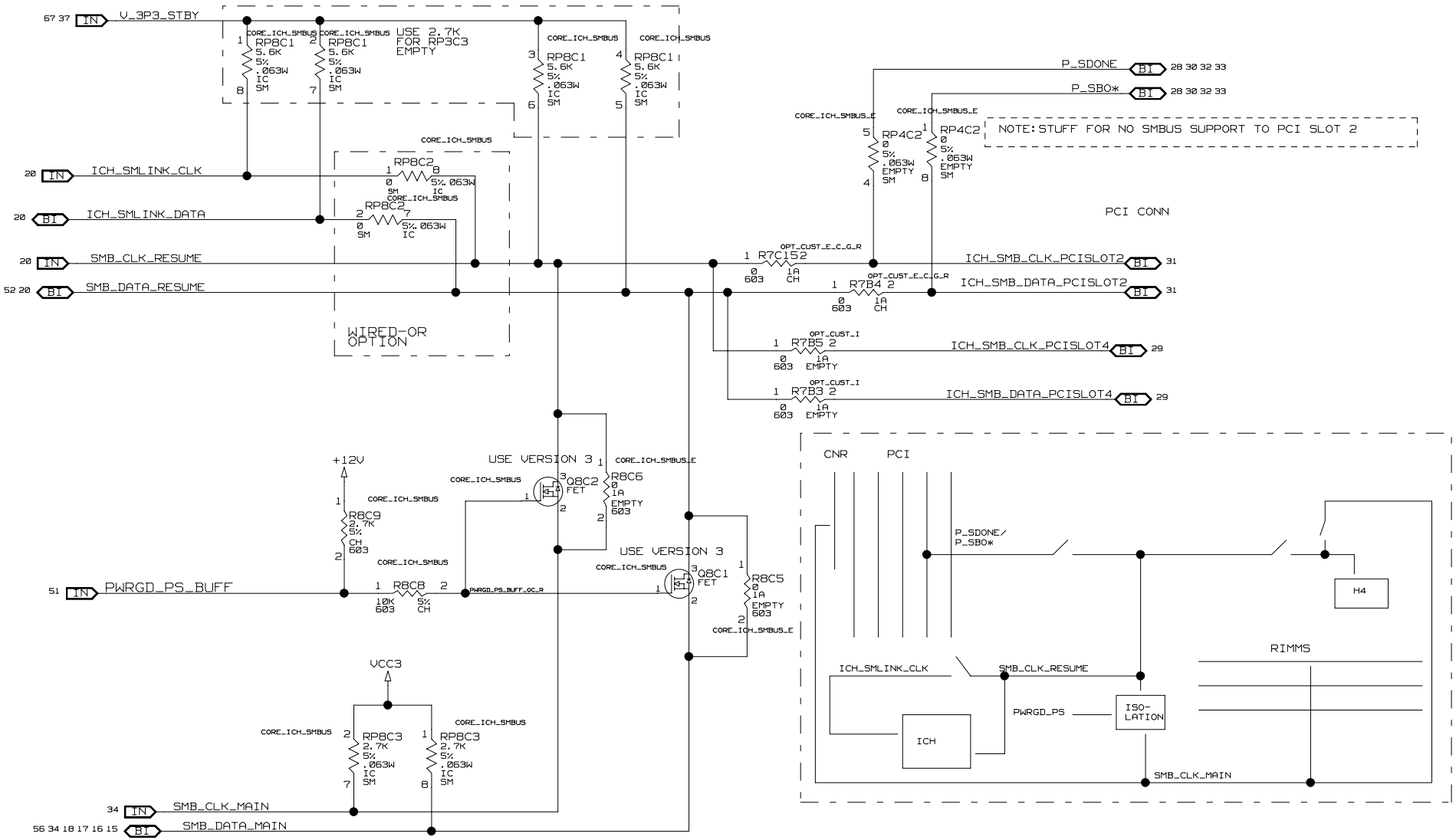
PAGE TITLE: FAN CONTROL		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:08 2001	SHEET: 57

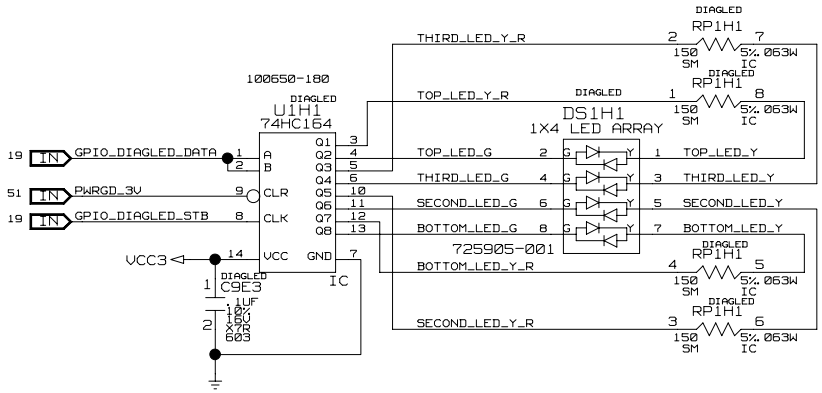


SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: SMBUS ISOLATION	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:36 2001
	SHEET: 58

[PAGE_TITLE=SMBUS_ISOLATION]

DRAWING

DIAGNOSTIC LEDS



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DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: DIAGNOSTIC LEDS		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:37 2001	SHEET: 59

CR-60

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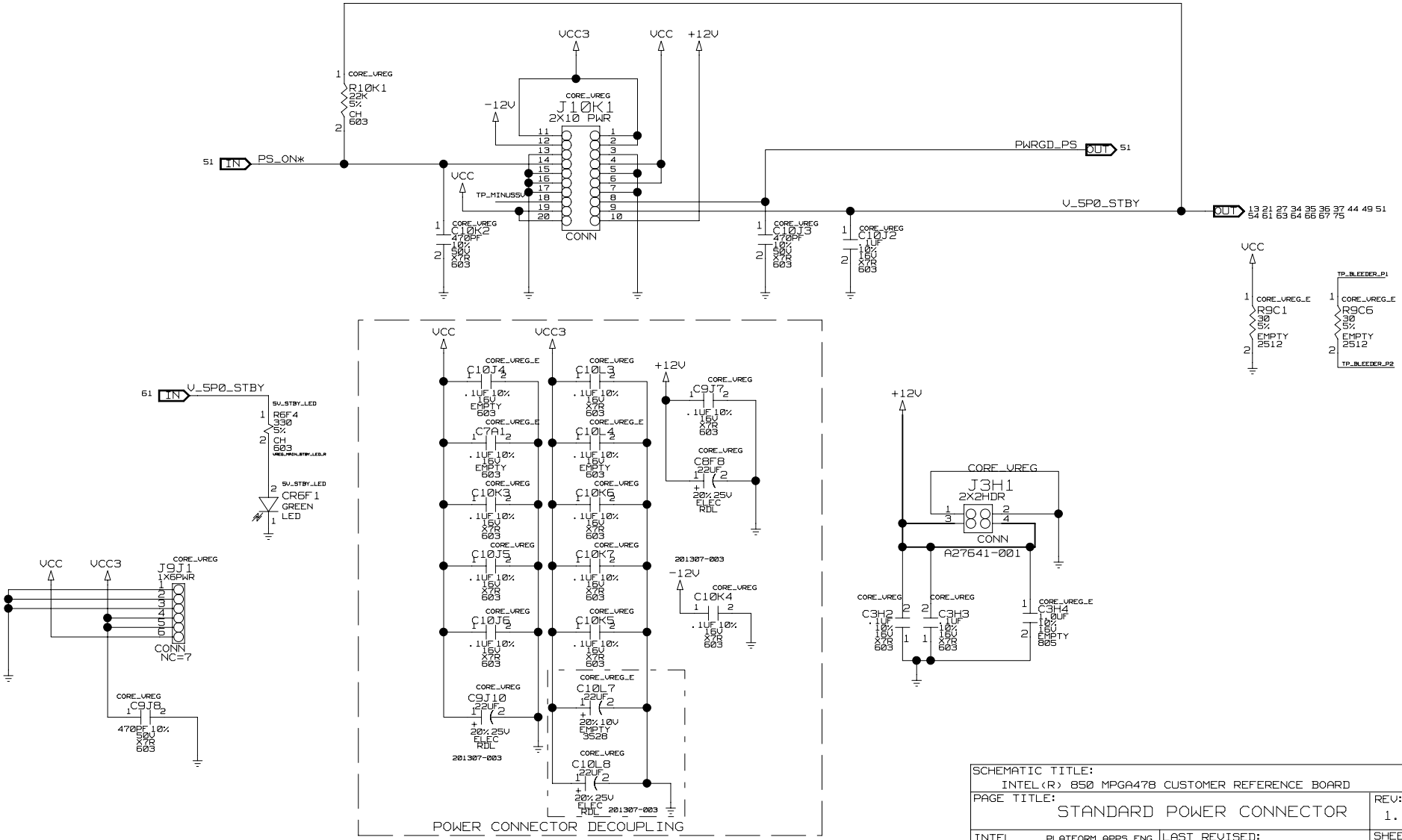
SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE:		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Mon Jul 09 17:38:40 2001	SHEET: 60

DRAWING

LAST USED
C0419V
CR0401V
J0402V
R0402V

ROOM=VREG_PWR_CONN
BOM=VREG_PWR_CONN
UNLESS OTHERWISE SPECIFIED



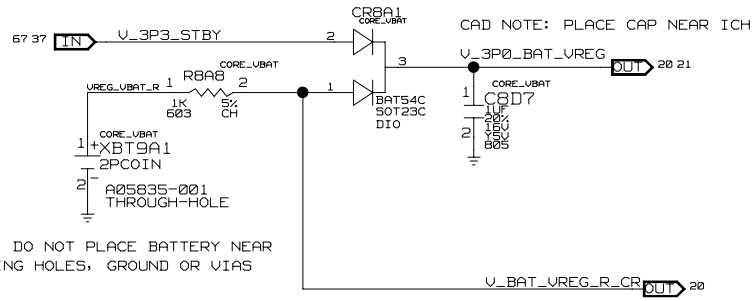
[SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2]
[MODULE=VREG] [MOD_PAGE=PAGE4] [MOD_REV=REV0_2D] [PAGE_TITLE=STANDARD_POWER_SUPPLY_CONNECTOR]
[LAST_MAKEGOLD: 7/29/99 10:10:19am]

DRAWING

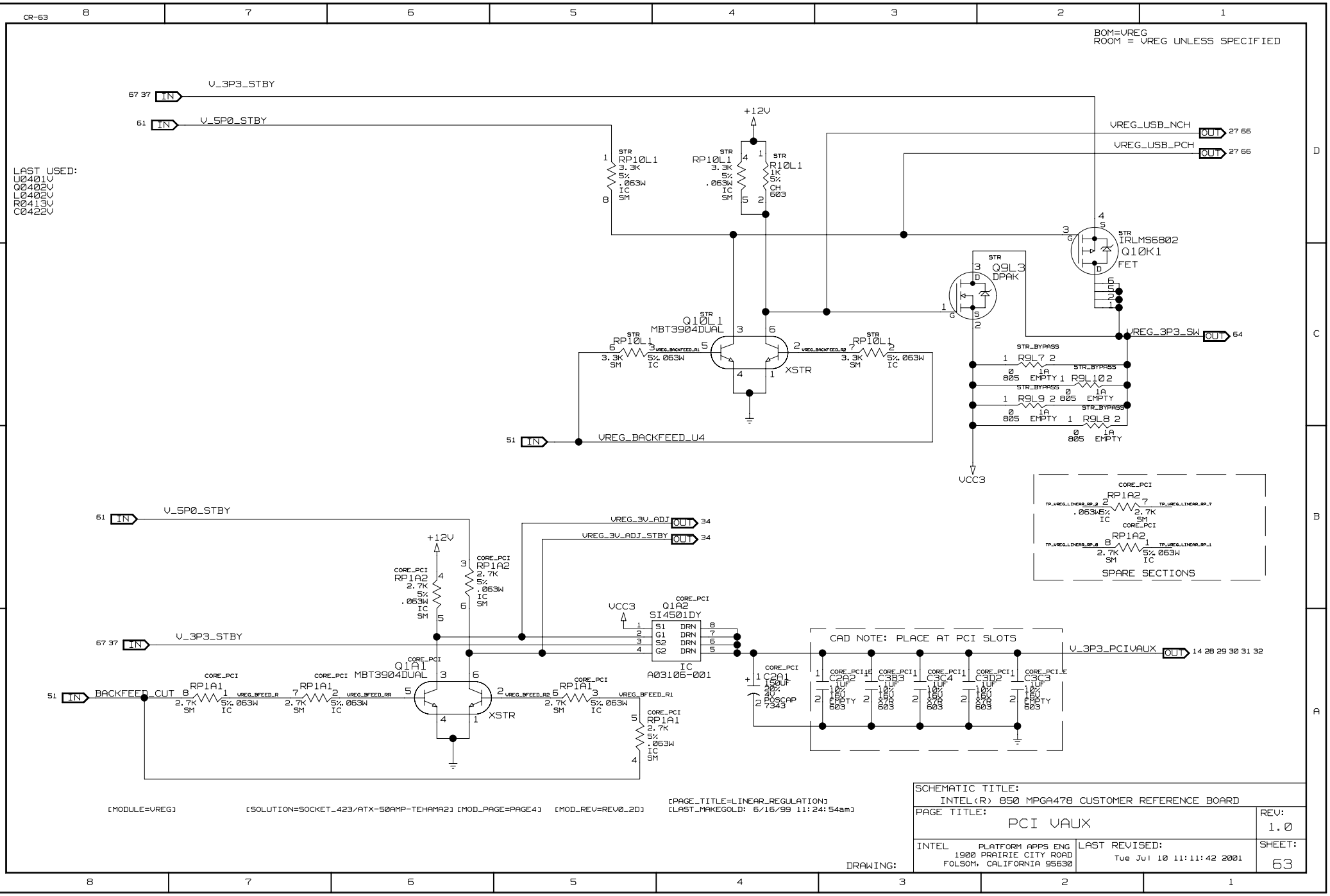
SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: STANDARD POWER CONNECTOR		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:39 2001	SHEET: 61

LAST USED:
BT0801V
C0801V
CR0801V
R0801V

BOM = VREG_CORE
ROOM = VREG_VBAT
UNLESS OTHERWISE SPECIFIED

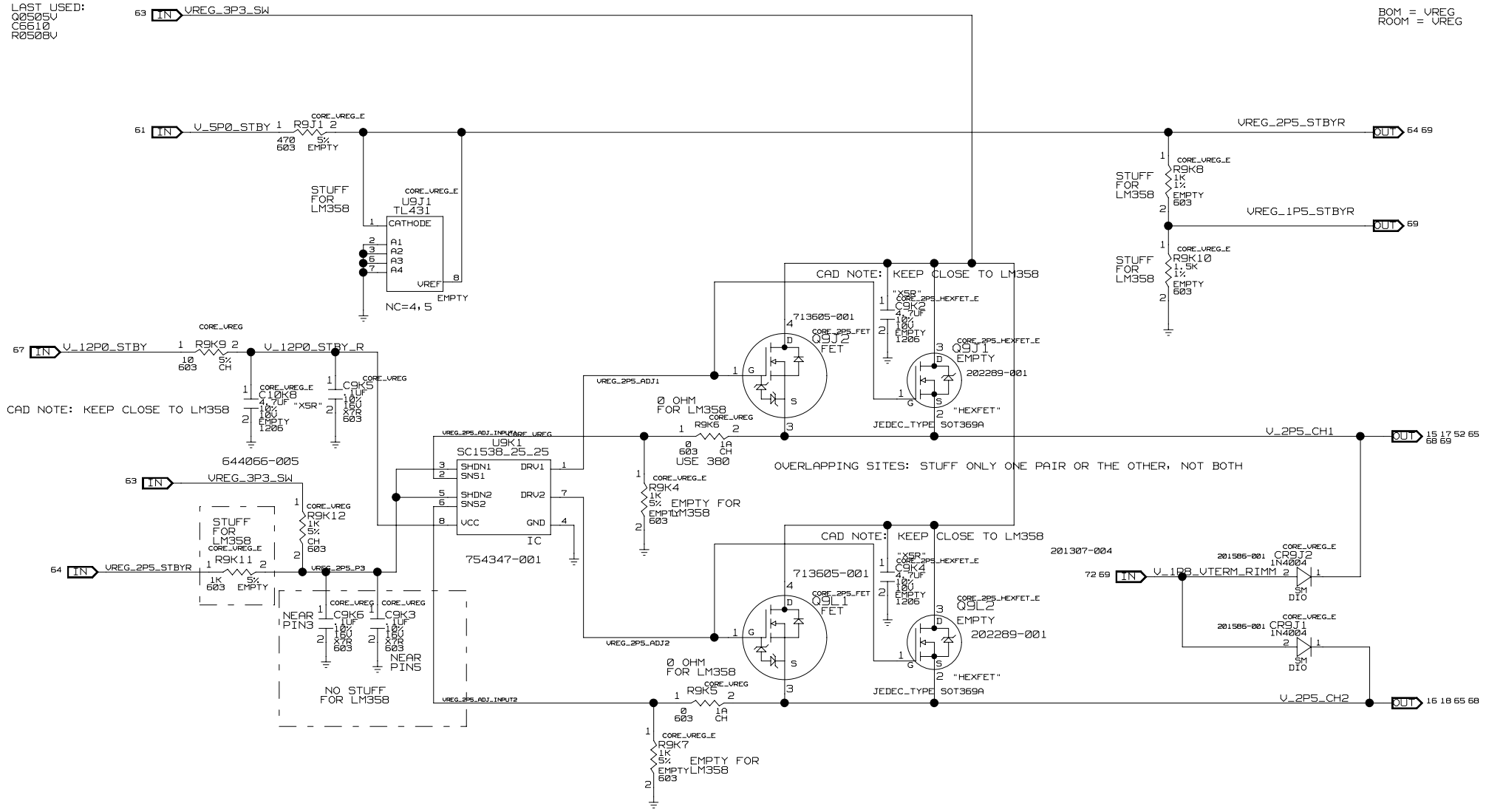


SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: BATTERY	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:40 2001
	SHEET: 62


CR-63
BOM=VREG
ROOM = VREG UNLESS SPECIFIED
LAST USED:
U0401V
Q0402V
L0402V
R0413V
C0422V
V_3P3_STBY
V_5P0_STBY
+12V
VREG_USB_NCH
VREG_USB_PCH
RP10L1
R10L1
IRLMS6802
Q10K1
FET
Q9L3
DPAK
Q10L1
MBT3904DUAL
XSTR
VREG_3P3_SW
R9L7
R9L10
R9L9
R9L8
VREG_BACKFEED_U4
VCC3
RP1A2
SPARE SECTIONS
VREG_3V_ADJ
VREG_3V_ADJ_STBY
Q1A2
SI4501DY
A03106-001
CAD NOTE: PLACE AT PCI SLOTS
V_3P3_PCIVAUX
BACKFEED_CUT
RP1A1
Q1A1
MBT3904DUAL
C2A1
C2A2
C3B3
C3C4
C3D2
C3C3
[MODULE=VREG]
[SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2] [MOD_PAGE=PAGE4] [MOD_REV=REV0_2D]
[PAGE_TITLE=LINEAR_REGULATION]
[LAST_MAKEGOLD: 6/16/99 11:24:54am]
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
PCI VAUX
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:42 2001
SHEET:
63
DRAWING:

LAST USED:
Q0505V
C6610
R0508V

BOM = VREG
ROOM = VREG

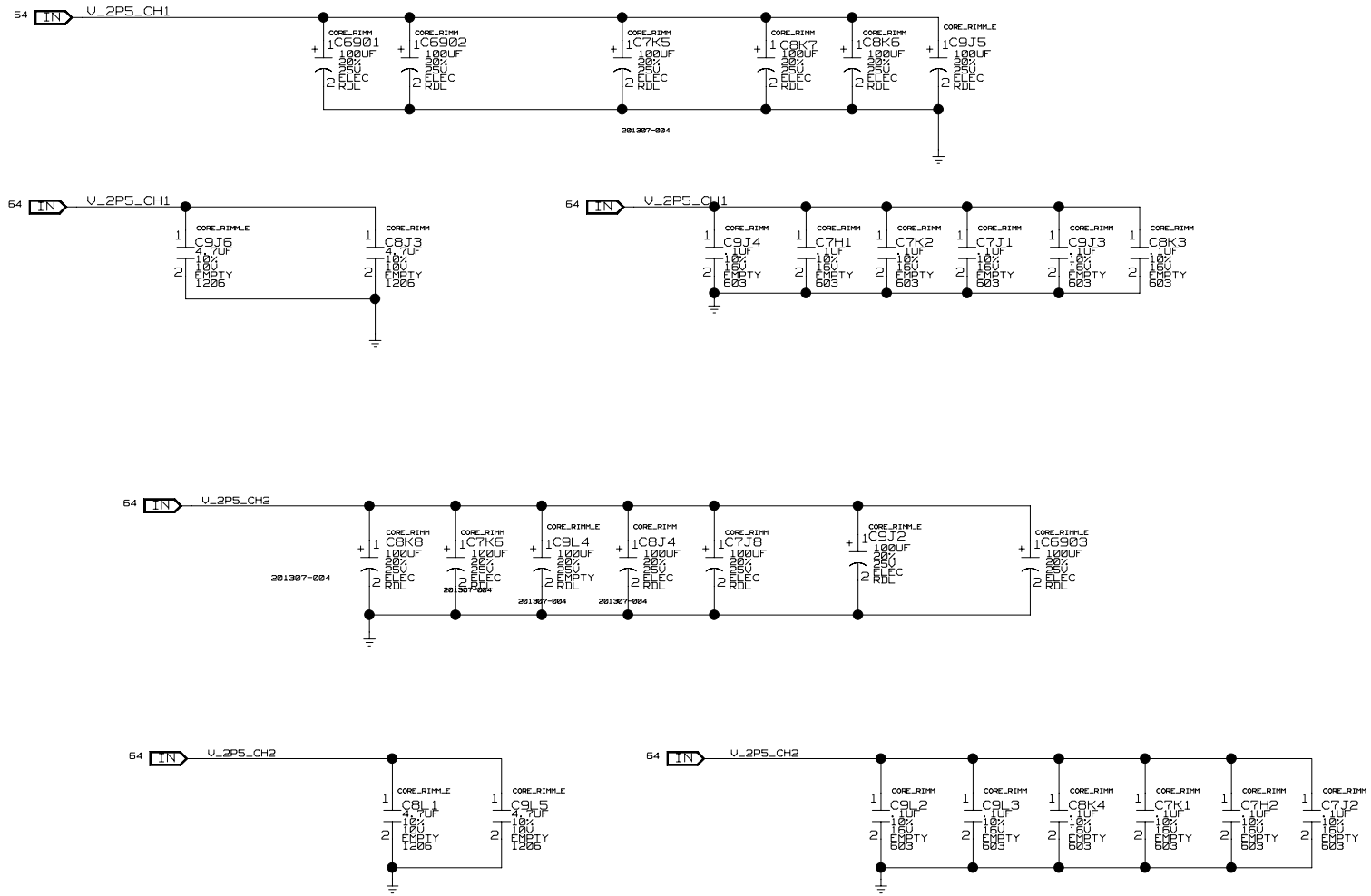


SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: 2.5V RIMM	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:44 2001
	SHEET: 64

[LAST_MAKEGOLD: 6/16/99 11:25:00am]
[PAGE_TITLE=LINEAR_REGULATION]
[MOD_REV=REV0_2D]

DRAWING:

[MODULE=VREG] [SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2] [MOD_PAGE=PAGE5]



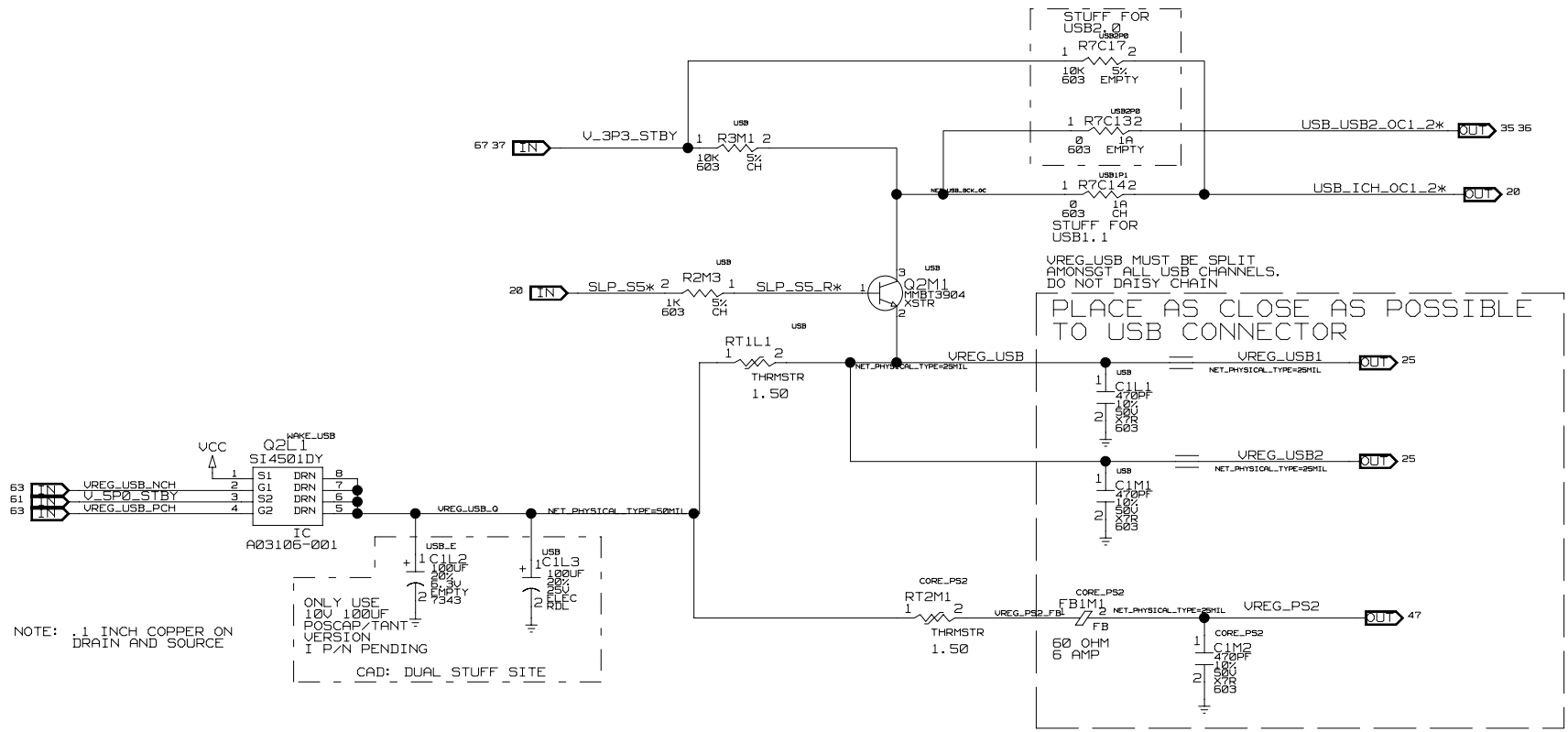
[PAGE_TITLE=BLANK]

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: RAMBUS 2.5V DECOUPLING	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:45 2001
DRAWING	SHEET: 65

[DONOR_REV=0.07/page35]
[DONOR_PROJ=wtvv_pdt]

LAST_USED
C0707R
CR0701R
Q0703R
R0712R
TH0703R
FB0704R

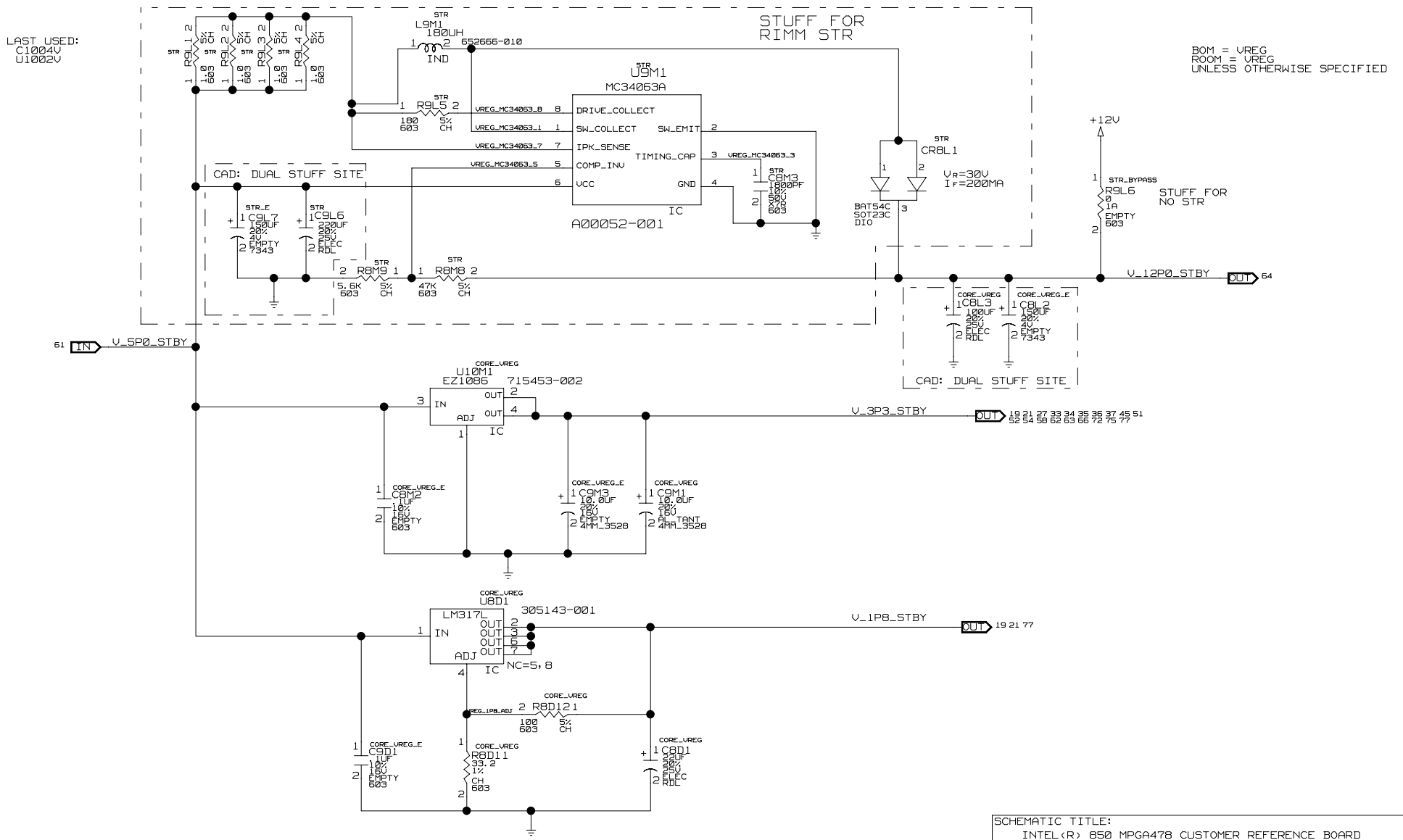
BOM=USB_PS2
ROOM= USB_OUT
UNLESS OTHERWISE SPECIFIED



SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: WAKE ON USB & PS2	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:46 2001 / SHEET: 66

DRAWING

[LAST_MAKEGOLD: 6/16/99 11:25:21am] [PAGE_TITLE=WAKE_ON_USB_&_PS/2]
[MODULE=VREG] [SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2] [MOD_PAGE=PAGE9] [MOD_REV=REV0_2D]



SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD

PAGE TITLE: 12V/3.3V/1.8V STANDBY

REV: 1.0

INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

LAST REVISED: Tue Jul 10 11:11:48 2001

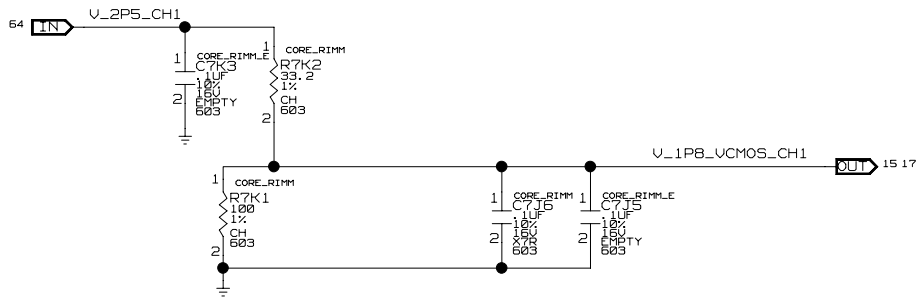
SHEET: 67

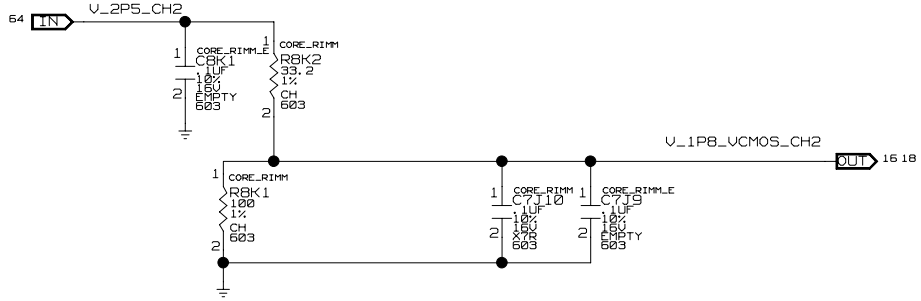
DRAWING

[LAST_MAKEGOLD: 6/16/99 11:24:18am]
[PAGE_TITLE=12V,_3.3V,_1.8V_STANDBY]
[MODULE=VREG] [SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2] [MOD_PAGE=PAGE10] [MOD_REV=REV0_2D]

LAST USED:
R1107V
C1107V

BOM=VREG_RIMM
ROOM = VREG_RIMM UNLESS SPECIFIED

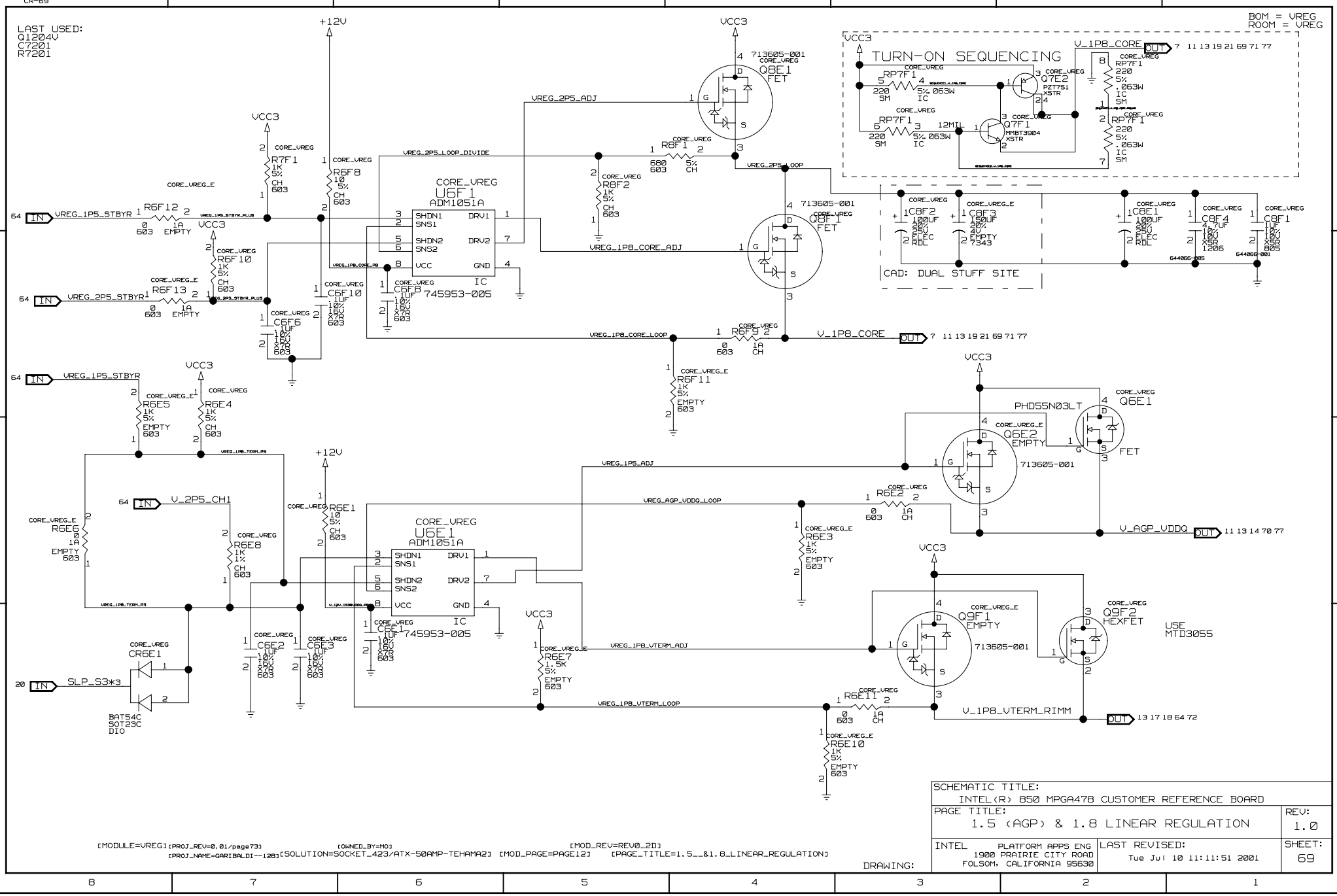


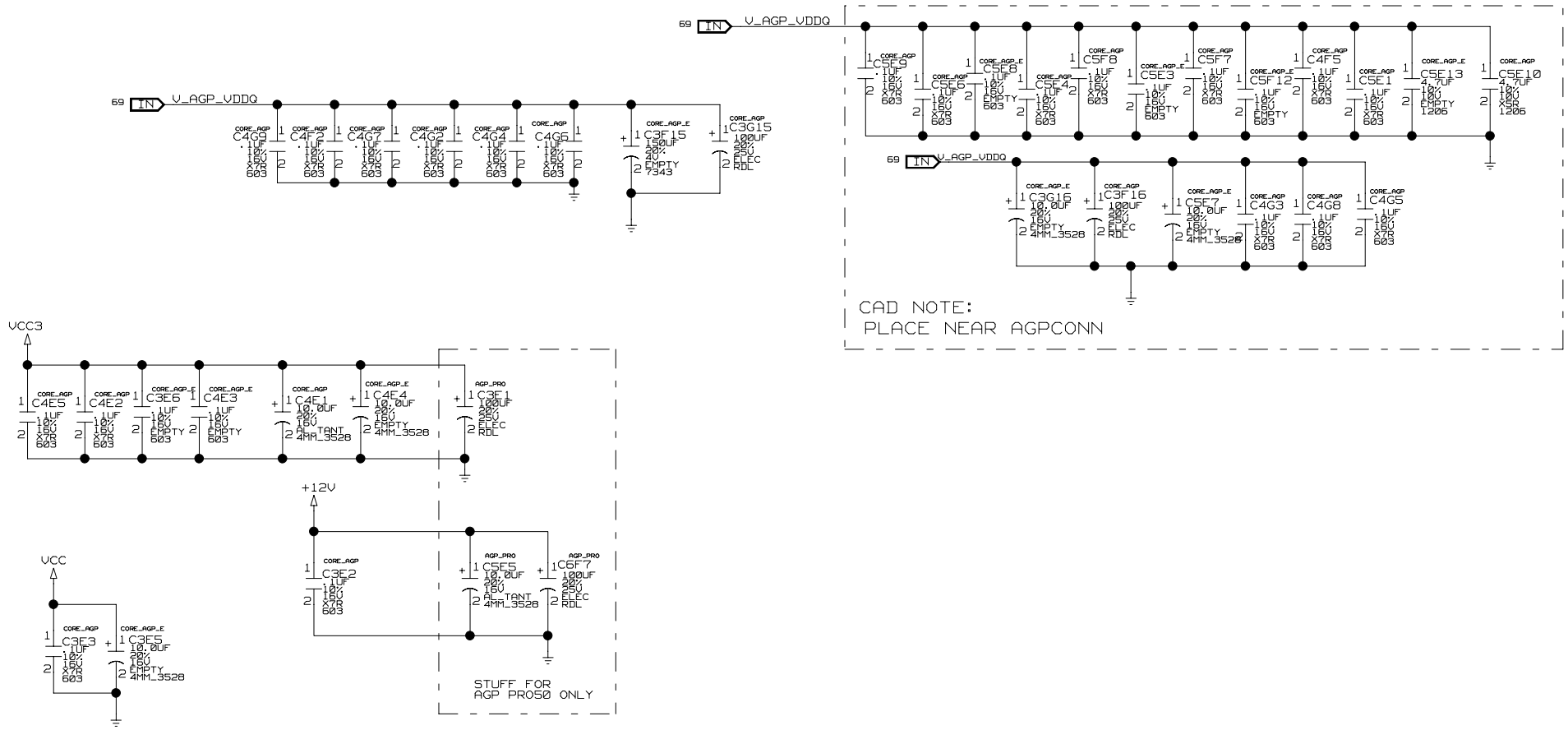


SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: VREG_1P8_VCMOS_RIMM	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:49 2001
	SHEET: 68

[LAST_MAKEGOLD: 6/16/99 11:24:21am]
[PAGE_TITLE=VREG_1P8_RIMM]
[MODULE=VREG] [SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2] [MOD_PAGE=PAGE11] [MOD_REV=REV0_2D]

DRAWING


CR-69
LAST USED:
Q1204V
C7201
R7201
BOM = VREG
ROOM = VREG
TURN-ON SEQUENCING
CAD: DUAL STUFF SITE
CORE_VREG
U6F1
ADM1051A
745953-005
U6E1
ADM1051A
745953-005
713605-001
Q8E1
FET
Q8F1
FET
PHD55N03LT
Q6E1
FET
Q6E2
EMPTY
Q9F1
EMPTY
Q9F2
HEXFET
USE
MTD3055
V_1P8_CORE
V_AGP_VDDQ
V_1P8_VTERM_RIMM
VREG_1P5_STBYR
VREG_2P5_STBYR
V_2P5_CH1
SLP_S3*3
BAT54C
SOT23C
DIO
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
1.5 (AGP) & 1.8 LINEAR REGULATION
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:51 2001
SHEET:
69
DRAWING:
[MODULE=VREG] [PROJ_REV=0.01/page73] [OWNED_BY=MO] [MOD_REV=REV0_2D]
[PROJ_NAME=GARIBALDI--128] [SOLUTION=SOCKET_423/ATX-50AMP-TEHAMA2] [MOD_PAGE=PAGE12] [PAGE_TITLE=1.5__&1.8_LINEAR_REGULATION]

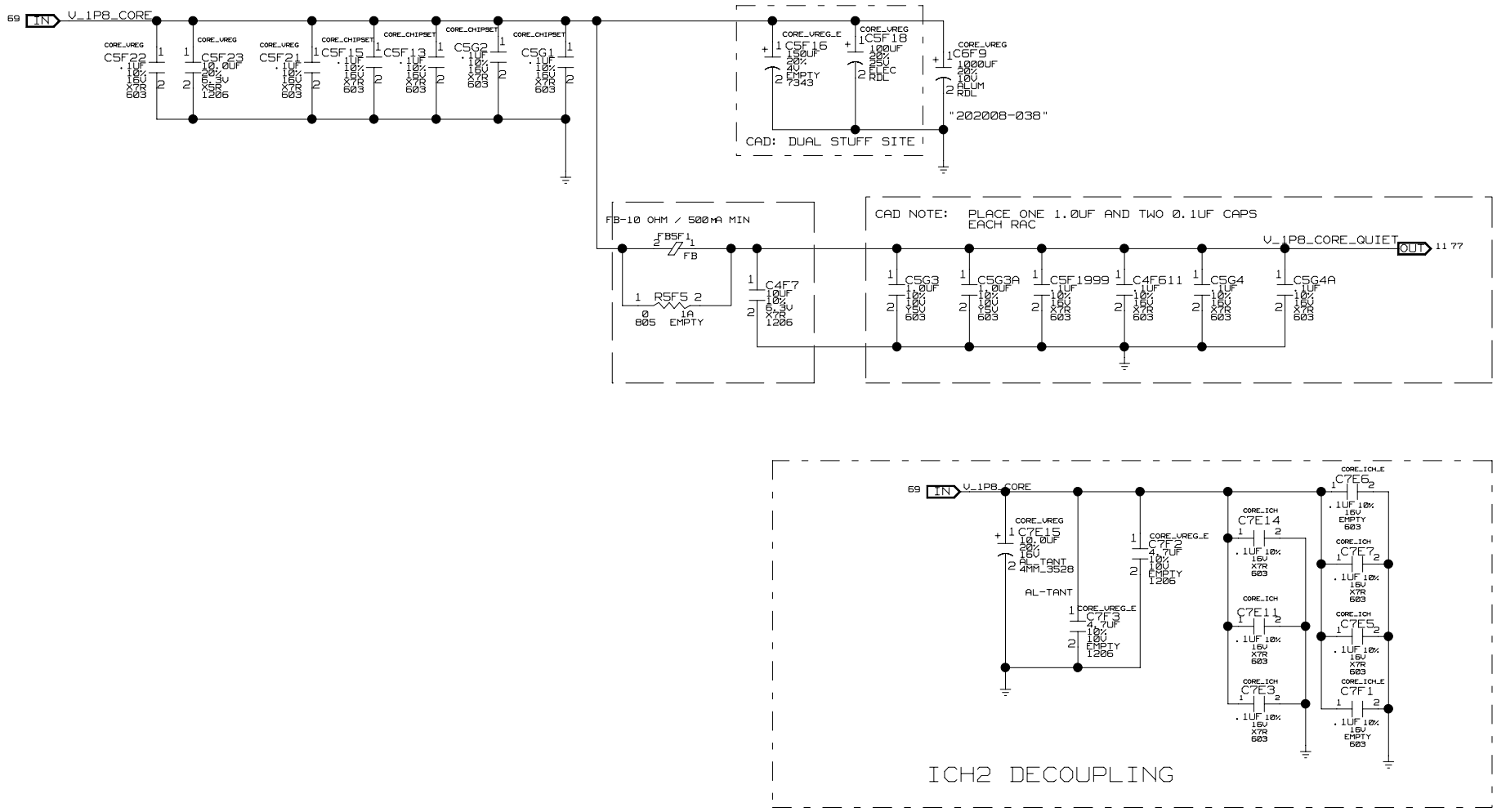


BOM NOTE:
4MM_3528 SUPPORTS
SM AL, TANT, AND CERAMIC

[PAGE_TITLE=BLANK]

DRAWING

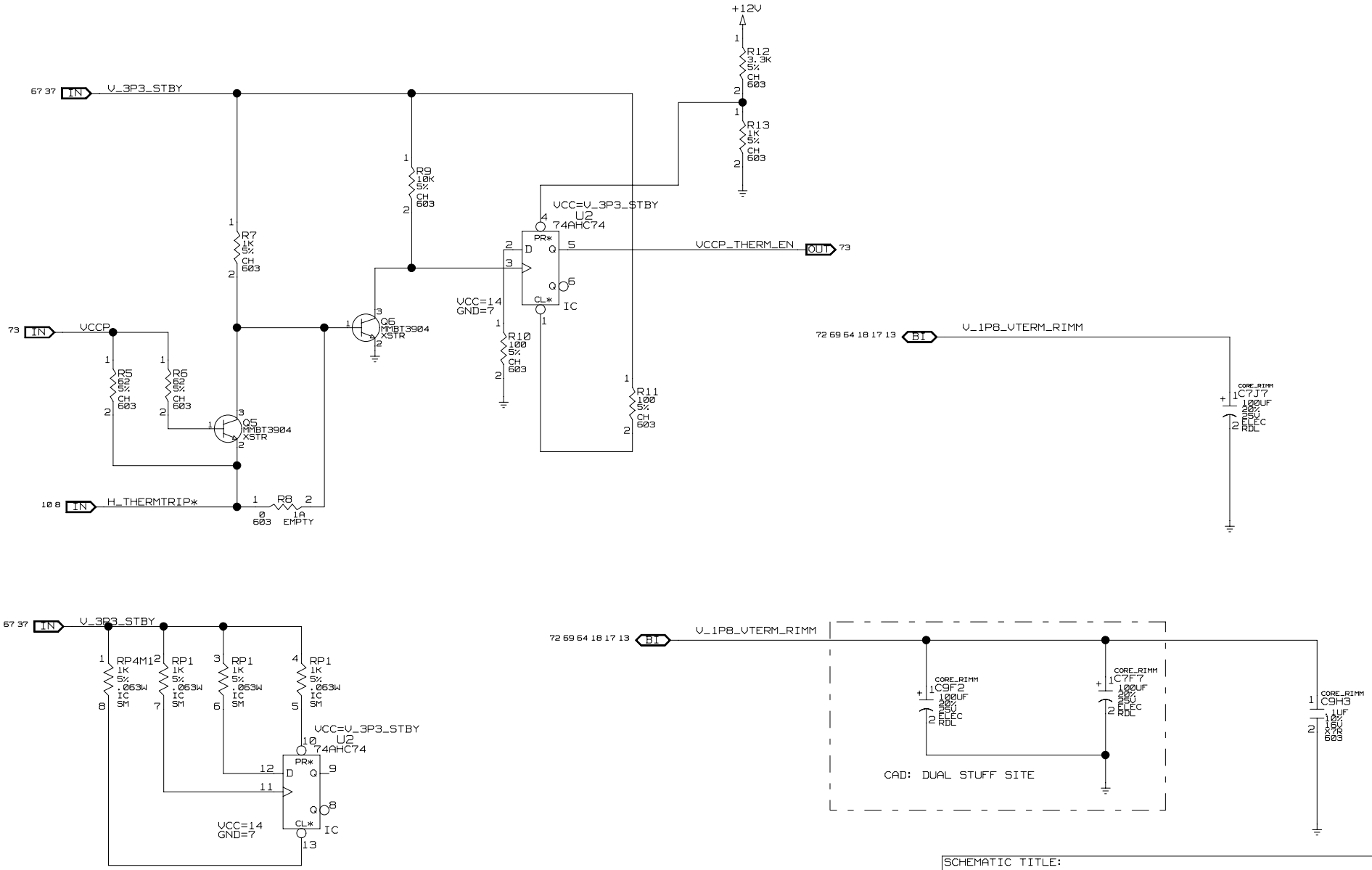
SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: AGP DECOUPLING	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:52 2001
	SHEET: 70



[PAGE_TITLE=BLANK]

DRAWING

SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: V_1P8_CORE DECOUPLING		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:53 2001	SHEET: 71



SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD

PAGE TITLE:
1.8V VTERM DECOUP/THERMTRIP SEQUENCING

REV: 1.0

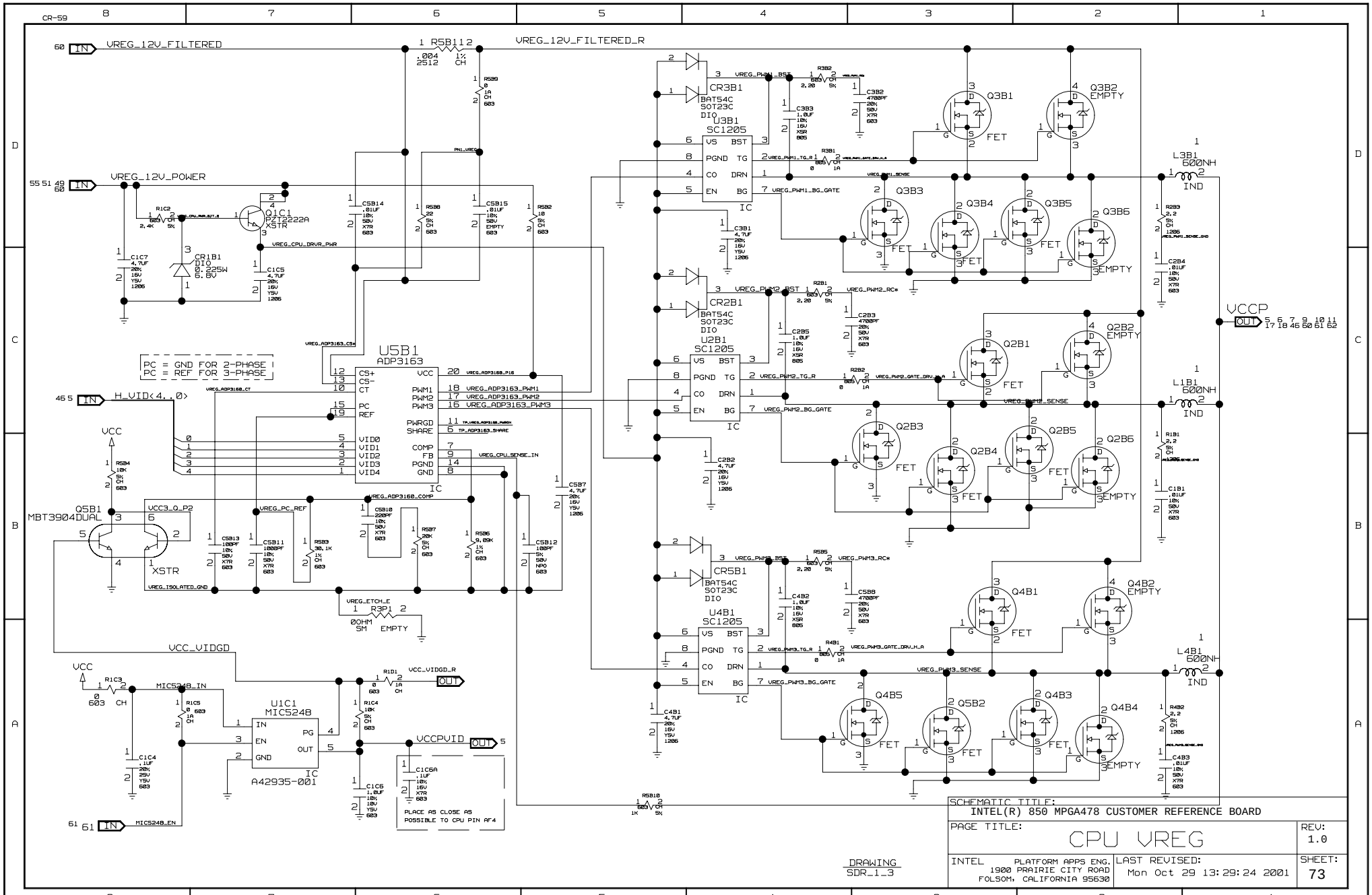
INTEL PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

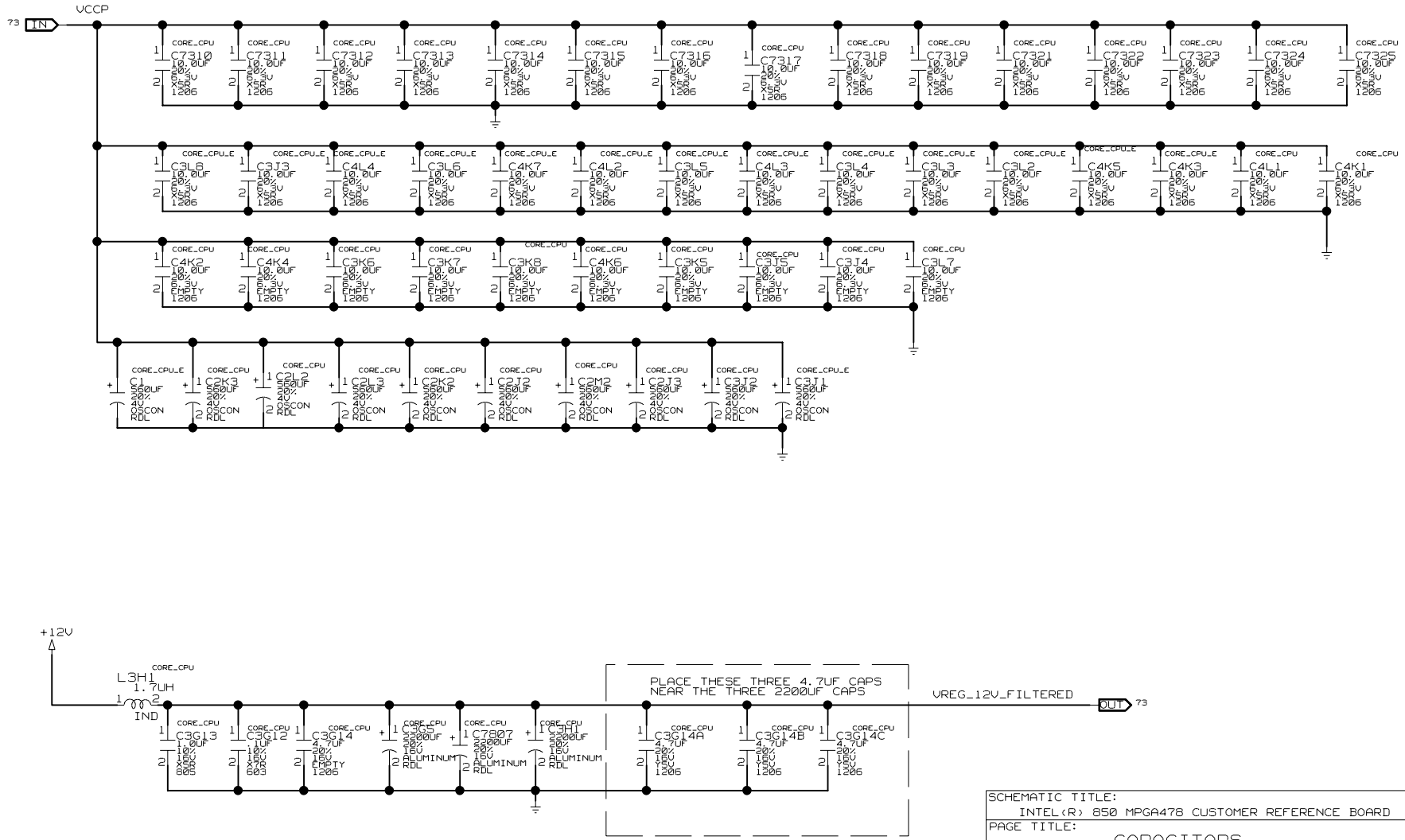
LAST REVISED:
Tue Jul 10 11:10:10 2001

SHEET: 72

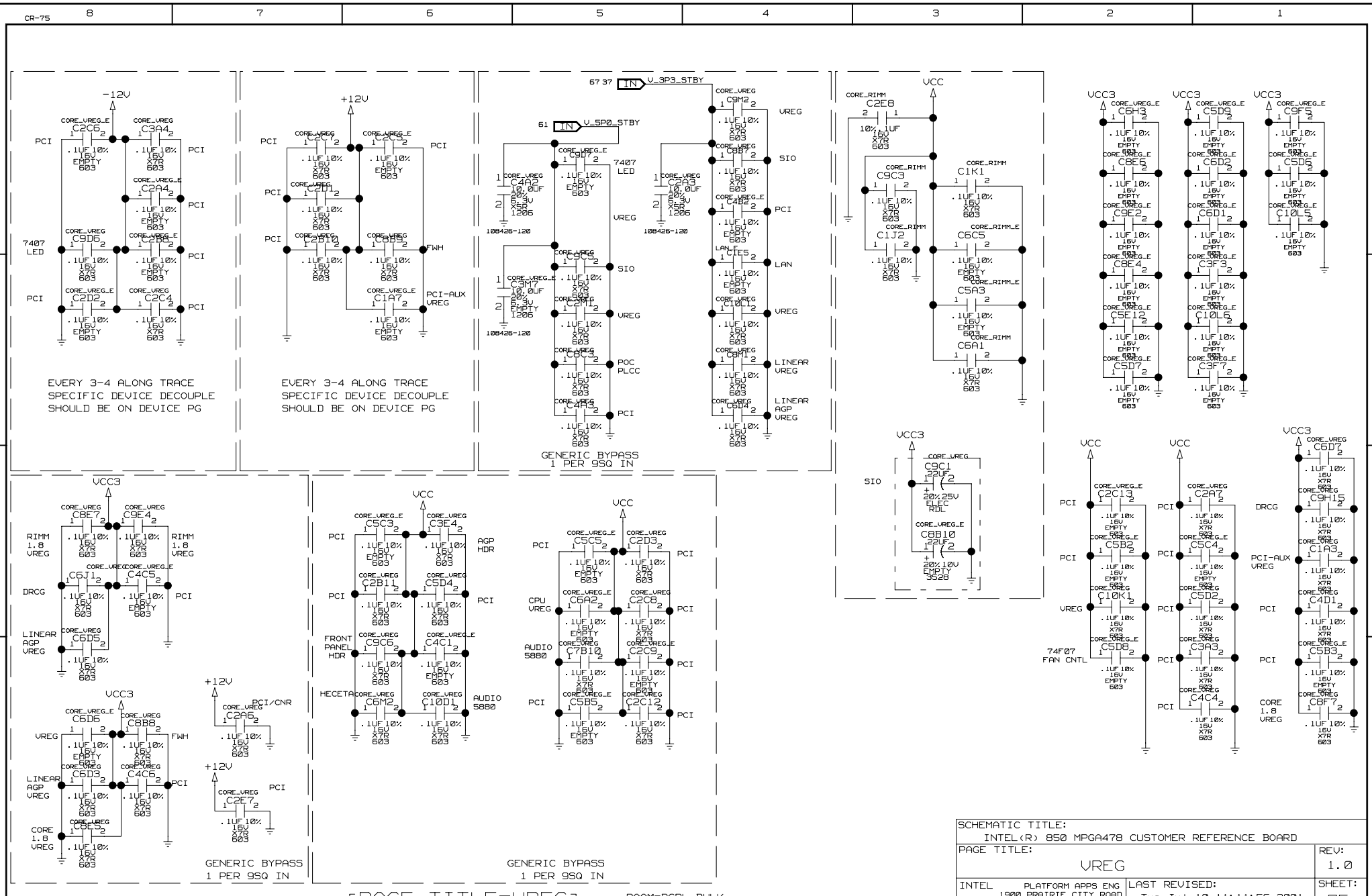
[PAGE_TITLE=BLANK]

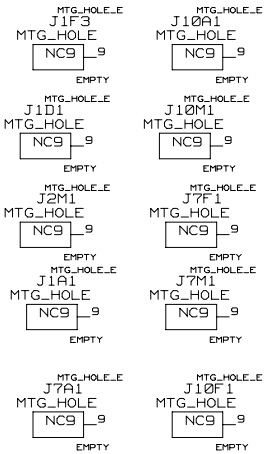
DRAWING


CR-59
VREG_12V_FILTERED
VREG_12V_FILTERED_R
R5B112
.004
2512
1%
CH
VREG_12V_POWER
Q1C1
PZT2222A
XSTR
R1C2
2.4K
C1C7
4.7UF
20%
16V
Y5V
1206
CR1B1
DIO
0.225W
5.6V
C1C5
4.7UF
20%
16V
Y5V
1206
C5B14
.01UF
10%
50V
X7R
603
R5B8
22
5%
CH
603
C5B15
.01UF
10%
50V
EMPTY
603
R5B2
10
5%
CH
603
VREG_CPU_DRVR_PWR
PC = GND FOR 2-PHASE
PC = REF FOR 3-PHASE
H_VID<4..0>
U5B1
ADP3163
CS+
CS-
CT
PC
REF
VID0
VID1
VID2
VID3
VID4
VCC
PWM1
PWM2
PWM3
PWRGD
SHARE
COMP
FB
PGND
GND
IC
VREG_ADP3163_PWM1
VREG_ADP3163_PWM2
VREG_ADP3163_PWM3
VREG_CPU_SENSE_IN
VREG_ADP3160_COMP
VREG_PC_REF
VREG_ISOLATED_GND
Q5B1
MBT3904DUAL
XSTR
VCC3_Q_P2
R5B4
10K
5%
CH
603
C5B13
100PF
10%
50V
X7R
603
C5B11
1000PF
10%
50V
X7R
603
R5B3
30.1K
1%
CH
603
C5B10
.220PF
10%
50V
X7R
603
R5B7
20K
5%
CH
603
R5B6
9.09K
1%
CH
603
C5B12
100PF
5%
50V
NPO
603
C5B7
4.7UF
20%
16V
Y5V
1206
VREG_ETCH_E
R3P1
0OHM
SM
EMPTY
VCC_VIDGD
VCC
R1C3
0
603
CH
MIC524B_IN
R1C5
0
603
1A
CH
U1C1
MIC524B
IN
EN
GND
PG
OUT
IC
A42935-001
C1C4
.1UF
20%
25V
Y5V
603
R1D1
0
603
1A
CH
VCC_VIDGD_R
R1C4
10K
5%
CH
603
VCCPVID
C1C6
1.0UF
10%
16V
Y5V
603
C1C6A
.1UF
10%
16V
X7R
603
PLACE AS CLOSE AS
POSSIBLE TO CPU PIN AF4
MIC524B_EN
R5B10
1K
5%
CR3B1
BAT54C
SOT23C
DIO
U3B1
SC1205
VS
BST
PGND
TG
CO
DRN
EN
BG
IC
VREG_PWM1_BST
VREG_PWM1_TG_R
VREG_PWM1_BG_GATE
VREG_PWM1_SENSE
R3B2
2.20
5%
C3B2
4700PF
20%
50V
X7R
603
C3B3
1.0UF
10%
16V
X5R
805
R3B1
0
1A
C3B1
4.7UF
20%
16V
Y5V
1206
CR2B1
BAT54C
SOT23C
DIO
U2B1
SC1205
VREG_PWM2_BST
VREG_PWM2_TG_R
VREG_PWM2_BG_GATE
VREG_PWM2_SENSE
R2B1
2.20
5%
VREG_PWM2_RC*
C2B3
4700PF
20%
50V
X7R
603
C2B5
1.0UF
10%
16V
X5R
805
R2B2
0
1A
C2B2
4.7UF
20%
16V
Y5V
1206
CR5B1
BAT54C
SOT23C
DIO
U4B1
SC1205
VREG_PWM3_BST
VREG_PWM3_TG_R
VREG_PWM3_BG_GATE
VREG_PWM3_SENSE
R5B5
2.20
5%
VREG_PWM3_RC*
C5B8
4700PF
20%
50V
X7R
603
C4B2
1.0UF
10%
16V
X5R
805
R4B1
0
1A
VREG_PWM3_GATE_DRV_H_A
C4B1
4.7UF
20%
16V
Y5V
1206
Q3B1
FET
Q3B2
EMPTY
Q3B3
FET
Q3B4
FET
Q3B5
FET
Q3B6
EMPTY
Q2B1
FET
Q2B2
EMPTY
Q2B3
FET
Q2B4
FET
Q2B5
FET
Q2B6
EMPTY
Q4B1
FET
Q4B2
EMPTY
Q4B5
FET
Q5B2
FET
Q4B3
FET
Q4B4
EMPTY
L3B1
600NH
IND
L1B1
600NH
IND
L4B1
600NH
IND
R2B3
2.2
5%
CH
1206
C2B4
.01UF
10%
50V
X7R
603
R1B1
2.2
5%
CH
C1B1
.01UF
10%
50V
X7R
603
R4B2
2.2
5%
CH
1206
C4B3
.01UF
10%
50V
X7R
603
VCCP
OUT
DRAWING
SDR_1_3
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
CPU VREG
REV:
1.0
INTEL
PLATFORM APPS ENG.
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Mon Oct 29 13:29:24 2001
SHEET:
73

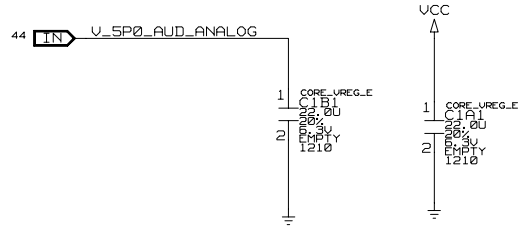


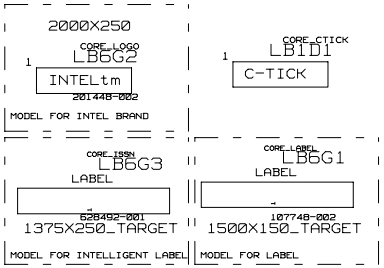
SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD	
PAGE TITLE: CAPACITORS	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Wed Jul 11 08:07:09 2001
DRAWING:	SHEET: 74

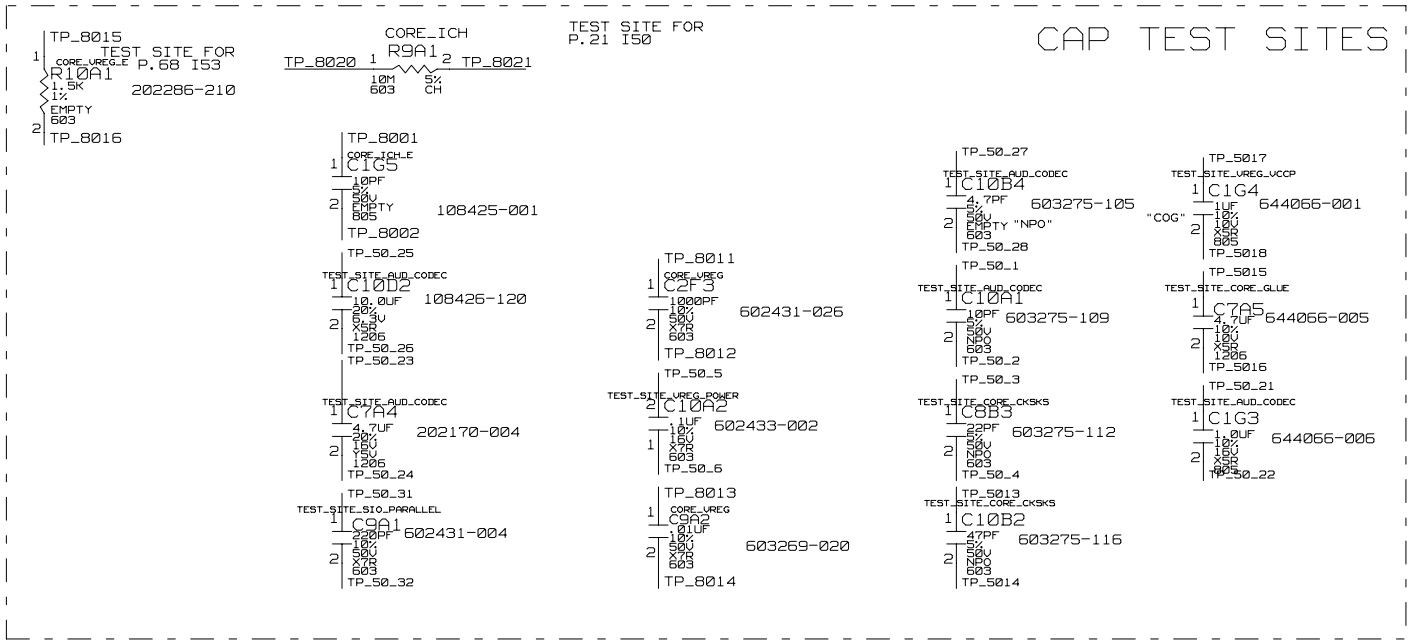

CR-75
-12V
+12V
V_3P3_STBY
V_5P0_STBY
7407 LED
PCI
FWH
PCI-AUX VREG
EVERY 3-4 ALONG TRACE
SPECIFIC DEVICE DECOUPLE
SHOULD BE ON DEVICE PG
GENERIC BYPASS
1 PER 9SQ IN
VCC
VCC3
SIO
LAN
LINEAR VREG
LINEAR AGP VREG
RIMM 1.8 VREG
DRCG
CORE 1.8 VREG
74F07 FAN CNTL
AGP HDR
FRONT PANEL HDR
HECETA
AUDIO 5880
CPU VREG
PCI/CNR
[PAGE_TITLE=VREG]
ROOM=DCPL_BULK
BOM=VREG_DCPL_BULK
DRAWING
SCHEMATIC TITLE:
INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD
PAGE TITLE:
VREG
REV:
1.0
INTEL
PLATFORM APPS ENG
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
LAST REVISED:
Tue Jul 10 11:11:56 2001
SHEET:
75



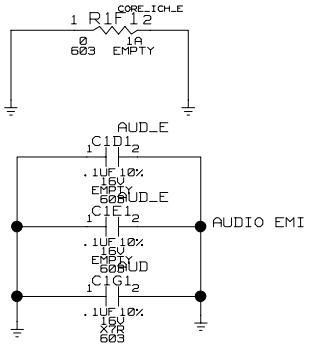
DESIGN NOTE: PIN 9 IS A NO-CONNECT







CHANGE GND LOCATION
FOR BACKPANEL ESD



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PAGE TITLE: FORCE_ON, TDR	REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:11:59 2001 / SHEET: 76

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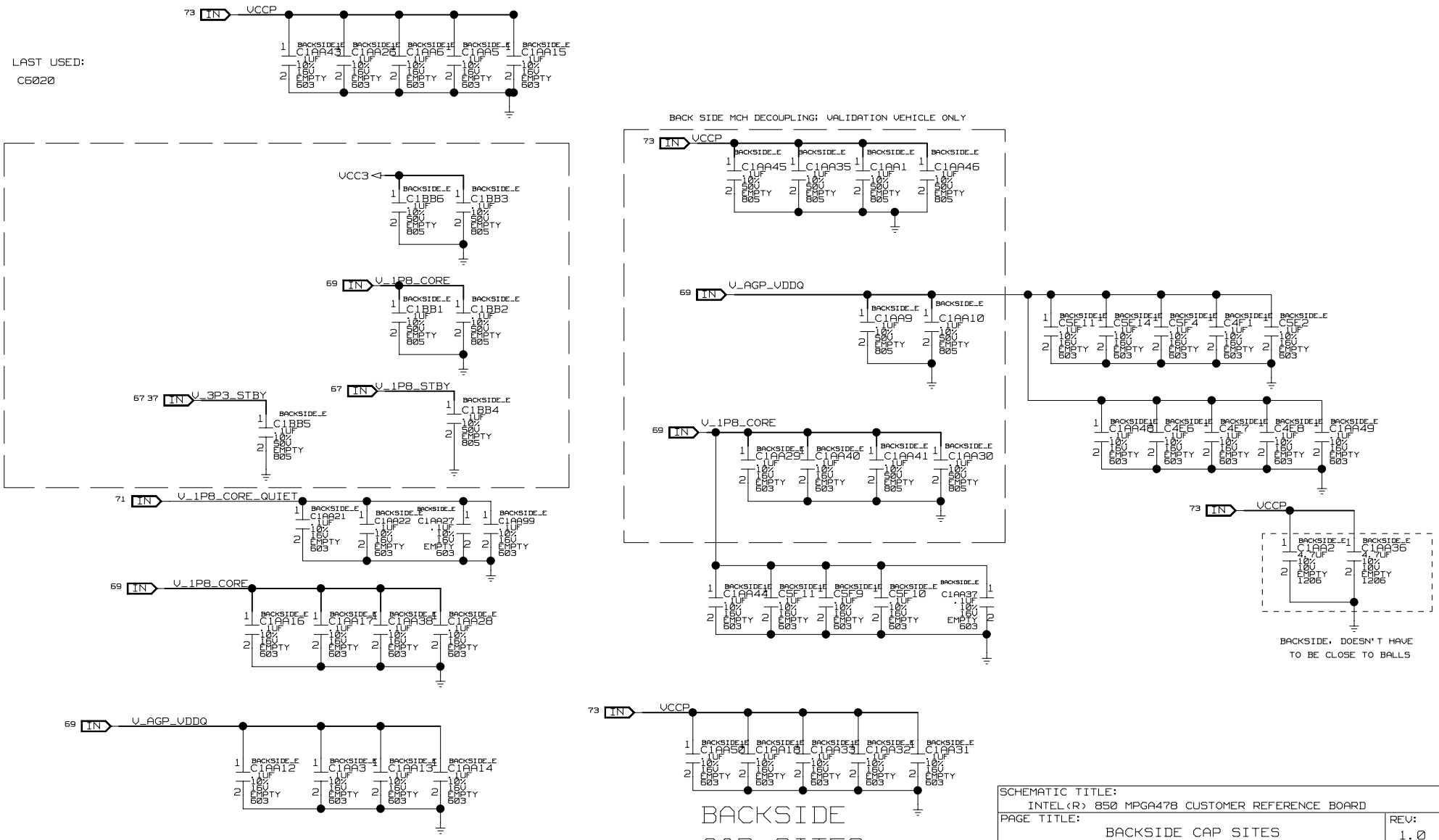
DRAWING

LAST USED:
C6020



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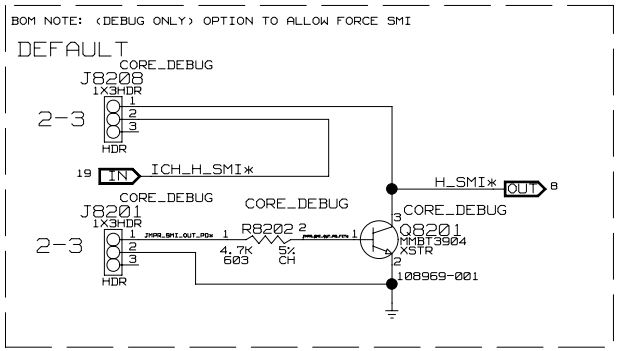
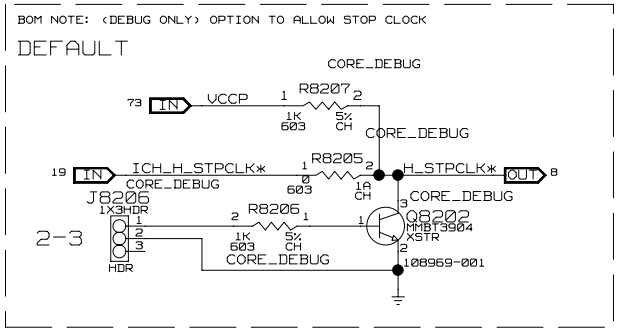
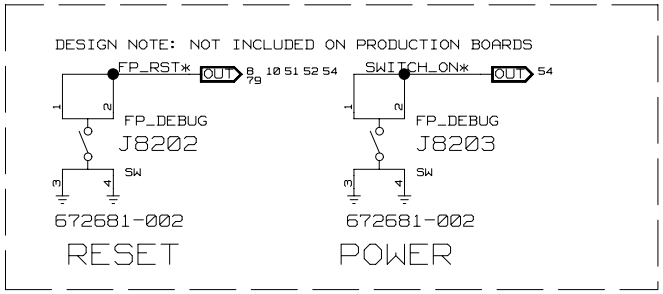
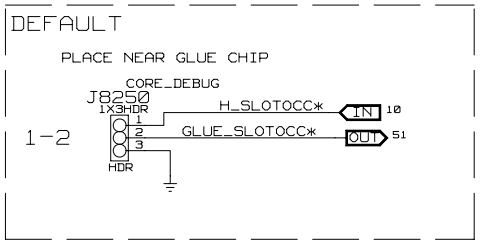
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:12:00 2001	SHEET: 77

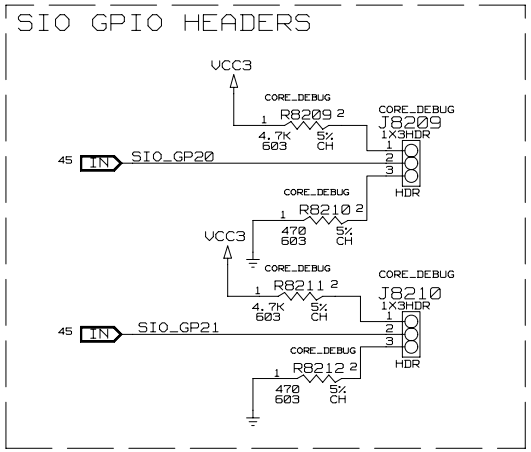
SWITCHES AND MISC DEBUG











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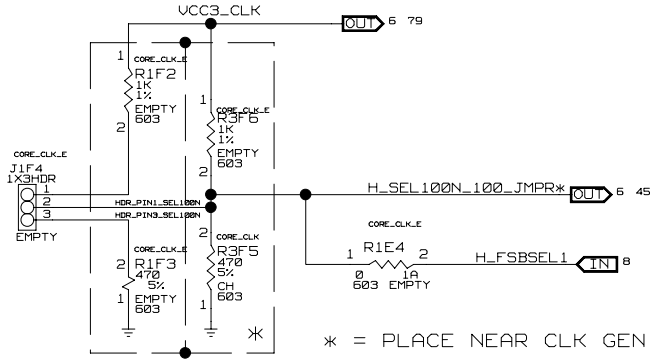

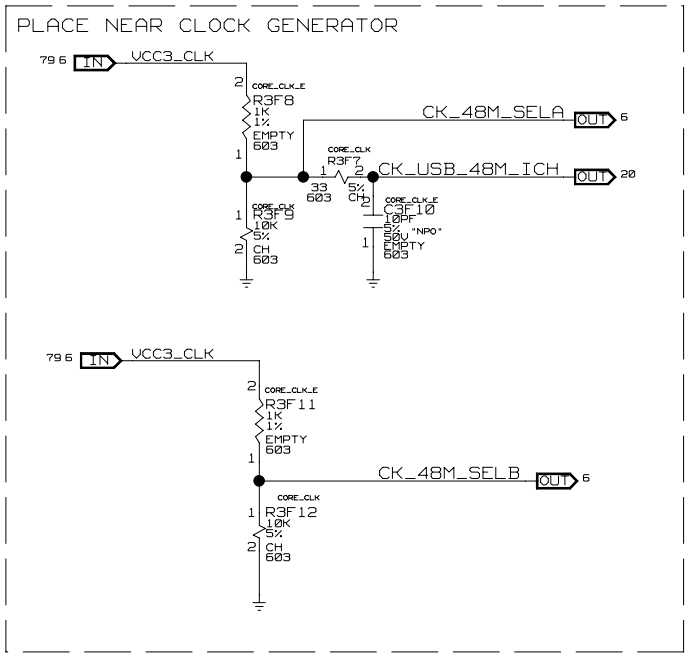

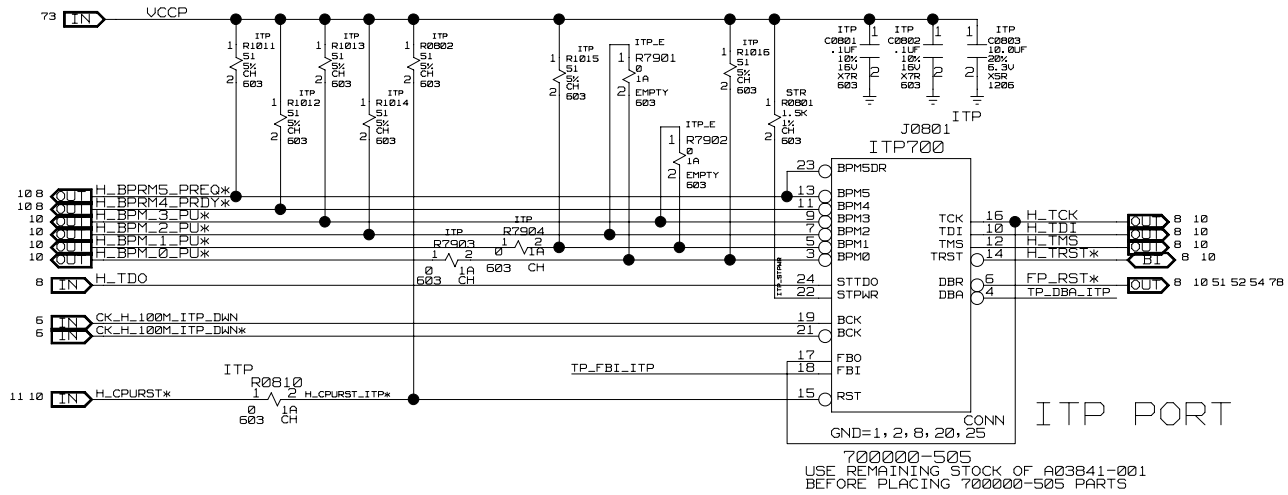

700000-505
USE REMAINING STOCK OF A03841-001
BEFORE PLACING 700000-505 PARTS

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SCHEMATIC TITLE: INTEL(R) 850 MPGA478 CUSTOMER REFERENCE BOARD		
PAGE TITLE: ITP AND MISC DEBUG		REV: 1.0
INTEL PLATFORM APPS ENG 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	LAST REVISED: Tue Jul 10 11:10:19 2001	SHEET: 79

CR-79 [MODULE=CORES]