Intel® NUC Board NUC5i5RYB and Intel® NUC Board NUC5i3RYB
Technical Product Specification

March 2019
Order Number: H50371-009

Intel® NUC Board NUC5i5RYB and Intel® NUC Board NUC5i3RYB may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata, if any, are documented in Intel® NUC Board NUC5i5RYB and Intel® NUC Board NUC5i3RYB Specification Update.
Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Revision History</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>First release of the Intel® NUC Board NUC5i5RYB and Intel® NUC Board NUC5i3RYB Technical Product Specification</td>
<td>December 2014</td>
</tr>
<tr>
<td>002</td>
<td>Specification Clarification</td>
<td>June 2015</td>
</tr>
<tr>
<td>003</td>
<td>Specification Clarification</td>
<td>March 2016</td>
</tr>
<tr>
<td>004</td>
<td>Specification Change</td>
<td>May 2016</td>
</tr>
<tr>
<td>005</td>
<td>Specification Change</td>
<td>January 2017</td>
</tr>
<tr>
<td>006</td>
<td>Specification Change</td>
<td>May 2017</td>
</tr>
<tr>
<td>007</td>
<td>Added refresh NUC5i3RYB and NUC5i3RYH sku</td>
<td>September 2018</td>
</tr>
<tr>
<td>008</td>
<td>Added information on new 5005U SOC only supporting PCIe/NVMe SSD’s in M.2</td>
<td>December 2018</td>
</tr>
<tr>
<td>009</td>
<td>Add refresh NUC5i5RYB and NUC5i5RYH</td>
<td>March 2019</td>
</tr>
</tbody>
</table>

Disclaimer

This product specification applies to only the standard Intel NUC Board, Kit or System with BIOS identifier RYBDWi35.86A.

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Board Identification Information

### Basic Intel® NUC Board NUC5i5RYB Identification Information

<table>
<thead>
<tr>
<th>AA Revision</th>
<th>BIOS Revision</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>H40999-502</td>
<td>RYBDWi35.86A.0130</td>
<td>1,2</td>
</tr>
<tr>
<td>K44993-500</td>
<td>RYBDWi35.86A.0377</td>
<td>1,2</td>
</tr>
</tbody>
</table>

Notes:
1. The AA number is found on a small label on the component side of the board.
2. The Intel® Core™ i5-5250U processor is used on this AA revision consisting of the following component:

<table>
<thead>
<tr>
<th>Device</th>
<th>Stepping</th>
<th>S-Spec Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel Core i5-5250U</td>
<td>F0</td>
<td>SR26C</td>
</tr>
<tr>
<td>Intel Core i5-5257U</td>
<td>F0</td>
<td>SR26K</td>
</tr>
</tbody>
</table>

### Basic Intel® NUC Board NUC5i3RYB Identification Information

<table>
<thead>
<tr>
<th>AA Revision</th>
<th>BIOS Revision</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>H41000-502</td>
<td>RYBDWi35.86A.0130</td>
<td>1,2</td>
</tr>
<tr>
<td>H41000-515</td>
<td>RYBDWi35.86A.0373</td>
<td>1,2</td>
</tr>
</tbody>
</table>

Notes:
1. The AA number is found on a small label on the component side of the board.
2. The Intel® Core™ i3-5010U processor is used on this AA revision consisting of the following component:

<table>
<thead>
<tr>
<th>Device</th>
<th>Stepping</th>
<th>S-Spec Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel Core i3-5010U</td>
<td>F0</td>
<td>SR23Z</td>
</tr>
<tr>
<td>Intel Core i3-5005U</td>
<td>F0</td>
<td>SR27G</td>
</tr>
</tbody>
</table>

### Specification Changes or Clarifications

The table below indicates the Specification Changes or Specification Clarifications that apply to the Intel NUC Board NUC5i5RYB and NUC5i3RYB.

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<table>
<thead>
<tr>
<th>Date</th>
<th>Type of Change</th>
<th>Description of Changes or Clarifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>June 2015</td>
<td>Spec Clarification</td>
<td>• Updated the following to show the connector used:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>→ Table 14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>→ Table 16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>→ Table 17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>→ Section 2.2.3.5</td>
</tr>
<tr>
<td>March 2016</td>
<td>Spec Clarification</td>
<td>Added a Note to Section — to clarify what the Auxiliary Power Connector is used for.</td>
</tr>
<tr>
<td>May 2016</td>
<td>Spec Change</td>
<td>Deleted the Near Field Communication (NFC) header and all related text.</td>
</tr>
<tr>
<td>January 2017</td>
<td>Spec Change</td>
<td>Deleted references to Intel Integrator Toolkit, including the section &quot;Custom Splash Screen&quot;</td>
</tr>
</tbody>
</table>
Errata

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for Intel® NUC Board NUC5i5RYB and Intel® NUC Board NUC5i3RYB.

Intended Audience

The TPS is intended to provide detailed, technical information about Intel® NUC Board NUC5i5RYB and Intel® NUC Board NUC5i3RYB and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically not intended for general audiences.

What This Document Contains

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A description of the hardware used on Intel® NUC Board NUC5i5RYB and Intel® NUC Board NUC5i3RYB</td>
</tr>
<tr>
<td>2</td>
<td>A map of the resources of the Intel NUC Board</td>
</tr>
<tr>
<td>3</td>
<td>The features supported by the BIOS Setup program</td>
</tr>
<tr>
<td>4</td>
<td>A description of the BIOS error messages, beep codes, and POST codes</td>
</tr>
<tr>
<td>5</td>
<td>Regulatory compliance and battery disposal information</td>
</tr>
</tbody>
</table>

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

**NOTE**

Notes call attention to important information.

**CAUTION**

Cautions are included to help you avoid damaging hardware or losing data.
## Other Common Notation

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>#</td>
<td>Used after a signal name to identify an active-low signal (such as USBP0#)</td>
</tr>
<tr>
<td>GB</td>
<td>Gigabyte (1,073,741,824 bytes)</td>
</tr>
<tr>
<td>GB/s</td>
<td>Gigabytes per second</td>
</tr>
<tr>
<td>Gb/s</td>
<td>Gigabits per second</td>
</tr>
<tr>
<td>KB</td>
<td>Kilobyte (1024 bytes)</td>
</tr>
<tr>
<td>Kb</td>
<td>Kilobit (1024 bits)</td>
</tr>
<tr>
<td>kb/s</td>
<td>1000 bits per second</td>
</tr>
<tr>
<td>MB</td>
<td>Megabyte (1,048,576 bytes)</td>
</tr>
<tr>
<td>MB/s</td>
<td>Megabytes per second</td>
</tr>
<tr>
<td>Mb</td>
<td>Megabit (1,048,576 bits)</td>
</tr>
<tr>
<td>Mb/s</td>
<td>Megabits per second</td>
</tr>
<tr>
<td>TDP</td>
<td>Thermal Design Power</td>
</tr>
<tr>
<td>xxh</td>
<td>An address or data value ending with a lowercase h indicates a hexadecimal value.</td>
</tr>
<tr>
<td>x.x V</td>
<td>Volts. Voltages are DC unless otherwise specified.</td>
</tr>
<tr>
<td>*</td>
<td>This symbol is used to indicate third-party brands and names that are the property of their respective owners.</td>
</tr>
</tbody>
</table>
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1 Product Description

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the major features of Intel® NUC Board NUC5i5RYB and Intel® NUC Board NUC5i3RYB.

Table 1. Feature Summary

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>4.0 inches by 4.0 inches (101.60 millimeters by 101.60 millimeters)</th>
</tr>
</thead>
</table>
| Processor   | • Intel® NUC Board NUC5i5RYB has a soldered-down 5th generation Intel® Core™ i5-5250U or a 5th generation Intel® Core™ i5-5257U dual-core processor with up to a maximum 25 W TDP (if thermal margin available)  
  — Integrated graphics HD6000  
  — Integrated memory controller  
  — Integrated PCH  
  • Intel® NUC Board NUC5i3RYB has a soldered-down 5th generation Intel® Core™ i3-5010U or a 5th generation Intel® Core™ i3-5005U dual-core processor with up to a maximum 25 W TDP (if thermal margin available)  
  — Integrated graphics HD5500  
  — Integrated memory controller  
  — Integrated PCH |
| Memory      | • Two 204-pin DDR3L SDRAM Small Outline Dual Inline Memory Module (SO-DIMM) sockets  
  • Support for DDR3L 1600/1333 MHz SO-DIMMs  
  • Support for 2 Gb and 4 Gb memory technology  
  • Support for up to 16 GB of system memory with two SO-DIMMs using 4 Gb memory technology  
  • Support for non-ECC memory  
  • Support for 1.35 V low voltage JEDEC memory only |
| Graphics    | • Integrated graphics support for processors with Intel® Graphics Technology:  
  — One Mini High Definition Multimedia Interface* (Mini HDMI*) back panel connector  
  — One Mini DisplayPort* back panel connector |
| Audio       | • Intel® High Definition (Intel® HD) Audio via the Mini HDMI v1.4a and Mini DisplayPort 1.2 interfaces through the processor  
  • Realtek HD Audio via a stereo microphone/headphone 3.5 mm jack on the front panel |
| Storage     | • SATA ports:  
  — One SATA 6.0 Gb/s port (blue) for 2.5" storage device  
  • One SATA 6.0 Gb/s port is reserved for an M.2 storage module supporting M.2 2242, M.2 2260, and M.2 2280 (key type M) modules  
  Note 1: Intel NUC Board NUC5i5RYB and Intel NUC Board NUC5i3RYB support key type M (PCI Express x1/x2/x4 and SATA)  
  Note 2: Intel NUC Board NUC5i3RYB with Intel® Core™ i3-5005U only supports NVMe M.2 SSD drives and does not support SATA based M.2 SSD drives |
| Peripheral Interfaces | • USB 3.0 ports: |
- Two ports are implemented with external front panel connectors (blue and orange)
- Two ports are implemented with external back panel connectors (blue)
- USB 2.0 ports:
  - Two ports via one dual-port internal 1x8 1.25 mm pitch header (white)
  - One port is reserved for an M.2 1216 module

**Table 1. Feature Summary (continued)**

<table>
<thead>
<tr>
<th>Expansion Capabilities</th>
<th>One M.2 connector supporting M.2 2242, M.2 2260, and M.2 2280 (key type M) modules</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIOS</td>
<td>Intel® BIOS resident in the Serial Peripheral Interface (SPI) Flash device</td>
</tr>
<tr>
<td></td>
<td>Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and</td>
</tr>
<tr>
<td></td>
<td>System Management BIOS (SMBIOS)</td>
</tr>
<tr>
<td>Instantly Available PC</td>
<td>Support for PCI Express*</td>
</tr>
<tr>
<td>Technology</td>
<td>Suspend to RAM support</td>
</tr>
<tr>
<td></td>
<td>Wake on PCI Express, LAN, front panel, CIR, and USB ports</td>
</tr>
<tr>
<td>LAN</td>
<td>Gigabit (10/100/1000 Mb/s) LAN subsystem using the Intel® I218-V Gigabit Ethernet</td>
</tr>
<tr>
<td></td>
<td>Controller</td>
</tr>
<tr>
<td>Hardware Monitor</td>
<td>Hardware monitoring subsystem, based on a Nuvoton NCT5577D embedded controller,</td>
</tr>
<tr>
<td>Subsystem</td>
<td>including:</td>
</tr>
<tr>
<td></td>
<td>Voltage sense to detect out of range power supply voltages</td>
</tr>
<tr>
<td></td>
<td>Thermal sense to detect out of range thermal values</td>
</tr>
<tr>
<td></td>
<td>One processor fan header</td>
</tr>
<tr>
<td></td>
<td>Fan sense input used to monitor fan activity</td>
</tr>
<tr>
<td></td>
<td>Fan speed control</td>
</tr>
<tr>
<td>Wireless</td>
<td>Intel® Dual Band Wireless-AC 7265</td>
</tr>
<tr>
<td></td>
<td>802.11ac, Dual Band, 2x2 Wi-Fi + Bluetooth 4.0</td>
</tr>
<tr>
<td></td>
<td>Maximum Transfer speed up to 867Mbps</td>
</tr>
<tr>
<td></td>
<td>Supports Intel® Wireless Display (WiDi)</td>
</tr>
<tr>
<td></td>
<td>Supports Intel® Smart Connect Technology</td>
</tr>
</tbody>
</table>
1.1.2 Board Layout (Top)

Figure 1 shows the location of the major components on the top-side of Intel NUC Board NUC5i5RYB and Intel NUC Board NUC5i3RYB.
Table 2 lists the components identified in Figure 1.

**Table 2. Components Shown in Figure 1**

<table>
<thead>
<tr>
<th>Item from Figure 1</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Thermal solution</td>
</tr>
<tr>
<td>B</td>
<td>Battery</td>
</tr>
<tr>
<td>C</td>
<td>Processor fan header</td>
</tr>
<tr>
<td>D</td>
<td>Onboard power button</td>
</tr>
<tr>
<td>E</td>
<td>Power LED (Dual Color)</td>
</tr>
<tr>
<td>F</td>
<td>Hard Disk Drive LED</td>
</tr>
<tr>
<td>G</td>
<td>Standby Power LED</td>
</tr>
</tbody>
</table>
1.1.3 Board Layout (Bottom)

Figure 2 shows the location of the major components on the bottom-side of Intel NUC Board NUC5i5RYB and Intel NUC Board NUC5i3RYB.

Figure 2. Major Board Components (Bottom)
<table>
<thead>
<tr>
<th>Item from Figure 2</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Back panel connectors</td>
</tr>
<tr>
<td>B</td>
<td>Auxiliary power connector</td>
</tr>
<tr>
<td>C</td>
<td>Front panel header</td>
</tr>
<tr>
<td>D</td>
<td>Intel Dual Band Wireless AC + Bluetooth 7265 module</td>
</tr>
<tr>
<td>E</td>
<td>SATA power connector (1.25 mm pitch)</td>
</tr>
<tr>
<td>F</td>
<td>M.2 connector (key type M) for 2242, 2260, and 2280 modules</td>
</tr>
<tr>
<td>G</td>
<td>Front panel dual-port USB 2.0 header (1.25 mm pitch)</td>
</tr>
<tr>
<td>H</td>
<td>Front panel USB 3.0 connector (blue)</td>
</tr>
<tr>
<td>I</td>
<td>Front panel USB 3.0 connector (orange, charging)</td>
</tr>
<tr>
<td>J</td>
<td>SATA 6.0 Gb/s connector</td>
</tr>
<tr>
<td>K</td>
<td>Front panel stereo microphone/headphone jack</td>
</tr>
<tr>
<td>L</td>
<td>Consumer Infrared (CIR) sensor</td>
</tr>
<tr>
<td>M</td>
<td>BIOS security jumper</td>
</tr>
<tr>
<td>N</td>
<td>DDR3L SO-DIMM 1 socket</td>
</tr>
<tr>
<td>O</td>
<td>DDR3L SO-DIMM 2 socket</td>
</tr>
</tbody>
</table>
1.1.4 Block Diagram

Figure 3 is a block diagram of the major functional areas of the board.
1.2 Online Support

To find information about...

Visit this World Wide Web site:

Intel NUC Board NUC5i5RYB and Intel NUC Board NUC5i3RYB
http://www.intel.com/NUC
Intel NUC Board Support
http://www.intel.com/NUCSupport
Available configurations for Intel NUC Board NUC5i5RYB and Intel NUC Board NUC5i3RYB
http://ark.intel.com
BIOS and driver updates
http://downloadcenter.intel.com
Tested memory
http://www.intel.com/NUCSupport
Integration information
http://www.intel.com/NUCSupport
Processor datasheet
http://ark.intel.com

1.3 Processor

Intel® NUC Board NUC5i5RYB has a soldered-down 5th generation Intel® Core™ i5-5250U or 5th generation Intel® Core™ i5-5257U dual-core processor with up to a maximum 25 W TDP (if thermal margin is available)
- Integrated graphics HD6000
- Integrated memory controller
- Integrated PCH

Intel® NUC Board NUC5i3RYB has a soldered-down 5th generation Intel® Core™ i3-5010U and 5th generation Intel® Core™ i3-5005U dual-core processor with up to a maximum 25 W TDP (if thermal margin is available)
- Integrated graphics with HD5500
- Integrated memory controller
- Integrated PCH

NOTE

There are specific requirements for providing power to the processor. Refer to Section 2.5.1 on page 55 for information on power supply requirements.
1.4 System Memory

The board has two 204-pin SO-DIMM sockets and supports the following memory features:

- 1.35 V DDR3L SDRAM SO-DIMMs with gold plated contacts
- Two independent memory channels with interleaved mode support
- Unbuffered, single-sided or double-sided SO-DIMMs
- 16 GB maximum total system memory (with 4 Gb memory technology). Refer to Section 2.1.1 on page 41 for information on the total amount of addressable memory.
- Minimum recommended total system memory: 2048 MB
- Non-ECC SO-DIMMs
- Serial Presence Detect
- DDR3L 1600/1333 MHz SDRAM SO-DIMMs

**NOTE**

To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with SO-DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the SO-DIMMs may not function under the determined frequency.

Table 4 lists the supported SO-DIMM configurations.

**Table 4. Supported Memory Configurations**

<table>
<thead>
<tr>
<th>DIMM Capacity</th>
<th>Configuration (Note)</th>
<th>SDRAM Density</th>
<th>SDRAM Organization Front-side/Back-side</th>
<th>Number of SDRAM Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>4096 MB</td>
<td>DS</td>
<td>2 Gbit</td>
<td>256 M x8/256 M x8</td>
<td>16</td>
</tr>
<tr>
<td>4096 MB</td>
<td>SS</td>
<td>4 Gbit</td>
<td>512 M x8/empty</td>
<td>8</td>
</tr>
<tr>
<td>8192 MB</td>
<td>DS</td>
<td>4 Gbit</td>
<td>512 M x8/512 M x8</td>
<td>16</td>
</tr>
</tbody>
</table>

Note: “DS” refers to double-sided memory modules (containing two rows of SDRAM) and “SS” refers to single-sided memory modules (containing one row of SDRAM).

For information about... Refer to:

Tested Memory [http://www.intel.com/NUCSupport](http://www.intel.com/NUCSupport)
1.4.1 Memory Configurations

The processor supports the following types of memory organization:

- **Dual channel (Interleaved) mode.** This mode offers the highest throughput for real world applications. Dual channel mode is enabled when the installed memory capacities of both SO-DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed SO-DIMMs are used between channels, the slowest memory timing will be used.

- **Single channel (Asymmetric) mode.** This mode is equivalent to single channel bandwidth operation for real world applications. This mode is used when only a single SO-DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speed SO-DIMMs are used between channels, the slowest memory timing will be used.

For information about... Refer to:

| Memory Configuration Examples | http://www.intel.com/NUCSupport |

Figure 4 illustrates the memory channel and SO-DIMM configuration.
1.5 Processor Graphics Subsystem

The board supports graphics through Intel HD Graphics.

1.5.1 Integrated Graphics

The board supports integrated graphics via the processor.

1.5.1.1 Intel® High Definition (Intel® HD) Graphics

The Intel HD graphics controller features the following:

- **3D Features**
  - DirectX® 11 support
  - OpenGL® 4.2 support

- **Video**

- **Next Generation Intel® Clear Video Technology HD support** is a collection of video playback and enhancement features that improve the end user's viewing experience

- **Encode/Transcode HD content**

- **Playback of high definition content including Blu-ray® disc**

- **Superior image quality with sharper, more colorful images**

- **DirectX® Video Acceleration (DXVA) support** for accelerating video processing

- **Full AVC/VC1/MPEG2/H.264 HW Decode**

- **Partial H.265 encoding** via graphics hardware and via the CPU

- **Intel HD Graphics with Advanced Hardware Video Transcoding (Intel® Quick Sync Video)**

**NOTE**

*Intel Quick Sync Video is enabled by an appropriate software application.*

1.5.1.2 Video Memory Allocation

Intel® Dynamic Video Memory Technology (DVMT) is a method for dynamically allocating system memory for use as graphics memory to balance 2D/3D graphics and system performance. If your computer is configured to use DVMT, graphics memory is allocated based on system requirements and application demands (up to the configured maximum amount). When memory is no longer needed by an application, the dynamically allocated portion of memory is returned to the operating system for other uses.
1.5.1.3 Mini High Definition Multimedia Interface* (Mini HDMI*)

The Mini High-Definition Multimedia Interface (Mini HDMI) is provided for transmitting uncompressed digital audio and video signals to television sets, projectors and other video displays. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The Mini HDMI display interface connecting the processor and display devices utilizes transition minimized differential signaling (TMDS) to carry audio visual information through the same Mini HDMI cable. The processor HDMI interface is designed according to the High-Definition Multimedia Interface Specification with 3D, Deep Color, and x.v.Color. The maximum supported resolution is 1920 x 1200 @ 60 Hz, 24bpp or up to 4096 x 2304 @ 24Hz, 24bpp. The Mini HDMI port is compliant with the HDMI 1.4a specification.

1.5.1.4 Mini DisplayPort*

DisplayPort is a digital communication interface that utilizes differential signaling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. DisplayPort is suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays. The maximum supported resolution is 3840 x 2160 @ 60 Hz, 30bpp. The Mini DisplayPort is compliant with the DisplayPort 1.2 specification.

DisplayPort output supports Multi-Stream Transport (MST) which allows for multiple independent video streams (daisy-chain connection with multiple monitors) over a single DisplayPort. This will require the use of displays that support DisplayPort 1.2 and allow for this feature.

For information about DisplayPort technology Refer to http://www.displayport.org

1.5.1.4.1 DisplayPort 1.2 Multi-Stream Transport Daisy-Chaining

Table 5 lists the maximum resolutions available when using DisplayPort 1.2 Multi-Stream Transport.

<table>
<thead>
<tr>
<th>DisplayPort Usage Models</th>
<th>Monitor 1</th>
<th>Monitor 2</th>
<th>Monitor 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 Monitors</td>
<td>1920 x 1200 @ 60 Hz</td>
<td>1920 x 1080 @ 60 Hz</td>
<td>1920 x 1080 @ 60 Hz</td>
</tr>
<tr>
<td>2 Monitors</td>
<td>2560 x 1600 @ 60 Hz</td>
<td>2560 x 1600 @ 60 Hz</td>
<td></td>
</tr>
<tr>
<td>3 Monitors (with DisplayPort 1.2 hub)</td>
<td>1920 x 1080 @ 60 Hz</td>
<td>1920 x 1080 @ 60 Hz</td>
<td>1920 x 1080 @ 60 Hz</td>
</tr>
</tbody>
</table>

1.5.1.5 Multiple DisplayPort and HDMI Configurations

Multiple DisplayPort and HDMI configurations feature the following:
- Two independent displays
- Single HDMI 1.4a with 1080P support
- Single DisplayPort 1.2 with 4K support
- Collage Display
Table 6. Multiple Display Configuration Maximum Resolutions

<table>
<thead>
<tr>
<th>Single Display HDMI</th>
<th>Dual Display DisplayPort and HDMI</th>
<th>Single Display DisplayPort</th>
</tr>
</thead>
<tbody>
<tr>
<td>1920 x 1200 @ 60 Hz</td>
<td>3840 x 2160 @ 60 Hz (DisplayPort)</td>
<td>3840 x 2160 @ 60 Hz</td>
</tr>
<tr>
<td></td>
<td>1920 x 1200 @ 60 Hz (HDMI)</td>
<td></td>
</tr>
<tr>
<td>4096 x 2304 @ 24Hz</td>
<td>3840 x 2160 @ 30 Hz (DisplayPort)</td>
<td>Same as above</td>
</tr>
<tr>
<td></td>
<td>3840 x 2160 @ 30 Hz (HDMI)</td>
<td></td>
</tr>
</tbody>
</table>

Note: Higher resolutions may be achievable but only at lower refresh rates

For information about Multiple display maximum resolutions Refer to https://www-ssl.intel.com/content/www/us/en/processors/core/CoreTechnicalResources.html (Generic link)

1.5.1.6 High-bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high definition content against unauthorized copy or interception between a source (computer, digital set top boxes, etc.) and the sink (panels, monitor, and TVs). The PCH supports HDCP 1.4a for content protection over wired displays (Mini DisplayPort and Mini HDMI).

1.5.1.7 Integrated Audio Provided by the Mini HDMI and Mini DisplayPort Interfaces

The Mini HDMI and Mini DisplayPort interfaces from the PCH support audio. The processor supports two High Definition audio streams on two digital ports simultaneously.

Table 7 shows the specific audio technologies supported by the PCH.

Table 7. Audio Formats Supported by the Mini HDMI and Mini DisplayPort Interfaces

<table>
<thead>
<tr>
<th>Audio Formats</th>
<th>Mini HDMI</th>
<th>Mini DisplayPort</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC-3 – Dolby* Digital</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Dolby Digital Plus</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>DTS-HD*</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>LPCM, 192 kHz/24 bit, 8 channel</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Dolby True HD, DTS-HD Master Audio* (Lossless Blu-ray Disc Audio Format)</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
1.6 USB

The board supports eight USB ports. All eight ports are high-speed, full-speed, and low-speed capable. The port arrangement is as follows:

- USB 3.0 ports:
  - Two ports are implemented with external front panel connectors (blue and orange)
  - Two ports are implemented with external back panel connectors (blue)
- USB 2.0 ports:
  - Two ports via one dual-port internal 1x8 1.25 mm pitch header (white)
  - One port is reserved for an M.2 1216 for the Wireless module

**NOTE**

**Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use a shielded cable that meets the requirements for full-speed devices.**

<table>
<thead>
<tr>
<th>For information about</th>
<th>Refer to</th>
</tr>
</thead>
<tbody>
<tr>
<td>The location of the USB connectors on the back panel</td>
<td>Figure 9, page 42</td>
</tr>
<tr>
<td>The location of the front panel USB headers</td>
<td>Figure 2, page 17</td>
</tr>
</tbody>
</table>

1.7 SATA Interface

The board provides the following SATA interfaces:

- One SATA 6.0 Gb/s port (blue)
- One SATA 6.0 Gb/s port is reserved for an M.2 (Type M) 2240, 2260 or 2280 module for SSD

The PCH provides independent SATA ports with a theoretical maximum transfer rate of 6 Gb/s. A point-to-point interface is used for host to device connections.

1.7.1 AHCI Mode

The board supports AHCI storage mode.

**NOTE**

*In order to use AHCI mode, AHCI must be enabled in the BIOS. Microsoft*®* Windows*® 7, Windows 8.1 or Windows 10 and include the necessary AHCI drivers without the need to install separate AHCI drivers during the operating system installation process; however, it is always good practice to update the AHCI drivers to the latest available by Intel.*
1.7.2 Intel® Rapid Storage Technology / SATA RAID

The PCH supports Intel® Rapid Storage Technology, providing both AHCI and integrated RAID functionality. The RAID capability provides high-performance RAID 0 and 1 functionality on all SATA ports. Other RAID features include hot spare support and SMART alerting. Software components include an Option ROM for pre-boot configuration and boot functionality, a Microsoft Windows compatible driver, and a user interface for configuration and management of the RAID capability of the PCH.

**NOTE 1**

Intel Rapid Storage Technology / SATA RAID is only supported if an M.2 SATA SSD module is used with the onboard SATA interface. Cannot get RAID with M.2 PCIe SSD module and onboard SATA interface.

**NOTE 2**

Intel NUC i3 5005u based product does not support SATA M.2 SSD drives. It only supports PCIe M.2 SSD drives.

1.7.3 Intel® Smart Response Technology

Intel® Smart Response Technology is a disk caching solution that can provide improved computer system performance with improved power savings. It allows configuration of a computer system with the advantage of having HDDs for maximum storage capacity with system performance at or near SSD performance levels.

For more information on Intel Smart Response Technology, go to [http://www.intel.com/support/chipsets/sb/CS-032826.htm](http://www.intel.com/support/chipsets/sb/CS-032826.htm)

**NOTE**

In order to use supported RAID and Intel Smart Response Technology features, you must first enable RAID in the BIOS.

1.8 Real-Time Clock Subsystem

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 °C with 3.3 VSB applied via the power supply 5 V STBY rail.
NOTE

If the battery and AC power fail, date and time values will be reset and the user will be notified during the POST.

When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate. Replace the battery with an equivalent one. Figure 1 on page 15 shows the location of the battery.
1.9 Audio Subsystem

The audio subsystem supports the following features:

- Analog line-out/Analog Headphone/Analog Microphone (front panel jack)
- Support for 44.1 kHz/48 kHz/96 kHz/192 kHz sample rates on all analog outputs
- Support for 44.1 kHz/48 kHz/96 kHz sample rates on all analog inputs
- Front Panel Audio Jack Support (see Figure 5 for 3.5 mm audio jack pin out):
  - Speakers only (Stereo)
  - Headphones only (Stereo)
  - Microphone only (mono)
  - Combo Headphone (Stereo)/Microphone (mono)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Tip</td>
<td>Left Audio Out</td>
</tr>
<tr>
<td>2</td>
<td>Ring</td>
<td>Right Audio Out</td>
</tr>
<tr>
<td>3</td>
<td>Ring</td>
<td>Common/Ground</td>
</tr>
<tr>
<td>4</td>
<td>Sleeve</td>
<td>Audio In/MIC</td>
</tr>
</tbody>
</table>

Figure 5. 4-Pin 3.5 mm (1/8 inch) Audio Jack Pin Out

NOTE

The analog circuit of the front panel audio connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (nonamplified) speakers are connected to this output.

1.9.1 Audio Subsystem Software

Audio software and drivers are available from Intel’s World Wide Web site.

For information about Refer to
Obtaining Audio software and drivers [http://downloadcenter.intel.com](http://downloadcenter.intel.com)
1.10 LAN Subsystem

The LAN subsystem consists of the following:
- Intel I218-V Gigabit Ethernet Controller (10/100/1000 Mb/s)
- RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:
- CSMA/CD protocol engine
- LAN connect interface between the Processor and the LAN controller
- Power management capabilities
  - ACPI technology support
  - LAN wake capabilities
- LAN subsystem software

1.10.1 Intel® I218-V Gigabit Ethernet Controller

The Intel I218-V Gigabit Ethernet Controller supports the following features:
- Compliant with the 1 Gb/s Ethernet 802.3, 802.3u, 802.3z, 802.3ab specifications
- Multi-speed operation: 10/100/1000 Mb/s
- Full-duplex operation at 10/100/1000 Mb/s; Half-duplex operation at 10/100 Mb/s
- Flow control support compliant with the 802.3X specification as well as the specific operation of asymmetrical flow control defined by 802.3z
- VLAN support compliant with the 802.3q specification
- Supports Jumbo Frames (up to 9 kB)
  - IEEE 1588 supports (Precision Time Protocol)
- MAC address filters: perfect match unicast filters, multicast hash filtering, broadcast filter, and promiscuous mode

1.10.2 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about | Refer to
--- | ---
Obtaining LAN software and drivers | [http://downloadcenter.intel.com](http://downloadcenter.intel.com)
1.10.3 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 6).

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Link LED (Green)</td>
</tr>
<tr>
<td>B</td>
<td>Data Rate LED (Green/Yellow)</td>
</tr>
</tbody>
</table>

**Figure 6. LAN Connector LED Locations**

Table 8 describes the LED states when the board is powered up and the LAN subsystem is operating.

**Table 8. LAN Connector LED States**

<table>
<thead>
<tr>
<th>LED</th>
<th>LED Color</th>
<th>LED State</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link</td>
<td>Green</td>
<td>Off</td>
<td>LAN link is not established.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On</td>
<td>LAN link is established.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Blinking</td>
<td>LAN activity is occurring.</td>
</tr>
<tr>
<td>Data Rate</td>
<td>Green/Yellow</td>
<td>Off</td>
<td>10Mb/s data rate is selected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Green</td>
<td>100Mb/s data rate is selected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Yellow</td>
<td>1000Mb/s data rate is selected.</td>
</tr>
</tbody>
</table>
1.10.4 Wireless Network Module

The Intel Dual Band Wireless-AC 7265 module provides high-speed wireless connectivity provided with the following capabilities:

- Compliant IEEE 802.11abgn, 802.11ac, 802.11ad, 802.11e, 802.11i, 802.11h, 802.11w specifications
- Maximum bandwidth of 867 Mbps
- Dual Mode Bluetooth* 2.1, 2.1+EDR, 3.0, 4.0 (BLE)
- OS certified with: Microsoft Windows 7, Microsoft Windows 8.1, Linux* (most features not available on Linux)
- Wi-Fi Direct* for peer to peer device connections
- Wi-Fi Miracast Source
- Wi-Fi Direct for peer to peer device connections
- Authentication: WPA and WPA2, 802.1X (EAP-TLS, TTLS, PEAP, LEAP, EAP-FAST), EAP-SIM, EAP-AKA
- Encryption: 64-bit and 128-bit WEP, AES-CCMP, TKIP, WPA2, AES-CCMP

For information about

Refer to

Obtaining WLAN software and drivers
http://downloadcenter.intel.com

Full Specifications
http://intel.com/wireless

1.11 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including thermal and voltage monitoring.

For information about

Refer to

Wired for Management (WfM) Specification
www.intel.com/design/archives/wfm/

1.11.1 Hardware Monitoring

The hardware monitoring and fan control subsystem is based on a Nuvoton NCT5577D embedded controller, which supports the following:

- Processor and system ambient temperature monitoring
- Chassis fan speed monitoring
- Voltage monitoring of +5 V, +3.3 V, Memory Vcc (V_SM), +Vccp,
- SMBus interface

1.11.2 Fan Monitoring

Fan monitoring can be implemented using third-party software.
1.11.3 Thermal Solution

Figure 7 shows the location of the thermal solution and processor fan header.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Processor fan header</td>
</tr>
<tr>
<td>B</td>
<td>Thermal solution</td>
</tr>
</tbody>
</table>

Figure 7. Thermal Solution and Fan Header
1.12 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power Input
  - Instantly Available PC technology
  - LAN wake capabilities
  - Wake from USB
  - WAKE# signal wake-up support
  - Wake from S5
  - Wake from CIR
  - +5 V Standby Power Indicator LED

1.12.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 11 on page 36)
- Support for a front panel power and sleep mode switch

Table 9 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

**Table 9. Effects of Pressing the Power Switch**

<table>
<thead>
<tr>
<th>If the system is in this state...</th>
<th>...and the power switch is pressed for</th>
<th>...the system enters this state</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off (ACPI G2/G5 – Soft off)</td>
<td>Less than four seconds</td>
<td>Power-on (ACPI G0 – working state)</td>
</tr>
<tr>
<td>On (ACPI G0 – working state)</td>
<td>Less than four seconds</td>
<td>Soft-off/Standby (ACPI G1 – sleeping state) <strong>Note</strong></td>
</tr>
<tr>
<td>On (ACPI G0 – working state)</td>
<td>More than six seconds</td>
<td>Fail safe power-off (ACPI G2/G5 – Soft off)</td>
</tr>
<tr>
<td>Sleep (ACPI G1 – sleeping state)</td>
<td>Less than four seconds</td>
<td>Wake-up (ACPI G0 – working state)</td>
</tr>
<tr>
<td>Sleep (ACPI G1 – sleeping state)</td>
<td>More than six seconds</td>
<td>Power-off (ACPI G2/G5 – Soft off)</td>
</tr>
</tbody>
</table>

**Note:** Depending on power management settings in the operating system.
1.12.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 10 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 10. Power States and Targeted System Power

<table>
<thead>
<tr>
<th>Global States</th>
<th>Sleeping States</th>
<th>Processor States</th>
<th>Device States</th>
<th>Targeted System Power (Note 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G0 – working state</td>
<td>S0 – working</td>
<td>C0 – working</td>
<td>D0 – working state.</td>
<td>Full power &gt; 30 W</td>
</tr>
<tr>
<td>G1 – sleeping state</td>
<td>S3 – Suspend to RAM. Context saved to RAM.</td>
<td>No power</td>
<td>D3 – no power except for wake-up logic.</td>
<td>Power &lt; 5 W (Note 2)</td>
</tr>
<tr>
<td>G1 – sleeping state</td>
<td>S4 – Suspend to disk. Context saved to disk.</td>
<td>No power</td>
<td>D3 – no power except for wake-up logic.</td>
<td>Power &lt; 5 W (Note 2)</td>
</tr>
<tr>
<td>G3 – mechanical off</td>
<td>No power to the system.</td>
<td>No power</td>
<td>D3 – no power for wake-up logic, except when provided by battery or external source.</td>
<td>No power to the system. Service can be performed safely.</td>
</tr>
</tbody>
</table>

Notes:
1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis’ power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.
1.12.1.2 Wake-up Devices and Events

Table 11 lists the devices or specific events that can wake the computer from specific states.

Table 11. Wake-up Devices and Events

<table>
<thead>
<tr>
<th>Devices/events that wake up the system...</th>
<th>...from this sleep state</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power switch</td>
<td>S3, S4, S5&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>RTC alarm</td>
<td>S3, S4, S5&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Monitor to remain in sleep state</td>
</tr>
<tr>
<td>LAN</td>
<td>S3, S4, S5&lt;sup&gt;1-3&lt;/sup&gt;</td>
<td>“S5 WOL after G3” must be supported; monitor to remain in sleep state</td>
</tr>
<tr>
<td>USB</td>
<td>S3, S4, S5&lt;sup&gt;1-2,3&lt;/sup&gt;</td>
<td>Wake S4, S5 controlled by BIOS option (not after G3)</td>
</tr>
<tr>
<td>WAKE#</td>
<td>S3, S4, S5&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Via WAKE; monitor to remain in sleep state</td>
</tr>
<tr>
<td>Consumer IR</td>
<td>S3, S4, S5&lt;sup&gt;1-3&lt;/sup&gt;</td>
<td>Will not wake when in Deep S4/S5 sleep state</td>
</tr>
</tbody>
</table>

Notes:
1. S4 implies operating system support only.
2. Will not wake from Deep S4/S5. USB S4/S5 Power is controlled by BIOS. USB S5 wake is controlled by BIOS. USB S4 wake is controlled by OS driver, not just BIOS option.
3. Windows 8.1 Fast startup will block wake from LAN, USB, and CIR from S5.

**NOTE**

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.12.2 Hardware Support

The board provides several power management hardware features, including:

- Wake from Power Button signal
- Instantly Available PC technology
- LAN wake capabilities
- Wake from USB (not after G3)
- WAKE# signal wake-up support
- Wake from S5
- Wake from CIR
- +5 V Standby Power Indicator LED

**NOTE**

The use of Wake from USB from an ACPI state requires an operating system that provides full ACPI support.
1.12.2.1 **Power Input**
When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

1.12.2.2 **Instantly Available PC Technology**
Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is only supplying Standby power, and the front panel LED will be amber or secondary color if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 11 on page 36 lists the devices and events that can wake the computer from the S3 state.

The use of Instantly Available PC technology requires operating system support and drivers for any installed M.2 add-in card.

1.12.2.3 **LAN Wake Capabilities**
LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer.

1.12.2.4 **Wake from USB**
USB bus activity wakes the computer from an ACPI S3 state (not after G3)

**NOTE**

*Wake from USB requires the use of a USB peripheral that supports Wake from USB.*

1.12.2.5 **WAKE# Signal Wake-up Support**
When the WAKE# signal on the PCI Express bus is asserted, the computer wakes from an ACPI S3, S4, or S5 state.

1.12.2.6 **Wake from S5**
When the RTC Date and Time is set in the BIOS, the computer will automatically wake from an ACPI S5 state.

1.12.2.7 **Wake from Consumer IR**
CIR activity wakes the computer from an ACPI S3, S4, or S5 state.
1.12.2.8 +5 V Standby Power Indicator LED

The standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 8 shows the location of the standby power LED.

⚠️ CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.

Figure 8. Location of the Standby Power LED
2 Technical Reference

2.1 Memory Resources

2.1.1 Addressable Memory

The board utilizes 16 GB of addressable system memory. Typically the address space that is allocated for PCI Conventional bus add-in cards, PCI Express configuration space, BIOS (SPI Flash device), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 32 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- BIOS/SPI Flash device (64 Mb)
- Local APIC (19 MB)
- Direct Media Interface (40 MB)
- PCI Express configuration space (256 MB)
- PCH base address registers PCI Express ports (up to 256 MB)
- Memory-mapped I/O that is dynamically allocated for M.2 add-in cards (256 MB)
- Integrated graphics shared memory (up to 512 MB; 64 MB by default)

The board provides the capability to reclaim the physical memory overlapped by the memory mapped I/O logical address space. The board remaps physical memory from the top of usable DRAM boundary to the 4 GB boundary to an equivalent sized logical address range located just above the 4 GB boundary. All installed system memory can be used when there is no overlap of system addresses.

2.2 Connectors and Headers

⚠️ CAUTION

Only the following connectors and headers have overcurrent protection: back panel and front panel USB.

The other internal connectors and headers are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors or headers to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.

Furthermore, improper connection of USB header single wire connectors may eventually overload the overcurrent protection and cause damage to the board.
This section describes the board's connectors and headers. The connectors and headers can be divided into these groups:

- Front panel I/O connectors
- Back panel I/O connectors
- On-board I/O connectors and headers (see page 43)

### 2.2.1 Front Panel Connectors

Figure 9 shows the location of the front panel connectors for the board.

![Front Panel Connectors](image)

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Front panel stereo microphone/headphone jack</td>
</tr>
<tr>
<td>B</td>
<td>USB 3.0 port (charging) (yellow)</td>
</tr>
<tr>
<td>C</td>
<td>USB 3.0 port (blue)</td>
</tr>
</tbody>
</table>

**Figure 9. Front Panel Connectors**

### 2.2.2 Back Panel Connectors

Figure 10 shows the location of the back panel connectors for the board.

![Back Panel Connectors](image)

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Mini HDMI connector</td>
</tr>
<tr>
<td>B</td>
<td>USB 3.0 ports (blue)</td>
</tr>
<tr>
<td>C</td>
<td>LAN</td>
</tr>
<tr>
<td>D</td>
<td>Mini DisplayPort connector</td>
</tr>
<tr>
<td>E</td>
<td>12-19 V DC input jack</td>
</tr>
</tbody>
</table>

**Figure 10. Back Panel Connectors**
2.2.3 Connectors and Headers (Bottom)

Figure 11 shows the locations of the connectors and headers on the bottom-side of the board.
Table 12 lists the connectors and headers identified in Figure 10.

**Table 12. Connectors and Headers Shown in Figure 10**

<table>
<thead>
<tr>
<th>Item from Figure 10</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Auxiliary power connector</td>
</tr>
<tr>
<td>B</td>
<td>Front panel connector</td>
</tr>
<tr>
<td>C</td>
<td>SATA power connector (1.25 mm pitch)</td>
</tr>
<tr>
<td>D</td>
<td>M.2 2242, 2260 or 2280 (key type M) connector</td>
</tr>
<tr>
<td>E</td>
<td>Front panel dual-port USB 2.0 header (1.25 mm pitch)</td>
</tr>
<tr>
<td>F</td>
<td>SATA 6.0 Gb/s connector</td>
</tr>
<tr>
<td>G</td>
<td>BIOS Security jumper</td>
</tr>
</tbody>
</table>
2.2.3.1 Signal Tables for the Connectors and Headers

Table 13. SATA Power Header (1.25 mm pitch)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5 V</td>
</tr>
<tr>
<td>2</td>
<td>5 V</td>
</tr>
<tr>
<td>3</td>
<td>3.3 V</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
</tr>
</tbody>
</table>

Table 14. Dual-Port Internal USB 2.0 Header (1.25 mm pitch)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>Pin</th>
<th>Signal Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+5 V DC</td>
<td>2</td>
<td>Data (negative) A</td>
</tr>
<tr>
<td>3</td>
<td>Data (positive) A</td>
<td>4</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>Ground</td>
<td>6</td>
<td>Data (positive) B</td>
</tr>
<tr>
<td>7</td>
<td>Data (negative) B</td>
<td>8</td>
<td>+5 V DC</td>
</tr>
</tbody>
</table>

**NOTE**

Connector used is Molex part number 53398-0871, 1.25 mm pitch PicoBlade* header, surface mount, vertical, lead-free, 8 circuits.

Table 15. M.2 2280 Module (key type M) Connector

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>Pin</th>
<th>Signal Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>74</td>
<td>3.3V</td>
<td>75</td>
<td>GND</td>
</tr>
<tr>
<td>72</td>
<td>3.3V</td>
<td>73</td>
<td>GND</td>
</tr>
<tr>
<td>70</td>
<td>3.3V</td>
<td>71</td>
<td>GND</td>
</tr>
<tr>
<td>68</td>
<td>SUSCLK(32kHz) (O)/O/3.3V</td>
<td>69</td>
<td>PEDET (NC-PCIe/GND-SATA)</td>
</tr>
<tr>
<td>66</td>
<td>Connector Key</td>
<td>67</td>
<td>N/C</td>
</tr>
<tr>
<td>64</td>
<td>Connector Key</td>
<td>65</td>
<td>Connector Key</td>
</tr>
<tr>
<td>62</td>
<td>Connector Key</td>
<td>63</td>
<td>Connector Key</td>
</tr>
<tr>
<td>60</td>
<td>Connector Key</td>
<td>61</td>
<td>Connector Key</td>
</tr>
<tr>
<td>58</td>
<td>N/C</td>
<td>59</td>
<td>Connector Key</td>
</tr>
<tr>
<td>56</td>
<td>N/C</td>
<td>57</td>
<td>GND</td>
</tr>
<tr>
<td>54</td>
<td>PEWAKE# (I/O)/O/3.3V or N/C</td>
<td>55</td>
<td>REFLKP</td>
</tr>
<tr>
<td>52</td>
<td>CLKREQ# (I/O)/O/3.3V or N/C</td>
<td>53</td>
<td>REFLKN</td>
</tr>
<tr>
<td>50</td>
<td>PERST# (O)/O/3.3V or N/C</td>
<td>51</td>
<td>GND</td>
</tr>
<tr>
<td>48</td>
<td>N/C</td>
<td>49</td>
<td>PETp0/SATA-A+</td>
</tr>
<tr>
<td>46</td>
<td>N/C</td>
<td>47</td>
<td>PETn0/SATA-A-</td>
</tr>
<tr>
<td>44</td>
<td>N/C</td>
<td>45</td>
<td>GND</td>
</tr>
<tr>
<td>42</td>
<td>N/C</td>
<td>43</td>
<td>PERp0/SATA-B-</td>
</tr>
</tbody>
</table>

continued
Table 15. M.2 2280 Module (key type M) Connector (continued)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>Pin</th>
<th>Signal Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>N/C</td>
<td>41</td>
<td>PERn0/SATA-B+</td>
</tr>
<tr>
<td>38</td>
<td>DEVSLP (O)</td>
<td>39</td>
<td>GND</td>
</tr>
<tr>
<td>36</td>
<td>N/C</td>
<td>37</td>
<td>PETp1</td>
</tr>
<tr>
<td>34</td>
<td>N/C</td>
<td>35</td>
<td>PETn1</td>
</tr>
<tr>
<td>32</td>
<td>N/C</td>
<td>33</td>
<td>GND</td>
</tr>
<tr>
<td>30</td>
<td>N/C</td>
<td>31</td>
<td>PERp1</td>
</tr>
<tr>
<td>28</td>
<td>N/C</td>
<td>29</td>
<td>PERn1</td>
</tr>
<tr>
<td>26</td>
<td>N/C</td>
<td>27</td>
<td>GND</td>
</tr>
<tr>
<td>24</td>
<td>N/C</td>
<td>25</td>
<td>PETp2</td>
</tr>
<tr>
<td>22</td>
<td>N/C</td>
<td>23</td>
<td>PETn2</td>
</tr>
<tr>
<td>20</td>
<td>N/C</td>
<td>21</td>
<td>GND</td>
</tr>
<tr>
<td>18</td>
<td>3.3V</td>
<td>19</td>
<td>PERp2</td>
</tr>
<tr>
<td>16</td>
<td>3.3V</td>
<td>17</td>
<td>PERn2</td>
</tr>
<tr>
<td>14</td>
<td>3.3V</td>
<td>15</td>
<td>GND</td>
</tr>
<tr>
<td>12</td>
<td>3.3V</td>
<td>13</td>
<td>PETp3</td>
</tr>
<tr>
<td>10</td>
<td>DAS/DSS# I/O/LED1# I/O/3.3V</td>
<td>11</td>
<td>PETn3</td>
</tr>
<tr>
<td>8</td>
<td>N/C</td>
<td>9</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>N/C</td>
<td>7</td>
<td>PERp3</td>
</tr>
<tr>
<td>4</td>
<td>3.3V</td>
<td>5</td>
<td>PERn3</td>
</tr>
<tr>
<td>2</td>
<td>3.3V</td>
<td>3</td>
<td>GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>GND</td>
</tr>
</tbody>
</table>

Table 16. Auxiliary Power Connector

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>Descriptive Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+5VSB</td>
<td>5V</td>
</tr>
<tr>
<td>2</td>
<td>PCH_GPIO24</td>
<td>Power draw sensor</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>4</td>
<td>+VIN</td>
<td>12V – 19V DC input</td>
</tr>
</tbody>
</table>

**NOTE**

*JTE (JOINT TECH): A1250WRA-S-04P A-Series (Wire to Board) Right Angle SMT Connector, 1.25mm pitch, 1A rating. Mates with JTE A1250 Series Housing.*

*Intel NUC5i3RYSN and NUC5i3RYS only supports PCIe based M.2 SSD drives. It does not support SATA based M.2 SSD drives.*
2.2.3.2 Add-in Card Connectors

The board supports M.2 2242, 2260, and 2280 (key type M) modules.

- Supports M.2 SSD SATA drives
  - 5th generation Intel\textsuperscript{\textregistered} Core\textsuperscript{\textregistered} i5-5257U
  - 5th generation Intel\textsuperscript{\textregistered} Core\textsuperscript{\textregistered} i5-5250U
  - 5th generation Intel\textsuperscript{\textregistered} Core\textsuperscript{\textregistered} i3-5100U
  - Maximum bandwidth is approximately 540 MB/s
- Supports M.2 SSD PCIe/NVMe drives (PCIe x1, x2, and x4)
  - Using PCIe x4 M.2 SSD maximum bandwidth is approximately 1600 MB/s
  - 5th generation Intel\textsuperscript{\textregistered} Core\textsuperscript{\textregistered} i5-5257U
  - 5th generation Intel\textsuperscript{\textregistered} Core\textsuperscript{\textregistered} i5-5250U
  - 5th generation Intel\textsuperscript{\textregistered} Core\textsuperscript{\textregistered} i3-5100U
  - 5th generation Intel\textsuperscript{\textregistered} Core\textsuperscript{\textregistered} i3-5005U

2.2.3.3 Power Supply Connector

The board has the following power supply connector:

- **External Power Supply** – the board can be powered through a 12-19 V DC connector on the back panel. The back panel DC connector is compatible with a 5.5 mm/OD (outer diameter) and 2.5 mm/ID (inner diameter) plug, where the inner contact is +12-19 (±10\%) V DC and the shell is GND. The maximum current rating is 10 A.

**NOTE**

External power voltage, 12-19 V DC, is dependent on the type of power brick used.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>Descriptive Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+5VSB</td>
<td>5V</td>
</tr>
<tr>
<td>2</td>
<td>PCH_GPIO24</td>
<td>Power draw sensor</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>4</td>
<td>+VIN</td>
<td>12V – 19V DC input</td>
</tr>
</tbody>
</table>

**NOTE**

The Auxiliary Power Connector is a limited voltage source (output) for 5V Standby and the voltage supplied to the board (typically 19V DC) for use by expansion peripherals. The Auxiliary Power Connector is limited to 1.5A max (fused).

**NOTE**

JTE (JOINT TECH): A1250WRA-S-04P A-Series (Wire to Board) Right Angle SMT Connector, 1.25mm pitch, 1A rating. Mates with JTE A1250 Series Housing.
<table>
<thead>
<tr>
<th>For information about</th>
<th>Refer to</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply considerations</td>
<td>Section 2.5.1, page 55</td>
</tr>
</tbody>
</table>
2.2.3.3.1 Power Sensing Circuit

The board has a power sensing circuit that:
- manages CPU power usage to maintain system power consumption below 65 W.
- is designed for use with 65 W AC-DC adapters.

**NOTE**

*It is recommended that you disable this feature (via BIOS option) when using an AC-DC adapter greater than 65 W.*

2.2.3.4 Front Panel Header (2.0 mm Pitch)

This section describes the functions of the front panel header. Table 18 lists the signal names of the front panel header. Figure 12 is a connection diagram for the front panel header.

**Table 18. Front Panel Header (2.0 mm Pitch)**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>Description</th>
<th>Pin</th>
<th>Signal Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HDD_POWER_LED</td>
<td>Pull-up resistor (750 Ω) to +5V</td>
<td>2</td>
<td>POWER_LED_MAIN</td>
<td>[Out] Front panel LED (main color)</td>
</tr>
<tr>
<td>3</td>
<td>HDD_LED#</td>
<td>[Out] Hard disk activity LED</td>
<td>4</td>
<td>POWER_LED_ALT</td>
<td>[Out] Front panel LED (alt color)</td>
</tr>
<tr>
<td>5</td>
<td>GROUND</td>
<td>Ground</td>
<td>6</td>
<td>POWER_SWITCH#</td>
<td>[In] Power switch</td>
</tr>
<tr>
<td>7</td>
<td>RESET_SWITCH#</td>
<td>[In] Reset switch</td>
<td>8</td>
<td>GROUND</td>
<td>Ground</td>
</tr>
<tr>
<td>9</td>
<td>+5V_DC</td>
<td>Power</td>
<td>10</td>
<td>Key</td>
<td>No pin</td>
</tr>
</tbody>
</table>

**Figure 12. Connection Diagram for Front Panel Header (2.0 mm Pitch)**
2.2.3.4.1 Hard Drive Activity LED Header

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires a SATA hard drive connected to an onboard SATA connector.

Note: When using the new M.2 SSD with PCIe there might not be any HDD activity if the storage vendor has not implemented that function.

2.2.3.4.2 Reset Switch Header

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.2.3.4.3 Power/Sleep LED Header

Pins 2 and 4 can be connected to a one- or two-color LED. Table 19 shows the possible LED states.

<table>
<thead>
<tr>
<th>LED State</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>Power off</td>
</tr>
<tr>
<td>Blinking</td>
<td>Standby</td>
</tr>
<tr>
<td>Steady</td>
<td>Normal operation</td>
</tr>
</tbody>
</table>

Table 19. States for a Dual-Color Power LED

<table>
<thead>
<tr>
<th>LED State</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>Power off</td>
</tr>
<tr>
<td>Secondary color blinking</td>
<td>Standby (amber)</td>
</tr>
<tr>
<td>Primary color steady</td>
<td>Normal operation</td>
</tr>
</tbody>
</table>

Table 20. States for a Dual-Color Power LED

NOTE

The LED behavior shown in Table 19 is default – other patterns may be set via BIOS setup.

2.2.3.4.4 Power Switch Header

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.
2.2.3.5 **Internal USB 2.0 Dual-Port Header (1.25 mm Pitch)**

Figure 13 is a connection diagram for the internal USB header.

Connector used is Molex part number 53398-0871, 1.25 mm pitch PicoBlade header, surface mount, vertical, lead-free, 8 circuits.

**NOTE**
- The +5 V DC power on the USB header is fused.
- Use only an internal USB connector that conforms to the USB 2.0 specification for high-speed USB devices.

![Connection Diagram for Internal USB 2.0 Dual-Port Header (1.25 mm Pitch)](image)

---

2.2.3.6 **Consumer Infrared (CIR) Sensor**

The Consumer Infrared (CIR) sensor on the front panel provides features that are designed to comply with Microsoft Consumer Infrared usage models (RC-6).

The CIR feature is made up of the receiving sensor. The receiving sensor consists of a filtered translated infrared input compliant with Microsoft CIR specifications.

Customers are required to provide their own media center compatible remote or smart phone application for use with the Intel NUC. Figure 14 shows the location of the CIR sensor.

![Location of the CIR Sensor](image)

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>CIR Sensor</td>
</tr>
</tbody>
</table>

---
2.3 BIOS Security Jumper

⚠️ CAUTION

*Do not move a jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.*

Figure 15 shows the location of the BIOS Security Jumper. The 3-pin jumper determines the BIOS Security program’s mode.

Table 20 describes the jumper settings for the three modes: normal, lockdown, and configuration.

---

**Figure 15. Location of the BIOS Security Jumper**
Table 20 lists the settings for the jumper.

**Table 20. BIOS Security Jumper Settings**

<table>
<thead>
<tr>
<th>Function/Mode</th>
<th>Jumper Setting</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>1-2</td>
<td>The BIOS uses current configuration information and passwords for booting.</td>
</tr>
<tr>
<td>Lockdown</td>
<td>2-3</td>
<td>The BIOS uses current configuration information and passwords for booting, except:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- All POST Hotkeys are suppressed (prompts are not displayed and keys are not accepted. For example, F2 for Setup, F10 for the Boot Menu).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Power Button Menu is not available (see Section 3.7.4 Power Button Menu).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BIOS updates are not available except for automatic Recovery due to flash corruption.</td>
</tr>
<tr>
<td>Configuration</td>
<td>None</td>
<td>BIOS Recovery Update process if a matching *.bio file is found. Recovery Update can be cancelled by pressing the Esc key.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If the Recovery Update was cancelled or a matching *.bio file was not found, a Config Menu will be displayed. The Config Menu consists of the following (selected Power Button Menu options):</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[1] Suppress this menu until the BIOS Security Jumper is replaced.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Section 3.7.4 Power Button Menu.</td>
</tr>
</tbody>
</table>
2.4 Mechanical Considerations

2.4.1 Form Factor

The board is designed to fit into a custom chassis. Figure 16 illustrates the mechanical form factor for the board. Dimensions are given in inches [millimeters].

![Figure 16. Board Dimensions](image)
2.5 Electrical Considerations

2.5.1 Power Supply Considerations

System power requirements will depend on actual system configurations chosen by the integrator, as well as end user expansion preferences. It is the system integrator's responsibility to ensure an appropriate power budget for the system configuration is properly assessed based on the system-level components chosen. See Section — 5th generation Intel® Core™ i5-5257U

- 5th generation Intel® Core™ i5-5250U
- 5th generation Intel® Core™ i3-5100U
- 5th generation Intel® Core™ i3-5005U

Power Supply Connector for more information.

2.5.2 Fan Header Current Capability

Table 21 lists the current capability of the fan headers.

<table>
<thead>
<tr>
<th>Fan Header</th>
<th>Maximum Available Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor fan</td>
<td>.25 A</td>
</tr>
</tbody>
</table>
2.6 Thermal Considerations

⚠️ CAUTION

A chassis with a maximum internal ambient temperature of 50 °C at the processor fan inlet is recommended. If the internal ambient temperature exceeds 50 °C, further thermal testing is required to ensure components do not exceed their maximum case temperature.

⚠️ CAUTION

Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board.

All responsibility for determining the adequacy of any thermal or system design remains solely with the system integrator. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

⚠️ CAUTION

Ensure that the ambient temperature does not exceed the board’s maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.8.

⚠️ CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in shorter than expected product lifetime.
Figure 18 shows the locations of the localized high temperature zones.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Processor voltage regulator area</td>
</tr>
<tr>
<td>B</td>
<td>Thermal solution</td>
</tr>
</tbody>
</table>

Figure 18. Localized High Temperature Zones
A thermal pad has been installed for the bottom of the chassis to improve the thermal performance when using M.2 devices that operate at higher temperatures. If the thermal pad ever needs to be replaced, Figure 19 shows the installation area of the thermal pad for the Intel NUC Kit NUC5i5RYK/NUC5i3RYK.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Thermal Pad</td>
</tr>
<tr>
<td>B</td>
<td>Thermal Pad Installation Area</td>
</tr>
</tbody>
</table>

Figure 19. Installation Area of Thermal Pad for Intel NUC Kit NUC5i5RYK/NUC5i3RYK
Figure 20 shows the installation area of the thermal pad for the Intel NUC Kit NUC5i5RYKH/NUC5i3RYKH.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Thermal Pad</td>
</tr>
<tr>
<td>B</td>
<td>Thermal Pad Installation Area</td>
</tr>
</tbody>
</table>

Figure 20. Installation area of Thermal Pad for Intel NUC Kit NUC5i5RYKH/NUC5i3RYKH
Table 22 provides maximum case temperatures for the components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

**Table 22. Thermal Considerations for Components**

<table>
<thead>
<tr>
<th>Component</th>
<th>Maximum Case Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor</td>
<td>For processor case temperature, see processor datasheets and processor specification updates</td>
</tr>
</tbody>
</table>

To ensure functionality and reliability, the component is specified for proper operation when Case Temperature is maintained at or below the maximum temperature listed in Table 23. This is a requirement for sustained power dissipation equal to Thermal Design Power (TDP is specified as the maximum sustainable power to be dissipated by the components). When the component is dissipating less than TDP, the case temperature should be below the Maximum Case Temperature. The surface temperature at the geometric center of the component corresponds to Case Temperature.

It is important to note that the temperature measurement in the system BIOS is a value reported by embedded thermal sensors in the components and does not directly correspond to the Maximum Case Temperature. The upper operating limit when monitoring this thermal sensor is Tcontrol.

**Table 23. Tcontrol Values for Components**

<table>
<thead>
<tr>
<th>Component</th>
<th>Tcontrol</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor</td>
<td>For processor case temperature, see processor datasheets and processor specification updates</td>
</tr>
</tbody>
</table>

**For information about** | **Refer to**
---|---
Processor datasheets and specification updates | Section 1.2, page 20
2.7 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Telcordia SR-332 Issue 2, Method I, Case 3, 55 °C ambient. The MTBF prediction is used to estimate repair rates and spare parts requirements. The MTBF for Intel NUC Board NUC5i3RYB is 68,099 hours. The MTBF for Intel NUC Board NUC5i5RYB is 66,569 hours.

2.8 Environmental

Table 24 lists the environmental specifications for the board.

Table 24. Environmental Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td></td>
</tr>
<tr>
<td>Non-Operating</td>
<td>-40 °C to +60 °C</td>
</tr>
<tr>
<td>Operating</td>
<td>0 °C to +50 °C</td>
</tr>
<tr>
<td></td>
<td>The operating temperature of the board may be determined by measuring the air temperature from the junction of the heatsink fins and fan, next to the attachment screw, in a closed chassis, while the system is in operation.</td>
</tr>
<tr>
<td>Shock</td>
<td></td>
</tr>
<tr>
<td>Unpackaged</td>
<td>50 g trapezoidal waveform</td>
</tr>
<tr>
<td></td>
<td>Velocity change of 170 inches/s²</td>
</tr>
<tr>
<td>Packaged</td>
<td>Half sine 2 millisecond</td>
</tr>
<tr>
<td></td>
<td>Product Weight (pounds) Free Fall (inches)</td>
</tr>
<tr>
<td></td>
<td>&lt;20 36 167</td>
</tr>
<tr>
<td></td>
<td>21-40 30 152</td>
</tr>
<tr>
<td></td>
<td>41-80 24 136</td>
</tr>
<tr>
<td></td>
<td>81-100 18 118</td>
</tr>
<tr>
<td>Vibration</td>
<td></td>
</tr>
<tr>
<td>Unpackaged</td>
<td>5 Hz to 20 Hz: 0.01 g² Hz sloping up to 0.02 g² Hz</td>
</tr>
<tr>
<td></td>
<td>20 Hz to 500 Hz: 0.02 g² Hz (flat)</td>
</tr>
<tr>
<td>Packaged</td>
<td>5 Hz to 40 Hz: 0.015 g² Hz (flat)</td>
</tr>
<tr>
<td></td>
<td>40 Hz to 500 Hz: 0.015 g² Hz sloping down to 0.00015 g² Hz</td>
</tr>
</tbody>
</table>

Note: Before attempting to operate this board, the overall temperature of the board must be above the minimum operating temperature specified. It is recommended that the board temperature be at least room temperature before attempting to power on the board. The operating and non-operating environment must avoid condensing humidity.
3 Overview of BIOS Features

3.1 Introduction

The board uses Intel Visual BIOS that is stored in the Serial Peripheral Interface Flash Memory (SPI Flash) and can be updated using a disk-based program. The SPI Flash contains the Visual BIOS Setup program, POST, the PCI auto-configuration utility, LAN EEPROM information, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as RYBDWi35.86A.

The Visual BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins.

NOTE

The maintenance menu is displayed only when the board is in configure mode. Section 2.3 on page 52 shows how to put the board in configure mode.
### 3.2 BIOS Flash Memory Organization

The Serial Peripheral Interface Flash Memory (SPI Flash) includes a 64 Mb flash memory device.

### 3.3 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information. Additional board information can be found in the BIOS under the Additional Information header under the Main BIOS page.

### 3.4 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.
To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system’s installation instructions.

3.5 BIOS Updates

The BIOS can be updated using one of the following methods:

- Intel Express BIOS Update Utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB hard drive), or a CD-ROM, or from the file location on the Web.
- Intel Flash Memory Update Utility, which requires booting from DOS. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB hard drive), or a CD-ROM.
- Intel® F7 switch during POST allows a user to select where the BIOS .bio file is located and perform the update from that location/device. Similar to performing a BIOS Recovery without removing the BIOS configuration jumper.
- Intel® Visual BIOS has an option to update the BIOS from a valid .bio file located on a hard disk or USB drive. Enter Intel Visual BIOS by pressing <F2> during POST.
- Using Front Panel menu option

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

<table>
<thead>
<tr>
<th>For information about</th>
<th>Refer to</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIOS update utilities</td>
<td><a href="http://support.intel.com/support/motherboards/desktop/sb/CS-034499.htm">http://support.intel.com/support/motherboards/desktop/sb/CS-034499.htm</a></td>
</tr>
</tbody>
</table>

3.5.1 Language Support

The BIOS Setup program and help messages are supported in US English. Check the Intel web site for support.
3.5.2 BIOS Recovery

It is unlikely that anything will interrupt a BIOS update; however, if an interruption occurs, the BIOS could be damaged. Table 25 lists the drives and media types that can and cannot be used for BIOS recovery. The BIOS recovery media does not need to be made bootable.

Table 25. Acceptable Drives/Media Types for BIOS Recovery

<table>
<thead>
<tr>
<th>Media Type (Note)</th>
<th>Can be used for BIOS recovery?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hard disk drive (connected to SATA or USB)</td>
<td>Yes</td>
</tr>
<tr>
<td>CD/DVD drive (connected to SATA or USB)</td>
<td>Yes</td>
</tr>
<tr>
<td>USB flash drive</td>
<td>Yes</td>
</tr>
<tr>
<td>USB diskette drive (with a 1.4 MB diskette)</td>
<td>No (BIOS update file is bigger than 1.4 MB size limit)</td>
</tr>
</tbody>
</table>

**NOTE**

Supported file systems for BIOS recovery:
- NTFS (sparse, compressed, or encrypted files are not supported)
- FAT32
- FAT16
- FAT12
- ISO 9660

For information about BIOS recovery, refer to:
3.6 Boot Options

In the BIOS Setup program, the user can choose to boot from a hard drive, optical drive, removable drive, or the network. The default setting is for the optical drive to be the first boot device, the hard drive second, removable drive third, and the network fourth.

3.6.1 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

3.6.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.6.3 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices. Table 26 lists the boot device menu options.

<table>
<thead>
<tr>
<th>Boot Device Menu Function Keys</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;↑&gt; or &lt;↓&gt;</td>
<td>Selects a default boot device</td>
</tr>
<tr>
<td>&lt;Enter&gt;</td>
<td>Exits the menu, and boots from the selected device</td>
</tr>
<tr>
<td>&lt;Esc&gt;</td>
<td>Exits the menu and boots according to the boot priority defined through BIOS setup</td>
</tr>
</tbody>
</table>
3.6.4 **Power Button Menu**

As an alternative to Back-to-BIOS Mode or normal POST Hotkeys, the user can use the power button to access a menu. The Power Button Menu is accessible via the following sequence:

1. System is in S4/S5 (not G3)
2. User pushes the power button and holds it down for 3 seconds
3. The system will emit three short beeps from the front panel (FP) audio port, then stop to signal the user to release the power button. The FP power button LED will also change from Blue to Amber when the user can release the power button.
4. User releases the power button before the 4-second shutdown override

If this boot path is taken, the BIOS will use default settings, ignoring settings in VPD where possible.

At the point where Setup Entry/Boot would be in the normal boot path, the BIOS will display the following prompt and wait for a keystroke:

<table>
<thead>
<tr>
<th>Key</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESC</td>
<td>Normal Boot</td>
</tr>
<tr>
<td>F2</td>
<td>Intel Visual BIOS</td>
</tr>
<tr>
<td>F3</td>
<td>Disable Fast Boot</td>
</tr>
<tr>
<td>F4</td>
<td>BIOS Recovery</td>
</tr>
<tr>
<td>F7</td>
<td>Update BIOS</td>
</tr>
<tr>
<td>F10</td>
<td>Enter Boot Menu</td>
</tr>
<tr>
<td>F12</td>
<td>Network Boot</td>
</tr>
</tbody>
</table>

**[F2] Enter Setup** is displayed instead if Visual BIOS is not supported.

**[F3] Disable Fast Boot** is only displayed if at least one Fast Boot optimization is enabled.

**[F9] Remote Assistance** is only displayed if Remote Assistance is supported.

If an unrecognized key is hit, then the BIOS will beep and wait for another keystroke. If one of the listed hotkeys is hit, the BIOS will follow the indicated boot path. Password requirements must still be honored.

If Disable Fast Boot is selected, the BIOS will disable all Fast Boot optimizations and reset the system.
3.7 Hard Disk Drive Password Security Feature

The Hard Disk Drive Password Security feature blocks read and write accesses to the hard disk drive until the correct password is given. Hard Disk Drive Passwords are set in BIOS SETUP and are prompted for during BIOS POST. For convenient support of S3 resume, the system BIOS will automatically unlock drives on resume from S3. Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 19 characters in length.

The User hard disk drive password, when installed, will be required upon each power-cycle until the Master Key or User hard disk drive password is submitted.

The Master Key hard disk drive password, when installed, will not lock the drive. The Master Key hard disk drive password exists as an unlock override in the event that the User hard disk drive password is forgotten. Only the installation of the User hard disk drive password will cause a hard disk to be locked upon a system power-cycle.

Table 27 shows the effects of setting the Hard Disk Drive Passwords.

<table>
<thead>
<tr>
<th>Password Set</th>
<th>Password During Boot</th>
</tr>
</thead>
<tbody>
<tr>
<td>Neither</td>
<td>None</td>
</tr>
<tr>
<td>Master only</td>
<td>None</td>
</tr>
<tr>
<td>User only</td>
<td>User only</td>
</tr>
<tr>
<td>Master and User Set</td>
<td>Master or User</td>
</tr>
</tbody>
</table>

During every POST, if a User hard disk drive password is set, POST execution will pause with the following prompt to force the user to enter the Master Key or User hard disk drive password:

Enter Hard Disk Drive Password:

Upon successful entry of the Master Key or User hard disk drive password, the system will continue with normal POST.

If the hard disk drive password is not correctly entered, the system will go back to the above prompt. The user will have three attempts to correctly enter the hard disk drive password. After the third unsuccessful hard disk drive password attempt, the system will halt with the message:

Hard Disk Drive Password Entry Error

A manual power cycle will be required to resume system operation.

NOTE

As implemented on Intel NUC Board NUC5i5RYB and Intel NUC Board NUC5i3RYB, Hard Disk Drive Password Security is only supported on either SATA port 0 (M.2) or SATA Port 1 (onboard SATA connector). The passwords are stored on the hard disk drive so if the drive is relocated to another computer that does not support Hard Disk Drive Password Security feature, the drive will not be accessible.
3.8 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.
- To clear a set password, enter a blank password after entering the existing password.

Table 28 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

**Table 28. Supervisor and User Password Functions**

<table>
<thead>
<tr>
<th>Password Set</th>
<th>Supervisor Mode</th>
<th>User Mode</th>
<th>Setup Options</th>
<th>Password to Enter Setup</th>
<th>Password During Boot</th>
</tr>
</thead>
<tbody>
<tr>
<td>Neither</td>
<td>Can change all options (Note)</td>
<td>Can change all options (Note)</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Supervisor only</td>
<td>Can change all options</td>
<td>Can change a limited number of options</td>
<td>Supervisor Password</td>
<td>Supervisor</td>
<td>None</td>
</tr>
<tr>
<td>User only</td>
<td>N/A</td>
<td>Can change all options</td>
<td>Enter Password Clear User Password</td>
<td>User</td>
<td>User</td>
</tr>
<tr>
<td>Supervisor and user set</td>
<td>Can change all options</td>
<td>Can change a limited number of options</td>
<td>Supervisor Password Enter Password</td>
<td>Supervisor or user</td>
<td>Supervisor or user</td>
</tr>
</tbody>
</table>

Note: If no password is set, any user can change all Setup options.
4  Error Messages and Blink Codes

4.1  Front-panel Power LED Blink Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's front panel power LED to blink an error message describing the problem (see Table 29).

Table 29. Front-panel Power LED Blink Codes

<table>
<thead>
<tr>
<th>Type</th>
<th>Pattern</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-on</td>
<td>Solid on primary color. Indicates S0 state.</td>
<td>Default to On; can be disabled via BIOS Setup</td>
</tr>
<tr>
<td>BIOS update in progress</td>
<td>Off when the update begins, then on for 0.5 seconds, then off for 0.5 seconds. The pattern repeats until the BIOS update is complete.</td>
<td></td>
</tr>
<tr>
<td>Video error (Note)</td>
<td>On-off (1.0 second each) two times, then 2.5-second pause (off), entire pattern repeats (blink and pause) until the system is powered off.</td>
<td>When no VGA option ROM is found</td>
</tr>
<tr>
<td>Memory error</td>
<td>On-off (1.0 second each) three times, then 2.5-second pause (off), entire pattern repeats (blinks and pause) until the system is powered off.</td>
<td></td>
</tr>
<tr>
<td>Thermal trip warning</td>
<td>Each beep will be accompanied by the following blink pattern: .25 seconds on, .25 seconds off, .25 seconds on, .25 seconds off. This will result in a total of 16 blinks.</td>
<td></td>
</tr>
</tbody>
</table>

Note: Disabled per default BIOS setup option.

4.2  BIOS Error Messages

Table 30 lists the error messages and provides a brief description of each.

Table 30. BIOS Error Messages

<table>
<thead>
<tr>
<th>Error Message</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Battery Low</td>
<td>The battery may be losing power. Replace the battery soon.</td>
</tr>
<tr>
<td>CMOS Checksum Bad</td>
<td>The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.</td>
</tr>
<tr>
<td>Memory Size Decreased</td>
<td>Memory size has decreased since the last boot. If no memory was removed, then memory may be bad.</td>
</tr>
<tr>
<td>No Boot Device Available</td>
<td>System did not find a device to boot.</td>
</tr>
</tbody>
</table>
5 Intel NUC Kit Features

5.1 Chassis Front Panel Features

See the Product Identification Information section on page Error! Bookmark not defined. to identify Intel NUC Boards and their respective kit or system. Figure 21 and Error! Reference source not found. shows the location of the features located on or near the front of the chassis.

Table 30 lists the components identified in Figure 21.

<table>
<thead>
<tr>
<th>Item from Figure 21</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Kensington* Anti-Theft Key Lock Hole</td>
</tr>
<tr>
<td></td>
<td>Power Switch and Power LED</td>
</tr>
<tr>
<td></td>
<td>Consumer Infrared Sensor</td>
</tr>
<tr>
<td></td>
<td>Speaker/Headset Jack</td>
</tr>
<tr>
<td></td>
<td>USB 3.1 Type A Connectors</td>
</tr>
</tbody>
</table>
5.2 Chassis Rear Panel Features

Figure 22 shows the location of the features located on the rear of the chassis.

Figure 22. Intel NUC Kit NUC5i3RYH Features – Rear

Table 31 lists the components identified in Figure 22.

Table 31. Components Shown in Figure 22

<table>
<thead>
<tr>
<th>Item from Figure 22</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>19V DC Power Inlet</td>
<td></td>
</tr>
<tr>
<td>Cooling Vents</td>
<td></td>
</tr>
<tr>
<td>Mini DisplayPort</td>
<td></td>
</tr>
<tr>
<td>USB 3.1 Type A connectors</td>
<td></td>
</tr>
<tr>
<td>Ethernet Port</td>
<td></td>
</tr>
<tr>
<td>Mini High Definition Multimedia Interface Connector</td>
<td></td>
</tr>
</tbody>
</table>