

REVISION HISTORY				
ZONE	REV	DESCRIPTION	DATE	APPROVED

# GALILEO

INTEL QUARK X1000

FAB D

PB: G87173-204

PBA: G87171-400

LB1



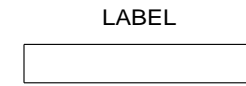
WEEE

LB6V1



1500X500\_TARGET  
SERIAL NUMBER

LB3



1375X250\_TARGET  
MAC ADDRESS LABEL

DRAWN BY	DATE	<b>INTEL CORPORATION</b> 2111 NE 25TH AVENUE HILLSBORO OR 97124		
APPROVED BY	DATE			
TITLE		DOCUMENT NUMBER	REV	
GALILEO		G87171	1.0	
SHEET 1 OF 27				

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D

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C

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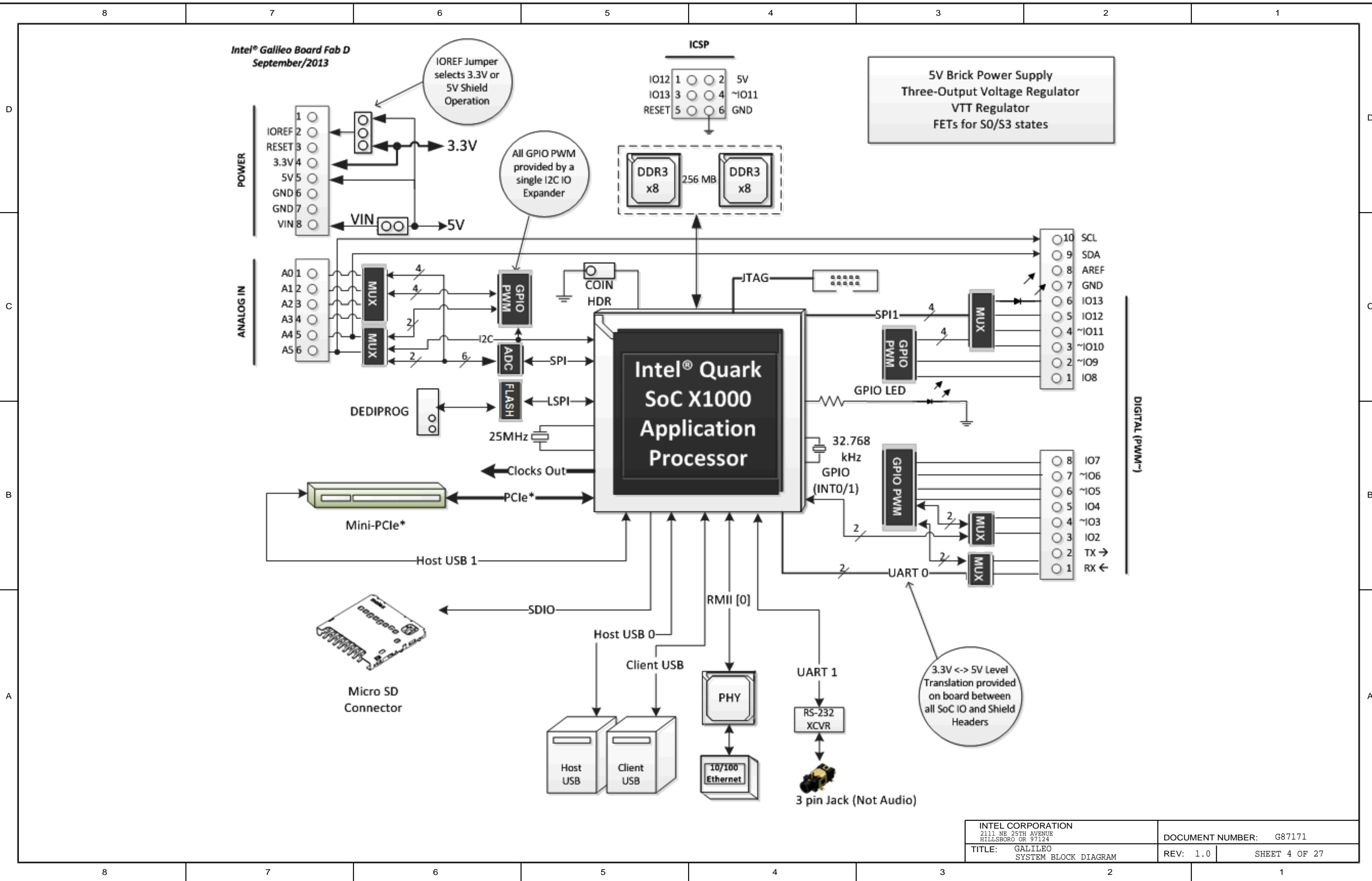
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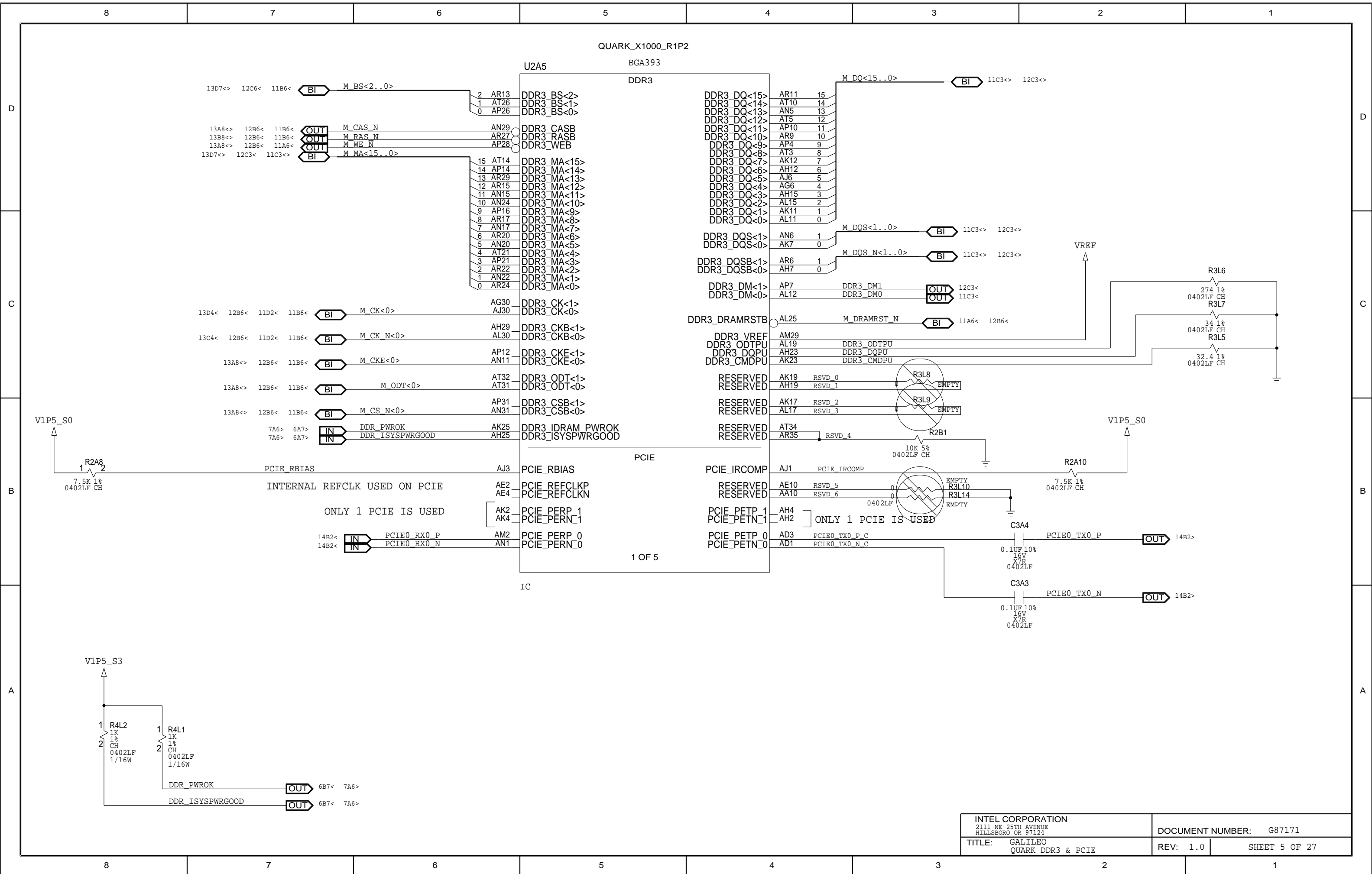
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A

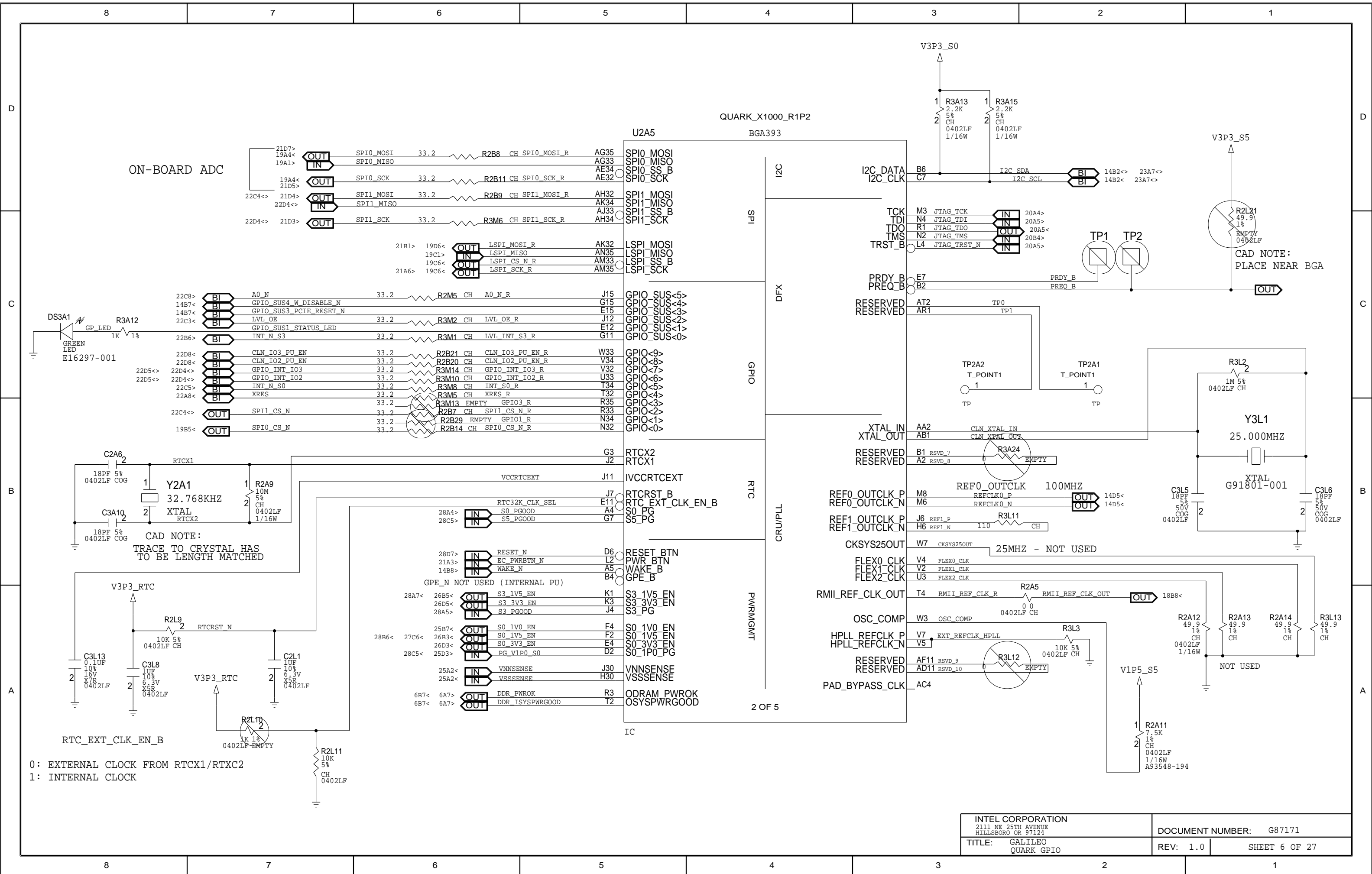
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INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO DISCLAIMER		REV: 1.0	SHEET 3 OF 27



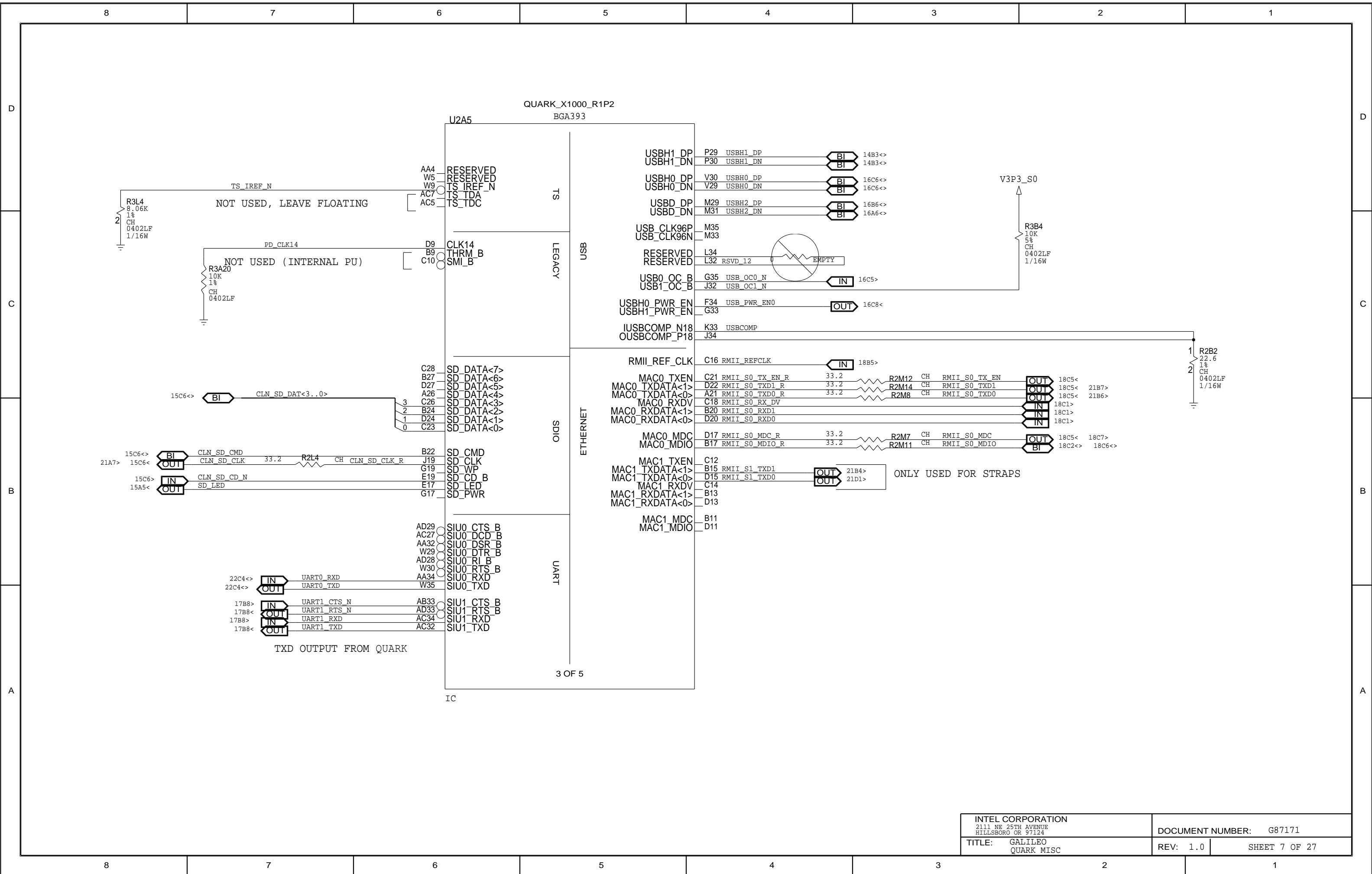


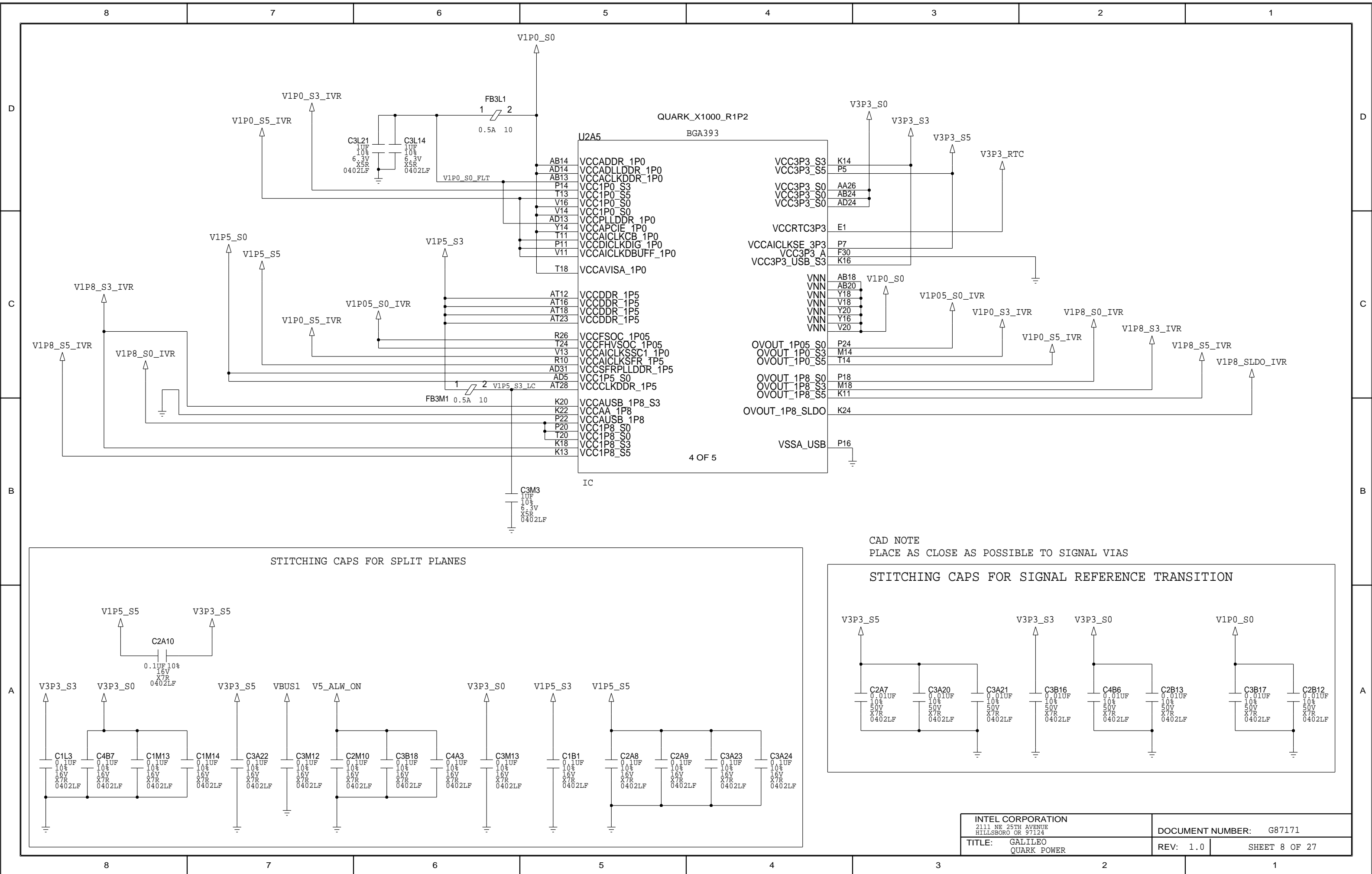
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO QUARK DDR3 & PCIE		REV: 1.0	SHEET 5 OF 27



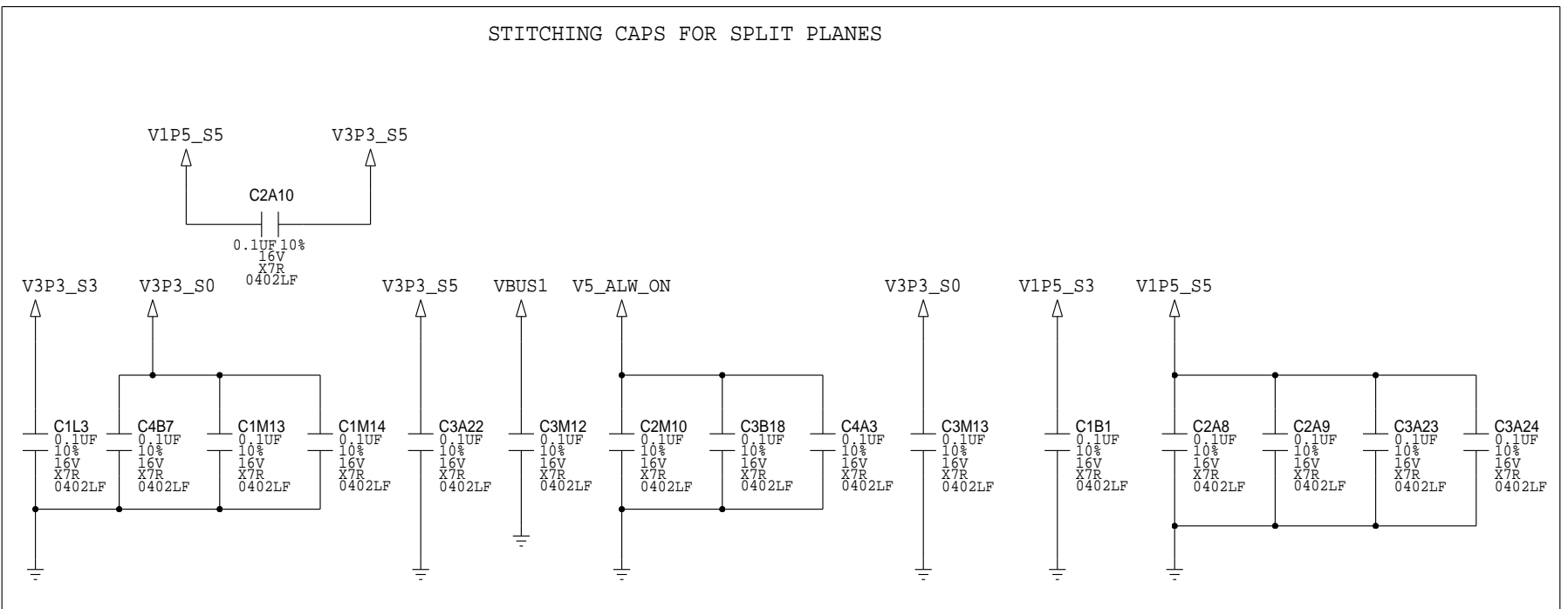
0: EXTERNAL CLOCK FROM RTCX1/RTCX2  
 1: INTERNAL CLOCK

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO QUARK GPIO		REV: 1.0	SHEET 6 OF 27



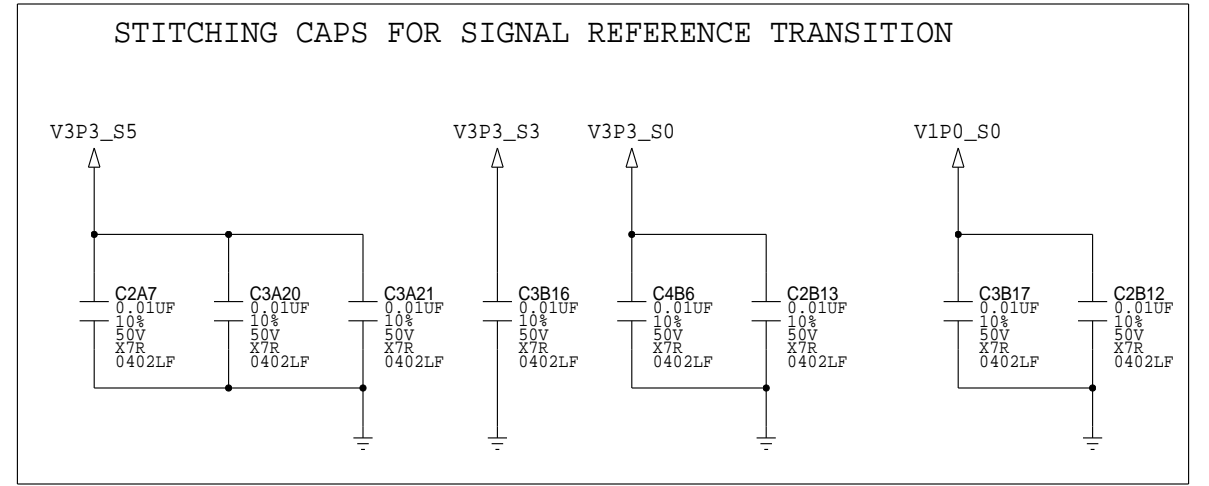


STITCHING CAPS FOR SPLIT PLANES



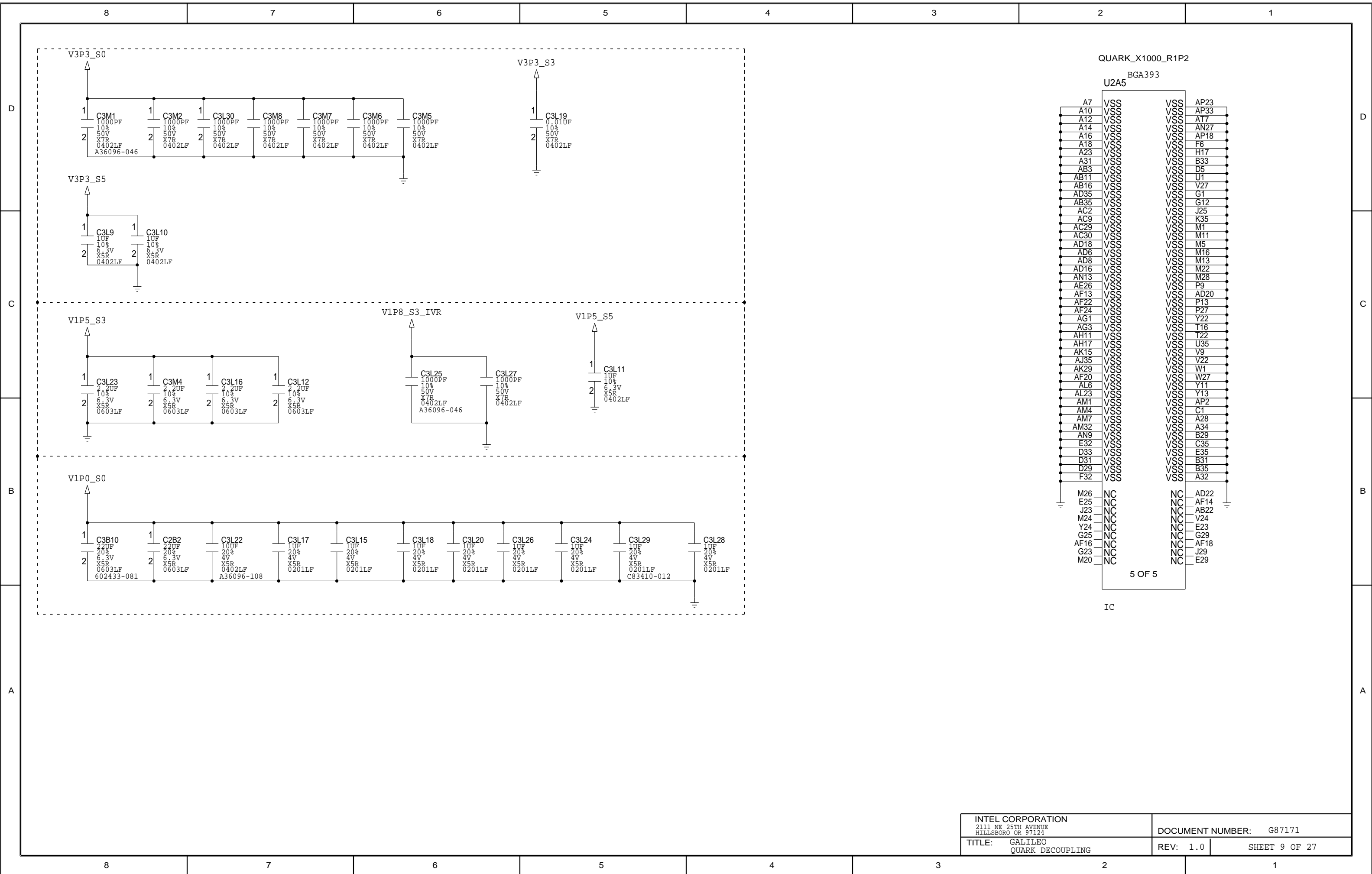
CAD NOTE  
PLACE AS CLOSE AS POSSIBLE TO SIGNAL VIAS

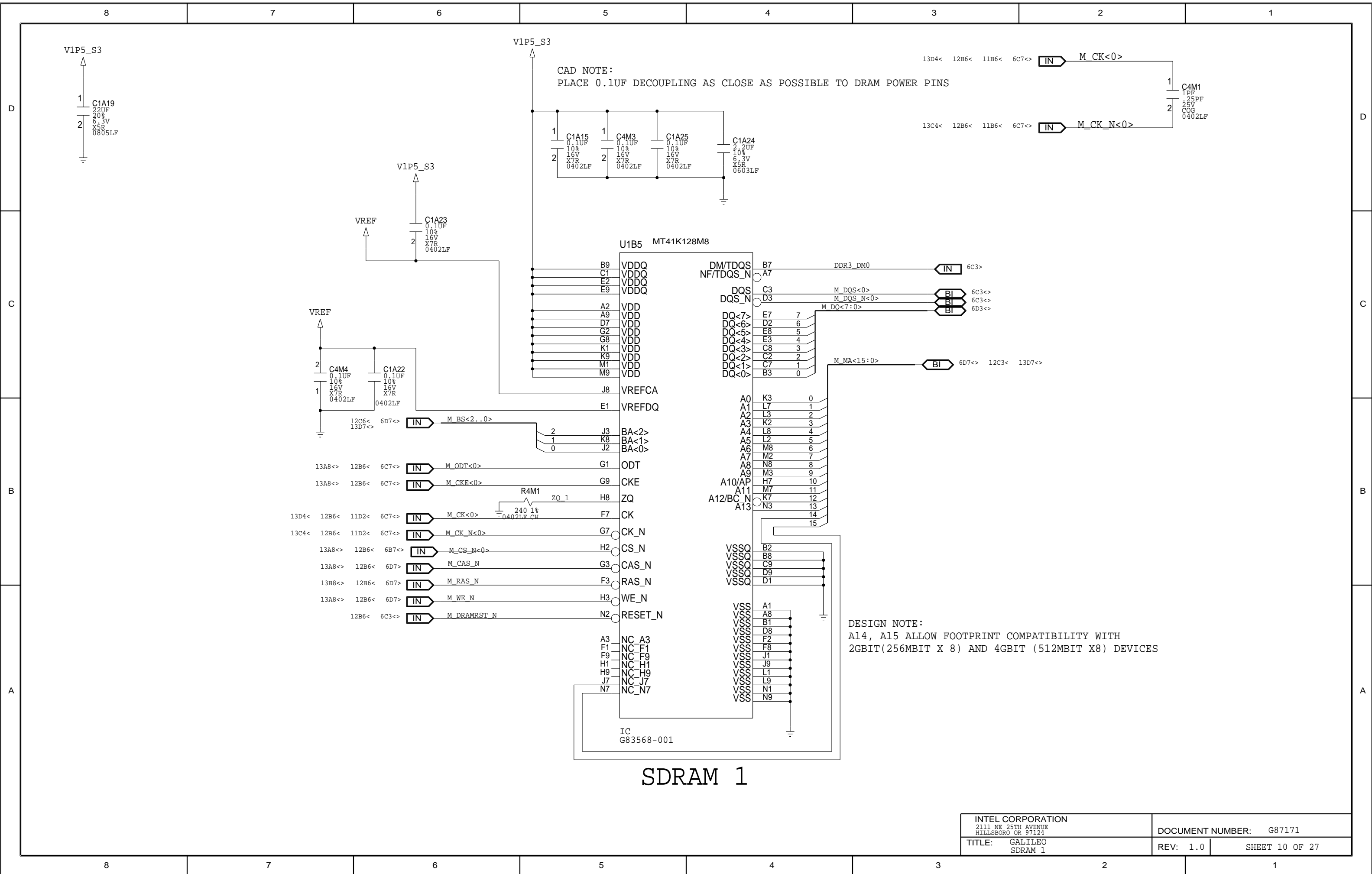
STITCHING CAPS FOR SIGNAL REFERENCE TRANSITION



INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO QUARK POWER		REV: 1.0	SHEET 8 OF 27







INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO SDRAM 1		REV: 1.0	SHEET 10 OF 27

D

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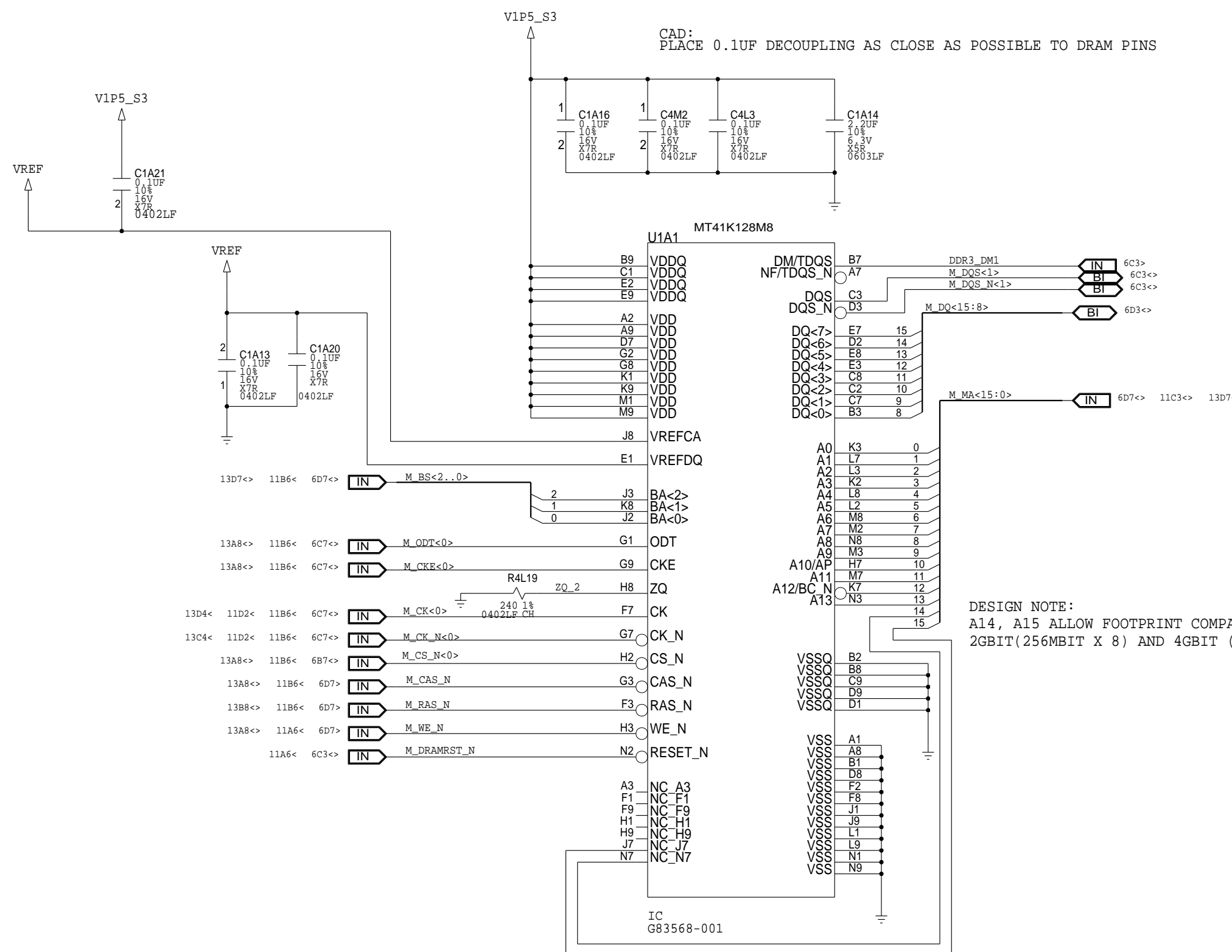
A

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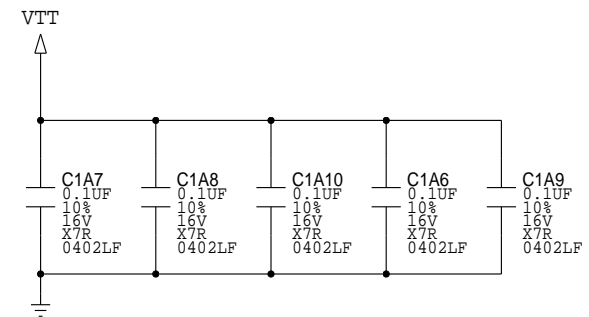
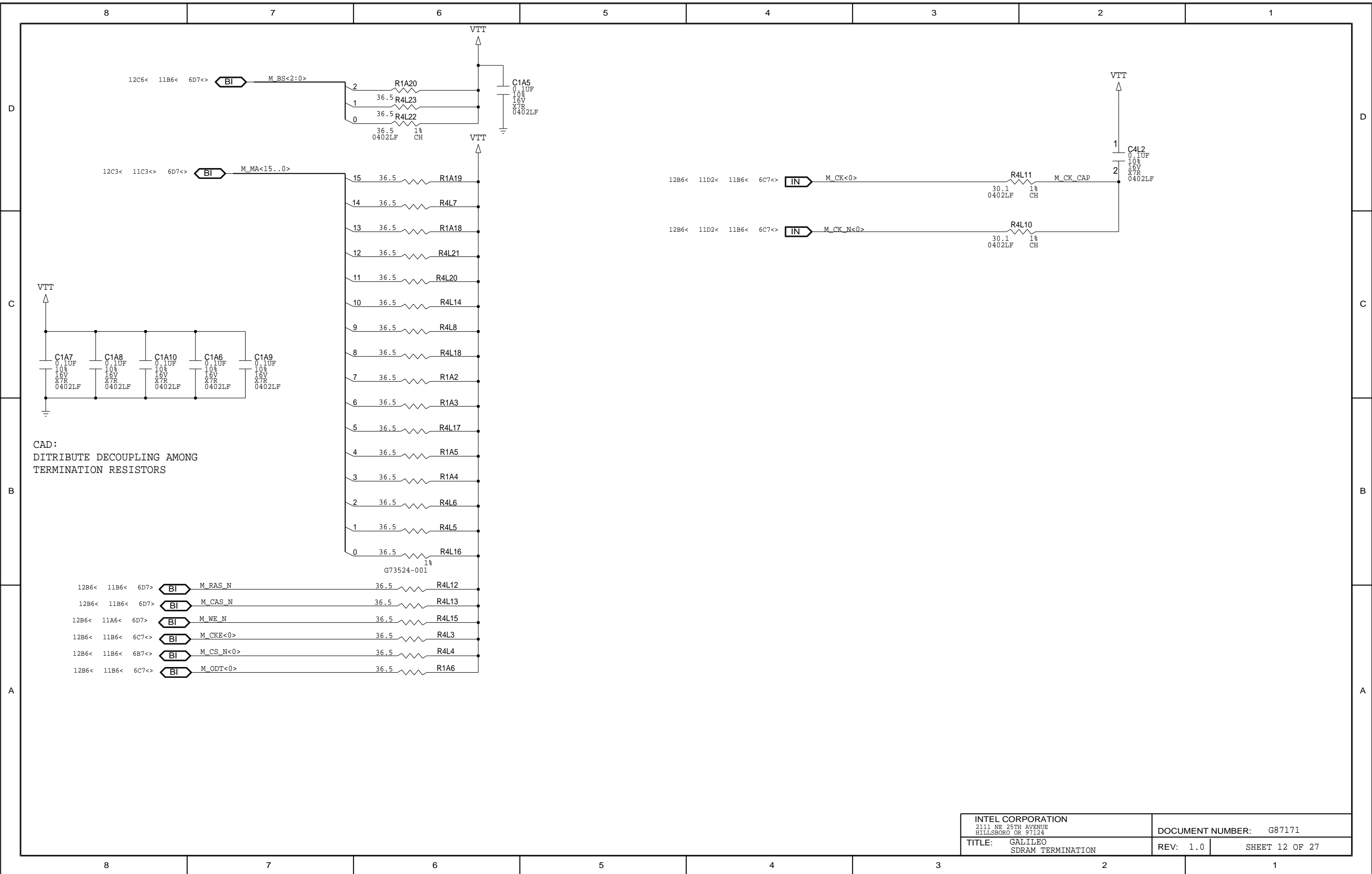
C

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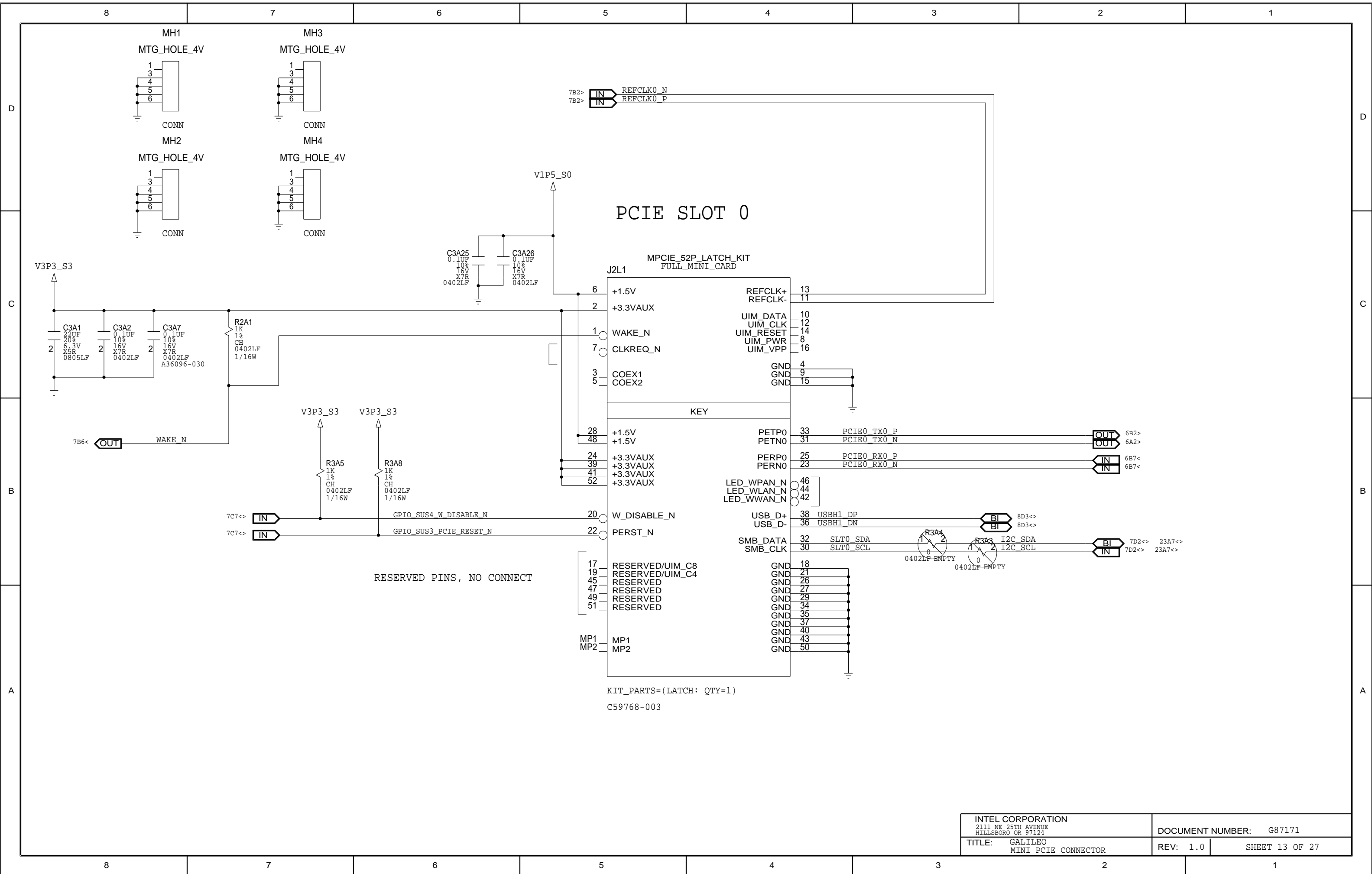


INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO SDRAM 2		REV: 1.0	SHEET 11 OF 27



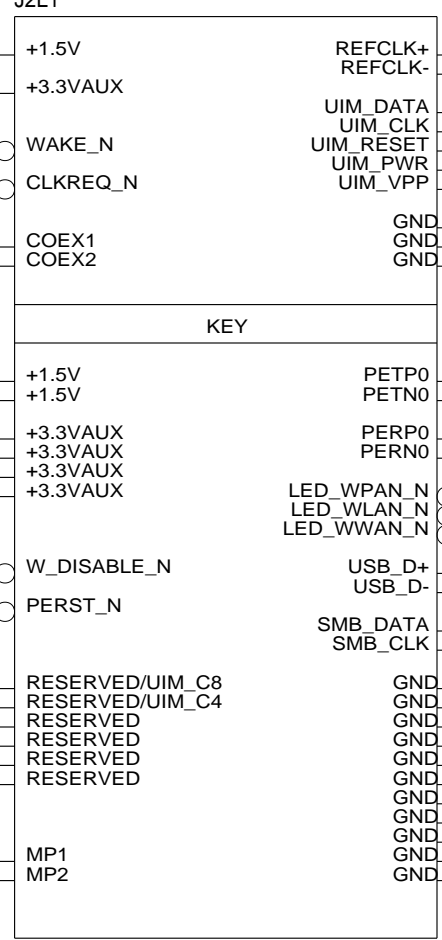
CAD:  
DITRIBUTE DECOUPLING AMONG  
TERMINATION RESISTORS

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO SDRAM TERMINATION		REV: 1.0	SHEET 12 OF 27



PCIE SLOT 0

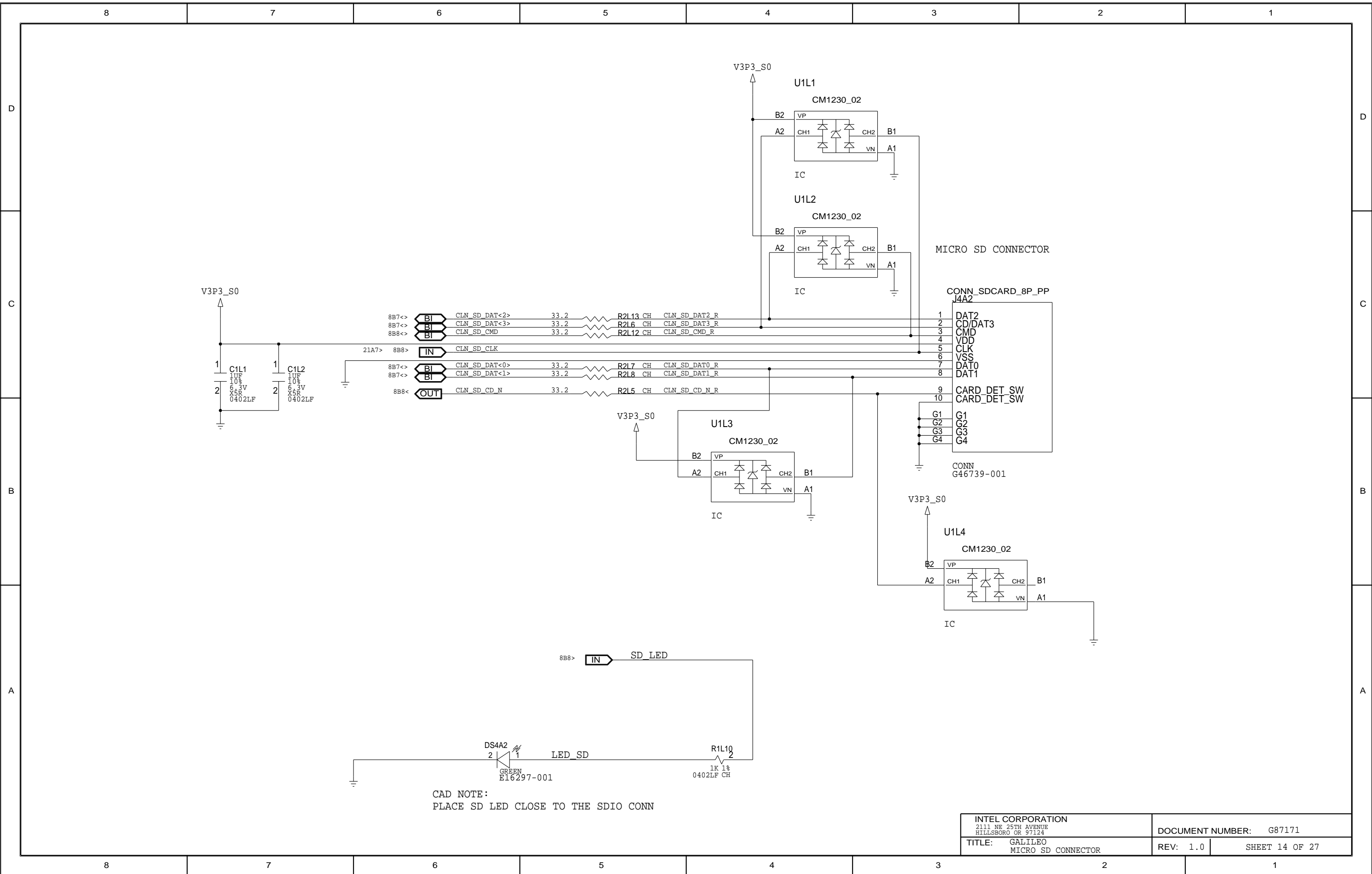
MPCIE\_52P\_LATCH\_KIT  
FULL\_MINI\_CARD



RESERVED PINS, NO CONNECT

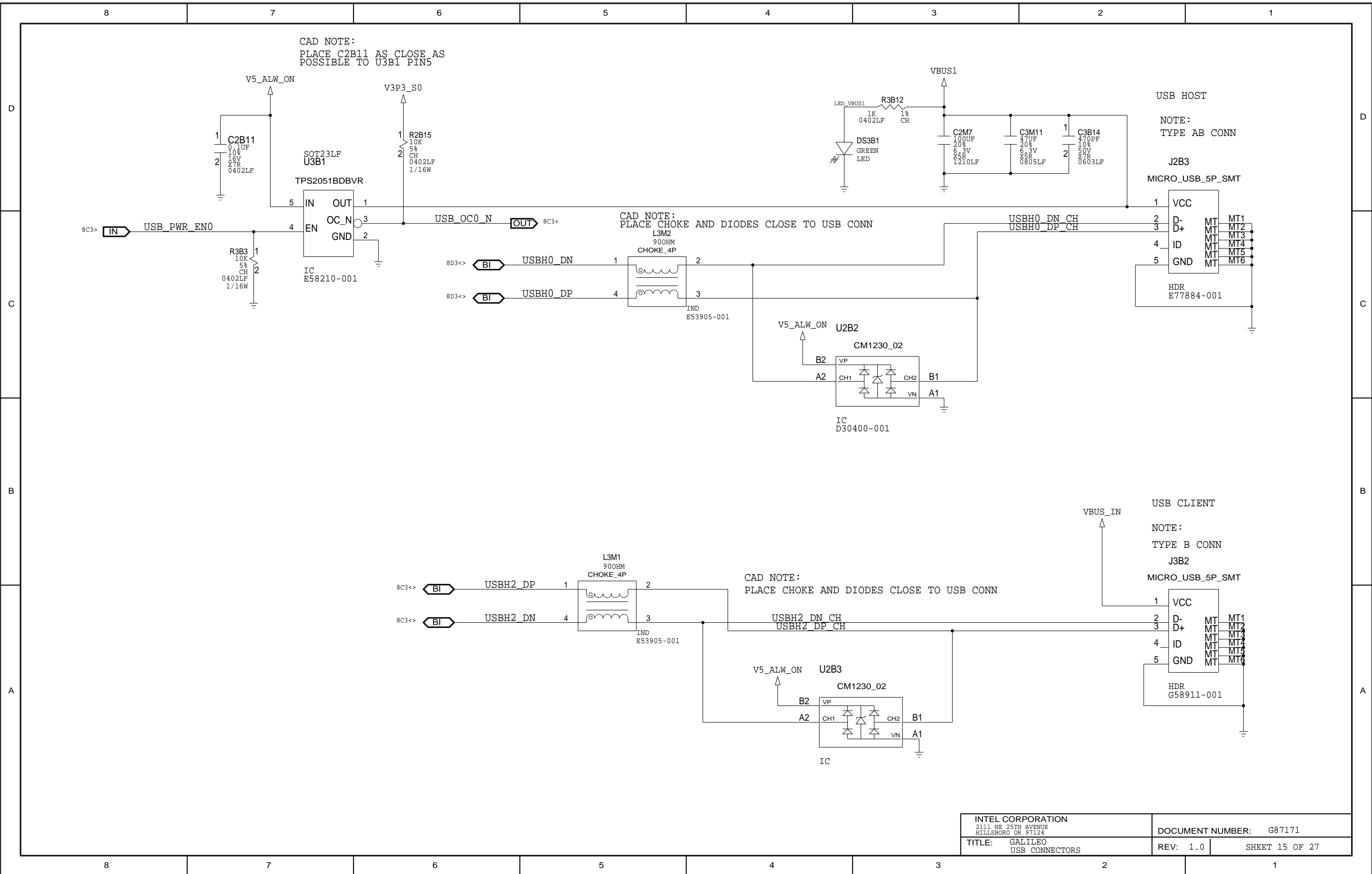
KIT\_PARTS=(LATCH: QTY=1)  
C59768-003

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO MINI PCIE CONNECTOR		REV: 1.0	SHEET 13 OF 27

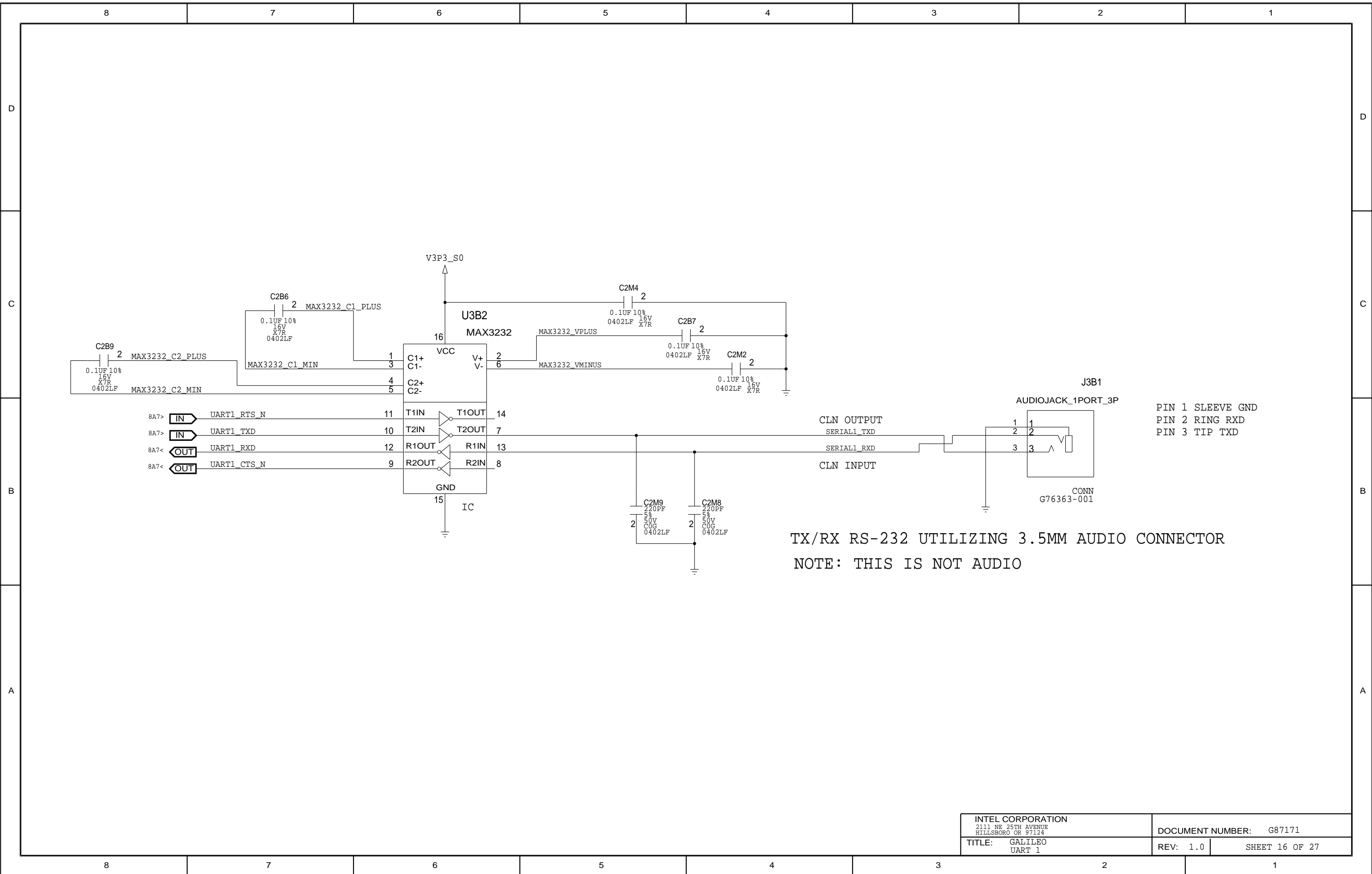


CAD NOTE:  
PLACE SD LED CLOSE TO THE SDIO CONN

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO MICRO SD CONNECTOR		REV: 1.0	SHEET 14 OF 27



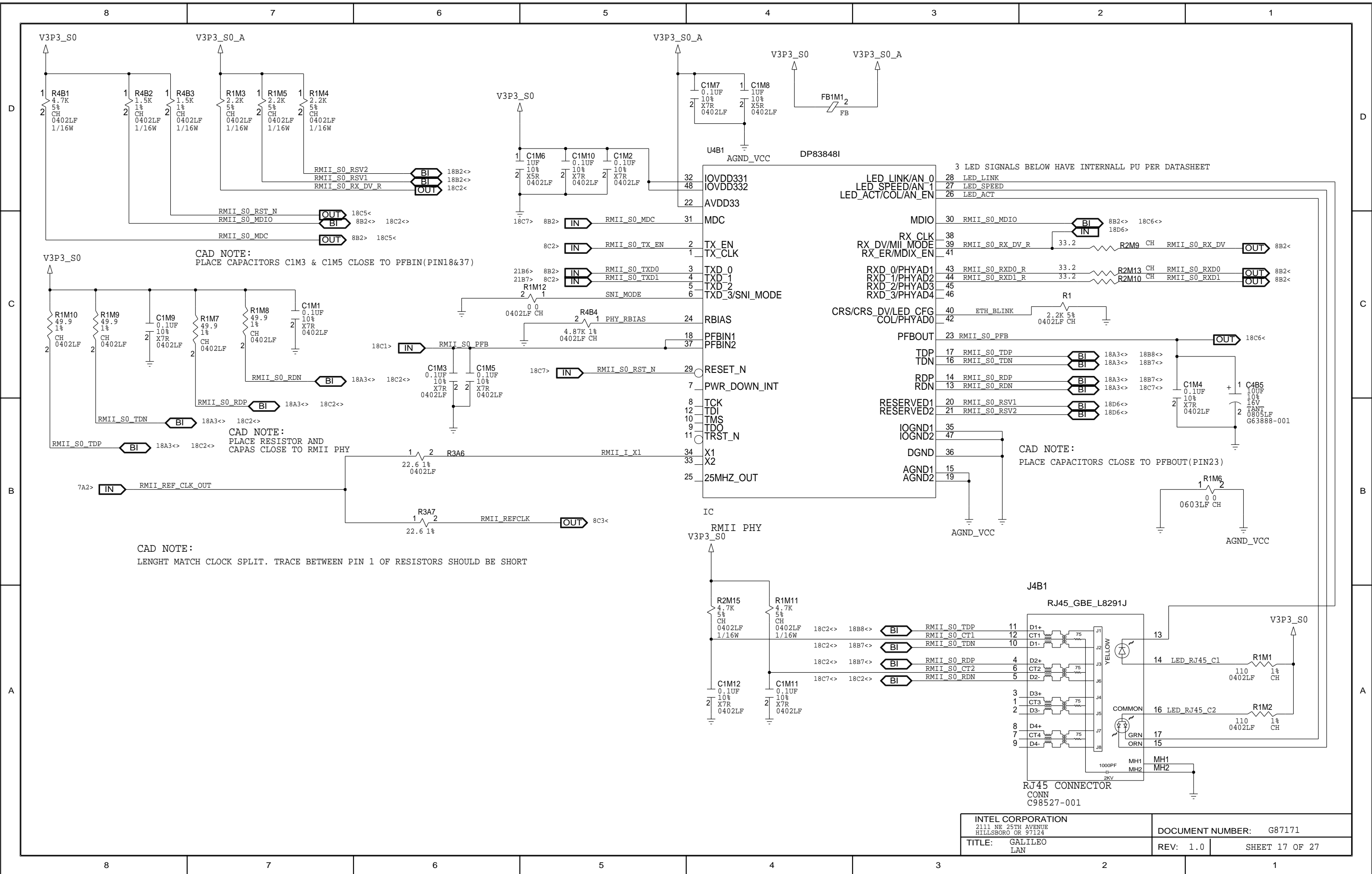
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO USB CONNECTORS		REV: 1.0	SHEET 15 OF 27



TX/RX RS-232 UTILIZING 3.5MM AUDIO CONNECTOR  
 NOTE: THIS IS NOT AUDIO

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO UART 1		REV: 1.0	SHEET 16 OF 27



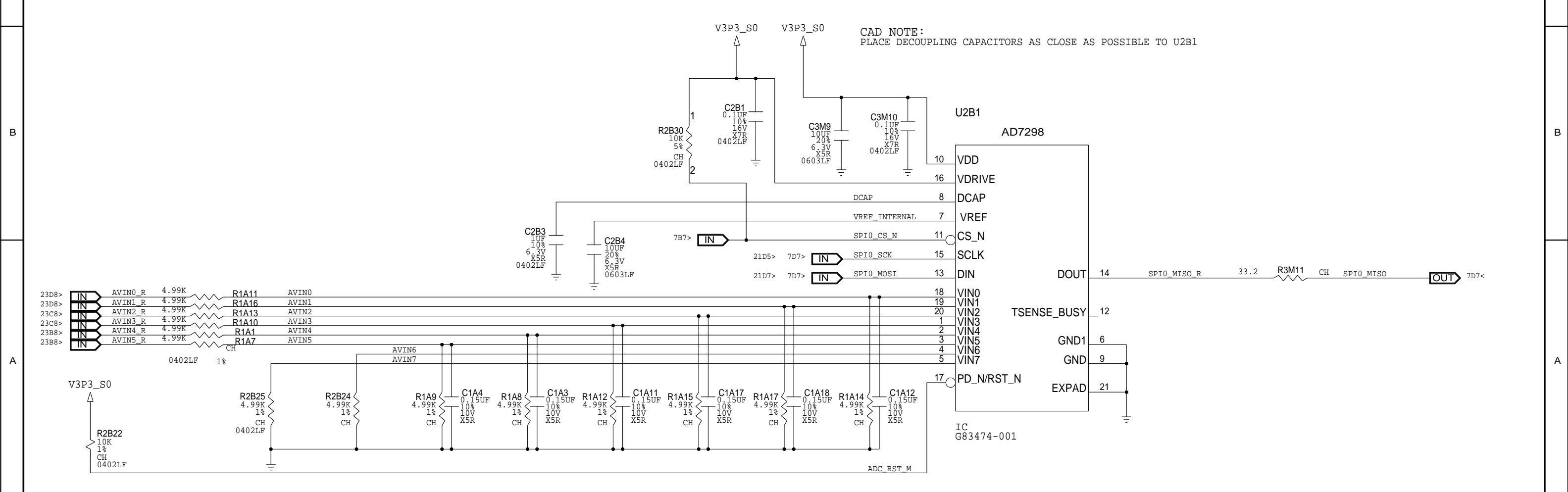
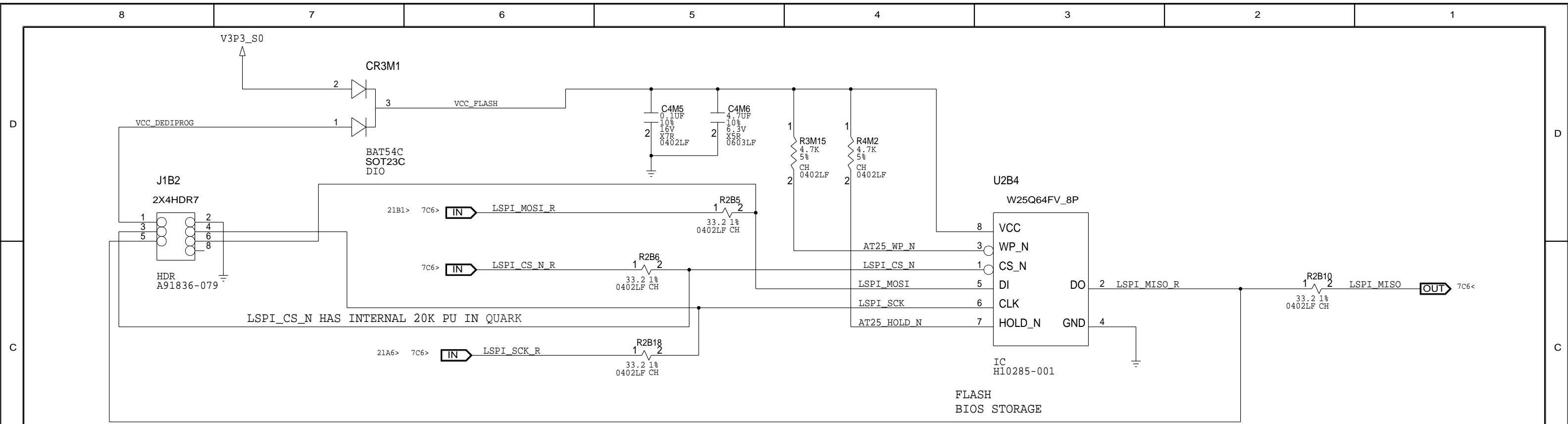


CAD NOTE:  
PLACE CAPACITORS C1M3 & C1M5 CLOSE TO PFBIN(PIN18&37)

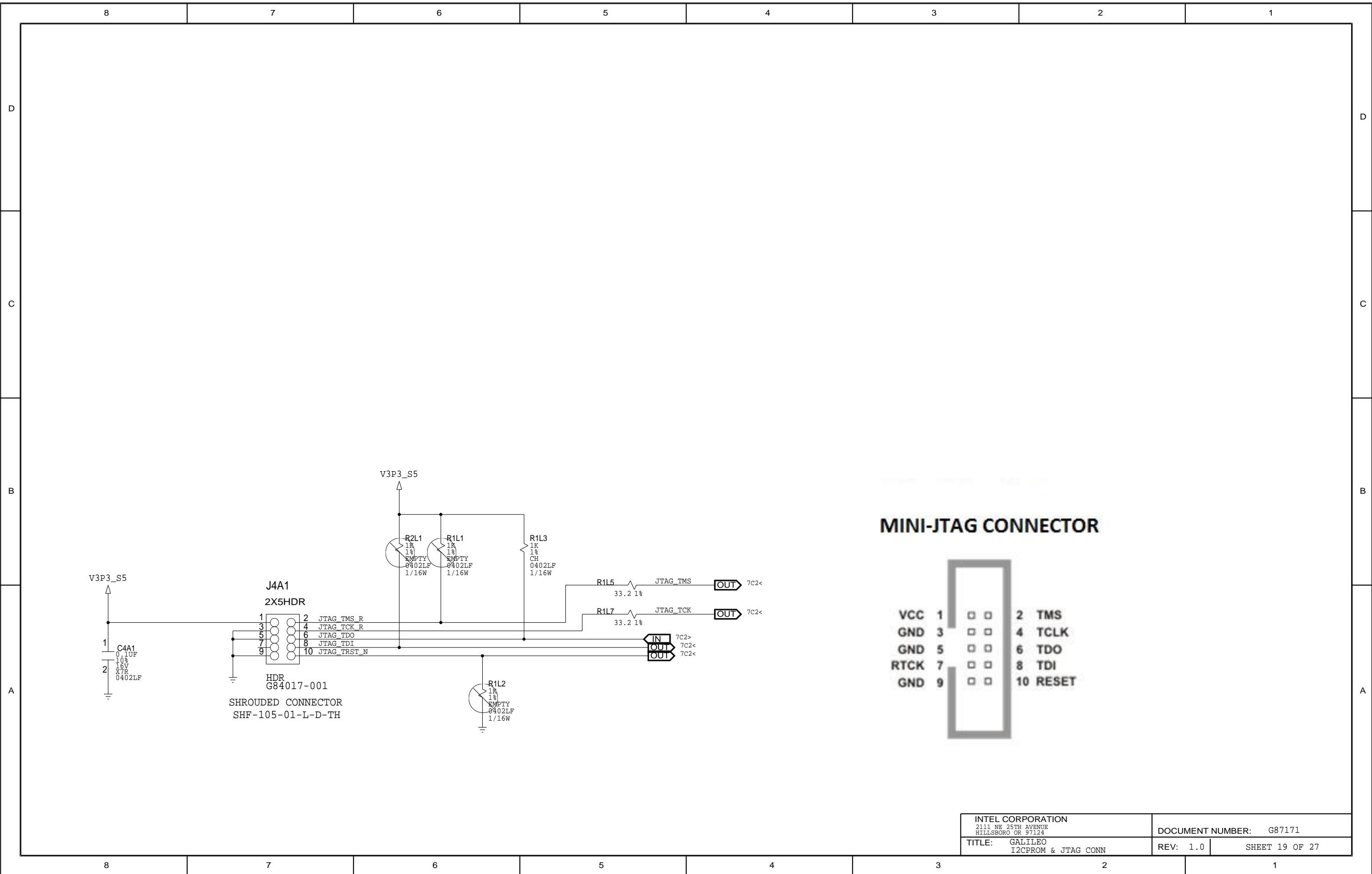
CAD NOTE:  
PLACE RESISTOR AND CAPAS CLOSE TO RMIIS0 PHY

CAD NOTE:  
LENGHT MATCH CLOCK SPLIT. TRACE BETWEEN PIN 1 OF RESISTORS SHOULD BE SHORT

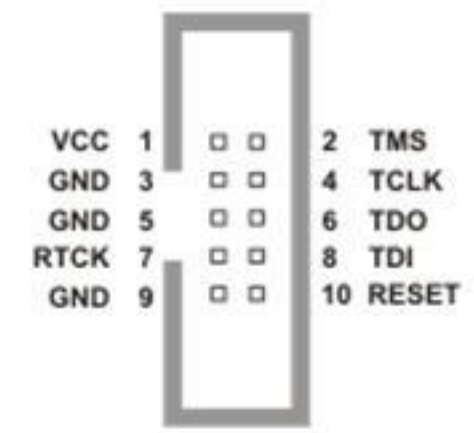
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171
TITLE: GALILEO LAN	REV: 1.0	SHEET 17 OF 27



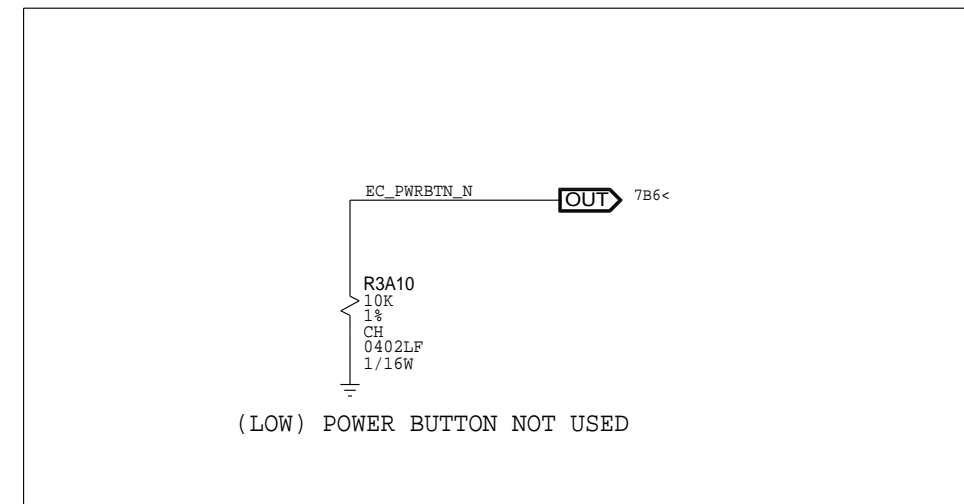
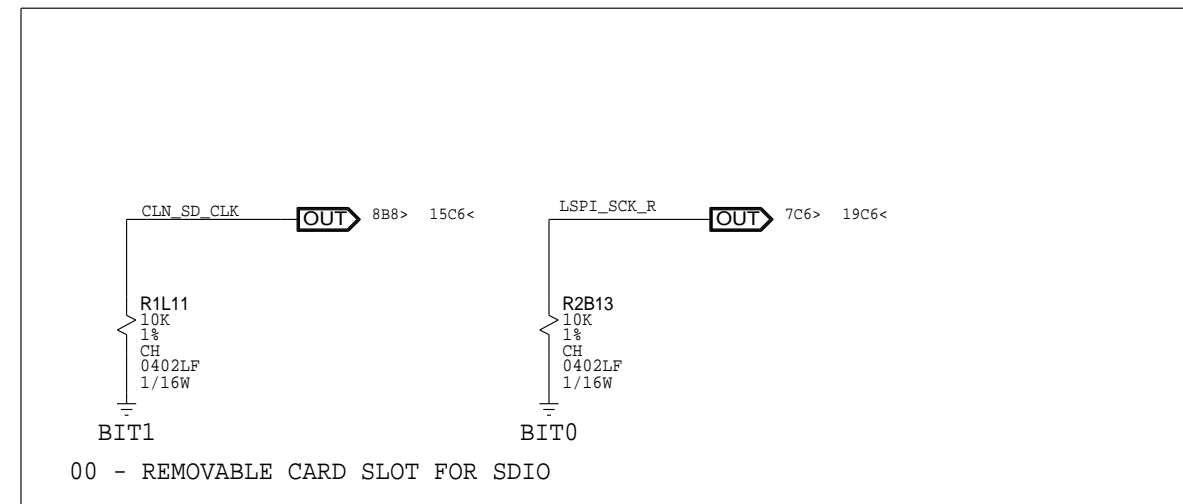
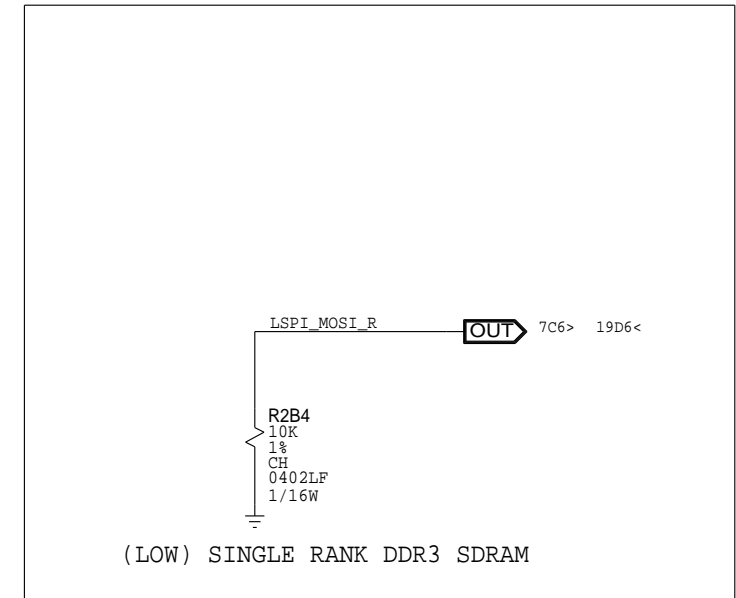
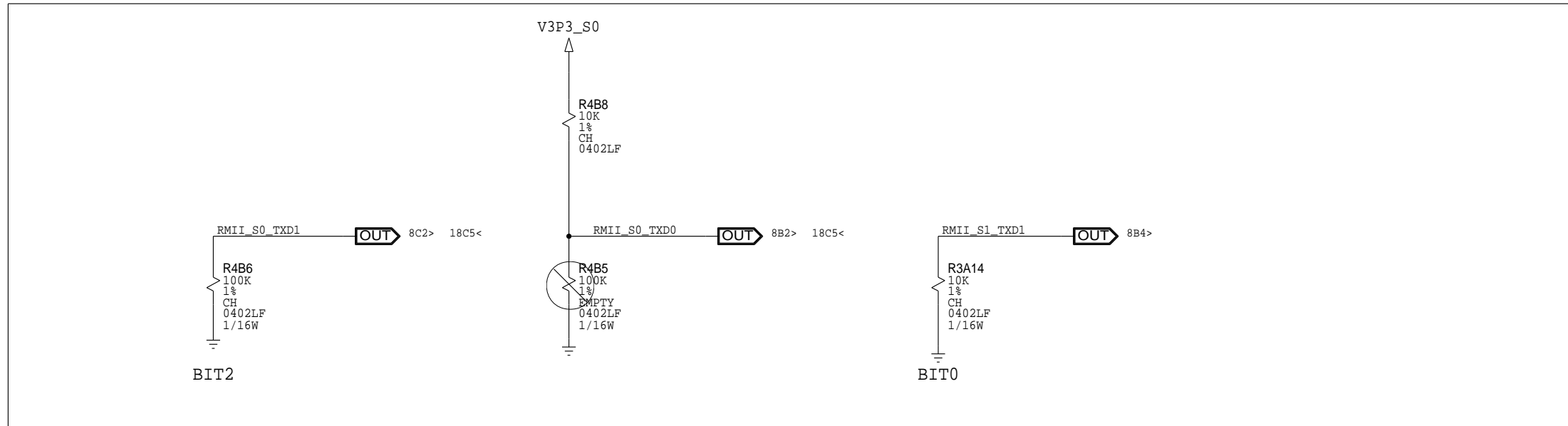
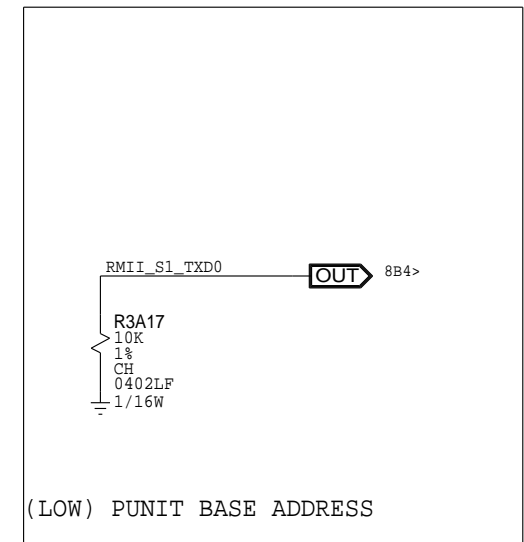
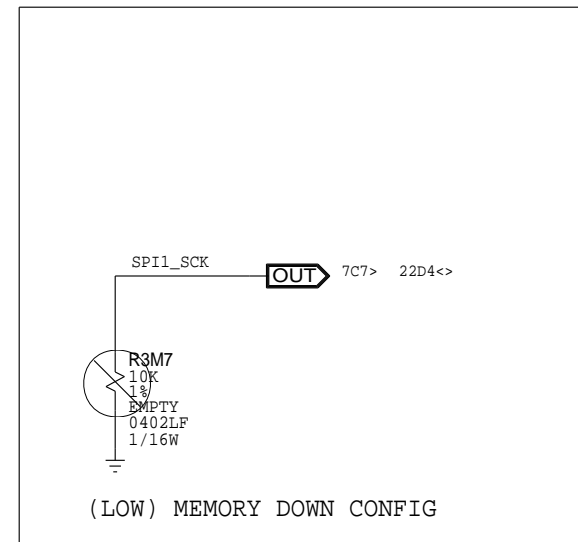
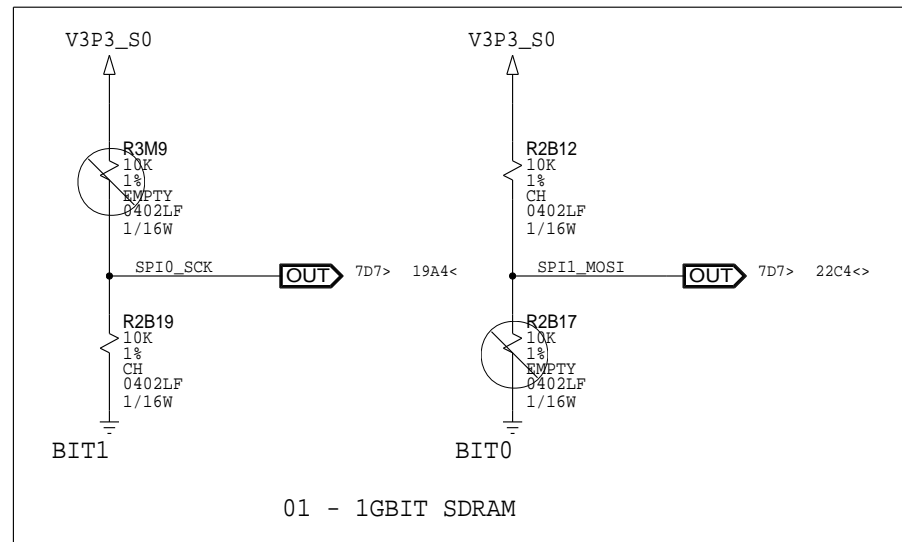
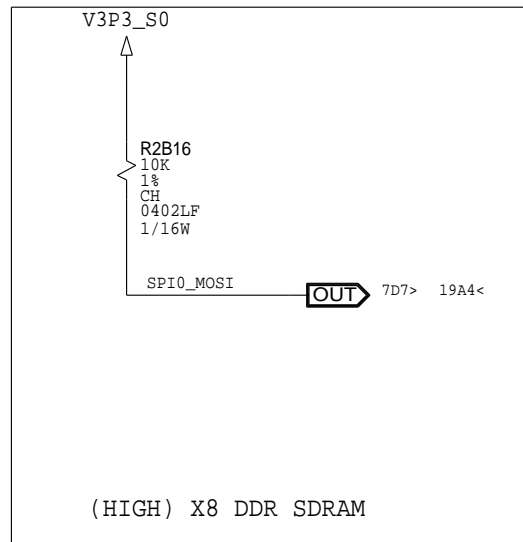
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO SPI: ADC&FLASH		REV: 1.0	SHEET 18 OF 27

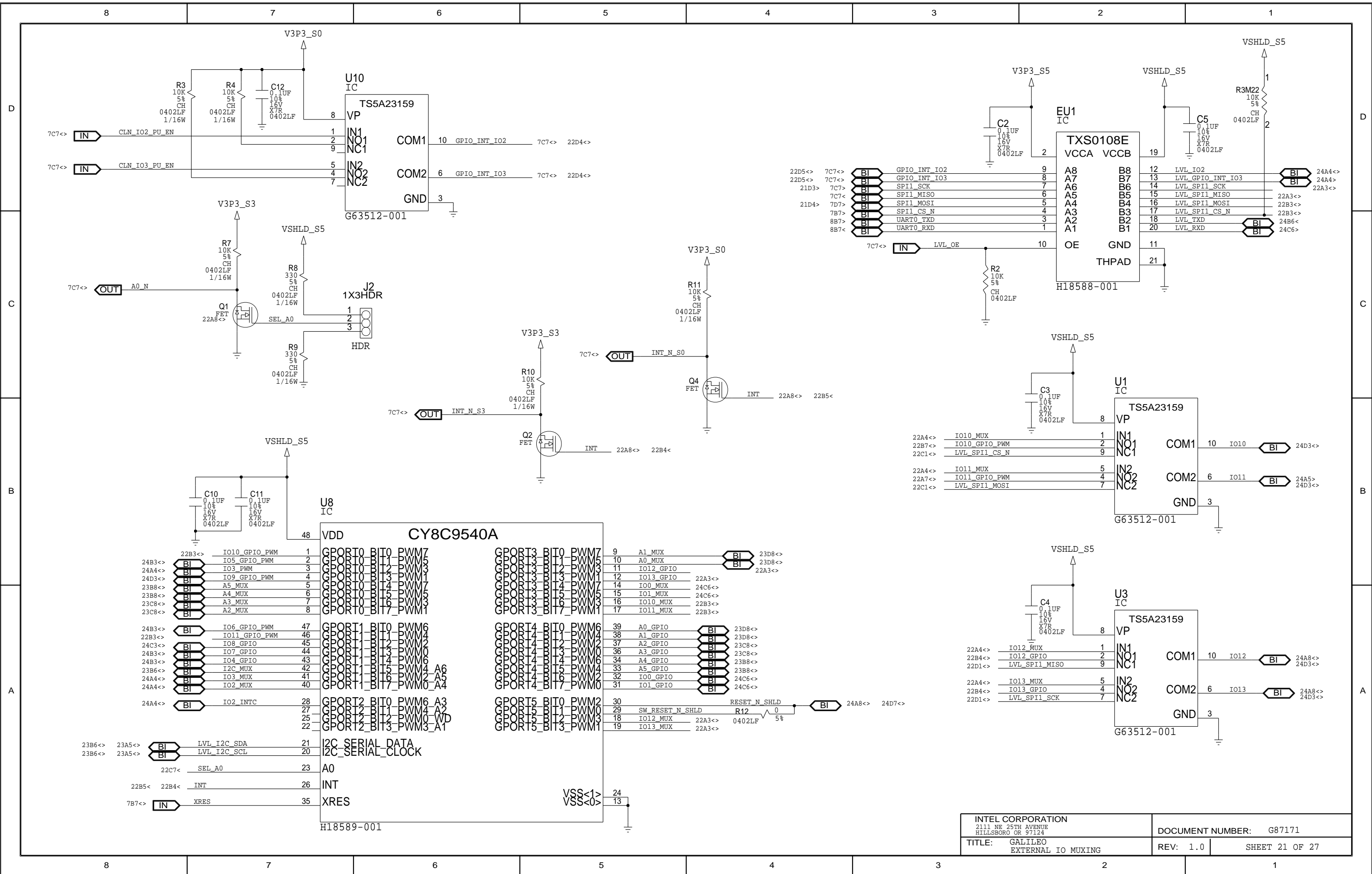


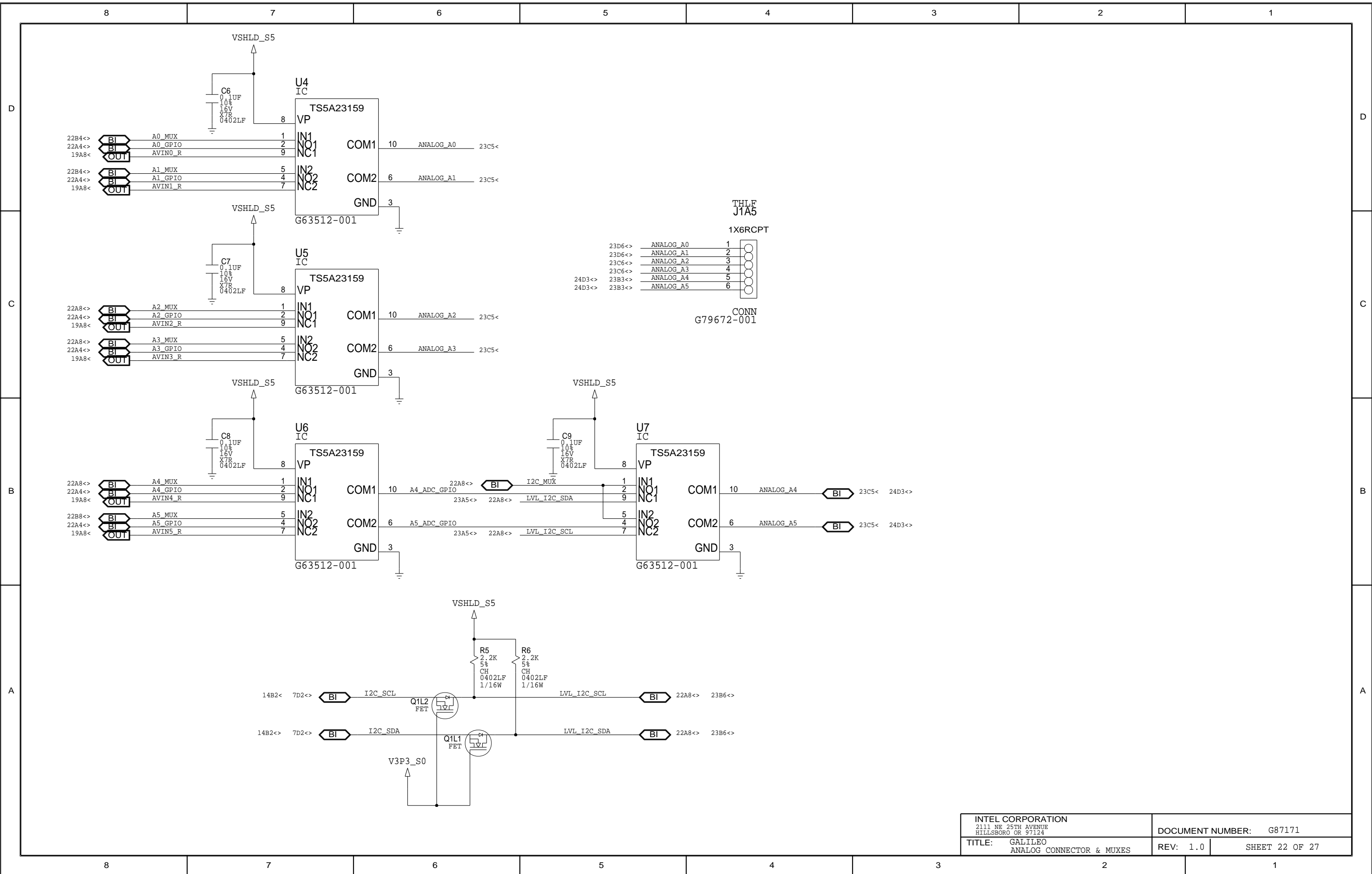
### MINI-JTAG CONNECTOR



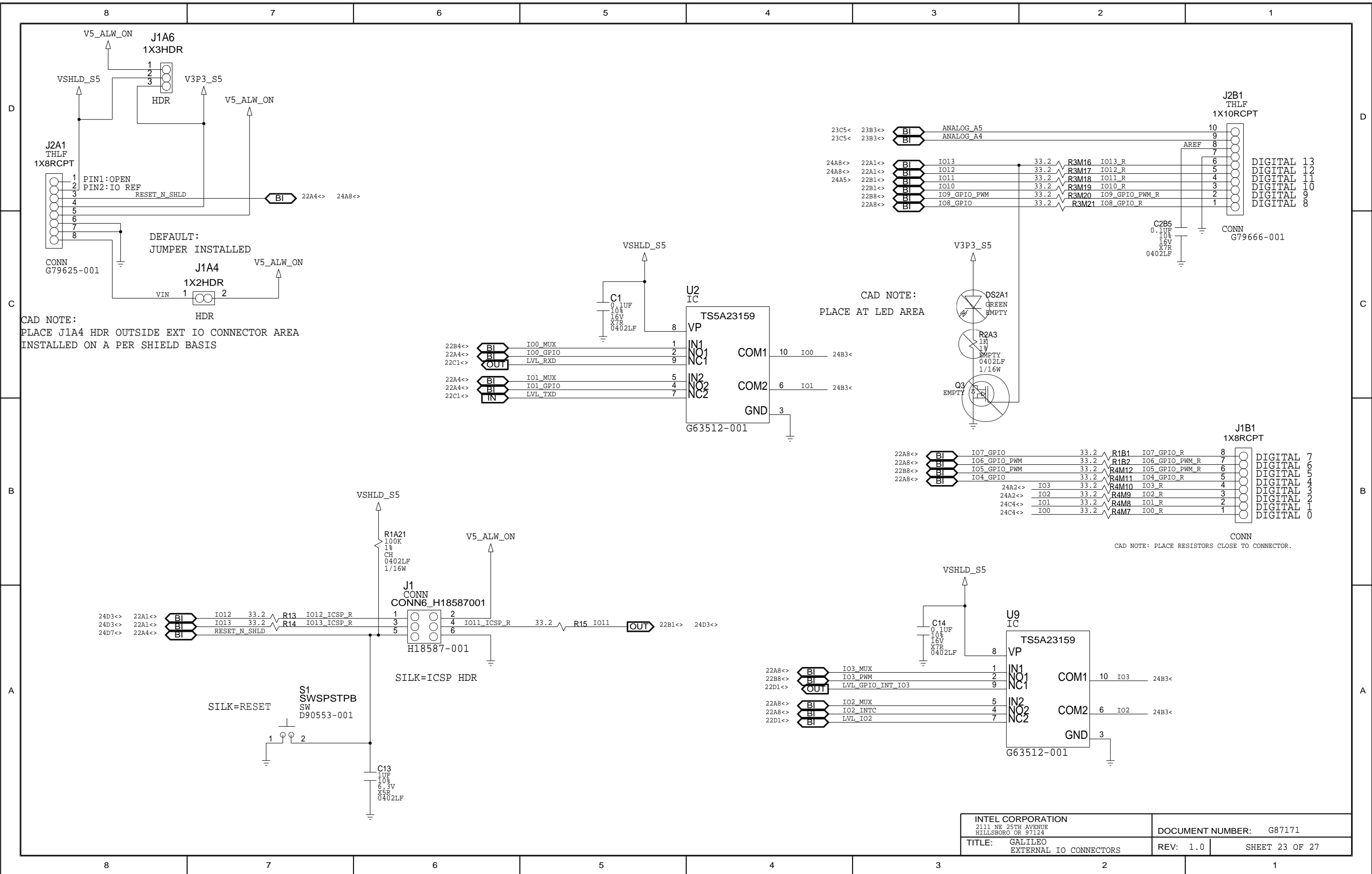
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO I2CPROM & JTAG CONN		REV: 1.0	SHEET 19 OF 27







INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO ANALOG CONNECTOR & MUXES		REV: 1.0	SHEET 22 OF 27

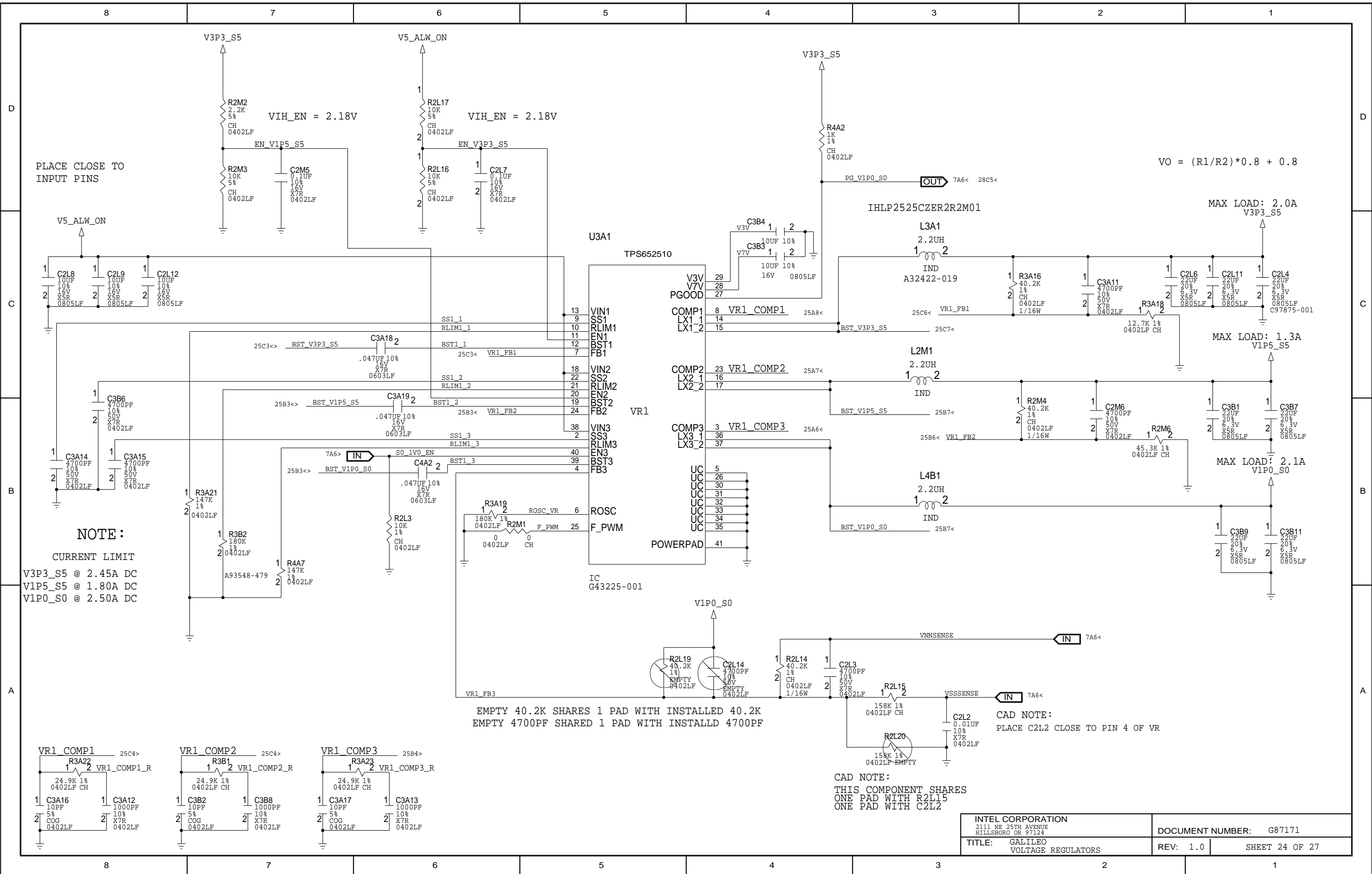


CAD NOTE:  
PLACE J1A4 HDR OUTSIDE EXT IO CONNECTOR AREA  
INSTALLED ON A PER SHIELD BASIS

CAD NOTE:  
PLACE AT LED AREA

CAD NOTE: PLACE RESISTORS CLOSE TO CONNECTOR.

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO EXTERNAL IO CONNECTORS		REV: 1.0	SHEET 23 OF 27



PLACE CLOSE TO INPUT PINS

$$VO = (R1/R2) * 0.8 + 0.8$$

MAX LOAD: 2.0A  
V3P3\_S5

MAX LOAD: 1.3A  
V1P5\_S5

MAX LOAD: 2.1A  
V1P0\_S0

**NOTE:**

CURRENT LIMIT  
V3P3\_S5 @ 2.45A DC  
V1P5\_S5 @ 1.80A DC  
V1P0\_S0 @ 2.50A DC

EMPTY 40.2K SHARES 1 PAD WITH INSTALLED 40.2K  
EMPTY 4700PF SHARED 1 PAD WITH INSTALLED 4700PF

CAD NOTE:  
PLACE C2L2 CLOSE TO PIN 4 OF VR

CAD NOTE:  
THIS COMPONENT SHARES  
ONE PAD WITH R2L15  
ONE PAD WITH C2L2

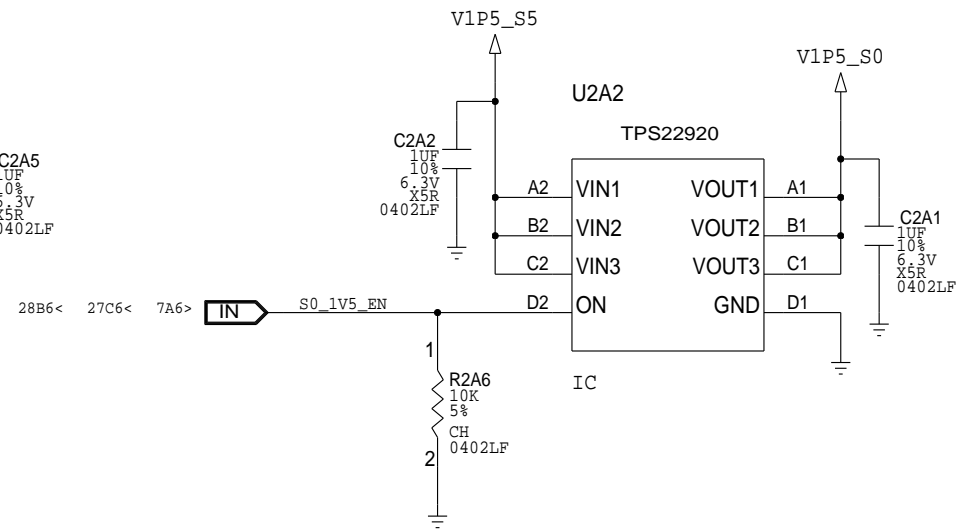
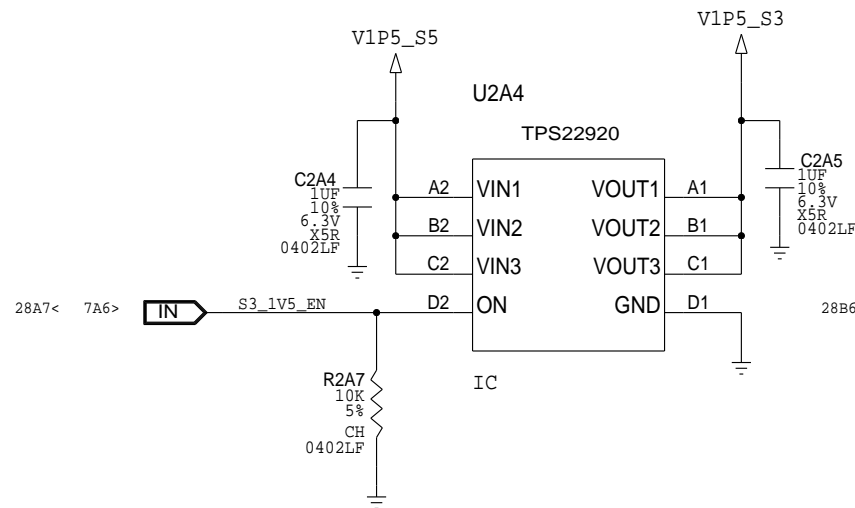
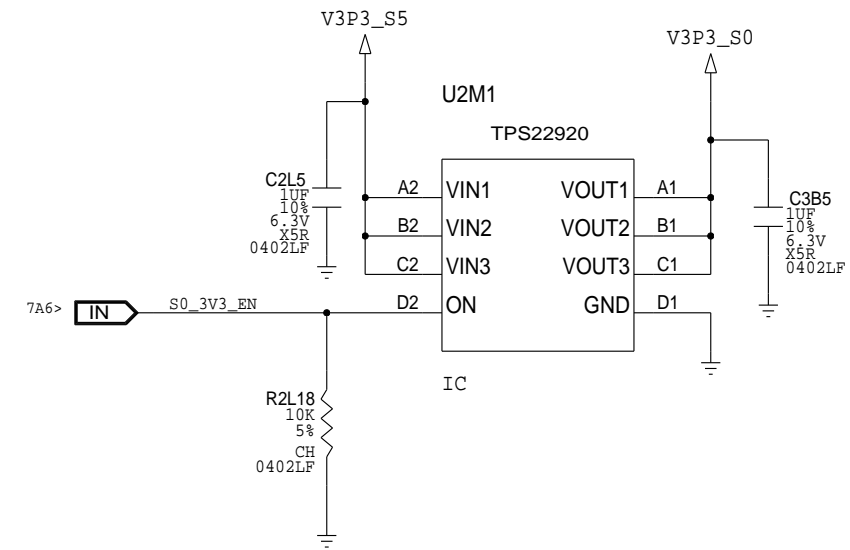
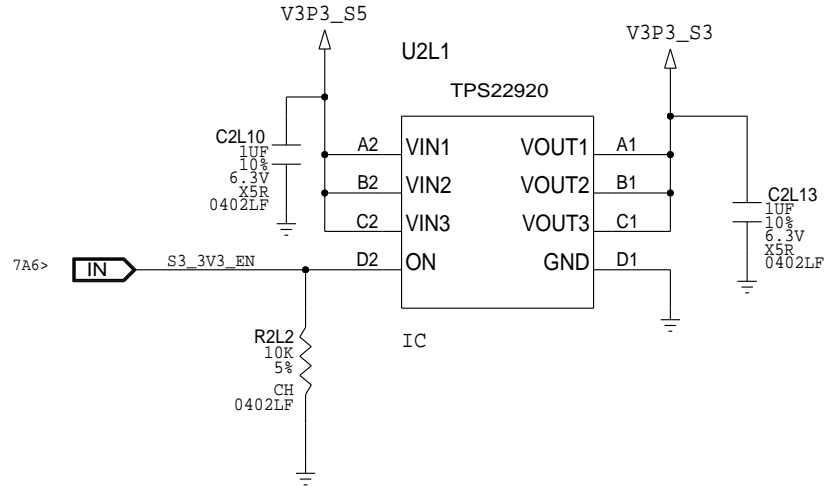
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO VOLTAGE REGULATORS		REV: 1.0	SHEET 24 OF 27



V3P3\_S5 IS GENERATED W ON-BRD REGULATOR

V1P5\_S5 IS GENERATED W ON-BRD REGULATOR

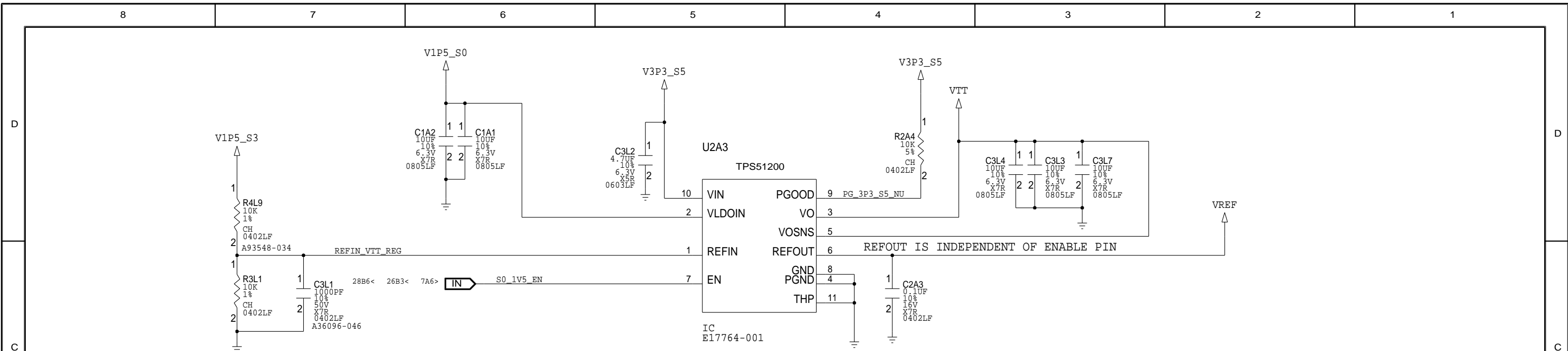
V1P0\_S5 IS GENERATED INTERNALLY



CAD NOTE:  
PLACE DECOUPLING CAPS AS CLOSE AS POSSIBLE TO SWITCH PINS

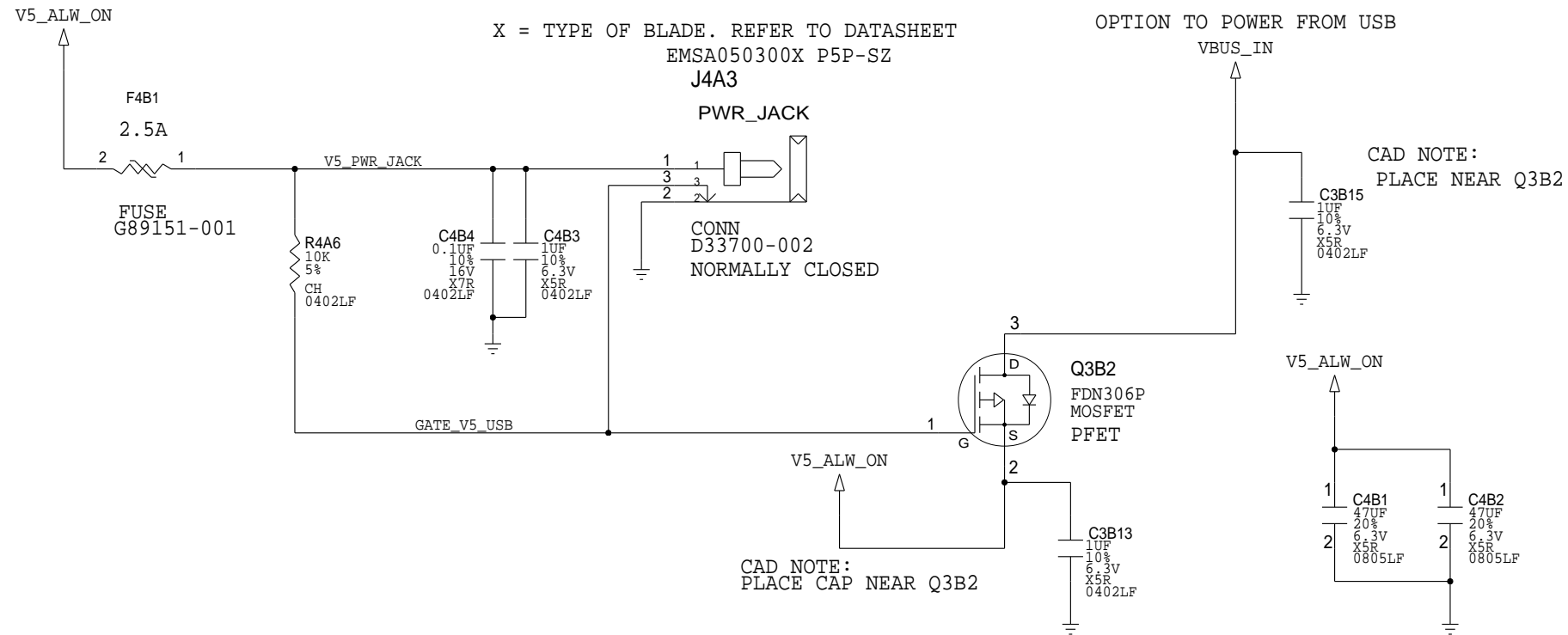
V1P0\_S3 IS GENERATED INTERNALLY

V1P0\_S0 IS GENERATED W ON-BRD REGULATOR



RECOMMENDED POWER SUPPLY:

X = TYPE OF BLADE. REFER TO DATASHEET  
 EMSA050300X P5P-SZ  
 J4A3



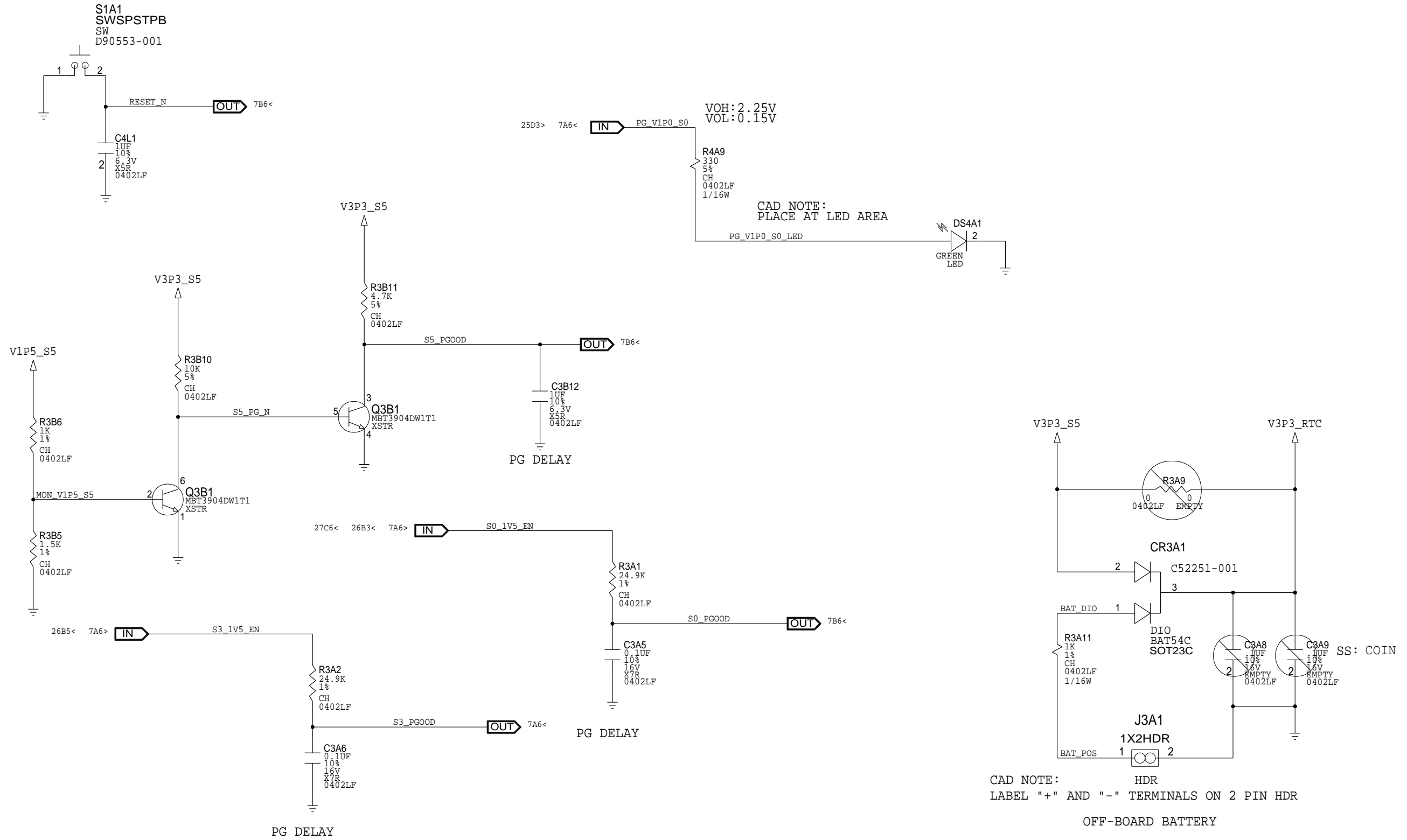
CONNECTOR TRUTH TABLE

PWR BRICK IN	PIN2&PIN3 DISCONNECTED	PIN3=PU TO 5V	V5_ALW_ON=BRICK PWR
PWR BRICK OUT	PIN2&PIN3 SHORTED	PIN3=GND	V5_ALW_ON=VBUS_IN

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO VOLTAGE REGULATORS		REV: 1.0	SHEET 26 OF 27

NOTE: RESET\_N HAS AN INTERNAL PU TO V3P3\_S3

SS:  
REBOOT



INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: G87171	
TITLE: GALILEO POWER BUTTONS & MISC		REV: 1.0	SHEET 27 OF 27