GALILEO GEN2
INTEL QUARK X1000

FAB H
PB: H48142-207
PBA: H48125-800
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>SHEET NUMBER</th>
<th>SHEET NAME</th>
<th>SHEET NUMBER</th>
<th>SHEET NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DESIGN TITLE PAGE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>TABLE OF CONTENTS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DISCLAIMER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SYSTEM BLOCK DIAGRAM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>QUARK DDR3 &amp; PCIE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>QUARK GPIO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>QUARK MISC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>QUARK POWER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>QUARK DECOUPLING</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>SDRAM 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>SDRAM 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>SDRAM TERMINATION</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>MICRO PCIE CONNECTOR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>MICRO SD CONNECTOR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>USB CONNECTORS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>UART 1 &amp; 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>I2C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>SPI1 ADC/FLASH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>QUARK STRAP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>EXTERNAL IO MUXING 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>EXTERNAL IO MUXING 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>LVL B BUFFER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>LVL C BUFFER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>MEZ &amp; EXTERNAL IO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>VOLTAGE REGULATORS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>VOLTAGE REGULATORS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>VOLTAGE REGULATORS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>POWER BUTTONS &amp; MISC</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Intel® Galileo Design Document

This Intel® Galileo design document is licensed by Intel under the terms of the Creative Commons Attribution Share-Alike License (ver. 3), subject to the following terms and conditions. The Intel® Galileo design document IS PROVIDED "AS IS" AND "WITH ALL FAULTS." Intel DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED REGARDING THE GALILEO DESIGN OR THIS GALILEO DESIGN DOCUMENT INCLUDING, BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Intel® may make changes to the specifications, schematics and product descriptions at any time, without notice. The Customer must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel® reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. ENJOY!
STITCHING CAPS FOR SPLIT PLANES

STITCHING CAPS FOR SIGNAL REFERENCE TRANSITION

CAD NOTE
PLACE AS CLOSE AS POSSIBLE TO SIGNAL VIAS
CAD NOTE:
PLACE 0.1UF DECOUPLING AS CLOSE AS POSSIBLE TO DRAM POWER PINS

SDRAM 1

DESIGN NOTE:
A14, A15 ALLOW FOOTPRINT COMPATIBILITY WITH 2GBIT (256MBIT X 8) AND 4GBIT (512MBIT X 8) DEVICES
A14, A15 ALLOW FOOTPRINT COMPATIBILITY WITH SDRAM 2

CAD: PLACE 0.1UF DECOUPLING AS CLOSE AS POSSIBLE TO DRAM PINS

DESIGN NOTE:
A14, A15 ALLOW FOOTPRINT COMPATIBILITY WITH 2GBIT(256MBIT X 8) AND 4GBIT (512MBIT X8) DEVICES
DISTRIBUTE DECOUPLING AMONG CAD:

TERMINATION RESISTORS
CAD NOTE:
PLACE SD LED CLOSE TO THE SDIO CONN
PLACE CHOKE AND DIODES CLOSE TO USB CONN

CAD NOTE:

NOTE:

NOTE:

CAD NOTE:

PLACE C2B11 AS CLOSE AS POSSIBLE TO U3B1 PIN5

USB HOST

NOTE:

TYPE B CONN

USB CLIENT

NOTE:

TYPE A CONN
CAD NOTE:
PLACE CONNECTOR ON SOLDER-SIDE.
CAD NOTE:
PLACE DECOUPLING CAPACITORS AS CLOSE AS POSSIBLE TO ADC
00 - QUARK SKU SETTINGS

- (LOW) PUNIT BASE ADDRESS

- (LOW) POWER BUTTON NOT USED

- (LOW) SINGLE RANK DDR3 SDRAM

- (LOW) MEMORY DOWN CONFIG

- REMOVABLE CARD SLOT FOR SDIO

- (HIGH) X8 DDR SDRAM

DESIGN NOTE:
SHORT TO GND TO ENTER RECOVERY MODE.

SILK=FWR

RECOVERY MODE.
V3P3_S5 IS GENERATED W ON-BRD REGULATOR

V1P5_S5 IS GENERATED W ON-BRD REGULATOR

V1P0_S5 IS GENERATED W ON-BRD REGULATOR

CAD NOTE:
PLACE DECOUPLING CAPS AS CLOSE AS POSSIBLE TO SWITCH PINS

V3P3_S0 IS GENERATED INTERNALLY

V1P0_S3 IS GENERATED INTERNALLY

V1P0_S0 IS GENERATED W ON-BRD REGULATOR

V1P0_S5 IS GENERATED W ON-BRD REGULATOR
RECOMMENDED POWER SUPPLY:

X = TYPE OF BLADE. REFER TO DATASHEET EMEA050300X P3P-S2

REFOUT IS INDEPENDENT OF ENABLE PIN

OPTION TO POWER FROM USB
NOTE: RESET_N HAS AN INTERNAL PU TO V3P3_S3

SS: REBOOT BUTTON

PG DELAY

LED

PG DELAY

V3P3_RTC

PUT THE SILKSCREEN NEXT TO THE CAP

LABEL "+" AND "-" TERMINALS ON 2 PIN HDR

OFF-BOARD BATTERY