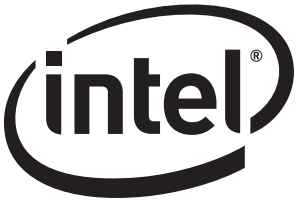

Intel® Desktop Board D975XBX2

Technical Product Specification

October 2006

*Order Number: D73645-001*US

The Intel® Desktop Board D975XBX2 may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D975XBX2 Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D975XBX2 Technical Product Specification	October 2006

This product specification applies to only the standard Intel® Desktop Board D975XBX2 with BIOS identifier BX97520J.86A.

Changes to this specification will be published in the Intel Desktop Board D975XBX2. Specification Update before being incorporated into a revision of this document.

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Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board D975XBX2. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the Intel Desktop Board D975XBX2 and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the Desktop Board D975XBX2
2	A map of the resources of the Desktop Board
3	The features supported by the BIOS Setup program
4	A description of the BIOS error messages, beep codes, and POST codes
5	Regulatory compliance and battery disposal information

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

INTEGRATOR'S NOTES

Integrator's notes are used to call attention to information that may be useful to system integrators.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the Desktop Board D975XBX2, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
GB	Gigabyte (1,073,741,824 bytes)
GB/sec	Gigabytes per second
Gbits/sec	Gigabits per second
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbits/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

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1 Product Description

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1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the major features of the board.

Table 1. Feature Summary

Form Factor	ATX (12.00 inches by 9.60 inches [304.80 millimeters by 243.84 millimeters])
Processor	• Intel® Core™2 Extreme Processor in an LGA775 socket with a 1066 MHz system bus • Intel® Core™2 Duo Processor in an LGA775 socket with a 1066 MHz system bus • Intel® Pentium® Processor Extreme Edition in an LGA775 socket with a 1066 or 800 MHz system bus • Intel® Pentium® 4 Processor Extreme Edition in an LGA775 socket with a 1066 MHz system bus • Intel® Pentium® D Processor in an LGA775 socket with an 800 MHz system bus • Intel® Pentium® 4 Processor in an LGA775 socket with an 800 MHz system bus
Memory	• Four 240-pin DDR2 SDRAM Dual Inline Memory Module (DIMM) sockets • Support for DDR2 800, DDR2 667, and DDR2 533 MHz DIMMs • Support for up to 8 GB of system memory • Support for ECC and non-ECC memory
Chipset	Intel® 975X Chipset, consisting of: • Intel® 82975X Memory Controller Hub (MCH) • Intel® 82801GR I/O Controller Hub (ICH7-R) or Intel® 82801GH I/O Controller Hub (ICH7-DH)
Audio	Intel® High Definition Audio subsystem
Legacy I/O Control	Legacy I/O controller for diskette drive, serial, parallel, and PS/2 ports
USB	Support for USB 2.0 devices
Peripheral Interfaces	• Eight USB ports • One serial port • One parallel port • Four Serial ATA interfaces with RAID support • One Parallel ATA IDE interface with UDMA 33, ATA-66/100 support • One diskette drive interface • PS/2* keyboard and mouse ports
BIOS	• Intel® BIOS resident in the SPI Flash device • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS • Watchdog timer providing automatic recovery after two failed power-on self-tests (POSTs)
Instantly Available PC Technology	• Support for PCI Local Bus Specification Revision 2.2 • Support for PCI Express* Revision 1.0a • Suspend to RAM support • Wake on PCI, RS-232, front panel, PS/2 devices, and USB ports
LAN Support	Gigabit (10/100/1000 Mbits/sec) LAN subsystem using the Intel® 82573E/82573L Gigabit Ethernet Controller

continued

Table 1. Feature Summary (continued)

Expansion Capabilities	• Two PCI* Conventional bus add-in card connectors (SMBus routed to both PCI Conventional bus add-in card connectors) • One Primary PCI Express x16 (electrical x16 or x8) bus add-in card connector • One Secondary PCI Express x16 (electrical x8) bus add-in card connector • One PCI Express x16 (electrical x4) bus add-in card connector
Hardware Monitor Subsystem	• Hardware monitoring and fan control ASIC • Voltage sense to detect out of range power supply voltages • Thermal sense to detect out of range thermal values • Three fan headers • Three fan sense inputs used to monitor fan activity • Fan speed control • Support for Product Environmental Control Interface (PECI)

1.1.2 Manufacturing Options

Table 2 describes the manufacturing options. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

Table 2. Manufacturing Options

AMT	BIOS support for Intel® Active Management Technology (Intel® AMT)
ATAPI CD-ROM Connector	A 1 x 4-pin ATAPI-style connector for connecting an internal ATAPI CD-ROM drive to the audio mixer
Audio Subsystem	Intel High Definition Audio subsystem in one of the following configurations: • 8-channel (7.1) audio subsystem with five analog audio outputs and two S/PDIF digital audio outputs (coaxial and optical) using the SigmaTel* 9274D audio codec • 6-channel (5.1) audio subsystem with three analog audio outputs using the Sigmatel 9227 audio codec
Auxiliary PCI Express Graphics Power Connector	Provides required additional power when using high power (75 W or greater) add-in cards in either or both the Secondary PCI Express x16 (electrical x8) and the PCI Express x16 (electrical x4) bus add-in card connectors
Discrete SATA RAID Controller	• Marvell* 88SE6145 SATA RAID controller • Four SATA connectors (in addition to the four SATA connectors on the ICH7-R/ICH7-DH SATA interface)
IEEE-1394a Interface	IEEE-1394a controller and two IEEE-1394a connectors: one back panel connector and one front-panel header
MCH Fan Header	A 3-pin header for powering a fan for the Intel® 82975X Memory Controller Hub (MCH)
Processor Core Power Connector	One of the following connectors for providing +12 V power to the processor voltage regulator: • 2 x 4-pin (requires a power supply with a dual-rail 2 x 4 power cable). Boards equipped with the 2 x 4-pin processor core power connector will also include heatsinks in the processor voltage regulator area. • 2 x 2-pin
SCSI Hard Drive LED Header	Allows add-in hard drive controllers (SCSI or other) to use the same LED as the onboard IDE controller
Trusted Platform Module (TPM)	A component that enhances platform security

For information about	Refer to
Available configurations for the board	Section 1.2, page 17

1.1.3 Board Layout

Figure 1 shows the location of the major components.

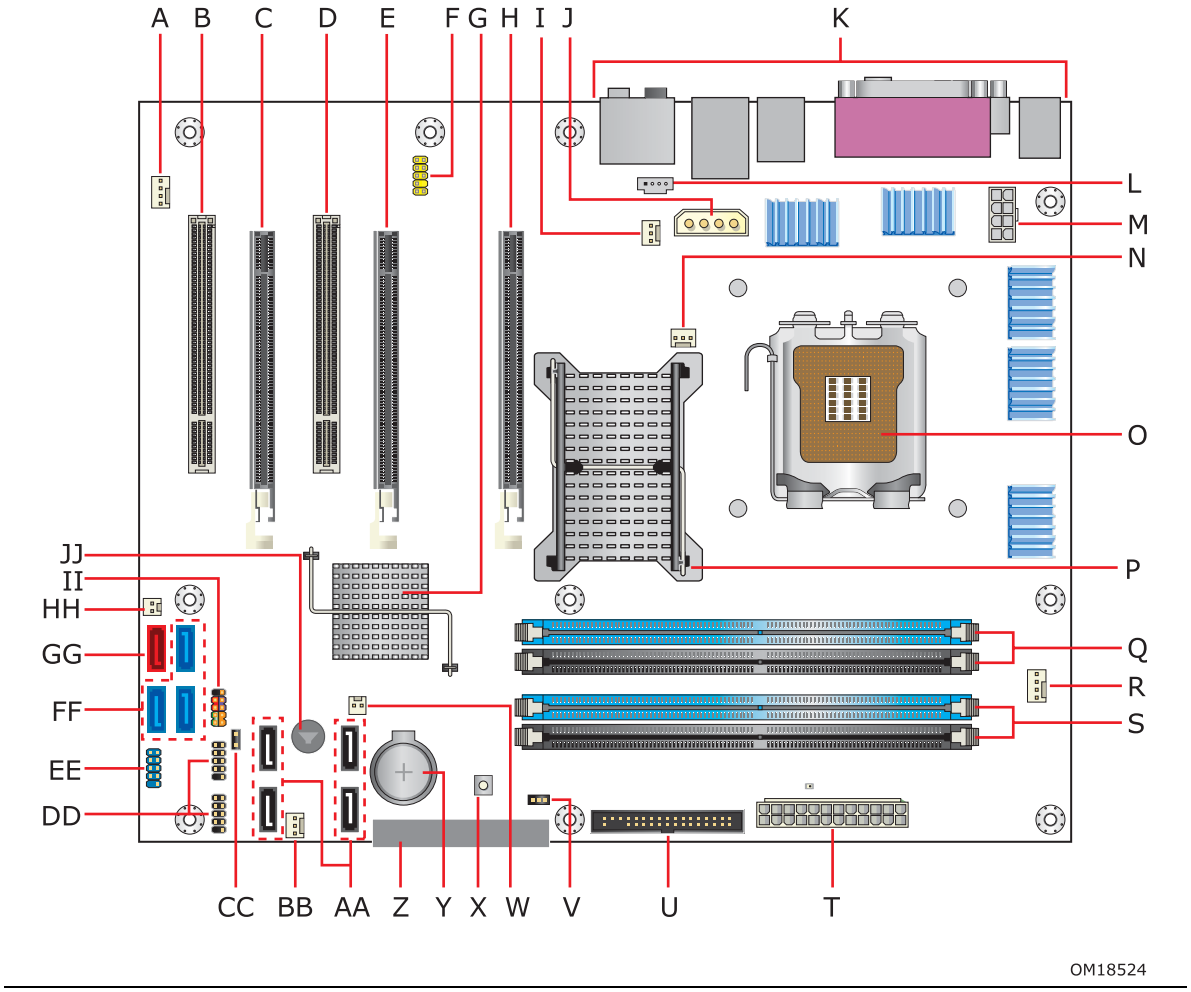


Figure 1. Desktop Board Components

Table 3 lists the components identified in Figure 1.

Table 3. Components Shown in Figure 1

Item/callout from Figure 1	Description
A	Auxiliary rear fan header
B	PCI Conventional bus add-in card connector 2
C	PCI Express x16 (electrical x4) bus add-in card connector
D	PCI Conventional bus add-in card connector 1
E	Secondary PCI Express x16 (electrical x8) bus add-in card connector
F	Front panel audio header
G	Intel® 82801G I/O Controller Hub (ICH7-R or ICH7-DH)
H	Primary PCI Express x16 (electrical x16 or x8) bus add-in card connector
I	Rear chassis fan header
J	Auxiliary PCI Express Graphics Power Connector (optional)
K	Back panel connectors
L	ATAPI CD-ROM connector (optional)
M	Processor core power connector
N	Memory Controller Hub (MCH) fan header (optional)
O	LGA775 processor socket
P	Intel 82975X MCH
Q	DIMM Channel A sockets [2]
R	Processor fan header
S	DIMM Channel B sockets [2]
T	Main power connector
U	Diskette drive connector
V	BIOS Setup configuration jumper block
W	Chassis intrusion header
X	Onboard power button
Y	Battery
Z	Parallel ATE IDE connector
AA	Serial ATA connectors (ICH7-R/ICH7-DH RAID) [4]
BB	Front chassis fan header
CC	Auxiliary front panel power LED header
DD	Front panel USB headers [2]
EE	IEEE-1394a front panel header
FF	Serial ATA RAID connectors (Discrete RAID) (optional) [3]
GG	Serial ATA RAID connector compatible with external Serial ATA adapter (red)
HH	SCSI Hard Drive Activity LED header (optional)
II	Front panel header
JJ	Speaker

1.1.4 Block Diagram

Figure 2 is a block diagram of the major functional areas of the board.

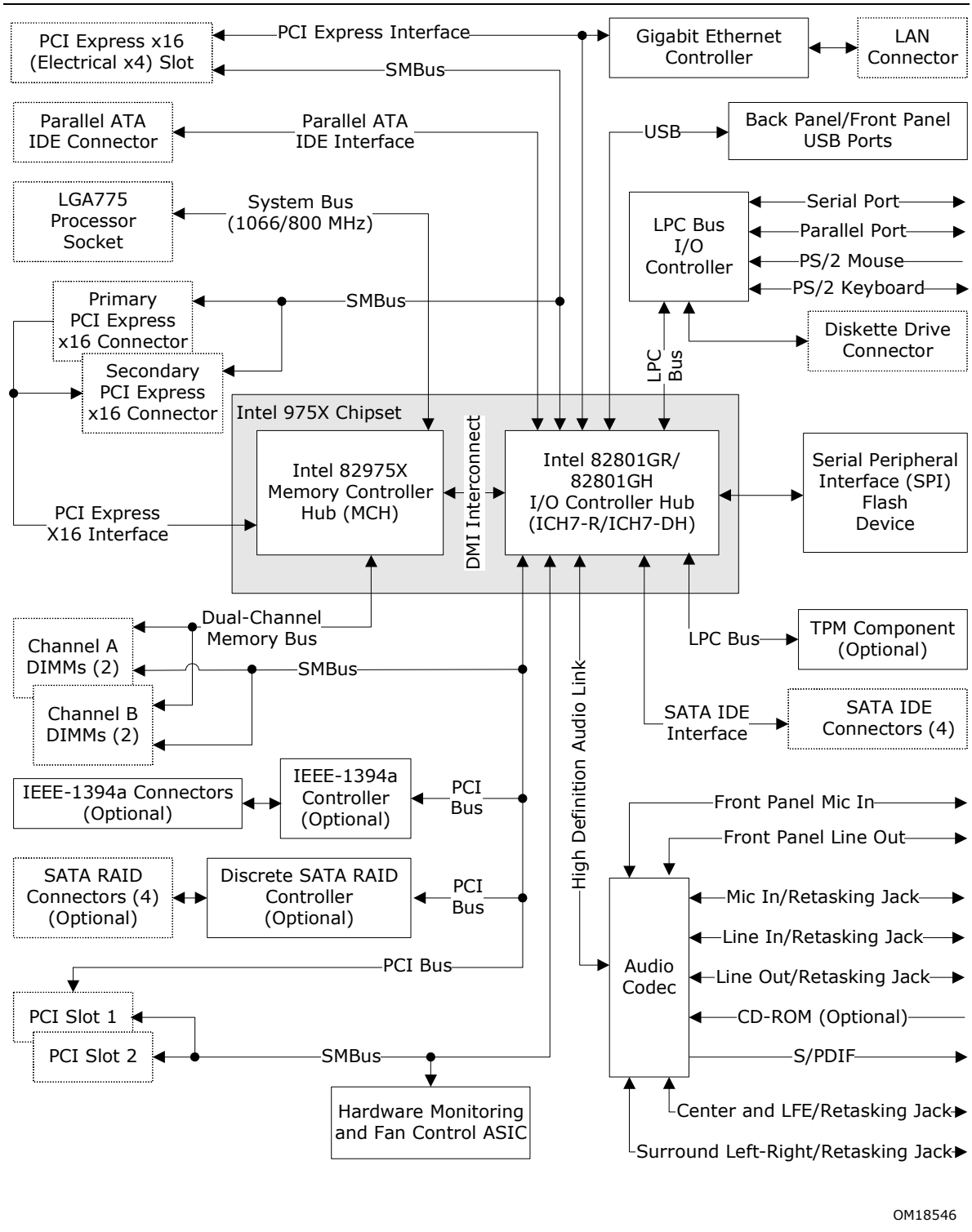


Figure 2. Block Diagram

1.2 Online Support

To find information about…	Visit this World Wide Web site:
Intel Desktop Board D975XBX2 under "Desktop Board Products" or "Desktop Board Support"	http://www.intel.com/design/motherbd http://support.intel.com/support/motherboards/desktop
Available configurations for the Desktop Board D975XBX2	http://developer.intel.com/design/motherbd/bx2/bx2_available.htm
Processor data sheets	http://www.intel.com/design/litcentr
ICH7-R/ICH7-DH addressing	http://developer.intel.com/design/chipsets/datashts
Custom splash screens	http://intel.com/design/motherbd/gen_indx.htm
Audio software and utilities	http://www.intel.com/design/motherbd
LAN software and drivers	http://www.intel.com/design/motherbd

1.3 Processor

The board is designed to support the following processors:

- Intel Core 2 Extreme Processor in an LGA775 socket with a 1066 MHz system bus
- Intel Core 2 Duo Processor in an LGA775 socket with a 1066 MHz system bus
- Intel Pentium Processor Extreme Edition in an LGA775 socket with a 1066 or 800 MHz system bus
- Intel Pentium 4 Processor Extreme Edition in an LGA775 socket with a 1066 MHz system bus
- Intel Pentium D Processor in an LGA775 socket with an 800 MHz system bus
- Intel Pentium 4 Processor in an LGA775 socket with an 800 MHz system bus

See the Intel web site listed below for the most up-to-date list of supported processors.

For information about…	Refer to:
Supported processors for the board	http://www.intel.com/design/motherbd/bx2/bx2_proc.htm

⚠ CAUTION

Use only the processors listed on web site above. Use of unsupported processors can damage the board, the processor, and the power supply.

INTEGRATOR'S NOTE

This board has specific requirements for providing power to the processor. Refer to Section 2.7.2.1 on page 63 for information on power supply requirements for this board.

1.4 System Memory

The board has four DIMM sockets and supports the following memory features:

- 1.8 V and 1.9 V DDR2 SDRAM DIMMs
- Unbuffered, single-sided or double-sided DIMMs with the following restriction: Double-sided DIMMS with x16 organization are not supported.
- 8 GB maximum total system memory. Refer to Section 2.1.1 on page 49 for information on the total amount of addressable memory.
- Minimum total system memory: 128 MB
- ECC DIMMs and non-ECC DIMMs
- Serial Presence Detect
- DDR2 800, DDR2 667, and DDR2 533 MHz SDRAM DIMMs

NOTES

- *Remove the Primary PCI Express x16 (electrical x16 or x8) video card before installing or upgrading memory to avoid interference with the memory retention mechanism.*
- *To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.*

Table 4 lists the supported DIMM configurations.

Table 4. Supported Memory Configurations

DIMM Capacity	Configuration (Note 1)	SDRAM Density	SDRAM Organization Front-side/Back-side	Number of SDRAM Devices (Note 2)
128 MB	SS	256 Mbit	16 M x 16/empty	4 [5]
256 MB	SS	256 Mbit	32 M x 8/empty	8 [9]
256 MB	SS	512 Mbit	32 M x 16/empty	4 [5]
512 MB	DS	256 Mbit	32 M x 8/32 M x 8	16 [18]
512 MB	SS	512 Mbit	64 M x 8/empty	8 [9]
512 MB	SS	1 Gbit	64 M x 16/empty	4 [5]
1024 MB	DS	512 Mbit	64 M x 8/64 M x 8	16 [18]
1024 MB	SS	1 Gbit	128 M x 8/empty	8 [9]
2048 MB	DS	1 Gbit	128 M x 8/128 M x 8	16 [18]

Notes:

1. In the second column, "DS" refers to double-sided memory modules (containing two rows of SDRAM) and "SS" refers to single-sided memory modules (containing one row of SDRAM).
2. In the fifth column, the number in brackets specifies the number of SDRAM devices on an ECC DIMM.

INTEGRATOR'S NOTE

Refer to Section 2.1.1, on page 49 for additional information on available memory.

NOTE

Regardless of the DIMM type used, the memory frequency will either be equal to or less than the processor system bus frequency. For example, if DDR2 800 memory is used with a 533 MHz system bus frequency processor, the memory will operate at 533 MHz. Table 5 lists the resulting operating memory frequencies based on the combination of DIMMs and processors.

Table 5. Memory Operating Frequencies

DIMM Type	Processor System Bus Frequency	Resulting Memory Frequency
DDR2 533	800 MHz	533 MHz
DDR2 533	1066 MHz	533 MHz
DDR2 667	800 MHz	667 MHz
DDR2 667	1066 MHz	667 MHz
DDR2 800	800 MHz	800 MHz
DDR2 800	1066 MHz	800 MHz

1.4.1 Memory Configurations

The Intel 82975X MCH supports two types of memory organization:

- **Dual channel (Interleaved) mode**. This mode offers the highest throughput for real world applications. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed DIMMs are used between channels, the slowest memory timing will be used.
- **Single channel (Asymmetric) mode**. This mode is equivalent to single channel bandwidth operation for real world applications. This mode is used when only a single DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speed DIMMs are used between channels, the slowest memory timing will be used.

Figure 3 illustrates the memory channel and DIMM configuration.

NOTE

The DIMM0 sockets of both channels are blue. The DIMM1 sockets of both channels are black.

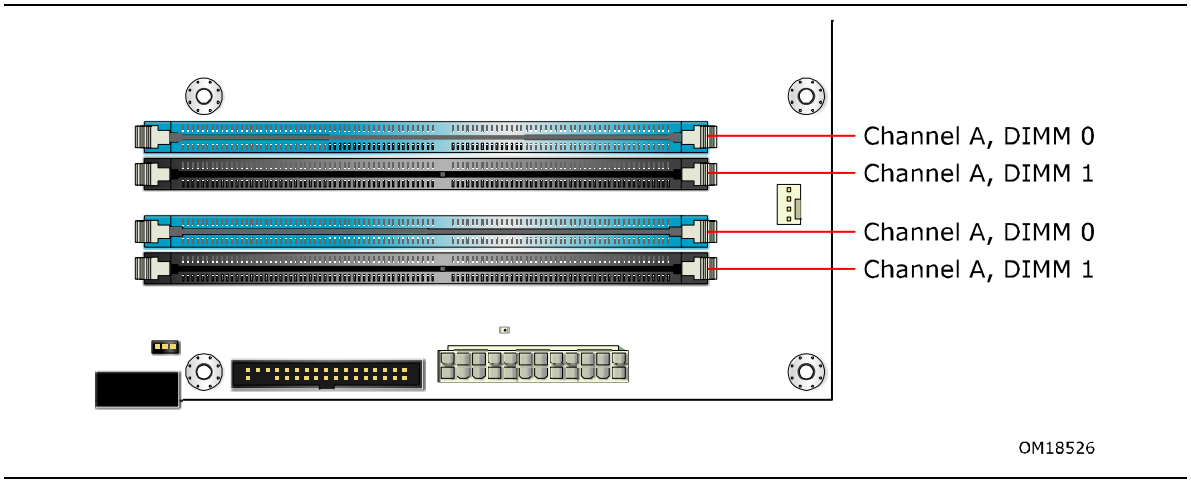


Figure 3. Memory Channel and DIMM Configuration

1.4.1.1 Dual Channel (Interleaved) Mode Configurations

Figure 4 shows a dual channel configuration using two DIMMs. In this example, the DIMM0 (blue) sockets of both channels are populated with identical DIMMs.

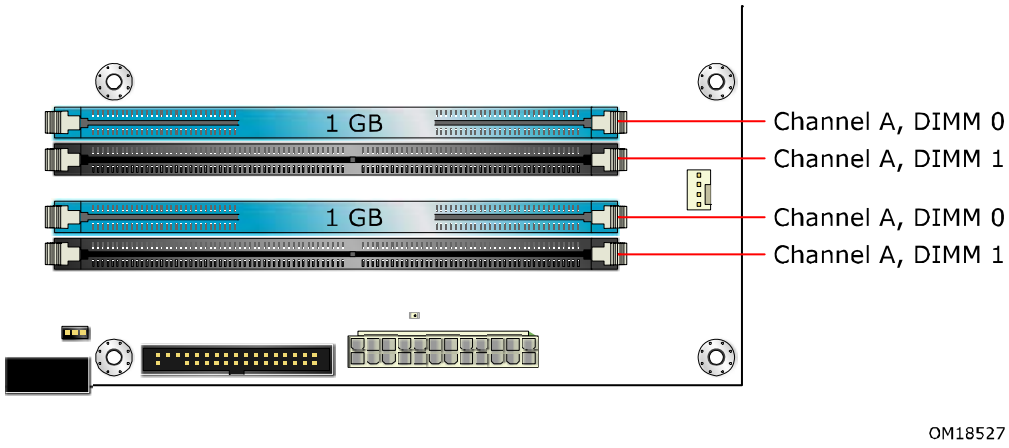


Figure 4. Dual Channel (Interleaved) Mode Configuration with Two DIMMs

Figure 5 shows a dual channel configuration using three DIMMs. In this example, the combined capacity of the two DIMMs in Channel A equal the capacity of the single DIMM in the DIMM0 (blue) socket of Channel B.

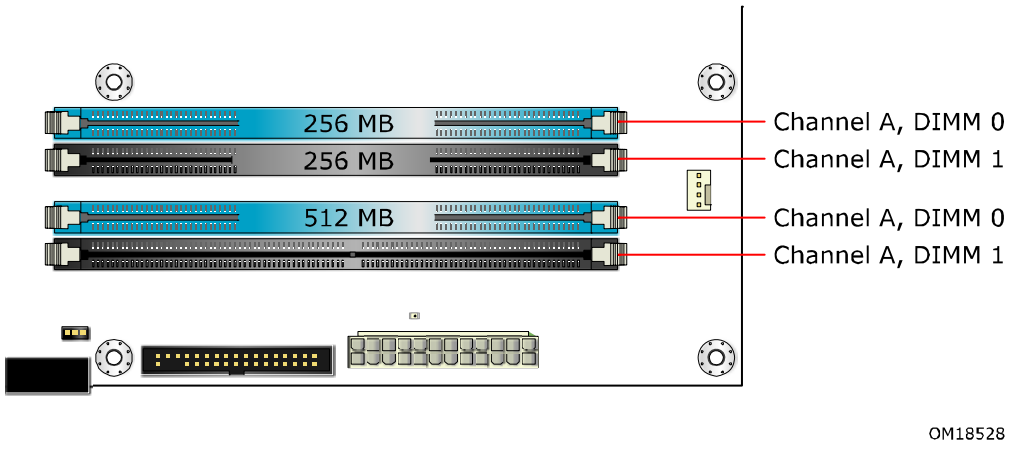


Figure 5. Dual Channel (Interleaved) Mode Configuration with Three DIMMs

Figure 6 shows a dual channel configuration using four DIMMs. In this example, the combined capacity of the two DIMMs in Channel A equal the combined capacity of the two DIMMs in Channel B. Also, the DIMMs are matched between DIMM0 and DIMM1 of both channels.

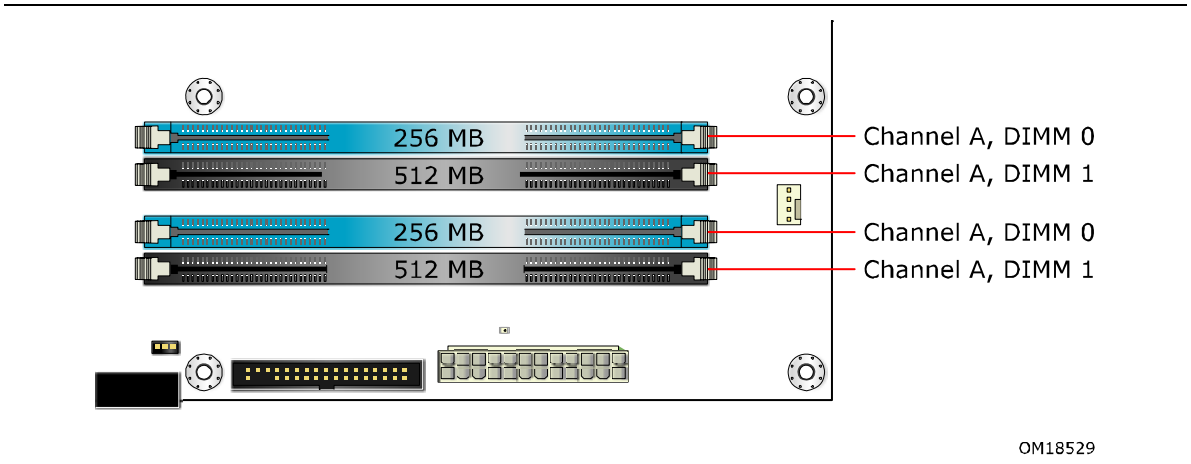


Figure 6. Dual Channel (Interleaved) Mode Configuration with Four DIMMs

1.4.1.2 Single Channel (Asymmetric) Mode Configurations

NOTE

Dual channel (Interleaved) mode configurations provide the highest memory throughput.

Figure 7 shows a single channel configuration using one DIMM. In this example, only the DIMM0 (blue) socket of Channel A is populated. Channel B is not populated.

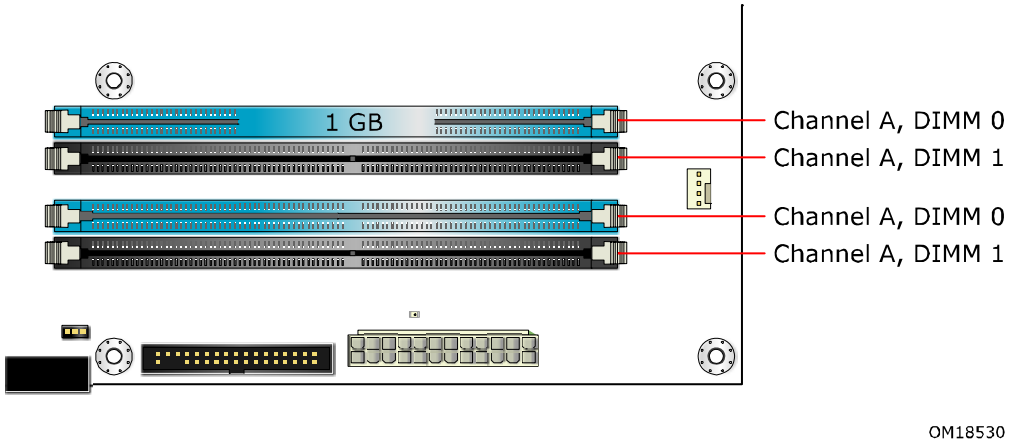


Figure 7. Single Channel (Asymmetric) Mode Configuration with One DIMM

Figure 8 shows a single channel configuration using three DIMMs. In this example, the combined capacity of the two DIMMs in Channel A does not equal the capacity of the single DIMM in the DIMM0 (blue) socket of Channel B.

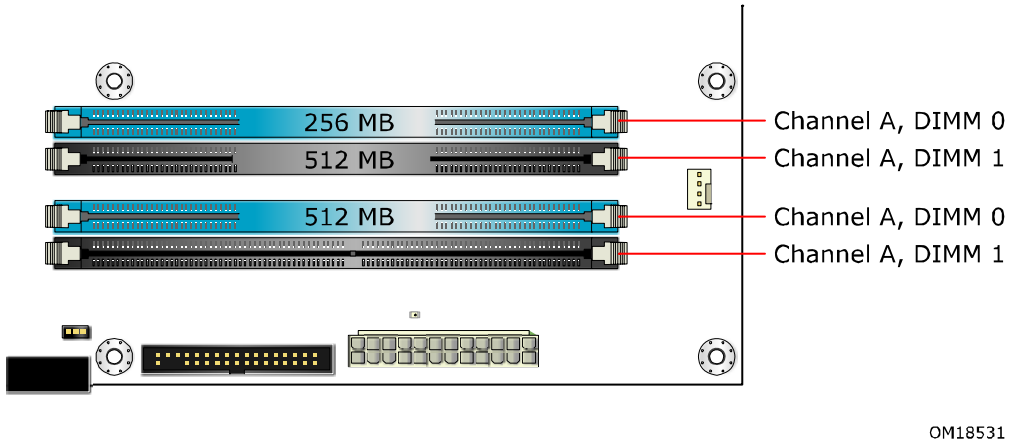


Figure 8. Single Channel (Asymmetric) Mode Configuration with Three DIMMs

1.5 Intel® 975X Chipset

The Intel 975X chipset consists of the following devices:

- Intel 82975X Memory Controller Hub (MCH) with Direct Media Interface (DMI) interconnect
- One of the following:
  - Intel 82801GR I/O Controller Hub (ICH7-R) with DMI interconnect
  - Intel 82801GH I/O Controller Hub (ICH7-DH) with DMI interconnect

The MCH is a centralized controller for the system bus, the memory bus, the PCI Express bus, and the DMI interconnect. The ICH7 is a centralized controller for the board's I/O paths. The BIOS code is stored in the Serial Peripheral Interface (SPI) Flash device.

For information about	Refer to
The Intel 975X chipset	http://developer.intel.com/
Resources used by the chipset	Chapter 2

1.5.1 USB

The board supports up to eight USB 2.0 ports, supports UHCI and EHCI, and uses UHCI- and EHCI-compatible drivers.

The ICH7-R/ICH7-DH provides the USB controller for all ports. The port arrangement is as follows:

- Four ports are implemented with dual stacked back panel connectors adjacent to the audio connectors
- Four ports are routed to two separate front panel USB headers

NOTES

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 19, page 58
The location of the front panel USB headers	Figure 20, page 59

1.5.2 IDE Support

The board provides five IDE interface connectors:

- One parallel ATA IDE connector that supports two devices
- Four serial ATA IDE connectors that support one device per connector

1.5.2.1 Parallel ATE IDE Interface

The ICH7-R/ICH7-DH's Parallel ATA IDE controller has one bus-mastering Parallel ATA IDE interface. The Parallel ATA IDE interface supports the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH7-R/ ICH7-DH's ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The Parallel ATA IDE interface also supports ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

For information about	Refer to
The location of the Parallel ATA IDE connector	Figure 20, page 59

1.5.2.2 Serial ATA Interfaces

The ICH7-R/ICH7-DH's Serial ATA controller offers four independent Serial ATA ports with a theoretical maximum transfer rate of 3 Gbits/sec per port. One device can be installed on each port for a maximum of four Serial ATA devices. A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used.

Native mode is the preferred mode for configurations using the Microsoft Windows* XP and Microsoft Windows 2000 operating systems.

NOTE

Many Serial ATA drives use new low-voltage power connectors and require adaptors or power supplies equipped with low-voltage power connectors.

For more information, see: http://www.serialata.org/

For information about	Refer to
The location of the Serial ATA IDE connectors on the D975XBX2 board	Figure 20, page 59

1.5.2.3 Serial ATA RAID

The ICH7-R/ICH7-DH supports the following RAID (Redundant Array of Independent Drives) levels:

- RAID 0 - data striping
- RAID 1 - data mirroring
- RAID 0+1 (or RAID 10) - data striping and mirroring
- RAID 5 - distributed parity

1.5.2.4 SCSI Hard Drive Activity LED Header (Optional)

The SCSI hard drive activity LED header is a 1 x 2-pin header that allows an add-in hard drive controller to use the same LED as the onboard IDE controller. For proper operation, this header should be wired to the LED output of the add-in hard drive controller. The LED indicates when data is being read from, or written to, either the add-in hard drive controller or the onboard IDE controller (Parallel ATA or Serial ATA).

For information about	Refer to
The location of the SCSI hard drive activity LED header	Figure 20, page 59
The signal names of the SCSI hard drive activity LED header	Table 22, page 62

1.5.3 Real-Time Clock, CMOS SRAM, and Battery

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate. Replace the battery with an equivalent one. Figure 1 on page 14 shows the location of the battery.

1.6 Discrete Serial ATA Interface (Optional)

1.6.1 Serial ATA Controller

As a manufacturing option, the board provides a Marvell 88SE6145 Serial ATA (SATA) controller and four connectors (that support one device per connector) for SATA devices. These connectors are in addition to the four SATA connectors of the ICH7-R/ICH7-DH SATA interface.

The Marvell 88SE6145 controller uses the PCI bus for data transfer with a theoretical maximum transfer rate of 3 Gbits/sec per port. The discrete SATA interface supports the following RAID levels:

- RAID 0
- RAID 1

NOTE

The Marvell 88SE6145 controller supports single drive non-RAID configurations as well as RAID configurations.

For information about	Refer to
The location of the discrete SATA RAID connectors	Figure 20, page 59

1.6.2 External Serial ATA Support

The red Serial ATA connector can be used with a back panel adapter for an external SATA drive. Figure 9 shows the location of the External Serial ATA-compatible SATA port.

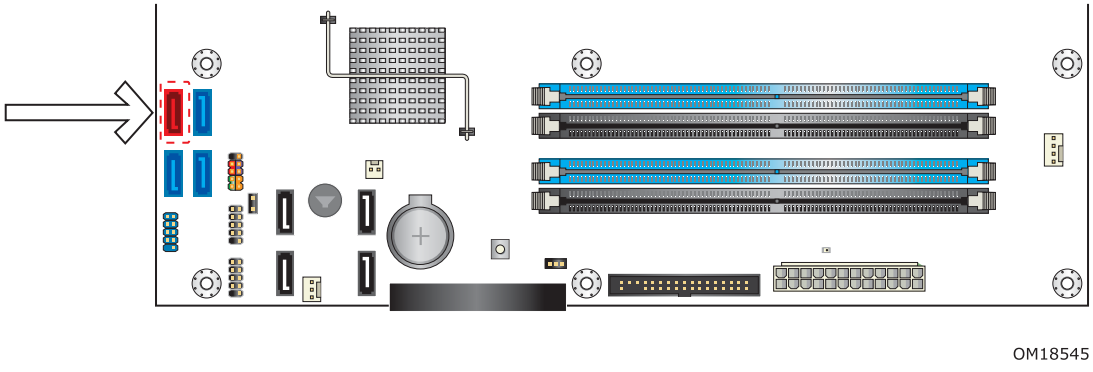


Figure 9. Location of External Serial ATA-Compatible SATA Port

1.7 PCI Express Connectors

The board provides the following PCI Express connectors:

- One Primary PCI Express x16 (electrical x16 or x8) bus add-in card connector. The x16 interface supports simultaneous (full duplex) transfers up to 8 GBytes/sec. Single-ended (half duplex) transfers are supported at up to 4 GBytes/sec.
- One Secondary PCI Express x16 (electrical x8) bus add-in card connector: The board provides a PCI Express add-in card connector in the form of a physical x16 connector with electrical routing of x8. This connector is an electrical equivalent of a PCI Express x8 bus add-in card connector. This connector also supports x4 and x1 PCI Express add-in cards.
- One PCI Express x16 (electrical x4) bus add-in card connector: The board provides a PCI Express add-in card connector in the form of a physical x16 connector with electrical routing of x4. This connector is an electrical equivalent of a PCI Express x4 bus add-in card connector. This connector supports x4 and x1 PCI Express add-in cards.

For optimum performance, observe the following recommendations for the PCI Express add-in card connectors:

- If you are installing a single PCI Express Graphics card, install it in the Primary PCI Express x16 (electrical x16 or x8) bus add-in card connector.
- If you are installing two PCI Express Graphics cards, install them in the Primary PCI Express x16 (electrical x16 or x8) bus add-in card connector and the Secondary PCI Express x16 (electrical x8) bus add-in card connector.

The PCI Express interfaces for the Primary and Secondary PCI Express x16 connectors are routed through the MCH. The PCI Express interface for the PCI Express x16 (electrical x4) connector is routed through the ICH7-R/ICH7-DH. Therefore, the Primary and Secondary PCI Express x16 connectors provide higher performance than the PCI Express x16 (electrical x4) bus add-in card connector.

For information about	Refer to
The locations of the specific PCI Express x16 add-in card connectors	Figure 1, page 14

INTEGRATOR'S NOTE

Although the PCI Express specification allows x16 cards to auto-negotiate down from x16 to x4 and x1 and may function properly, such configurations have not been validated on this board. Please consult your add-in card vendor prior to attempting to use a PCI Express x16 add-in card in this connector.

The PCI Express interface supports the PCI Conventional bus configuration mechanism so that the underlying PCI Express architecture is compatible with PCI Conventional compliant operating systems. Additional features of the PCI Express interface includes the following:

- Support for the PCI Express enhanced configuration mechanism
- Automatic discovery, link training, and initialization
- Support for Active State Power Management (ASPM)
- SMBus 2.0 support

- Wake# signal supporting wake events from ACPI S1, S3, S4, or S5
- Software compatible with the PCI Power Management Event (PME) mechanism defined in the *PCI Power Management Interface Specification, Rev. 1.1*

1.8 IEEE-1394a Connectors (Optional)

The optional IEEE-1394 interface addresses interconnection of both computer peripherals and consumer electronics with these features:

- IEEE-1394a operation
- Support for up to 63 peer-to-peer devices
- Operation ranging from 100 Mbits/sec to 400 Mbits/sec (depending on cable type)
- Connection over short and long distances
- Support for both asynchronous and isochronous data transfer

As a manufacturing option, the board includes two IEEE-1394a connectors as follows:

- One IEEE-1394a connector located on the back panel.
- One IEEE-1394a front-panel header located on the component side.

For information about	Refer to
The location of the back panel IEEE-1394a connector	Figure 18, page 57
The location of the front panel IEEE-1394a header	Figure 20, page 59
The signal names of the front panel IEEE-1394a header	Section 2.7.2.6, page 69

1.9 Legacy I/O Controller

The legacy I/O controller provides the following features:

- One serial port
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI Conventional bus systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.44 MB or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI Conventional bus power management support

The BIOS Setup program provides configuration options for the legacy I/O controller.

1.9.1 Serial Port

The board has one serial port connector located on the back panel. The serial port supports data transfers at rates of up to 115.2 kbits/sec with BIOS support.

For information about	Refer to
The location of the serial port A connector	Figure 19, page 58

1.9.2 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. Use the BIOS Setup program to set the parallel port mode.

For information about	Refer to
The location of the parallel port connector	Figure 19, page 58

1.9.3 Diskette Drive Controller

The legacy I/O controller supports one diskette drive. Use the BIOS Setup program to configure the diskette drive interface.

For information about	Refer to
The location of the diskette drive connector on the D975XBX2 board	Figure 20, page 59

1.9.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 19, page 58

1.10 Audio Subsystem

The board supports the Intel High Definition audio subsystem based on the SigmaTel 9274D or the SigmaTel 9227 audio codec. The audio subsystem supports the following features:

- Advanced jack sense for the back panel audio jacks that enables the audio codec to recognize the device that is connected to an audio port. The back panel audio jacks are capable of retasking according to user's definition, or can be automatically switched depending on the recognized device type.
- Stereo input and output for all back panel jacks
- Line out and Mic in functions for front panel audio jacks
- A signal-to-noise (S/N) ratio of 90 dB

1.10.1 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.2, page 17

1.10.2 Audio Connectors

The board contains audio connectors and headers on both the back panel and the component side of the board. The component-side audio connectors include the following:

- Front panel audio (a 2 x 5-pin header that provides mic in and line out signals for front panel audio connectors)
- ATAPI CD-ROM (an optional 1 x 4-pin ATAPI-style connector for connecting an internal ATAPI CD-ROM drive to the audio mixer)

The functions of the back panel audio connectors are dependent on which subsystem is present. The 8-channel (7.1) audio subsystem is described in Section 1.10.3; the 6-channel (5.1) audio subsystem is described in Section 1.10.4.

For information about	Refer to
The locations of the front panel audio header and the optional ATAPI CD-ROM connector	Figure 20, page 59
The signal names of the front panel audio header	Table 18, page 61
The signal names of the optional ATAPI CD-ROM connector	Table 17, page 61
The back panel audio connectors	Section 2.7.1, page 56

1.10.3 8-Channel (7.1) Audio Subsystem

The 8-channel (7.1) audio subsystem includes the following:

- Intel 82801G I/O Controller Hub (ICH7-R/ICH7-DH)
- SigmaTel 9274D audio codec
- Microphone input that supports a single dynamic, condenser, or electret microphone

The back panel audio connectors are configurable through the audio device drivers. The available configurable audio ports are shown in Figure 10.

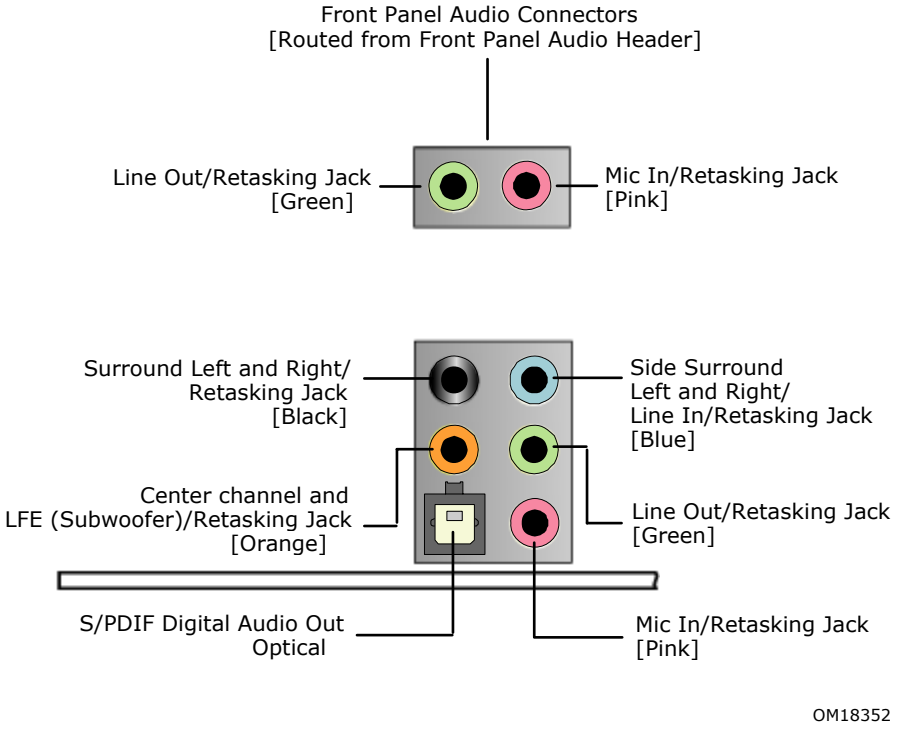


Figure 10. Front/Back Panel Audio Connector Options for 8-Channel (7.1) Audio Subsystem

For information about	Refer to
The back panel audio connectors	Section 2.7.1, page 56

1.10.4 6-Channel (5.1) Audio Subsystem

The 6-channel (5.1) audio subsystem includes the following:

- Intel 82801G I/O Controller Hub (ICH7-R/ICH7-DH)
- SigmaTel 9227 audio codec
- Microphone input that supports a single dynamic, condenser, or electret microphone

The back panel audio connectors are configurable through the audio device drivers. The available configurable audio ports are shown in Figure 11.

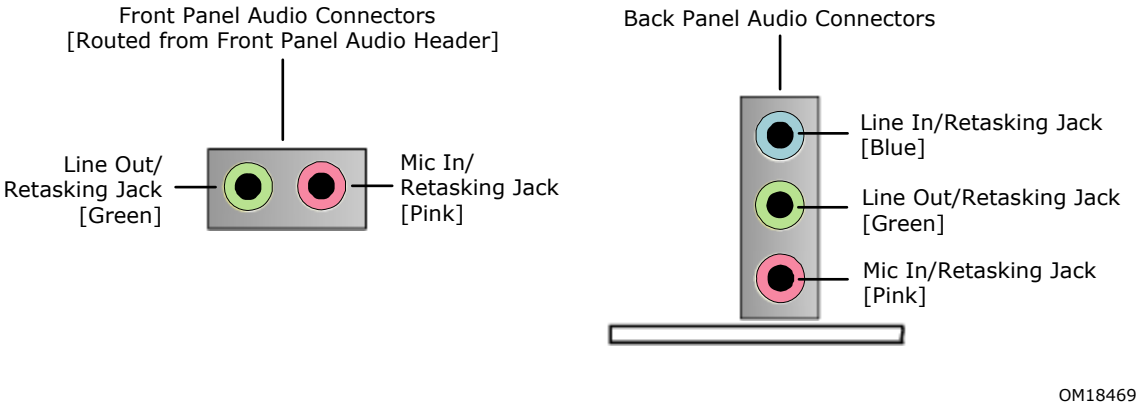


Figure 11. Front/Back Panel Audio Connector Options for 6-Channel (5.1) Audio Subsystem

For information about	Refer to
The back panel audio connectors	Section 2.7.1, page 56

1.11 LAN Subsystem

The LAN subsystem includes the Intel® 82573 Gigabit (10/100/1000 Mbits/sec) Ethernet Controller and an RJ-45 LAN connector with integrated status LEDs.

1.11.1 Intel® 82573E/82573L Gigabit Ethernet Controller

The Intel 82573E/82573L Gigabit Ethernet Controller supports the following features:

- PCI Express link
- 10/100/1000 IEEE 802.3 compliant
- Compliant to IEEE 802.3x flow control support
- Jumbo frame support
- TCP, IP, UDP checksum offload
- Transmit TCP segmentation
- Advanced packet filtering
- Full device driver compatibility
- PCI Express Power Management Support

The 82573E Gigabit Ethernet Controller supports Alert Standard Format (ASF) 2.0 and Intel Active Management Technology (Intel AMT).

1.11.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 12 below).

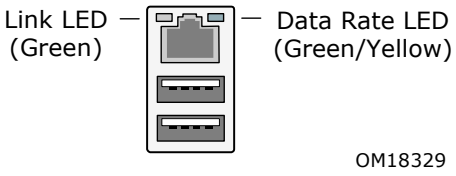


Figure 12. LAN Connector LED Locations

Table 6 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 6. LAN Connector LED States

LED	LED Color	LED State	Condition
Link	Green	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring.
Data Rate	Green/Yellow	Off	10 Mbits/sec data rate is selected.
		Green	100 Mbits/sec data rate is selected.
		Yellow	1000 Mbits/sec data rate is selected.

1.11.3 Alert Standard Format (ASF) Support

The board provides the following ASF support for PCI Express x1 bus add-in LAN cards and PCI Conventional bus add-in LAN cards:

- Monitoring of system firmware progress events, including:
  - BIOS present
  - Primary processor initialization
  - Memory initialization
  - Video initialization
  - PCI resource configuration
  - Hard-disk initialization
  - User authentication
  - Starting operating system boot process
- Monitoring of system firmware error events, including:
  - Memory missing
  - Memory failure
  - No video device
  - Keyboard failure
  - Hard-disk failure
  - No boot media
- Boot options to boot from different types of boot devices
- Reset, shutdown, power cycle, and power up options
- LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

1.11.4 Intel® Active Management Technology (Optional)

Intel Active Management Technology (Intel AMT) offers IT organizations tamper-resistant and persistent management capabilities. Specifically, Intel AMT is a hardware-based solution that offers encrypted and persistent asset management and remote diagnostics and/or recovery capabilities for networked platforms. With Intel AMT, IT organizations can easily get accurate platform information, and can perform remote updating, diagnostics, debugging and repair of a system, regardless of the state of the operating system and the power state of the system. Intel AMT enables IT organizations to discover, heal, and protect all of their computing assets, regardless of system state in the manner described below.

- Discovering hardware and software computing assets:
  - Intel AMT stores hardware and software asset information in non-volatile memory and allows IT to read the asset information anytime, even if the PC is off
  - Users cannot remove or prevent IT organization access to the information because it does not rely on software agents

- Healing systems remotely, regardless of the operating system or system state:
  - Intel AMT provides out-of-band diagnostics and recovery capabilities for IT organizations to remotely diagnose and repair PCs after software, operating system, or hardware failures
  - Alerting and event logging help IT organizations detect and diagnose problems quickly to reduce end-user downtime
- Protecting the enterprise against malicious software attacks:
  - Intel AMT helps IT organizations keep software versions and virus protection consistent and up-to-date across the enterprise
  - Version information is stored in non-volatile memory for access anytime by third party software to check and, if necessary, wake a system to perform off-hours updates.

The key features of Intel AMT include:

- Secure Out of Band (OOB) system management that allows remote management of PCs regardless of system power or operating system state:
  - SSL3.1/TLS encryption
  - HTTP authentication
  - TCP/IP
  - HTTP web GUI
  - XML/SOAP API
- Remote troubleshooting and recovery that can significantly reduce desk-side visits and potentially increasing efficiency of IT technical staff:
  - System event log
  - IDE-R or PXE boot; Network drive or remote CD boot
  - Serial over LAN
  - OOB diagnostics
  - Remote control
  - Remote BIOS update
- Proactive alerting that decreases downtime and minimizes time to repair:
  - Programmable policies
  - Operating system lock-up alert
  - Boot failure alert
  - Hardware failure alerts
- Third party non-volatile storage that prevents users from removing critical inventory, remote control, or virus protection agents:
  - Nonvolatile storage for agents
  - Tamper-resistant
- Remote hardware and software asset tracking that eliminates time-consuming manual inventory tracking, which also reduces asset accounting costs:
  - E-Asset Tag
  - HW/SW inventory

For information about	Refer to
Intel Active Management Technology	http://www.intel.com/technology/manage/iamt/index.htm

1.11.5 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.2, page 17

1.12 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Fan monitoring and control (through the hardware monitoring and fan control ASIC)
- Thermal and voltage monitoring
- Chassis intrusion detection
- Support for Product Environmental Control Interface (PECI)

1.12.1 Hardware Monitoring and Fan Control ASIC

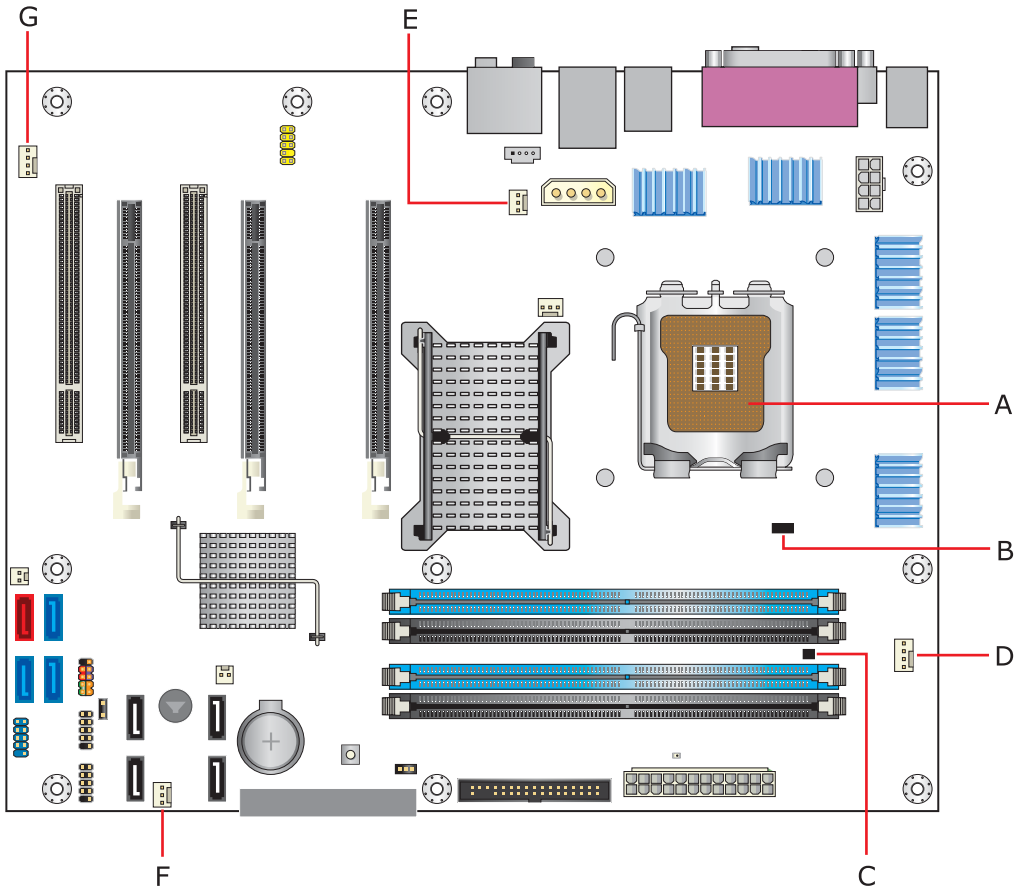
The features of the hardware monitoring and fan control ASIC include:

- Internal ambient temperature sensor
- Two remote thermal diode sensors for direct monitoring of processor temperature and ambient temperature sensing
- Power supply monitoring of five voltages (+5 V, +12 V, +3.3 VSB, +1.5 V, and +VCCP) to detect levels above or below acceptable values
- Thermally monitored closed-loop fan control, for all three fans, that can adjust the fan speed or switch the fans on or off as needed
- SMBus interface

For information about	Refer to
The location of the fan headers and sensors for thermal monitoring	Figure 13, page 38

1.12.2 Thermal Monitoring

Figure 13 shows the location of the sensors and fan headers.



Item	Description
A	Thermal diode, located on processor die
B	Ambient temperature sensor, internal to hardware monitoring and fan control ASIC
C	Remote ambient temperature sensor
D	Processor fan header
E	Rear chassis fan header
F	Front chassis fan header
G	Auxiliary chassis fan header

Figure 13. Sensors and Fan Connectors

1.12.3 Fan Monitoring

Fan monitoring can be implemented using Intel Desktop Utilities or third-party software. The level of monitoring and control is dependent on the hardware monitoring ASIC used with the Desktop Board.

For information about	Refer to
The functions of the fan headers	Section 1.13.2.2, page 43

1.12.4 Chassis Intrusion and Detection

The board supports a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion header. When the chassis cover is removed, the mechanical switch is in the closed position.

1.13 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan headers
  - LAN wake capabilities
  - Instantly Available PC technology
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event signal (PME#) wake-up support
  - PCI Express WAKE# signal support

1.13.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 9 on page 42)
- Support for a front panel power and sleep mode switch

Table 7 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 7. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

1.13.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 8 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 8. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 52.5 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.13.1.2 Wake-up Devices and Events

Table 9 lists the devices or specific events that can wake the computer from specific states.

Table 9. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
LAN	S1, S3, S4, S5 (Note)
Modem (back panel Serial Port A)	S1, S3
PME# signal	S1, S3, S4, S5 (Note)
Power switch	S1, S3, S4, S5
PS/2 devices	S1, S3
RTC alarm	S1, S3, S4, S5
USB	S1, S3
WAKE#	S1, S3, S4, S5

Note: For LAN and PME# signal, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.13.2 Hardware Support

CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

The board provides several power management hardware features, including:

- Power connector
- Fan headers
- LAN wake capabilities
- Instantly Available PC technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# signal wake-up support
- WAKE# signal wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal).

NOTE

The use of Resume on Ring and Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.

1.13.2.1 Power Connector

When an ACPI-enabled system receives the appropriate command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the main power connector	Figure 20, page 59
The signal names of the main power connector	Table 24, page 63

1.13.2.2 Fan Headers

The function/operation of the fan headers is as follows:

- The fans are on when the board is in the S0 or S1 state.
- The fans are off when the board is off or in the S3, S4, or S5 state.
- Each fan header is wired to a fan tachometer input of the hardware monitoring and fan control ASIC
- All fan headers support closed-loop fan control that can adjust the fan speed or switch the fan on or off as needed
- All fan headers have a +12 V DC connection

For information about	Refer to
The location of the fan headers	Figure 20, page 59
The location of the fan headers and sensors for thermal monitoring	Figure 13, page 38
The signal names of the fan headers	Section 2.7.1.1, page 57

1.13.2.3 LAN Wake Capabilities

⚠ CAUTION

For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the board supports LAN wake capabilities with ACPI in the following ways:

- The PCI Express WAKE# signal
- The PCI Conventional bus PME# signal for PCI 2.2 compliant LAN designs
- The onboard LAN subsystem

1.13.2.4 Instantly Available PC Technology

⚠ CAUTION

For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.

Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 9 on page 42 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification*. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.2 compliant add-in cards, PCI Express add-in cards, and drivers.

1.13.2.5 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from ACPI S1 or S3 states
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

1.13.2.6 Wake from USB

USB bus activity wakes the computer from ACPI S1 or S3 states.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.13.2.7 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1 or S3 state.

1.13.2.8 PME# Signal Wake-up Support

When the PME# signal on the PCI Conventional bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with Wake on PME enabled in the BIOS).

1.13.2.9 WAKE# Signal Wake-up Support

When the WAKE# signal on the PCI Express bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state.

1.13.2.10 +5 V Standby Power Indicator LED

The +5 V standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 14 shows the location of the standby power indicator LED on the D975XBX2 board.

CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.

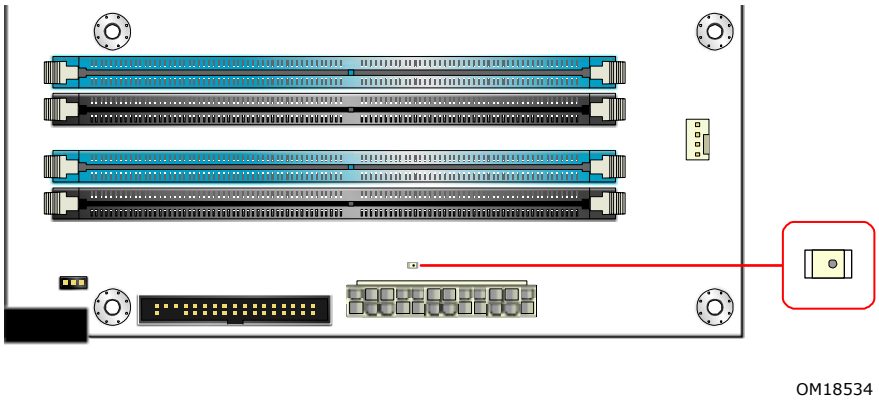


Figure 14. Location of the Standby Power Indicator LED

1.14 Onboard Power Button

CAUTION

Electrostatic discharge (ESD) can damage components. The onboard power button should be used only at an ESD workstation using an antistatic wrist strap and a conductive foam pad. If such a station is not available, some ESD protection can be provided by wearing an antistatic wrist strap and attaching it to a metal part of the computer chassis.

The board provides a power button that can be used to turn the computer on or off. This button is intended for use at integration facilities to remove standby power before making changes to the system configuration, or for testing purposes.

The power button on the front panel is recommended for all other instances of turning the computer on or off. To turn the computer off using the onboard power button, keep the button pressed down for three seconds.

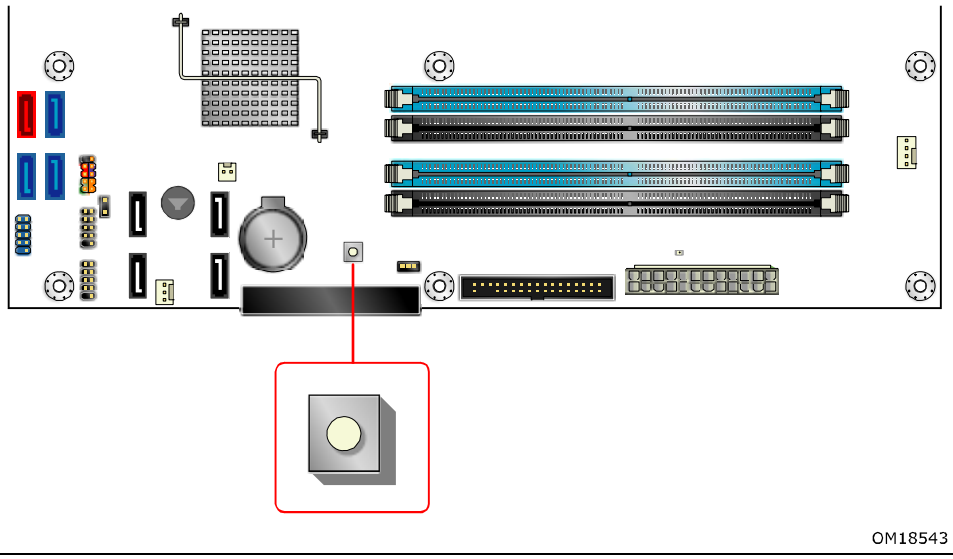


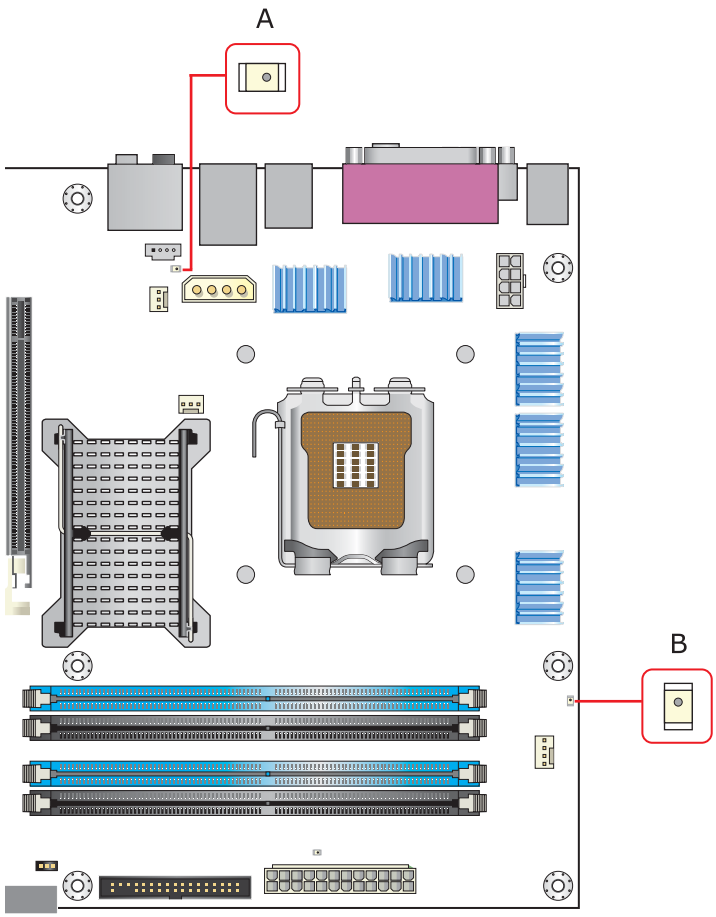
Figure 15. Location of the Onboard Power Button

1.15 Onboard LEDs

In addition to the standby power indicator, the board contains two LEDs that indicate the following:

- The CPU LED indicates an elevated temperature on the processor that could effect performance
- The VR LED indicates an elevated temperature in the processor voltage regulator circuit that could effect performance

Figure 16 shows the locations of the LEDs.



Item	Description	LED Color
A	CPU LED	Red
B	VR LED	Red

Figure 16. Location of the CPU and Processor Voltage Regulator LEDs

1.16 Trusted Platform Module (Optional)

The optional Trusted Platform Module (TPM) is a component on the desktop board that is specifically designed to enhance platform security above-and-beyond the capabilities of today's software by providing a protected space for key operations and other security critical tasks. Using both hardware and software, the TPM protects encryption and signature keys at their most vulnerable stages—operations when the keys are being used unencrypted in plain-text form. The TPM is specifically designed to shield unencrypted keys and platform authentication information from software-based attacks.

For information about	Refer to
TPM	http://www.intel.com/design/motherbd/bx2/

2 Technical Reference

What This Chapter Contains

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2.2 DMA Channels 51
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2.6 PCI Conventional Interrupt Routing Map 55
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2.11 Thermal Considerations 76
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2.1 Memory Resources

2.1.1 Addressable Memory

The board utilizes 8 GB of addressable system memory. Typically the address space that is allocated for PCI Conventional bus add-in cards, PCI Express configuration space, BIOS (SPI Flash device), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 8 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- BIOS/SPI Flash device (8 Mbit)
- Local APIC (19 MB)
- Digital Media Interface (40 MB)
- Front side bus interrupts (17 MB)
- PCI Express configuration space (256 MB)
- MCH base address registers, internal graphics ranges, PCI Express ports (up to 512 MB)
- Memory-mapped I/O that is dynamically allocated for PCI Conventional and PCI Express add-in cards

The board provides the capability to reclaim the physical memory overlapped by the memory mapped I/O logical address space. The board remaps physical memory from the top of usable DRAM boundary to the 4 GB boundary to an equivalent sized logical address range located just above the 4 GB boundary. Figure 17 shows a schematic of

the system memory map. All installed system memory can be used when there is no overlap of system addresses.

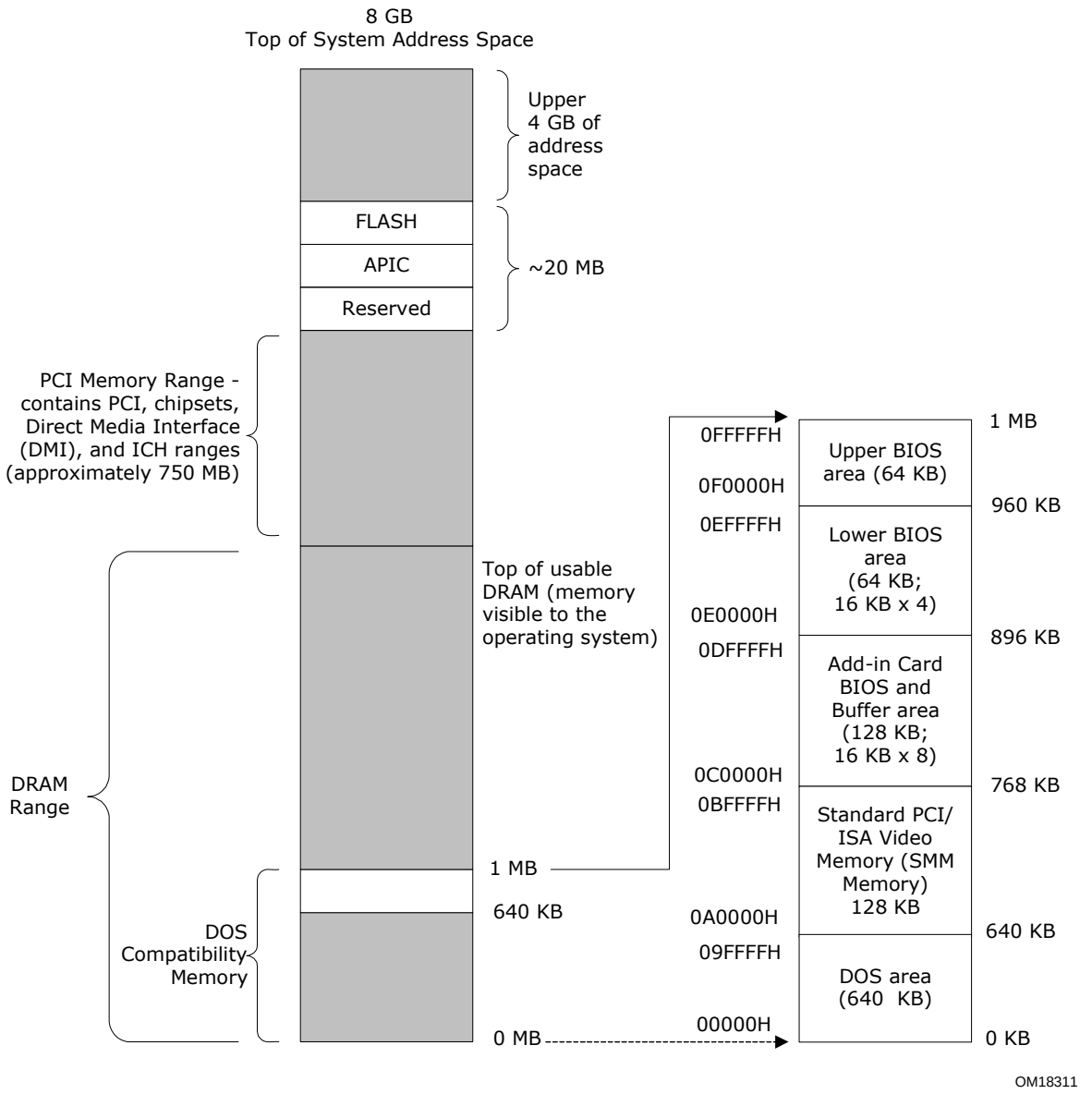


Figure 17. Detailed System Memory Address Map

2.1.2 Memory Map

Table 10 lists the system memory map.

Table 10. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 8388608 K	100000 - 1FFFFFFFF	8191 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Potential available high DOS memory (open to the PCI Conventional bus). Dependent on video adapter used.
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.2 DMA Channels

Table 11. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP or EPP)
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.3 Fixed I/O Map

Table 12. I/O Map

Address (hex)	Size	Description
0000 - 00FF	256 bytes	Used by the Desktop Board D975XBX2. Refer to the ICH7-R/ICH7-DH data sheet for dynamic addressing information.
0170 - 0177	8 bytes	Secondary Parallel ATA IDE channel command block
01F0 - 01F7	8 bytes	Primary Parallel ATA IDE channel command block
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4
02F8 - 02FF (Note 1)	8 bytes	COM2
0374 - 0377	4 bytes	Secondary Parallel ATA IDE channel control block
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT1
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette channel
03F4 – 03F7	1 byte	Primary Parallel ATA IDE channel control block
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI Conventional bus configuration address register
0CF9 (Note 3)	1 byte	Reset control register
0CFC - 0CFF	4 bytes	PCI Conventional bus configuration data register
FFA0 - FFA7	8 bytes	Primary Parallel ATA IDE bus master registers
FFA8 - FFAF	8 bytes	Secondary Parallel ATA IDE bus master registers

Notes:

1. Default, but can be changed to another address range.
2. Dword access only.
3. Byte access only.

NOTE

Some additional I/O addresses are not available due to ICH7-R/ICH7-DH address aliasing. The ICH7-R/ICH7-DH data sheet provides more information on address aliasing.

For information about	Refer to
Obtaining the ICH7-R/ICH7-DH data sheet	Section 1.2 on page 17

2.4 PCI Configuration Space Map

Table 13. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82975X component
00	01	00	PCI Express x16 graphics port
00	1B	00	Intel High Definition Audio controller
00	1C	00	PCI Express port 1
00	1C	01	PCI Express port 2 (Gigabit Ethernet controller bridge)
00	1C	02	PCI Express port 3
00	1C	03	PCI Express port 4 (not used)
00	1D	00	USB UHCI controller 1
00	1D	01	USB UHCI controller 2
00	1D	02	USB UHCI controller 3
00	1D	03	USB UHCI controller 4
00	1D	07	EHCI controller
00	1E	00	PCI bridge
00	1F	00	PCI controller
00	1F	01	Parallel ATA IDE controller
00	1F	02	Serial ATA controller
00	1F	03	SMBus controller
(Note)	00	00	Gigabit Ethernet controller
(Note)	00	00	PCI Conventional bus connector 1
(Note)	01	00	PCI Conventional bus connector 2
(Note)	05	00	IEEE-1394a controller

Note: Bus number is dynamic and can change based on add-in cards used.

2.5 Interrupts

The interrupts can be routed through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the ICH7-R/ICH7-DH component. The PIC is supported in Microsoft Windows 98 SE and Microsoft Windows ME and uses the first 16 interrupts. The APIC is supported in Microsoft Windows 2000 and Microsoft Windows XP and supports a total of 24 interrupts.

Table 14. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	User available
4	COM1 (Note 1)
5	User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	User available
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary Parallel ATA/Serial ATA – Legacy Mode (if present, else user available)
15	Secondary Parallel ATA/Serial ATA – Legacy Mode (if present, else user available)
16 (Note 2)	User available (through PIRQA)
17 (Note 2)	User available (through PIRQB)
18 (Note 2)	User available (through PIRQC)
19 (Note 2)	User available (through PIRQD)
20 (Note 2)	User available (through PIRQE)
21 (Note 2)	User available (through PIRQF)
22 (Note 2)	User available (through PIRQG)
23 (Note 2)	User available (through PIRQH)

Notes:

1. Default, but can be changed to another IRQ.
2. Available in APIC mode only.

2.6 PCI Conventional Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI Conventional bus connectors and onboard PCI Conventional devices. The PCI Conventional specification describes how interrupts can be shared between devices attached to the PCI Conventional bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI Conventional device should not share an interrupt with other PCI Conventional devices. Use the following information to avoid sharing an interrupt with a PCI Conventional add-in card.

PCI Conventional devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH7-R/ICH7-DH has eight Programmable Interrupt Request (PIRQ) input signals. All PCI Conventional interrupt sources either onboard or from a PCI Conventional add-in card connect to one of these PIRQ signals. Some PCI Conventional interrupt sources are electrically tied together on the board and therefore share the same interrupt. Table 15 shows an example of how the PIRQ signals are routed.

Table 15. PCI Interrupt Routing Map

	ICH7-R/ICH7-DH PIRQ Signal Name							
PCI Interrupt Source	**PIRQA**	**PIRQB**	**PIRQC**	**PIRQD**	**PIRQE**	**PIRQF**	**PIRQG**	**PIRQH**
PCI bus connector 1					INTD	INTA	INTB	INTC
PCI bus connector 2	INTD	INTC	INTA	INTB				
IEEE-1394a controller			INTA					
Discrete SATA Controller		INTA						

NOTE

In PIC mode, the ICH7-R/ICH7-DH can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. Refer to Table 14 for the allocation of PIRQ lines to IRQ signals in APIC mode.

PCI interrupt assignments to the USB ports, Serial ATA ports, and PCI Express ports are dynamic.

2.7 Connectors

CAUTION

Only the following connectors have overcurrent protection: back panel USB, front panel USB, and PS/2.

The other internal connectors and headers are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors or headers to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.

This section describes the board's connectors. The connectors can be divided into these groups:

- Back panel I/O connectors
- Component-side I/O connectors and headers (see page 59)

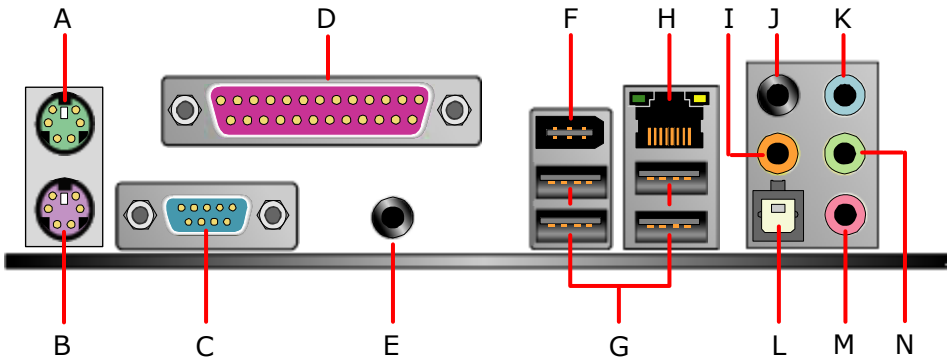
2.7.1 Back Panel Connectors

The back panel configuration is dependent upon which audio subsystem is present. The configurations are as follows:

- 8-channel (7.1) audio subsystem (five analog audio output connectors and two digital audio output connectors), described on page 57
- 6-channel (5.1) audio subsystem (three analog audio output connectors), described on page 58

2.7.1.1 Back Panel Connectors For 8-Channel (7.1) Audio Subsystem

Figure 18 shows the location of the back panel connectors for boards equipped with the 8-channel (7.1) audio subsystem.



Item	Description
A	PS/2 mouse port
B	PS/2 keyboard port
C	Serial port A
D	Parallel port
E	Digital audio out coaxial
F	IEEE-1394a connector
G	USB ports (four)
H	LAN
I	Center channel and LFE (subwoofer) audio out/ Retasking Jack G
J	Surround left/right channel audio out/Retasking Jack H
K	Audio line in/Retasking Jack C
L	Digital audio out optical
M	Mic in/Retasking Jack B
N	Front left/right channel audio out/Two channel audio line out/Retasking Jack D

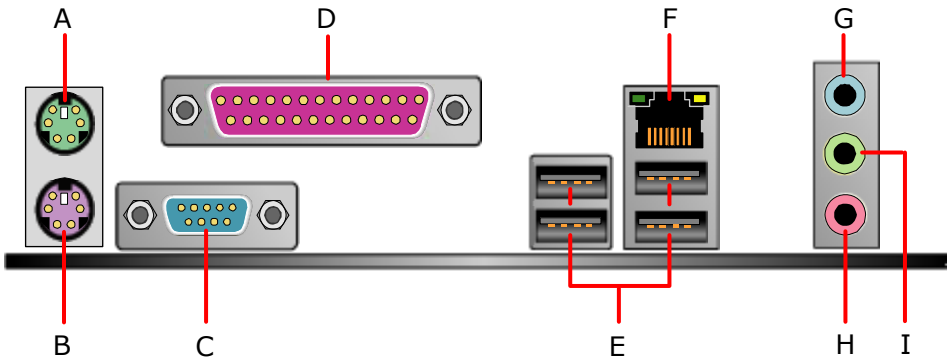
Figure 18. Back Panel Connectors for 8-Channel (7.1) Audio Subsystem

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

2.7.1.2 Back Panel Connectors For 6-Channel (5.1) Audio Subsystem

Figure 19 shows the location of the back panel connectors for boards equipped with the 6-channel (5.1) audio subsystem.



Item	Description
A	PS/2 mouse port
B	PS/2 keyboard port
C	Serial port A
D	Parallel port
E	USB ports (four)
F	LAN
G	Audio line in/Retasking Jack C
H	Mic in/Retasking Jack B
I	Front left/right channel audio out/Two channel audio line out/Retasking Jack D

Figure 19. Back Panel Connectors for 6-Channel (5.1) Audio Subsystem

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

2.7.2 Component-side Connectors and Headers

Figure 20 shows the locations of the component-side connectors and headers.

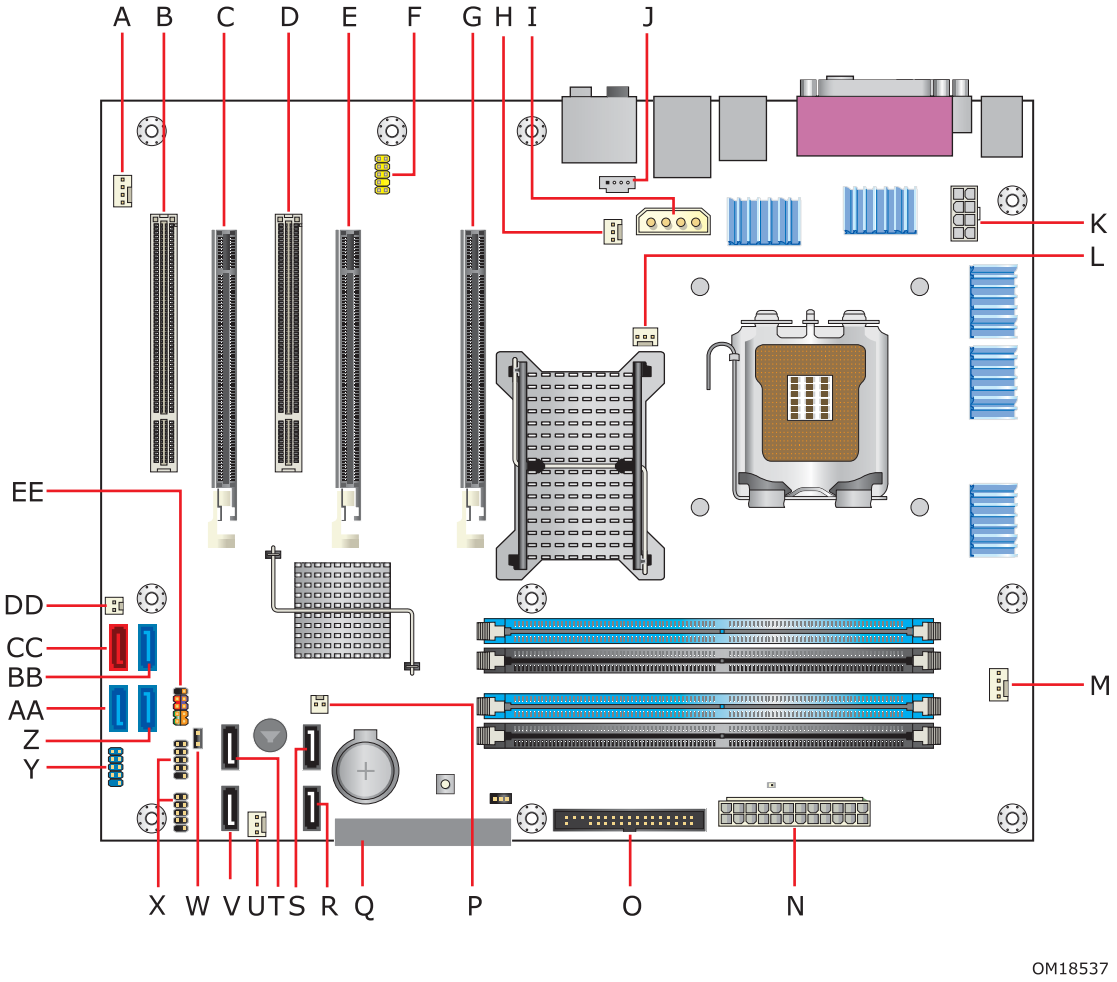


Figure 20. Component-side Connectors and Headers

Table 16 lists the component-side connectors and headers identified in Figure 20.

Table 16. Component-side Connectors and Headers Shown in Figure 20

Item/callout from Figure 20	Description
A	Auxiliary rear fan header
B	PCI Conventional bus add-in card connector 2
C	PCI Express x16 (electrical x4) bus add-in card connector
D	PCI Conventional bus add-in card connector 1
E	Secondary PCI Express x16 (electrical x8) bus add-in card connector
F	Front panel audio header
G	Primary PCI Express x16 (electrical x16 or x8) bus add-in card connector
H	Rear chassis fan header
I	Auxiliary PCI Express Graphics Power connector (optional)
J	ATAPI CD-ROM connector (optional)
K	Processor core power connector
L	MCH fan header (optional)
M	Processor fan header
N	Main power connector
O	Diskette drive connector
P	Chassis intrusion header
Q	Parallel ATA IDE connector
R	Serial ATA connector 3 (ICH7-R/ICH7-DH RAID)
S	Serial ATA connector 2(ICH7-R/ICH7-DH RAID)
T	Serial ATA connector 1 (ICH7-R/ICH7-DH RAID)
U	Front chassis fan header
V	Serial ATA connector 0 (ICH7-R/ICH7-DH RAID)
W	Auxiliary front panel power LED header
X	Front panel USB headers
Y	Front panel IEEE-1394a header [blue] (optional)
Z	Serial ATA connector 7 (Discrete RAID) (optional)
AA	Serial ATA connector 6 (Discrete RAID) (optional)
BB	Serial ATA connector 5 (Discrete RAID) (optional)
CC	Serial ATA RAID connector compatible with external Serial ATA adapter (optional)
DD	SCSI hard drive activity indicator LED header (optional)
EE	Front panel header

Table 17. ATAPI CD-ROM Connector (Optional)

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

Table 18. Front Panel Audio Header

Pin	Signal Name	Pin	Signal Name
1	Port E [Port 1] Left Channel	2	Ground
3	Port E [Port 1] Right Channel	4	Presence# (dongle present)
5	Port F [Port 2] Right Channel	6	Port E [Port 1] Sense return (jack detection)
7	Port E [Port 1] and Port F [Port 2] Sense send (jack detection)	8	Key
9	Port F [Port 2] Left Channel	10	Port F [Port 2] Sense return (jack detection)

INTEGRATOR'S NOTE

The front panel audio header is colored yellow.

Table 19. Front Chassis, Rear Chassis, and MCH Fan Headers

Pin	Signal Name
1	Control
2	+12 V
3	Tach

Table 20. Processor Fan and Auxiliary Rear Fan Header

Pin	Signal Name
1	Ground
2	+12 V
3	FAN_TACH
4	FAN_CONTROL

Table 21. Chassis Intrusion Header

Pin	Signal Name
1	Intruder
2	Ground

Table 22. SCSI Hard Drive Activity LED Header (Optional)

Pin	Signal Name
1	ACT#
2	No connect

Table 23. Serial ATA Connectors

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

2.7.2.1 Power Supply Connectors

The board has three power supply connectors:

- **Main power** – a 2 x 12 connector. The board requires a power supply with a 2 x 12 main power cable.
- **Processor core power** – This connector provides power directly to the processor voltage regulator and must always be used. Depending on manufacturing options, the board will contain either a 2 x 4 or a 2 x 2 connector for the processor voltage regulator.
- **Auxiliary PCI Express graphics power** – a 1 x 4 connector. This connector provides the required additional power when using high power (75 W or greater) add-in cards in either or both the Secondary PCI Express x16 (electrical x8) and the PCI Express x16 (electrical x4) bus add-in card connectors.

⚠ CAUTION

Regardless of the connector type (2 x 4 or a 2 x 2), the Processor core power connector must always be used. Failure to do so will prevent the board from booting.

If the board is equipped with a 2 x 4 power connector, you must use a power supply with a dual-rail 2 x 4 Processor core power cable. Failure to do so may cause damage to the board.

⚠ CAUTION

If high power (75 W or greater) add-in cards are installed in either or both the Secondary PCI Express x16 (electrical x8) and the PCI Express x16 (electrical x4) bus add-in card connectors, the Auxiliary PCI Express graphics power connector must be used. Failure to do so may cause damage to the board and the add-in cards.

Table 24. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	13	+3.3 V
2	+3.3 V	14	-12 V
3	Ground	15	Ground
4	+5 V	16	PS-ON# (power supply remote on/off)
5	Ground	17	Ground
6	+5 V	18	Ground
7	Ground	19	Ground
8	PWRGD (Power Good)	20	No connect
9	+5 V (Standby)	21	+5 V
10	+12 V	22	+5 V
11	+12 V	23	+5 V
12	2 x 12 connector detect	24	Ground

Table 25. Processor Core Power Connector (2 x 4 Pin)

Pin	Signal Name	Pin	Signal Name
1	Ground	5	+12 V – Rail 1
2	Ground	6	+12 V – Rail 1
3	Ground	7	+12 V – Rail 2
4	Ground	8	+12 V – Rail 2

Table 26. Processor Core Power Connector (2 x 2 Pin)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	+12 V
2	Ground	4	+12 V

Table 27. Auxiliary PCI Express Graphics Power

Pin	Signal Name
1	+12 V
2	1 x 4 connector detect
3	Ground
4	+5 V

2.7.2.2 Add-in Card Connectors

The board has the following add-in card connectors:

- Primary PCI Express x16 (electrical x16 or x8) bus add-in card connector; one connector supporting simultaneous transfers up to 8 GBytes/sec
- Secondary PCI Express x16 (electrical x8) bus add-in card connector; one connector supporting simultaneous transfers up to 4 GBytes/sec
- PCI Express x16 (electrical x4) add-in card connector; one connector supporting simultaneous transfers up to 1 GBytes/sec. This connector can also be used for PCI Express x1 add-in cards.
- PCI Conventional (rev 2.2 compliant) bus; two PCI Conventional bus add-in card connectors.

Note the following considerations for the PCI Conventional bus connectors:

- All of the PCI Conventional bus connectors are bus master capable.
- SMBus signals are routed to both PCI Conventional bus connectors. This enables PCI Conventional bus add-in boards with SMBus support to access sensor data on the Desktop Board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40.
  - The SMBus data line is connected to pin A41.

2.7.2.3 Auxiliary Front Panel Power/Sleep LED Header

Pins 1 and 3 of this header duplicate the signals on pins 2 and 4 of the front panel header.

Table 28. Auxiliary Front Panel Power/Sleep LED Header

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.7.2.4 Front Panel Header

This section describes the functions of the front panel header. Table 29 lists the signal names of the front panel header. Figure 21 is a connection diagram for the front panel header.

Table 29. Front Panel Header

Pin	Signal	In/ Out	Description	Pin	Signal	In/ Out	Description
Hard Drive Activity LED [Orange]				**Power LED [Green]**			
1	HD_PWR	Out	Hard disk LED pull-up to +5 V	2	HDR_BLNK_ GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_ YEL	Out	Front panel yellow LED
Reset Switch [Blue]				**On/Off Switch [Red]**			
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
Power				**Not Connected**			
9	+5 V		Power	10	N/C		Not connected

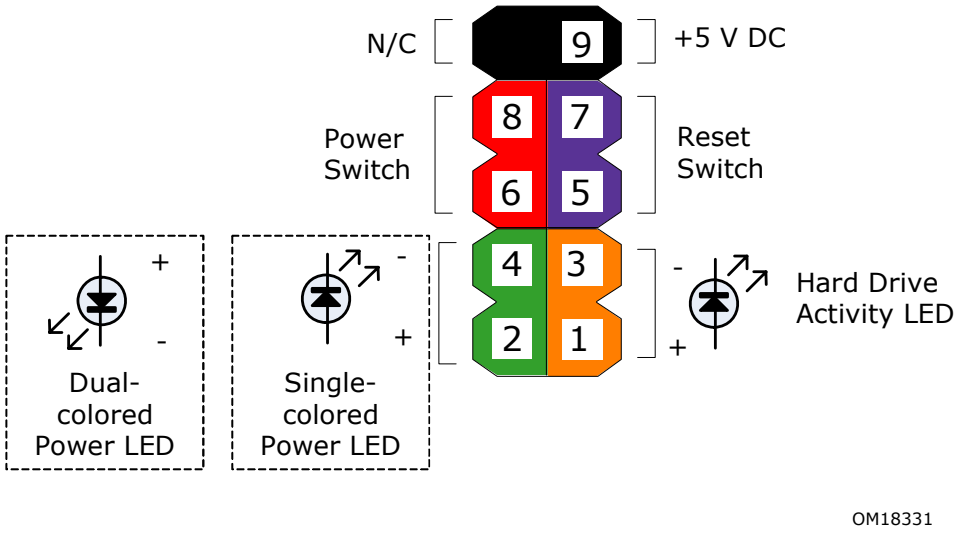


Figure 21. Connection Diagram for Front Panel Header

2.7.2.4.1 Hard Drive Activity LED Header [Orange]

Pins 1 and 3 [Orange] can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires one of the following:

- A Serial ATA hard drive connected to an onboard Serial ATA connector
- An IDE hard drive connected to an onboard IDE connector

2.7.2.4.2 Reset Switch Header [Blue]

Pins 5 and 7 [Blue] can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.7.2.4.3 Power/Sleep LED Header [Green]

Pins 2 and 4 [Green] can be connected to a one- or two-color LED. Table 30 shows the possible states for a one-color LED. Table 31 shows the possible states for a two-color LED.

Table 30. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running

Table 31. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Steady Yellow	Sleeping

NOTE

The colors listed in Table 30 and Table 31 are suggested colors only. Actual LED colors are product- or customer-specific.

2.7.2.4.4 Power Switch Header [Red]

Pins 6 and 8 [Red] can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.7.2.5 Front Panel USB Headers

Figure 22 is a connection diagram for the front panel USB headers.

INTEGRATOR'S NOTES

- *The +5 V DC power on the USB headers is fused.*
- *Pins 1, 3, 5, and 7 comprise one USB port.*
- *Pins 2, 4, 6, and 8 comprise one USB port.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-performance USB devices.*

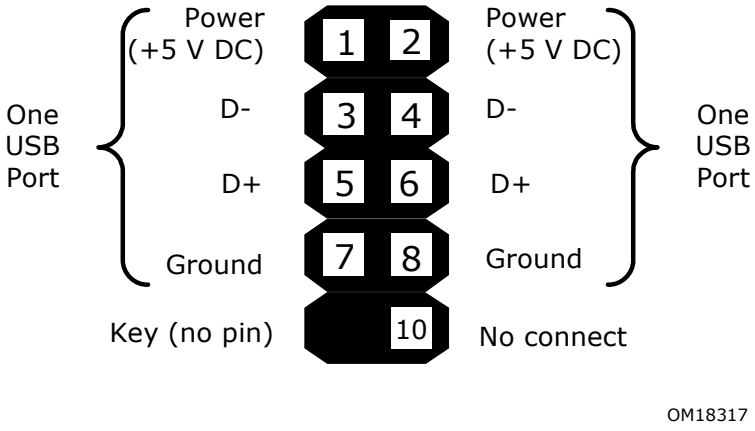


Figure 22. Connection Diagram for Front Panel USB Headers

2.7.2.6 Front Panel IEEE 1394a Header (Optional)

Figure 23 is a connection diagram for the IEEE 1394a header.

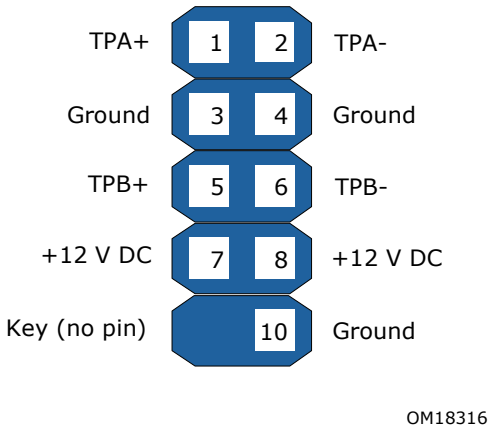


Figure 23. Connection Diagram for Front Panel IEEE 1394a Header

INTEGRATOR'S NOTES

- *The IEEE 1394a header is blue.*
- *The +12 V DC power on the IEEE 1394a header is fused.*
- *The IEEE 1394a header provides one IEEE 1394a port.*

2.8 Jumper Block

CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 24 shows the location of the jumper block. The 3-pin jumper block determines the BIOS Setup program's mode. Table 32 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configure mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

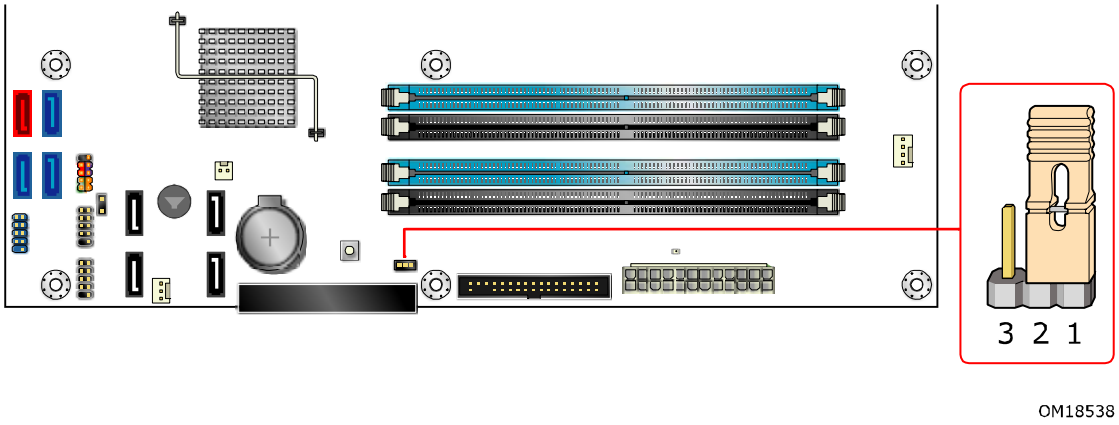
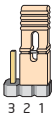
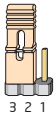


Figure 24. Location of the Jumper Block

Table 32. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

2.9 Mechanical Considerations

2.9.1 Form Factor

The board is designed to fit into an ATX-form-factor chassis. Figure 25 illustrates the mechanical form factor for the board. Dimensions are given in inches [millimeters]. The outer dimensions are 12.00 inches by 9.60 inches [304.80 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.

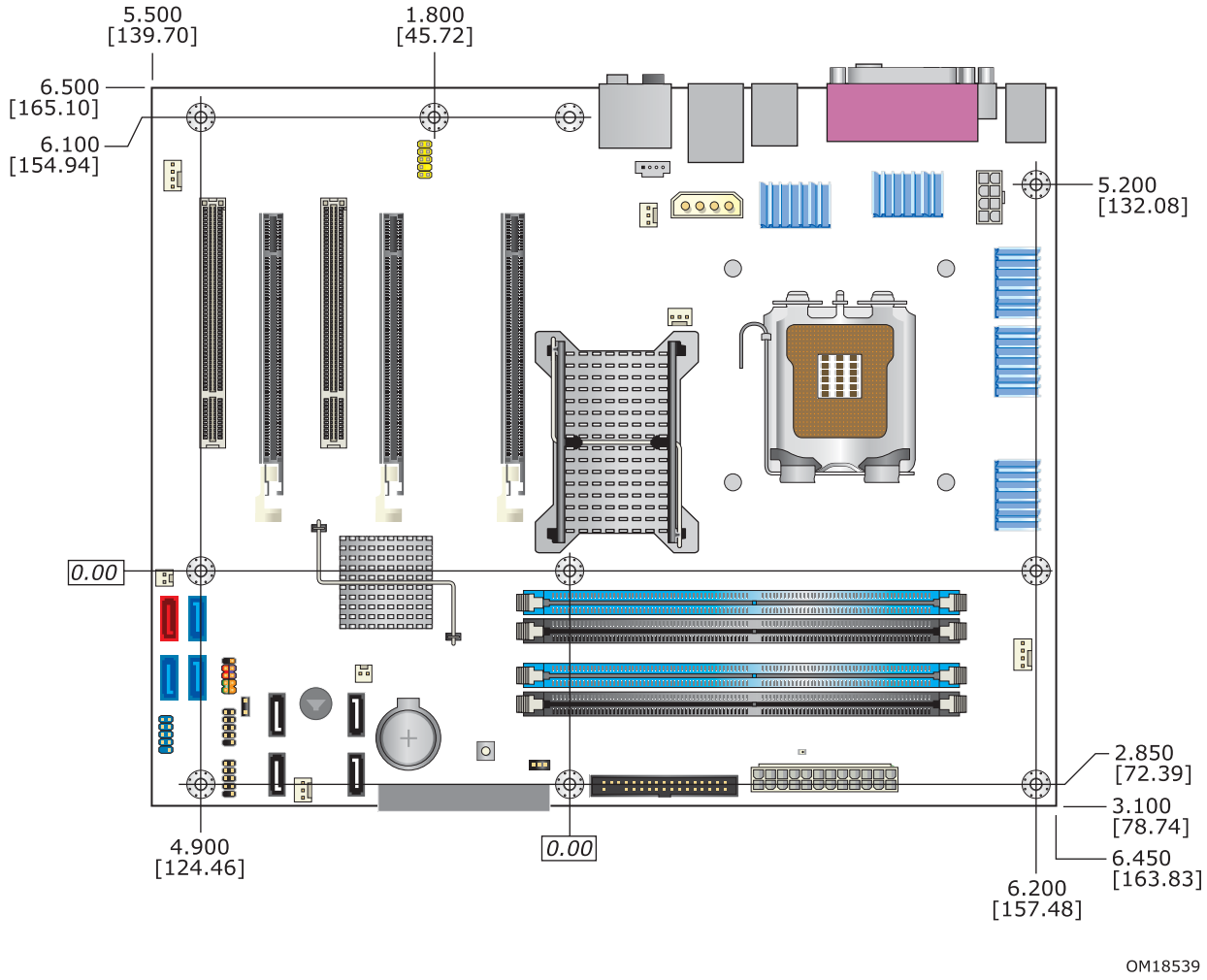


Figure 25. Board Dimensions

2.9.2 I/O Shield

The back panel I/O shield for the board must meet specific dimension and material requirements. Systems based on this board need the back panel I/O shield to pass certification testing. Figure 26 shows the I/O shield for boards with the 8-channel (7.1) audio subsystem. Figure 27 shows the I/O shield for boards with the 6-channel (5.1) audio subsystem. Dimensions are given in inches to a tolerance of ±0.02 inches. The figures also indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification.

NOTE

The I/O shield drawings in this document are for reference only. I/O shields compliant with the ATX chassis specification are available from Intel.

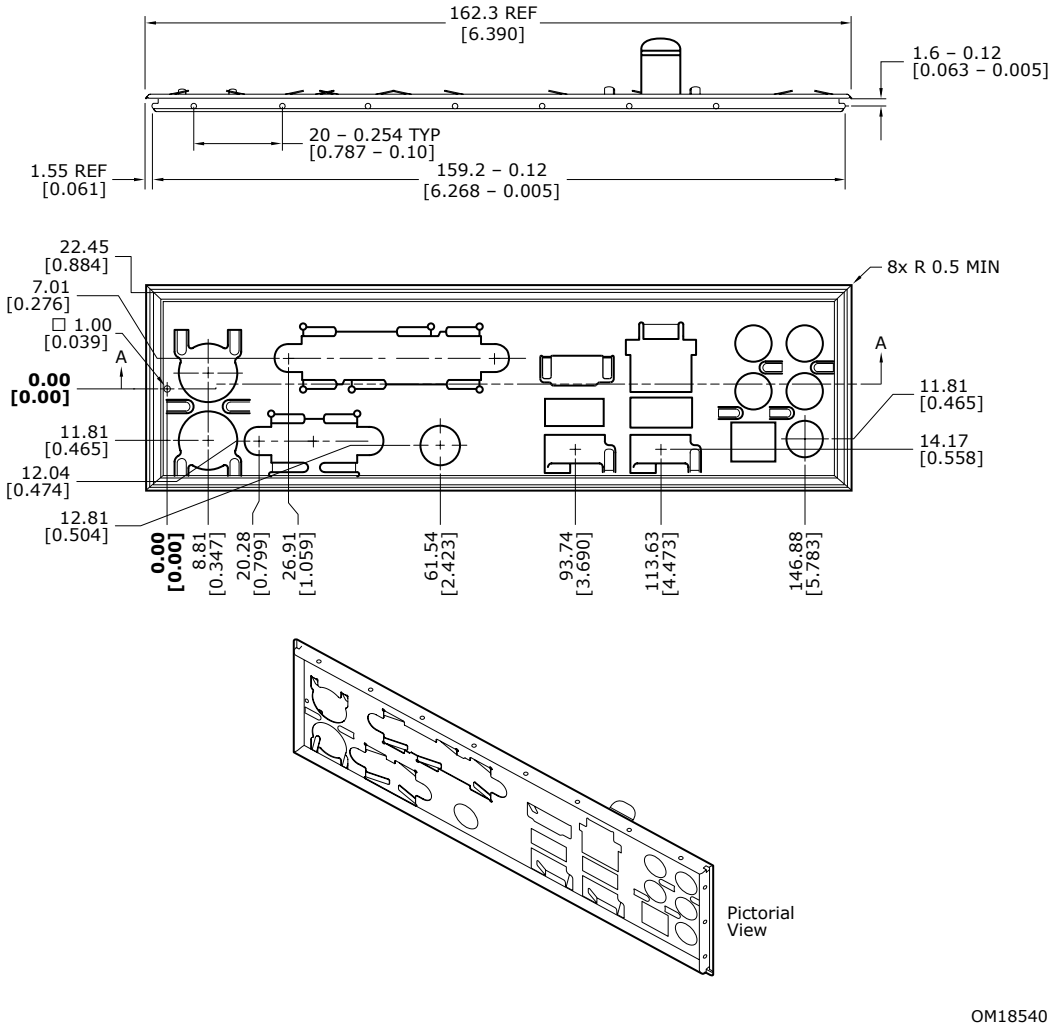


Figure 26. I/O Shield Dimensions for Boards with the 8-Channel (7.1) Audio Subsystem

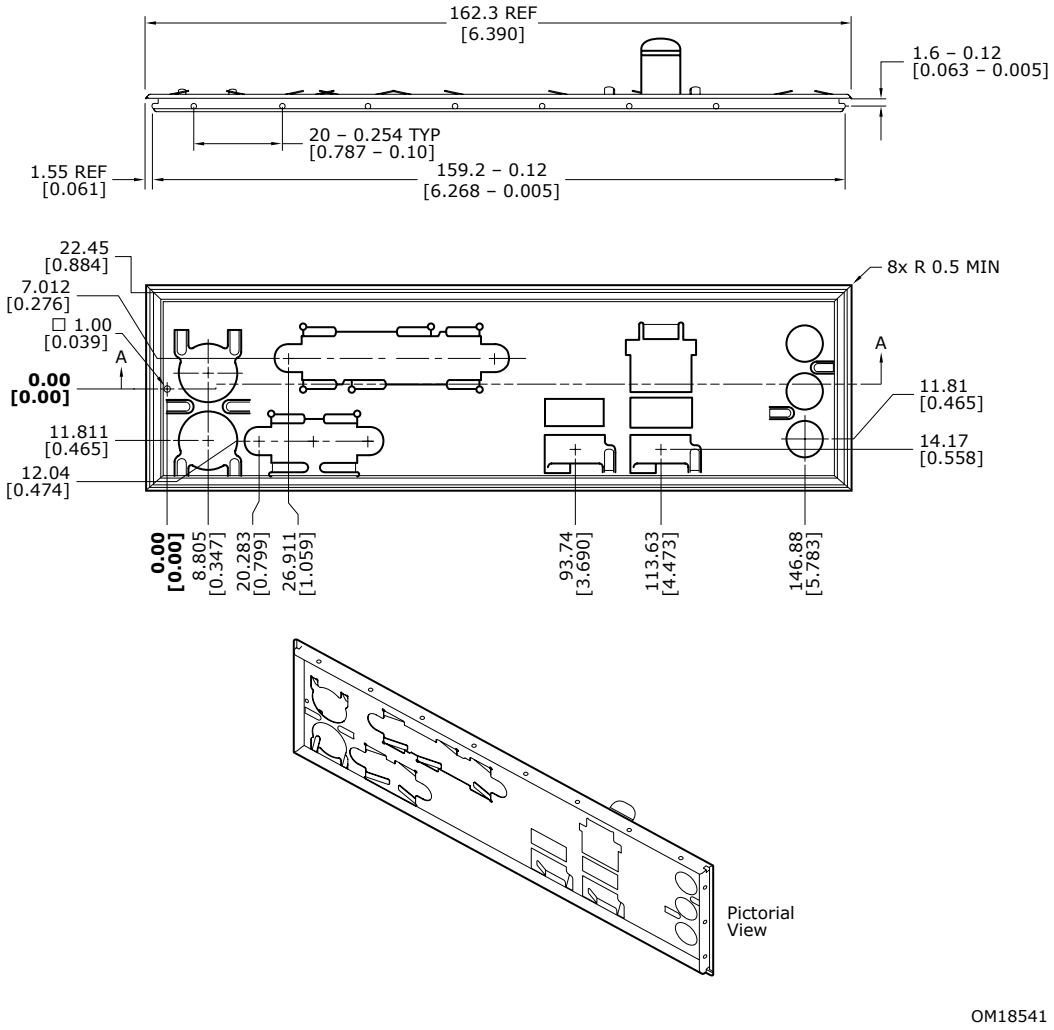


Figure 27. I/O Shield Dimensions for Boards with the 6-Channel (5.1) Audio Subsystem

2.10 Electrical Considerations

2.10.1 DC Loading

Table 33 lists the DC loading characteristics of the board. This data is based on a DC analysis of all active components within the board that impact its power delivery subsystems. The analysis does not include PCI add-in cards. Minimum values assume a light load placed on the board that is similar to an environment with no applications running and no USB current draw. Maximum values assume a load placed on the board that is similar to a heavy gaming environment with a 500 mA current draw per USB port. These calculations are not based on specific processor values or memory configurations but are based on the minimum and maximum current draw possible from the board's power delivery subsystems to the processor, memory, and USB ports.

Use the datasheets for add-in cards, such as PCI, to determine the overall system power requirements. The selection of a power supply at the system level is dependent on the system's usage model and not necessarily tied to a particular processor clock frequency.

Table 33. DC Loading Characteristics

		DC Current at:				
Mode	**DC Power**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 VSB**
Minimum loading	300 W	5 A	11 A	19 A	0 A	0.34 A (S0) 1.25 A (S3)
Maximum loading	750 W	25 A	27 A	46 A	0.40 A	0.34 A (S0) 1.25 A (S3)

2.10.2 Add-in Board Considerations

The board is designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards for the desktop board is as follows: a fully loaded board (all five expansion slots) must not exceed 10 A.

2.10.3 Fan Header Current Capability

⚠ CAUTION

The processor fan must be connected to the processor fan header, not to a chassis fan header. Connecting the processor fan to a chassis fan header may result in onboard component damage that will halt fan operation.

Table 34 lists the current capability of the fan headers.

Table 34. Fan Header Current Capability

Fan Connector	Maximum Available Current
Processor fan	3.0 A
Front chassis fan	1.5 A
Rear chassis fan	1.5 A
Auxiliary rear fan	3.0 A
MCH fan (optional)	1.5 A

2.10.4 Power Supply Considerations

⚠ CAUTION

The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

System integrators should refer to the power usage values listed in Table 33 when selecting a power supply for use with the board.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails
- The current capability of the +5 VSB line
- All timing parameters
- All voltage tolerances

2.11 Thermal Considerations

This board features a thermal protection circuit in the processor voltage regulator area. This circuit protects the processor voltage regulator from overheating and damaging the board. The thermal protection circuit in the processor voltage regulator sensor is triggered at approximately 120 °C. This trigger will cause the processor to enter a throttling mode (slowing down the processor if it exceeds its maximum operating temperature) and allow the processor voltage regulator to cool down.

INTEGRATOR'S NOTE

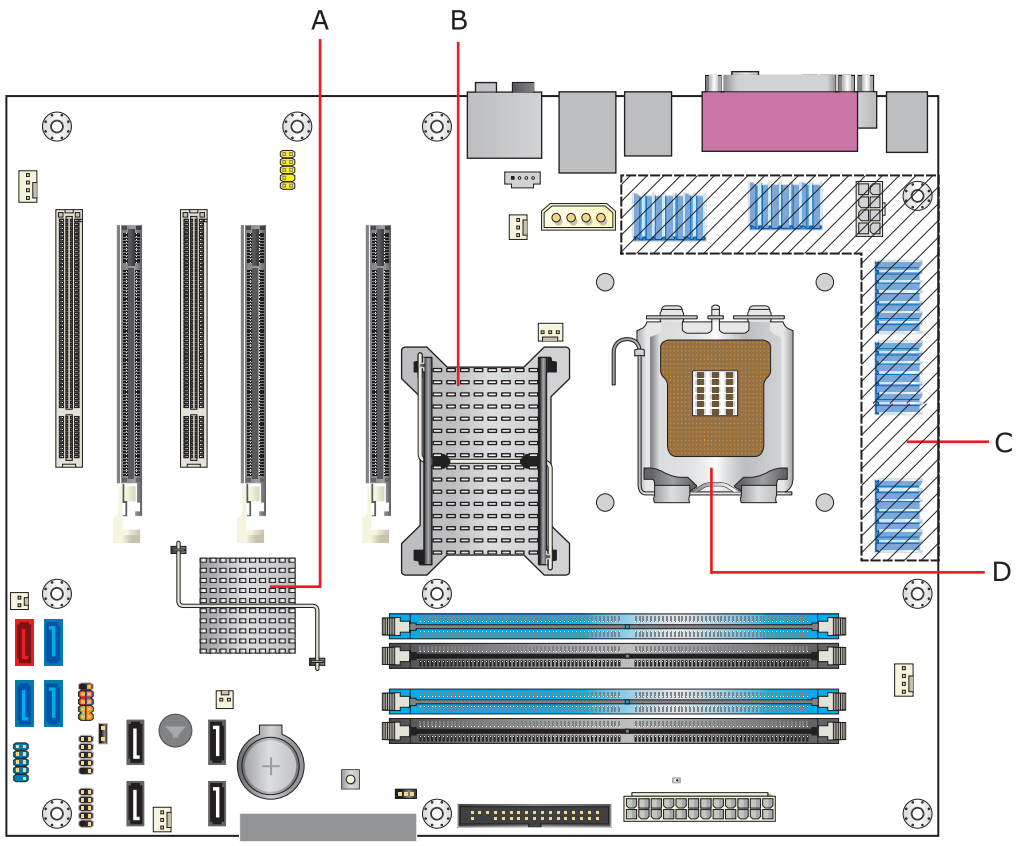
Use a processor heatsink that provides omni-directional airflow to maintain required airflow across the processor voltage regulator area.

CAUTION

When using BIOS Setup program options to increase processor voltage and frequency above the supported ranges, the temperature in the processor voltage regulator area will rise. This area of the board will require increased airflow. Direct airflow over the processor voltage regulator is crucial to preventing throttling and keeping the processor voltage regulator area cool. This is particularly important when using liquid cooling.

All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

Figure 28 shows the locations of the localized high temperature zones.



Item	Description
A	Intel 82801G ICH7-R/ICH7-DH
B	Intel 82975X MCH
C	Processor voltage regulator area
D	Processor

Figure 28. Localized High Temperature Zones

⚠ CAUTION

Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.13.

Table 35 provides maximum case temperatures for the components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

Table 35. Thermal Considerations for Components

Component	Temperature
Intel 82801G ICH7-R/ICH7-DH	110 °C (under bias)
Intel 82975X MCH	99 °C (under bias)
Processor	For processor case temperature, see processor datasheets and processor specification updates
Processor voltage regulator area	120 °C (under bias)

NOTE

For hardware monitoring application software, an alert point of 110 °C is recommended as a starting point for the processor voltage regulator area.

For information about	Refer to
Intel Pentium 4 processor datasheets and specification updates	Section 1.2, page 17

2.12 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 55 ºC. The MTBF for the board is 99,721 hours.

2.13 Environmental

Table 36 lists the environmental specifications for the board.

Table 36. Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second²		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec²)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz: 0.02 g² Hz (flat)		
Packaged	5 Hz to 40 Hz: 0.015 g² Hz (flat)		
	40 Hz to 500 Hz: 0.015 g² Hz sloping down to 0.00015 g² Hz		

3 Overview of BIOS Features

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3.5 Legacy USB Support 84
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3.8 BIOS Security Features 87

3.1 Introduction

The BIOS is stored in the Serial Peripheral Interface (SPI) Flash device and can be updated using a disk-based program. The SPI contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as BX97520J.86A.

When the BIOS Setup configuration jumper is set to configure mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Performance	Security	Power	Boot	Exit

NOTE

The maintenance menu is displayed only when the board is in configure mode. Section 2.8 on page 70 shows how to put the board in configure mode.

The performance menu is an optional menu and not present on all versions of the board.

Table 37 lists the BIOS Setup program menu features.

Table 37. BIOS Setup Program Menu Bar

Menu	Function
Maintenance	Clears passwords and displays processor information
Main	Displays processor and memory configuration
Advanced	Configures advanced features available through the chipset
Performance	Allows adjustment of processor and memory timing parameters
Security	Sets passwords and security features
Power	Configures power management features and power supply controls
Boot	Selects boot options
Exit	Saves or discards changes to Setup program options

Table 38 lists the function keys available for menu screens.

Table 38. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (moves the cursor left or right)
<↑> or <↓>	Selects an item (moves the cursor up or down)
<Tab>	Selects a field (not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

3.2 Resource Configuration

3.2.1 PCI Autoconfiguration

The BIOS automatically configures PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

3.2.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the PCI IDE connector with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives. The interface also supports second-generation SATA drives. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for

Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.3 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor clock frequency
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Microsoft Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

3.4 Watchdog Timer

The board includes a watchdog timer circuit. The watchdog timer provides automatic recovery after two failed power-on self-tests (POSTs) following use of the BIOS performance menu.

3.5 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system.
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, follow the operating system's installation instructions.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Microsoft Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette or a CD-ROM.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 17

3.6.1 Language Support

The BIOS Setup program and help messages are supported in US English. Additional languages are available in the Integrator's Toolkit utility. Check the Intel website for details.

3.6.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. The Integrator's Toolkit that is available from Intel can be used to create a custom splash screen.

NOTE

If you add a custom splash screen, it will share space with the Intel branded logo.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 17

3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.7.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

3.7.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

3.7.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.7.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program's Boot Device Priority Submenu). Table 39 lists the boot device menu options.

Table 39. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without saving changes

3.8 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.

Table 40 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 40. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

4 Error Messages and Beep Codes

What This Chapter Contains

4.1 Speaker 89
4.2 BIOS Beep Codes 89
4.3 BIOS Error Messages 89
4.4 Port 80h POST Codes 90

4.1 Speaker

The board-mounted speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker	Figure 1, page 14

4.2 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 41).

Table 41. Beep Codes

Type	Pattern	Frequency
Memory error	Three long beeps	1280 Hz
Thermal warning	Four alternating beeps: High tone, low tone, high tone, low tone	High tone: 2000 Hz Low tone: 1600 Hz

4.3 BIOS Error Messages

Table 42 lists the error messages and provides a brief description of each.

Table 42. BIOS Error Messages

Error Message	Explanation
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.

4.4 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

NOTE

The POST card must be installed in PCI bus connector 1.

The following tables provide information about the POST codes generated by the BIOS:

- Table 43 lists the Port 80h POST code ranges
- Table 44 lists the Port 80h POST codes themselves
- Table 45 lists the Port 80h POST sequence

NOTE

In the tables listed above, all POST codes and range values are listed in hexadecimal.

Table 43. Port 80h POST Code Ranges

Range	Category/Subsystem
00 – 0F	Debug codes: Can be used by any PEIM/driver for debug.
10 – 1F	Host Processors: 1F is an unrecoverable CPU error.
20 – 2F	Memory/Chipset: 2F is no memory detected or no useful memory detected.
30 – 3F	Recovery: 3F indicated recovery failure.
40 – 4F	Reserved for future use
50 – 5F	I/O buses: PCI, USB, ISA, ATA, etc. 5F is an unrecoverable error. Start with PCI.
60 – 6F	Reserved for future use (for new buses)
70 – 7F	Output devices: All output consoles. 7F is an unrecoverable error.
80 – 8F	Reserved for future use (new output console codes)
90 – 9F	Input devices: Keyboard/Mouse. 9F is an unrecoverable error.
A0 – AF	Reserved for future use (new input console codes)
B0 – BF	Boot devices: Includes fixed media and removable media. BF is an unrecoverable error.
C0 – CF	Reserved for future use
D0 – DF	Boot device selection
E0 – FF	F0 – FF: FF processor exception. E0 – EE: Miscellaneous codes. See Table 44. EF boot/S3: resume failure.

Table 44. Port 80h POST Codes

POST Code	Description of POST Operation
	Host Processor
10	Power-on initialization of the host processor (Boot Strap Processor)
11	Host processor Cache initialization (including APs)
12	Starting Application processor initialization
13	SMM initialization
	Chipset
21	Initializing a chipset component
	Memory
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
24	Programming timing parameters in the memory controller and the DIMMs
25	Configuring memory
26	Optimizing memory settings
27	Initializing memory, such as ECC init
28	Testing memory
	PCI Bus
50	Enumerating PCI buses
51	Allocating resources to PCI bus
52	Hot Plug PCI controller initialization
53 – 57	Reserved for PCI Bus
	USB
58	Resetting USB bus
59	Reserved for USB
	ATA/ATAPI/SATA
5A	Resetting PATA/SATA bus and all devices
5B	Reserved for ATA
	SMBus
5C	Resetting SMBUS
5D	Reserved for SMBUS
	Local Console
70	Resetting the VGA controller
71	Disabling the VGA controller
72	Enabling the VGA controller
	Remote Console
78	Resetting the console controller
79	Disabling the console controller
7A	Enabling the console controller

continued

Table 44. Port 80h POST Codes (continued)

POST Code	Description of POST Operation
	Keyboard (PS2 or USB)
90	Resetting keyboard
91	Disabling the keyboard
92	Detecting the presence of the keyboard
93	Enabling the keyboard
94	Clearing keyboard input buffer
95	Instructing keyboard controller to run Self Test (PS2 only)
	Mouse (PS2 or USB)
98	Resetting mouse
99	Detecting mouse
9A	Detecting presence of mouse
9B	Enabling mouse
	Fixed Media
B0	Resetting fixed media
B1	Disabling fixed media
B2	Detecting presence of a fixed media (IDE hard drive detection, etc.)
B3	Enabling/configuring a fixed media
	Removable media
B8	Resetting removable media
B9	Disabling removable media
BA	Detecting presence of a removable media (IDE, CD-ROM detection, etc.)
BC	Enabling/configuring a removable media
	BDS
D*y*	Trying boot selection y (y=0 to 15)
	PEI Core
E0	Started dispatching PEIMs (emitted on first report of EFI_SW_PC_INIT_BEGIN EFI_SW_PEI_PC_HANDOFF_TO_NEXT)
E2	Permanent memory found
E1, E3	Reserved for PEI/PEIMs
	DXE Core
E4	Entered DXE phase
E5	Started dispatching drivers
E6	Started connecting drivers

continued

Table 44. Port 80h POST Codes (continued)

POST Code	Description of POST Operation
	DXE Drivers
E7	Waiting for user input
E8	Checking password
E9	Entering BIOS setup
EB	Calling Legacy Option ROMs
	Runtime Phase/EFI OS Boot
F4	Entering Sleep state
F5	Exiting Sleep state
F8	EFI boot service ExitBootServices ( ) has been called
F9	EFI runtime service SetVirtualAddressMap ( ) has been called
FA	EFI runtime service ResetSystem ( ) has been called
	PEIMs/Recovery
30	Crisis Recovery has initiated per user request
31	Crisis Recovery has initiated by software (corrupt flash)
34	Loading recovery capsule
35	Handing off control to the recovery capsule
3F	Unable to recover

Table 45. Typical Port 80h POST Sequence

POST Code	Description
21	Initializing a chipset component
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
25	Configuring memory
28	Testing memory
34	Loading recovery capsule
E4	Entered DXE phase
12	Starting Application processor initialization
13	SMM initialization
50	Enumerating PCI buses
51	Allocating resourced to PCI bus
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
95	Keyboard Self Test
EB	Calling Video BIOS
58	Resetting USB bus
5A	Resetting PATA/SATA bus and all devices
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
5A	Resetting PATA/SATA bus and all devices
28	Testing memory
90	Resetting keyboard
94	Clearing keyboard input buffer
E7	Waiting for user input
01	INT 19
00	Ready to boot

5 Regulatory Compliance and Battery Disposal Information

What This Chapter Contains

5.1 Regulatory Compliance 95
5.2 Battery Disposal Information 103

5.1 Regulatory Compliance

This section contains the following regulatory compliance information for Desktop Board D975XBX2:

- Safety regulations
- European Union Declaration of Conformity statement
- Product Ecology statements
- Electromagnetic Compatibility (EMC) regulations
- Product certification markings

5.1.1 Safety Regulations

Desktop Board D975XBX2 complies with the safety regulations stated in Table 46 when correctly installed in a compatible host system.

Table 46. Safety Regulations

Regulation	Title
UL 60950-1:2003/ CSA C22.2 No. 60950-1-03	Information Technology Equipment – Safety - Part 1: General Requirements (USA and Canada)
EN 60950-1:2002	Information Technology Equipment – Safety - Part 1: General Requirements (European Union)
IEC 60950-1:2001, First Edition	Information Technology Equipment – Safety - Part 1: General Requirements (International)

5.1.2 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the product Intel® Desktop Board D975XBX2 is in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 89/336/EEC (EMC Directive) and Council Directive 73/23/EEC (Safety/Low Voltage Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.

This product follows the provisions of the European Directives 89/336/EEC and 73/23/EEC.

Čeština Tento výrobek odpovídá požadavkům evropských směrnic 89/336/EEC a 73/23/EEC.

Dansk Dette produkt er i overensstemmelse med det europæiske direktiv 89/336/EEC & 73/23/EEC.

Dutch Dit product is in navolging van de bepalingen van Europees Directief 89/336/EEC & 73/23/EEC.

Eesti Antud toode vastab Euroopa direktiivides 89/336/EEC ja 73/23/EEC kehtestatud nõuetele.

Suomi Tämä tuote noudattaa EU-direktiivin 89/336/EEC & 73/23/EEC määräyksiä.

Français Ce produit est conforme aux exigences de la Directive Européenne 89/336/EEC & 73/23/EEC.

Deutsch Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 89/336/EEC & 73/23/EEC.

Ελληνικά Το παρόν προϊόν ακολουθεί τις διατάξεις των Ευρωπαϊκών Οδηγιών 89/336/ΕΟΚ και 73/23/ΕΟΚ.

Magyar E termék megfelel a 89/336/EEC és 73/23/EEC Európai Irányelv előírásainak.

Icelandic Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 89/336/ EEC & 73/23/EEC.

Italiano Questo prodotto è conforme alla Direttiva Europea 89/336/EEC & 73/23/EEC.

Latviešu Šis produkts atbilst Eiropas Direktīvu 89/336/EEC un 73/23/EEC noteikumiem.

Lietuvių Šis produktas atitinka Europos direktyvų 89/336/EEC ir 73/23/EEC nuostatas.

Malti Dan il-prodott hu konformi mal-provvedimenti tad-Direttivi Ewropej 89/336/EEC u 73/23/EEC.

Norsk Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 89/336/ EEC & 73/23/EEC.

Polski Niniejszy produkt jest zgodny z postanowieniami Dyrektyw Unii Europejskiej 89/336/EWG i 73/23/EWG.

Portuguese Este produto cumpre com as normas da Diretiva Européia 89/336/EEC & 73/23/EEC.

Español Este producto cumple con las normas del Directivo Europeo 89/336/EEC & 73/23/EEC.

Slovensky Tento produkt je v súlade s ustanoveniami európskych direktív 89/336/EEC a 73/23/EEC.

Slovenščina Izdelek je skladen z določbami evropskih direktiv 89/336/EGS in 73/23/EGS.

Svenska Denna produkt har tillverkats i enlighet med EG-direktiv 89/336/EEC & 73/23/EEC.

Türkçe Bu ürün, Avrupa Birliği'nin 89/336/EEC ve 73/23/EEC yönergelerine uyar.

5.1.3 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

5.1.3.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

5.1.3.2 Recycling Considerations

As part of its commitment to environmental responsibility, Intel has implemented the Intel Product Recycling Program to allow retail consumers of Intel's branded products to return used products to select locations for proper recycling.

Please consult the http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm for the details of this program, including the scope of covered products, available locations, shipping instructions, terms and conditions, etc.

中文

作为其对环境责任之承诺的部分，英特尔已实施 Intel Product Recycling Program（英特尔产品回收计划），以允许英特尔品牌产品的零售消费者将使用过的产品退还至指定地点作恰当的重复使用处理。

请参考http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm 了解此计划的详情，包括涉及产品之范围、回收地点、运送指导、条款和条件等。

Deutsch

Als Teil von Intels Engagement für den Umweltschutz hat das Unternehmen das Intel Produkt-Recyclingprogramm implementiert, das Einzelhandelskunden von Intel Markenprodukten ermöglicht, gebrauchte Produkte an ausgewählte Standorte für ordnungsgemäßes Recycling zurückzugeben.

Details zu diesem Programm, einschließlich der darin eingeschlossenen Produkte, verfügbaren Standorte, Versandanweisungen, Bedingungen usw., finden Sie auf der http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm

Español

Como parte de su compromiso de responsabilidad medioambiental, Intel ha implantado el programa de reciclaje de productos Intel, que permite que los consumidores al detalle de los productos Intel devuelvan los productos usados en los lugares seleccionados para su correspondiente reciclado.

Consulte la http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm para ver los detalles del programa, que incluye los productos que abarca, los lugares disponibles, instrucciones de envío, términos y condiciones, etc.

Français

Dans le cadre de son engagement pour la protection de l'environnement, Intel a mis en œuvre le programme Intel Product Recycling Program (Programme de recyclage des produits Intel) pour permettre aux consommateurs de produits Intel de recycler les produits usés en les retournant à des adresses spécifiées.

Visitez la page Web http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm pour en savoir plus sur ce programme, à savoir les produits concernés, les adresses disponibles, les instructions d'expédition, les conditions générales, etc.

日本語

インテルでは、環境保護活動の一環として、使い終えたインテル
ブランド製品を指定の場所へ返送していただき、リサイクルを適切に行えるよう、インテル製品リサイクル
プログラムを発足させました。

対象製品、返送先、返送方法、ご利用規約など、このプログラムの詳細情報は、http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm（英語）をご覧ください。

Malay

Sebagai sebahagian daripada komitmennya terhadap tanggungjawab persekitaran, Intel telah melaksanakan Program Kitar Semula Produk untuk membenarkan pengguna-pengguna runcit produk jenama Intel memulangkan produk terguna ke lokasi-lokasi terpilih untuk dikitarkan semula dengan betul.

Sila rujuk http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm untuk mendapatkan butir-butir program ini, termasuklah skop produk yang dirangkumi, lokasi-lokasi tersedia, arahan penghantaran, terma & syarat, dsb.

Portuguese

Como parte deste compromisso com o respeito ao ambiente, a Intel implementou o Programa de Reciclagem de Produtos para que os consumidores finais possam enviar produtos Intel usados para locais selecionados, onde esses produtos são reciclados de maneira adequada.

Consulte o site http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm (em Inglês) para obter os detalhes sobre este programa, inclusive o escopo dos produtos cobertos, os locais disponíveis, as instruções de envio, os termos e condições, etc.

Russian

В качестве части своих обязательств к окружающей среде, в Intel создана программа утилизации продукции Intel (Product Recycling Program) для предоставления конечным пользователям марок продукции Intel возможности возврата используемой продукции в специализированные пункты для должной утилизации.

Пожалуйста, обратитесь на веб-сайт http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm за информацией об этой программе, принимаемых продуктах, местах приема, инструкциях об отправке, положениях и условиях и т.д.

Türkçe

Intel, çevre sorumluluğuna bağımlılığının bir parçası olarak, perakende tüketicilerin Intel markalı kullanılmış ürünlerini belirlenmiş merkezlere iade edip uygun şekilde geri dönüştürmesini amaçlayan Intel Ürünleri Geri Dönüşüm Programı'nı uygulamaya koymuştur.

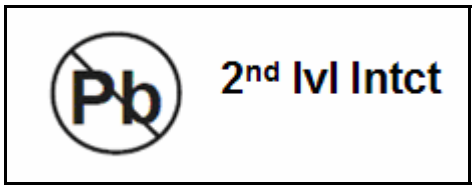
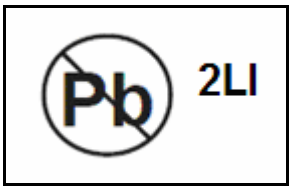
Bu programın ürün kapsamı, ürün iade merkezleri, nakliye talimatları, kayıtlar ve şartlar v.s dahil bütün ayrıntılarını ögrenmek için lütfen http://www.intel.com/intel/other/ehs/product_ecology/Recycling_Program.htm

Web sayfasına gidin.

5.1.3.3 Lead Free Desktop Board

This desktop board is lead free although certain discrete components used on the board contain a small amount of lead which is necessary for component performance and/or reliability. This desktop board is referred to as "Lead-free second level interconnect." The board substrate and the solder connections from the board to the components (second-level connections) are all lead free. Table 47 shows the various forms of the "Lead-Free 2nd Level Interconnect" mark as it appears on the board and accompanying collateral.

Table 47. Lead-Free Board Markings

Description	Mark
Lead-Free 2nd Level Interconnect: This symbol is used to identify electrical and electronic assemblies and components in which the lead (Pb) concentration level in the desktop board substrate and the solder connections from the board to the components (second-level interconnect) is not greater than 0.1% by weight (1000 ppm).	 **or**  **or** 

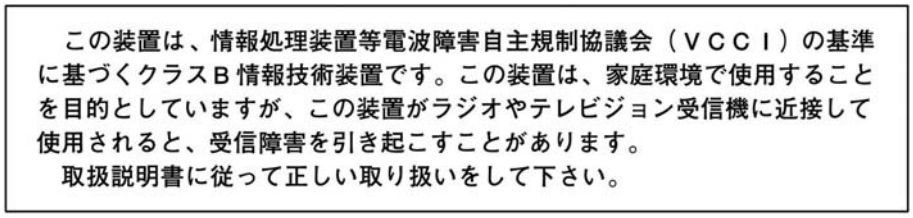
5.1.4 EMC Regulations

Desktop Board D975XBX2 complies with the EMC regulations stated in Table 48 when correctly installed in a compatible host system.

Table 48. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radio Frequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022: 1998 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS CISPR 22 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 3rd Edition, (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurement. (International)
VCCI (Class B)	Voluntary Control Council for Interference by Information Technology Equipment. (Japan)

Japanese Kanji statement translation: this is a Class B product based on the standard of the Voluntary Control Council for Interference from Information Technology Equipment (VCCI). If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.



Korean Class B statement translation: this is household equipment that is certified to comply with EMC requirements. You may use this equipment in residential environments and other non-residential environments.

이 기기는 가정용으로 전자파적합등록을 한 기기로서
주거지역에서는 물론 모든 지역에서 사용할 수 있습니다.

5.1.5 Product Certification Markings (Board Level)

Desktop Board D975XBX2 has the product certification markings shown in Table 49:

Table 49. Product Certification Markings

Description	Mark
UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel desktop boards: E210882.	
FCC Declaration of Conformity logo mark for Class B equipment. Includes Intel name and D975XBX2 model designation.	
CE mark. Declaring compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC).	
Australian Communications Authority (ACA) C-tick mark. Includes adjacent Intel supplier code number, N-232.	
Japan VCCI (Voluntary Control Council for Interference) mark.	
S. Korea MIC (Ministry of Information and Communication) mark. Includes adjacent MIC certification number: CPU-D975XBX2 For information about MIC certification, go to http://support.intel.com/support/motherboards/desktop/	
Taiwan BSMI (Bureau of Standards, Metrology and Inspections) mark. Includes adjacent Intel company number, D33025.	
Printed wiring board manufacturer's recognition mark. Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side).	V-0

5.2 Battery Disposal Information

CAUTION

Risk of explosion if the battery is replaced with an incorrect type. Batteries should be recycled where possible. Disposal of used batteries must be in accordance with local environmental regulations.

PRECAUTION

Risque d'explosion si la pile usagée est remplacée par une pile de type incorrect. Les piles usagées doivent être recyclées dans la mesure du possible. La mise au rebut des piles usagées doit respecter les réglementations locales en vigueur en matière de protection de l'environnement.

FORHOLDSREGEL

Eksplosionsfare, hvis batteriet erstattes med et batteri af en forkert type. Batterier bør om muligt genbruges. Bortskaffelse af brugte batterier bør foregå i overensstemmelse med gældende miljølovgivning.

OBS!

Det kan oppstå eksplosjonsfare hvis batteriet skiftes ut med feil type. Brukte batterier bør kastes i henhold til gjeldende miljølovgivning.

VIKTIGT!

Risk för explosion om batteriet ersätts med felaktig batterityp. Batterier ska kasseras enligt de lokala miljövårdsbestämmelserna.

VARO

Räjähdysvaara, jos pariston tyyppi on väärä. Paristot on kierrätettävä, jos se on mahdollista. Käytetyt paristot on hävitettävä paikallisten ympäristömääräysten mukaisesti.

VORSICHT

Bei falschem Einsetzen einer neuen Batterie besteht Explosionsgefahr. Die Batterie darf nur durch denselben oder einen entsprechenden, vom Hersteller empfohlenen Batterietyp ersetzt werden. Entsorgen Sie verbrauchte Batterien den Anweisungen des Herstellers entsprechend.

AVVERTIMENTO

Esiste il pericolo di un esplosione se la pila non viene sostituita in modo corretto. Utilizzare solo pile uguali o di tipo equivalente a quelle consigliate dal produttore. Per disfarsi delle pile usate, seguire le istruzioni del produttore.

PRECAUCIÓN

Existe peligro de explosión si la pila no se cambia de forma adecuada. Utilice solamente pilas iguales o del mismo tipo que las recomendadas por el fabricante del equipo. Para deshacerse de las pilas usadas, siga igualmente las instrucciones del fabricante.

WAARSCHUWING

Er bestaat ontploffingsgevaar als de batterij wordt vervangen door een onjuist type batterij. Batterijen moeten zoveel mogelijk worden gerecycled. Houd u bij het weggooien van gebruikte batterijen aan de plaatselijke milieuwetgeving.

ATENÇÃO

Haverá risco de explosão se a bateria for substituída por um tipo de bateria incorreto. As baterias devem ser recicladas nos locais apropriados. A eliminação de baterias usadas deve ser feita de acordo com as regulamentações ambientais da região.

AŚCIAROŽZNAŚĆ

Існуе рызыка выбуху, калі заменены акумулятар неправільнага тыпу. Акумулятары павінны, па магчымасці, перепрацоўвацца. Пазбаўляцца ад старых акумулятараў патрэбна згодна з мясцовым заканадаўствам па экалогіі.

UPOZORNÌNÍ

V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.

Προσοχή

Υπάρχει κίνδυνος για έκρηξη σε περίπτωση που η μπαταρία αντικατασταθεί από μία λανθασμένου τύπου. Οι μπαταρίες θα πρέπει να ανακυκλώνονται όταν κάτι τέτοιο είναι δυνατό. Η απόρριψη των χρησιμοποιημένων μπαταριών πρέπει να γίνεται σύμφωνα με τους κατά τόπο περιβαλλοντικούς κανονισμούς.

VIGYAZAT

Ha a telepet nem a megfelelő típusú telepre cseréli, az felrobbanhat. A telepeket lehetőség szerint újra kell hasznosítani. A használt telepeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.

注意

異なる種類の電池を使用すると、爆発の危険があります。リサイクルが可能な地域であれば、電池をリサイクルしてください。使用後の電池を破棄する際には、地域の環境規制に従ってください。

AWAS

Risiko letupan wujud jika bateri digantikan dengan jenis yang tidak betul. Bateri sepatutnya dikitar semula jika boleh. Pelupusan bateri terpakai mestilah mematuhi peraturan alam sekitar tempatan.

OSTRZEŻENIE

Istnieje niebezpieczeństwo wybuchu w przypadku zastosowania niewłaściwego typu baterii. Zużyte baterie należy w miarę możliwości utylizować zgodnie z odpowiednimi przepisami ochrony środowiska.

PRECAUŢIE

Risc de explozie, dacă bateria este înlocuită cu un tip de baterie necorespunzător. Bateriile trebuie reciclate, dacă este posibil. Depozitarea bateriilor uzate trebuie să respecte reglementările locale privind protecţia mediului.

ВНИМАНИЕ

При использовании батареи несоответствующего типа существует риск ее взрыва. Батареи должны быть утилизированы по возможности. Утилизация батарей должна проводится по правилам, соответствующим местным требованиям.

UPOZORNENIE

Ak batériu vymeníte za nesprávny typ, hrozí nebezpečenstvo jej výbuchu.
Batérie by sa mali podľa možnosti vždy recyklovať. Likvidácia použitých batérií sa musí vykonávať v súlade s miestnymi predpismi na ochranu životného prostredia.

POZOR

Zamenjava baterije z baterijo drugačnega tipa lahko povzroči eksplozijo.
Če je mogoče, baterije reciklirajte. Rabljene baterije zavrzite v skladu z lokalnimi okoljevarstvenimi predpisi.

คำเตือน

ระวังการระเบิดที่เกิดจากเปลี่ยนแบตเตอรี่ผิดประเภท หากเป็นไปได้ ควรนำแบตเตอรี่ไปรีไซเคิล การทิ้งแบตเตอรี่ใช้แล้วต้องเป็นไปตามกฎข้อบังคับด้านสิ่งแวดล้อมของท้องถิ่น.

UYARI

Yanlış türde pil takıldığında patlama riski vardır. Piller mümkün olduğunda geri dönüştürülmelidir. Kullanılmış piller, yerel çevre yasalarına uygun olarak atılmalıdır.

ОСТОРОГА

Використовуйте батареї правильного типу, інакше існуватиме ризик вибуху.
Якщо можливо, використані батареї слід утилізувати. Утилізація використаних батарей має бути виконана згідно місцевих норм, що регулюють охорону довкілля.

UPOZORNĚNÍ

V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.

ETTEVAATUST

Kui patarei asendatakse uue ebasobivat tüüpi patareiga, võib tekkida plahvatusoht. Tühjad patareid tuleb võimaluse korral viia vastavasse kogumispunkti. Tühjade patareide äraviskamisel tuleb järgida kohalikke keskkonnakaitse alaseid reegleid.

FIGYELMEZTETÉS

Ha az elemet nem a megfelelő típusúra cseréli, felrobbanhat. Az elemeket lehetőség szerint újra kell hasznosítani. A használt elemeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.

UZMANĪBU

Pastāv eksplozijas risks, ja baterijas tiek nomainītas ar nepareiza veida baterijām. Ja iespējams, baterijas vajadzētu nodot attiecīgos pieņemšanas punktos. Bateriju izmešanai atkritumos jānotiek saskaņā ar vietējiem vides aizsardzības noteikumiem.

DĖMESIO

Naudojant netinkamo tipo baterijas įrenginys gali sprogti. Kai tik įmanoma, baterijas reikia naudoti pakartotinai. Panaudotas baterijas išmesti būtina pagal vietinius aplinkos apsaugos nuostatus.

ATTENZJONI

Riskju ta' splużjoni jekk il-batterija tinbidel b'tip ta' batterija mhux korrett. Il-batteriji għandhom jiġu riċiklati fejn hu possibbli. Ir-rimi ta' batteriji użati għandu jsir skond ir-regolamenti ambjentali lokali.

OSTRZEŻENIE

Ryzyko wybuchu w przypadku wymiany na baterie niewłaściwego typu. W miarę możliwości baterie należy poddać recyklingowi. Zużytych baterii należy pozbywać się zgodnie z lokalnie obowiązującymi przepisami w zakresie ochrony środowiska.