



Intel® Desktop Board D955XCS Specification Update

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The Intel® Desktop Board D955XCS may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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The Intel® desktop board D955XCS may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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REVISION HISTORY

Date of Revision	Version	Description
July 13, 2005	-001	This document is the first Specification Update for the Intel® Desktop Board D955XCS.
October 2005	-002	Added Erratum 1 and updated General Information table.
June 2006	-003	Added Erratum 2 and 3, Documentation Changes 1. Updated Basic Desktop Board D955XCS Identification Information table.
November 2006	-004	Added Erratum 4 and Specification Change 1.
February 2007	-005	Added Specification Change 2.



PREFACE

This document is an update to the specifications contained in the *Intel® Desktop Board D955XCS Technical Product Specification* (Order Number D14066). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

For specification updates concerning the Intel processor that may apply to this desktop board, refer to the following:

- *Intel® Pentium® D Processor 900Δ Sequence and Intel® Pentium® Processor Extreme Edition 955Δ, 965Δ Specification Update* (Order Number 310307)
- *Intel® Pentium® D Processor 800Δ Sequence and Intel® Pentium® Processor Extreme Edition 840Δ Specification Update* (Order Number 306832)
- *Intel® Pentium® 4 Processor 6x1Δ Sequence Specification Update* (Order Number 310309)
- *Intel® Pentium® 4 Processor on 90 nm Process Specification Update* (Order Number 302352)
- *Intel® Pentium® 4 Processor Specification Update* (Order Number 249199)

Unless otherwise noted in this document, it should be assumed that any processor errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Refer to the *Intel® 955X Express Chipset Specification Update* (Order Number 306829) for specification updates concerning the 82955X MCH Controller and that may apply to the desktop board D955XCS. Unless otherwise noted in this document, it should be assumed that any MCH errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Refer to the *Intel® IO Controller Hub 7 (ICH7) Family Specification Update* (Order Number 307014) for specification updates concerning the 82801GB I/O Controller Hub and that may apply to the desktop board D955XCS. Unless otherwise noted in this document, it should be assumed that any ICH 7 errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the desktop board D955XCS's behavior to deviate from published specifications. Hardware and software designed to be used with any given Altered Assembly (AA) and BIOS revision level must assume that all errata documented for that AA and BIOS revision level are present on all desktop boards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for the Intel® Desktop Board D955XCS



GENERAL INFORMATION

Basic Desktop Board D955XCS Identification Information

AA Revision	BIOS Revision	Notes
C93516-304	BK95510J.86A.1618	1,2
C93516-401	BK95510J.86A.1784	1,2
C93516-402	BK95510J.86A.1784	1,2
C93516-403	BK95510J.86A.2015	1,2

NOTES:

1. The AA number is found on a small label on the component side of the board.
2. The 82955XE Chipset kit used on this AA revision consists of two components as follows:

Device	Stepping	S-Spec Numbers
82955X MCH	A1	SL8FW
82801GR ICH7	A1	SL8FY



Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes that apply to the Intel® Desktop Board D955XCS. Intel intends to fix some of the errata in a future revision of the desktop board, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future revision of the desktop board, driver, or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Plan Fix	Changes to Section 1.11.2 Audio Connectors
2	Doc	Changes to Section 1.12.1 Intel® 82573E/82573V Gigabit Ethernet Controller
NO.	PLANS	ERRATA
1	Plan Fix	Intel® Precision Cooling Could Fail and Only Run at a Maximum or Minimum PWM for CPU Fan
2	Plan Fix	Hardware Monitoring and Fan Control Could Fail and Only Run at a Maximum or Minimum PWM for CPU Fan
3	Plan Fix	Silkscreen Markings for the Front and Rear Fan are Reversed
4	Plan Fix	Voltage Regulator Controllers may cause system to hang/freeze during the operating system boot
NO.	PLANS	DOCUMENTATION CHANGES
1	Doc	Change to Section 3.7.2, BIOS Boot Optimizations



SPECIFICATION CHANGES

1. *The following note will be added to the Technical Product Specification in Section 1.11.2 Audio Connectors:*



INTEGRATOR'S NOTES

Electrostatic discharge (ESD) can damage desktop board components. Front-panel connectors should provide sufficient protection to prevent ESD damage to components inside the chassis enclosure.

2. *Section 1.12.1 of the Technical Specification will be updated in its entirety as follows to remove reference to Jumbo frame support.*

1.12.1 INTEL® 82573E/82573V GIGABIT ETHERNET CONTROLLER

The Intel® 82573E/82573V Gigabit Ethernet Controller supports the following features:

- PCI Express link
- 10/100/1000 IEEE 802.3 compliant
- Compliant to IEEE 802.3x flow control support
- TCP, IP, UDP checksum offload
- Transmit TCP segmentation
- Advanced packet filtering
- Full device driver compatibility
- PCI Express Power Management Support



ERRATA

1. *Intel® Precision Cooling Could Fail and Only Run at a Maximum or Minimum PWM for CPU Fan*

PROBLEM: The Hardware Monitoring ASIC (Heceta 6e) used for Intel® Precision Cooling may only support up to 3.6 V on their Pulse Width Modulation (PWM) outputs. The 4-pin fans used with this Intel® Desktop Board could have a pull up voltage as high as 5.25 V, potentially causing failures in the ASIC used in the Intel Precision Cooling implementation.

IMPLICATION: If Intel Precision Cooling fails due to this erratum, the CPU fan could run at either 100% PWM, or at minimum PWM (normally set to 30% PWM for 4-pin CPU fans). A failure at 100% PWM could result in louder system acoustics. A failure at minimum PWM could result in a system running slow due to CPU thermal throttling.

WORKAROUND: None

STATUS: This erratum may be fixed in a future board revision.

2. *Hardware Monitoring and Fan Control Could Fail and Only Run at a Maximum or Minimum PWM for CPU Fan*

PROBLEM: The Hardware Monitoring and Fan Control may only support up to 3.6V on its Pulse Width Modulation (PWM) outputs. The 4-pin fans used with the Intel Desktop board could have a pull up voltage as high as 5.25V, potentially causing failures in the circuit used for fan control on this Intel Desktop Board.

IMPLICATION: If Hardware Monitoring and Fan Control fails due to this erratum, the CPU fan could run at either 100% PWM, or at a minimum PWM (normally set to 30% PWM for four-pin CPU fans). A failure at 100% PWM could result in louder system acoustics. A failure at minimum PWM may result in the reduced heat sink efficiency being insufficient to fully support the processor thermal requirements at some higher work loads. A variety of conditions such as room temperature, heat sink characteristics, application, workload and chassis design will affect the impact of the PWM failure. If the thermal requirements of the processor are not met, the processor will attempt to reduce its own temperature. Depending on the severity of the ASIC failure, this may result in a noticeable performance reduction.

WORKAROUND: None

STATUS: This erratum has been fixed. Refer to the Product Change Notification 105493-01 available at <http://developer.intel.com/design/pcn/MTHRBRD/index.htm>.

3. *Silkscreen Markings for the Front and Rear Fan are Reversed*

PROBLEM: Silkscreen markings for the front and rear fan connectors are reversed. The front fan header is marked VR FAN and should be marked FRONT FAN. The rear fan is marked FRONT FAN and should be marked REAR FAN.

IMPLICATION: Markings for the front and rear fan are reversed in the silkscreen on the board. There is no impact to the functionality of the fan connectors.

WORKAROUND: None

STATUS: This erratum has been fixed in board revisions AA C93516-401 and greater.



4. *Voltage Regulator Controllers May Cause System to Hang/Freeze During the Operating System Boot*

PROBLEM: The voltage controller samples the Voltage ID (VID) lines every 200ns instead of 400ns as designed.

IMPLICATION: When booting the system the Operating System (OS) may hang or freeze.

WORKAROUND: None.

STATUS: This erratum may be fixed in a future hardware revision.



DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *Intel® Desktop Board D955XCS Technical Product Specification* (Order Number D14066). All Documentation Changes will be incorporated into a future version of that specification.

1. ***Change to Section 3.7.2, BIOS Boot Optimizations***

Section 3.7.2, will change in its entirety as follows:

3.7.2 BIOS BOOT OPTIMIZATIONS

Use of the following BIOS Setup program settings reduces the POST execution time:

- In the Boot menu, set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from three to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the Drive Configuration Submenu of the BIOS Setup program).