Intel® Desktop Board D850EMD2/D850EMV2

Technical Product Specification

April 2002

Order Number: A94395-001

The Intel® Desktop Boards D850EMD2/D850EMV2 may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D850EMD2/D850EMV2 Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D850EMD2/D850EMV2 Technical Product Specification.	April 2002

This product specification applies to only standard desktop boards D850EMD2 and D850EMV2 with BIOS identifier MV85010A.86A.

Changes to this specification will be published in the Intel Desktop Board D850EMD2/D850EMV2 Specification Update before being incorporated into a revision of this document.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT.

Intel Corporation may have patents or pending patent applications, trademarks, copyrights, or other intellectual property rights that relate to the presented subject matter. The furnishing of documents and other materials and information does not provide any license, express or implied, by estoppel or otherwise, to any such patents, trademarks, copyrights, or other intellectual property rights.

Intel products are not intended for use in medical, life saving, or life sustaining applications or for any other application in which the failure of the Intel product could create a situation where personal injury or death may occur.

Intel may make changes to specifications, product descriptions, and plans at any time, without notice.

The Intel® Desktop Boards D850EMD2 and D850EMV2 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 5937
Denver, CO 80217-9808

or call in North America 1-800-548-4725, Europe 44-0-1793-431-155, France 44-0-1793-421-777, Germany 44-0-1793-421-333, other Countries 708-296-9333.

Intel and Pentium are registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

† Other names and brands may be claimed as the property of others.

Copyright © 2002, Intel Corporation. All rights reserved.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for these Intel desktop boards: D850EMD2 and D850EMV2. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the desktop boards D850EMD2 and D850EMV2 and their components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the desktop boards D850EMD2 and D850EMV2
2	A map of the resources of the desktop boards
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, POST codes, and diagnostic LEDs

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions, which if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USB#).
(NxnX)	When used in the description of a component, *N* indicates the component type, *xn* are the relative coordinates of its location on the desktop board, and *X* is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
GB	Gigabyte (1,073,741,824 bytes)
GB/sec	Gigabytes per second
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbit/sec	Megabits per second
xxh	An address or data value ending with a lowercase *h* indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
†	This symbol is used to indicate other names and brands may be claimed as the property of others.

Contents

1 Product Description

1.1 Board Differences 11
1.2 Overview 12
1.2.1 Feature Summary 12
1.2.2 Manufacturing Options 13
1.2.3 Board Layouts 14
1.2.4 Block Diagram 16
1.3 Online Support 18
1.4 Operating System Support 18
1.5 Design Specifications 19
1.6 Processor 22
1.7 System Memory 23
1.7.1 Memory Features 23
1.7.2 Continuity RIMM Modules 23
1.7.3 RDRAM Memory Configuration 24
1.8 Intel® 850E Chipset 25
1.8.1 AGP 26
1.8.2 USB 26
1.8.3 IDE Support 28
1.8.4 Real-Time Clock, CMOS SRAM, and Battery 29
1.8.5 4 Mbit FWH 29
1.9 I/O Controller 30
1.9.1 Serial Port 30
1.9.2 Parallel Port 30
1.9.3 Diskette Drive Controller 31
1.9.4 Keyboard and Mouse Interface 31
1.10 Audio Subsystem 32
1.10.1 Audio Connectors 33
1.10.2 Audio Subsystem Software 33
1.11 LAN Subsystem (Optional) 34
1.11.1 Intel® 82562ET PLC Device 34
1.11.2 RJ-45 LAN Connector with Integrated LEDs 34
1.11.3 LAN Subsystem Software 35
1.12 CNR (Optional) 35
1.13 Hardware Management Subsystem 36
1.13.1 Hardware Monitoring ASICs 36
1.13.2 Fan Control and Monitoring 38
1.14 Power Management 39
1.14.1 ACPI 39
1.14.2 Hardware Support 41

2 Technical Reference

2.1 Introduction....47
2.2 Memory Map....47
2.3 Fixed I/O Map....48
2.4 DMA Channels....49
2.5 PCI Configuration Space Map....49
2.6 Interrupts....50
2.7 PCI Interrupt Routing Map....51
2.8 Connectors....53
2.8.1 Back Panel Connectors....54
2.8.2 Internal I/O Connectors....57
2.8.3 External I/O Connectors....70
2.9 Jumper Blocks....74
2.9.1 Front Panel Audio Connector/Jumper Block....74
2.9.2 BIOS Setup Configuration Jumper Block....75
2.10 Mechanical Considerations....76
2.10.1 Desktop Board D850EMD2 Form Factor....76
2.10.2 Desktop Board D850EMV2 Form Factor....77
2.10.3 I/O Shield....78
2.11 Electrical Considerations....79
2.11.1 Power Consumption....79
2.11.2 Add-in Board Considerations....79
2.11.3 Standby Current Requirements....80
2.11.4 Fan Connector Current Capability....81
2.11.5 Power Supply Considerations....81
2.12 Thermal Considerations....82
2.13 Reliability....83
2.14 Environmental....84
2.15 Regulatory Compliance....85
2.15.1 Safety Regulations....85
2.15.2 EMC Regulations....85
2.15.3 Product Certification Markings (Board Level)....86

3 Overview of BIOS Features

3.1 Introduction....87
3.2 BIOS Flash Memory Organization....87
3.3 Resource Configuration....87
3.3.1 PCI Autoconfiguration....87
3.3.2 PCI IDE Support....88
3.4 SMBIOS....88
3.5 Legacy USB Support....89
3.6 BIOS Updates....89
3.6.1 Language Support....90
3.6.2 Custom Splash Screen....90

3.7 Recovering BIOS Data 91
3.8 Boot Options....91
3.8.1 CD-ROM Boot 91
3.8.2 Network Boot....92
3.8.3 Booting Without Attached Devices 92
3.8.4 Changing the Default Boot Device During POST....92
3.9 Fast Booting Systems with Intel® Rapid BIOS Boot....92
3.9.1 Peripheral Selection and Configuration 92
3.9.2 Intel Rapid BIOS Boot 93
3.9.3 Operating System 93
3.10 BIOS Security Features....93

4 BIOS Setup Program

4.1 Introduction....95
4.2 Maintenance Menu 96
4.2.1 Extended Configuration Submenu....97
4.3 Main Menu....98
4.4 Advanced Menu....99
4.4.1 PCI Configuration Submenu....100
4.4.2 Boot Configuration Submenu 101
4.4.3 Peripheral Configuration Submenu....102
4.4.4 IDE Configuration Submenu....104
4.4.5 Diskette Configuration Submenu....107
4.4.6 Event Log Configuration Submenu....108
4.4.7 Video Configuration Submenu....109
4.5 Security Menu 110
4.6 Power Menu 111
4.6.1 APM Submenu 112
4.6.2 ACPI Submenu 112
4.7 Boot Menu 113
4.7.1 Boot Device Priority Submenu....114
4.7.2 Hard Disk Drives Submenu 115
4.7.3 Removable Devices Submenu 115
4.7.4 ATAPI CD-ROM Drives Submenu 116
4.8 Exit Menu 116

5 Error Messages and Beep Codes

5.1 BIOS Error Messages....117
5.2 Port 80h POST Codes....119
5.3 Bus Initialization Checkpoints 123
5.4 Speaker....124
5.5 BIOS Beep Codes 124

Figures

1. Desktop Board D850EMD2 Components 14
2. Desktop Board D850EMV2 Components....15
3. Standard Block Diagram....16
4. Block Diagram with Optional USB 2.0 Support 17
5. Intel 850E Chipset Block Diagram 25
6. USB 1.1 Port Configuration (Optional)....27
7. USB 2.0 Port Configuration (Optional)....28
8. Audio Subsystem Block Diagram....32
9. ICH2 and CNR Signal Interface 35
10. Thermal Monitoring....38
11. Location of the Standby Power Indicator LED 45
12. Back Panel Connectors 54
13. Audio Connectors 58
14. Power and Hardware Control Connectors 60
15. Add-in Board and Peripheral Interface Connectors (Desktop Board D850EMD2)....63
16. Add-in Board and Peripheral Interface Connectors (Desktop Board D850EMV2)....64
17. External I/O Connectors 70
18. Location of the Jumper Blocks....74
19. Desktop Board D850EMD2 Dimensions 76
20. Desktop Board D850EMV2 Dimensions 77
21. I/O Shield Dimensions 78
22. Localized High-Temperature Zones....82

Tables

1. Summary of Board Differences....11
2. Feature Summary....12
3. Manufacturing Options 13
4. Specifications 19
5. Supported Processors 22
6. Supported Memory Configurations 24
7. Memory Support Matrix 24
8. Supported IDE Modes 28
9. LAN Connector LED States 34
10. Effects of Pressing the Power Switch 39
11. Power States and Targeted System Power 40
12. Wake-up Devices and Events....41
13. Fan Connector Descriptions for Boards that use the Hardware Monitoring ASIC 43
14. Fan Connector Descriptions for Boards that use the Hardware Monitoring and Fan Control ASIC 43
15. System Memory Map....47
16. Fixed I/O Map....48
17. DMA Channels 49
18. PCI Configuration Space Map 49
19. Interrupts 50
20. PCI Interrupt Routing Map 52

21. PS/2 Mouse/Keyboard Connectors....55
22. USB Connectors....55
23. Parallel Port Connector....55
24. Serial Port Connectors....56
25. LAN Connector (Optional)....56
26. Audio Line In Connector....56
27. Audio Line Out Connector....56
28. Mic In Connector....56
29. Auxiliary Line In Connector....59
30. ATAPI CD-ROM Connector....59
31. Fan 3 Connector (Desktop Board D850EMV2 Only)....61
32. Chassis Intrusion Connector....61
33. ATX12V Power Connector....61
34. Processor Fan Connector....61
35. Fan 1 Connector....62
36. Main Power Connector....62
37. Fan 2 Connector....62
38. CNR Connector (Optional)....65
39. PCI Bus Connectors....66
40. AGP Connector....67
41. Diskette Drive Connector....68
42. IDE Connectors....69
43. SCSI Hard Drive Activity LED Connector....69
44. Front Panel Audio Connector....71
45. Front Panel USB Connector....71
46. Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector....71
47. Front Panel Connector....72
48. States for a One-Color Power LED....72
49. States for a Two-Color Power LED....73
50. Front Panel Audio Connector/Jumper Block....75
51. BIOS Setup Configuration Jumper Settings....75
52. Power Usage....79
53. Standby Current Requirements....80
54. Thermal Considerations for Components....83
55. Desktop Boards D850EMD2/D850EMV2 Environmental Specifications....84
56. Safety Regulations....85
57. EMC Regulations....85
58. Component Side Markings....86
59. Solder Side Markings....86
60. Boot Device Menu Options....92
61. Supervisor and User Password Functions....94
62. BIOS Setup Program Menu Bar....95
63. BIOS Setup Program Function Keys....96
64. Maintenance Menu....96
65. Extended Configuration Submenu....97
66. Main Menu....98
67. Advanced Menu....99
68. PCI Configuration Submenu....100

69. Boot Configuration Submenu 101
70. Peripheral Configuration Submenu 102
71. IDE Configuration Submenu 104
72. Primary/Secondary IDE Master/Slave Submenus 105
73. Diskette Configuration Submenu 107
74. Event Log Configuration Submenu 108
75. Video Configuration Submenu 109
76. Security Menu 110
77. Power Menu 111
78. APM Submenu 112
79. ACPI Submenu 112
80. Boot Menu 113
81. Boot Device Priority Submenu 114
82. Hard Disk Drives Submenu 115
83. Removable Devices Submenu 115
84. ATAPI CD-ROM Drives Submenu 116
85. Exit Menu 116
86. BIOS Error Messages 117
87. Uncompressed INIT Code Checkpoints 119
88. Boot Block Recovery Code Checkpoints 119
89. Run-Time Code Uncompressed in F000 Shadow RAM 120
90. Bus Initialization Checkpoints 123
91. Upper Nibble High Byte Functions 123
92. Lower Nibble High Byte Functions 124
93. Beep Codes 125

1 Product Description

What This Chapter Contains

1.1 Board Differences 11
1.2 Overview 12
1.3 Online Support 18
1.4 Operating System Support 18
1.5 Design Specifications 19
1.6 Processor 22
1.7 System Memory 23
1.8 Intel® 850E Chipset 25
1.9 I/O Controller 30
1.10 Audio Subsystem 32
1.11 LAN Subsystem (Optional) 34
1.12 CNR (Optional) 35
1.13 Hardware Management Subsystem 36
1.14 Power Management 39

1.1 Board Differences

This TPS describes these Intel® desktop boards: D850EMD2 and D850EMV2. The boards are identical except for the differences listed in Table 1 below.

Table 1. Summary of Board Differences

Desktop Board D850EMD2	• microATX form factor (9.60 inches by 9.60 inches) • Three PCI bus connectors • Three fan connectors
Desktop Board D850EMV2	• ATX form factor (12.00 inches by 9.60 inches) • Five PCI bus connectors • Four fan connectors

NOTE

All illustrations show the desktop board D850EMD2 unless there are significant differences between the two boards. Any significant differences are indicated in each figure.

1.2 Overview

1.2.1 Feature Summary

Table 2 summarizes the desktop boards D850EMD2/D850EMV2's major features.

Table 2. Feature Summary

Form Factor	Desktop Board D850EMD2: microATX (9.60 inches by 9.60 inches) Desktop Board D850EMV2: ATX (12.00 inches by 9.60 inches)
Processor	• Support for an Intel® Pentium® 4 processor in a µPGA478 socket • 400/533 MHz system data bus
Memory	• Two Direct-RDRAM channels with two RIMM†s per channel (four RIMM sockets) • Support for up to 2 GB of system memory
Chipset	Intel® 850E Chipset, consisting of: • Intel® 82850E Memory Controller Hub (MCH) • Intel® 82801BA I/O Controller Hub (ICH2) • 4 Mbit Firmware Hub (FWH)
I/O Control	SMSC LPC47M142 LPC bus I/O controller
Video	AGP connector supporting 1.5 V 4X AGP cards only
Peripheral Interfaces	• Up to seven Universal Serial Bus (USB) ports • Two serial ports • One parallel port • Two IDE interfaces with Ultra DMA 33 and ATA-66/100 support • One diskette drive interface • PS/2† keyboard and mouse ports
Expansion Capabilities	• Desktop Board D850EMD2: Three PCI bus add-in card connectors (SMBus routed to PCI bus connector 2) • Desktop Board D850EMV2: Five PCI bus add-in card connectors (SMBus routed to PCI bus connector 2)
BIOS	• Intel/AMI BIOS (resident in the 4 Mbit FWH) • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and System Management BIOS (SMBIOS)
Instantly Available PC	• Support for *PCI Local Bus Specification Revision 2.2* • Suspend to RAM support • Wake on PCI, CNR, RS-232, front panel, PS/2 keyboard, and USB ports
LAN Wake Capabilities	Support for system wake-up using an add-in network interface card with remote wake-up capability via the PME# signal

continued

Table 2. Feature Summary (continued)

Hardware Management Subsystem	One of the following: • Hardware monitoring ASIC — Voltage sense to detect out-of-range power supply voltages — Thermal sense to detect out-of-range thermal values — Fan monitoring • Hardware monitoring and fan control ASIC — Voltage sense to detect out-of-range power supply voltages — Thermal sense to detect out-of-range thermal values — Fan monitoring and control
Audio (Integrated)	Audio subsystem that uses the Analog Devices AD1885 analog codec for AC '97 processing

For information about	Refer to
The board's compliance level with ACPI, Plug and Play, and SMBIOS.	Section 1.5, page 19

1.2.2 Manufacturing Options

Table 3 describes the manufacturing options. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

Table 3. Manufacturing Options

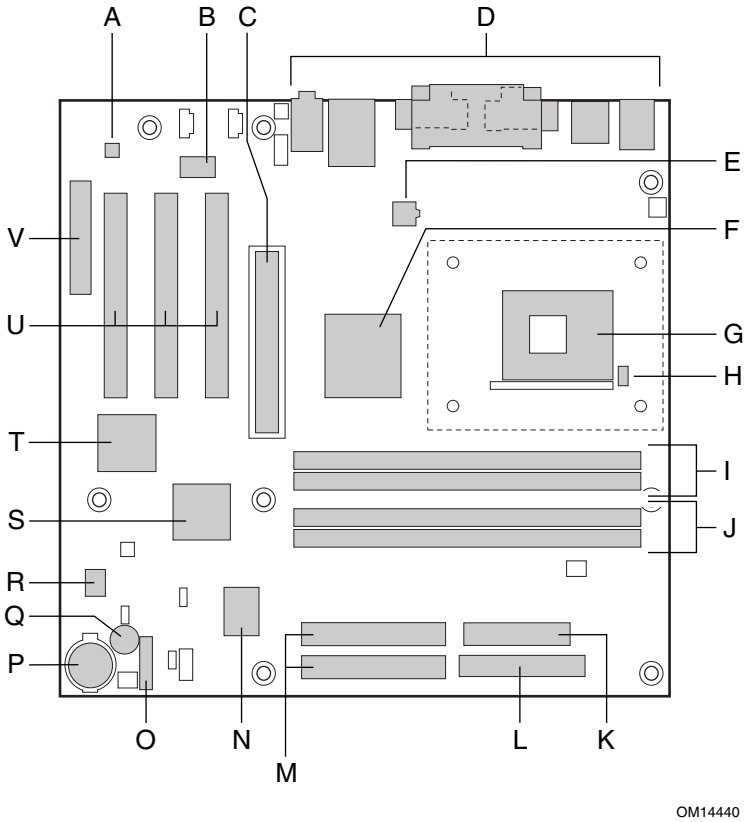
LAN	Intel® 82562ET 10/100 Mbit/sec Platform LAN Connect (PLC) device
CNR	One Communication and Networking Riser (CNR) connector (slot shared with PCI bus connector 3 on the desktop board D850EMD2 and with PCI bus connector 6 on the desktop board D850EMV2)
USB 2.0	Support for USB 2.0 devices. The USB 2.0 option supports up to five USB ports. It uses the following components: • NEC µPD720100 USB 2.0 host controller • SMSC LPC47M132 LPC bus I/O controller The USB 1.1 ports routed through the ICH2 are not available with the USB 2.0 option.

NOTE

The LAN and the CNR manufacturing options are mutually exclusive.

1.2.3 Board Layouts

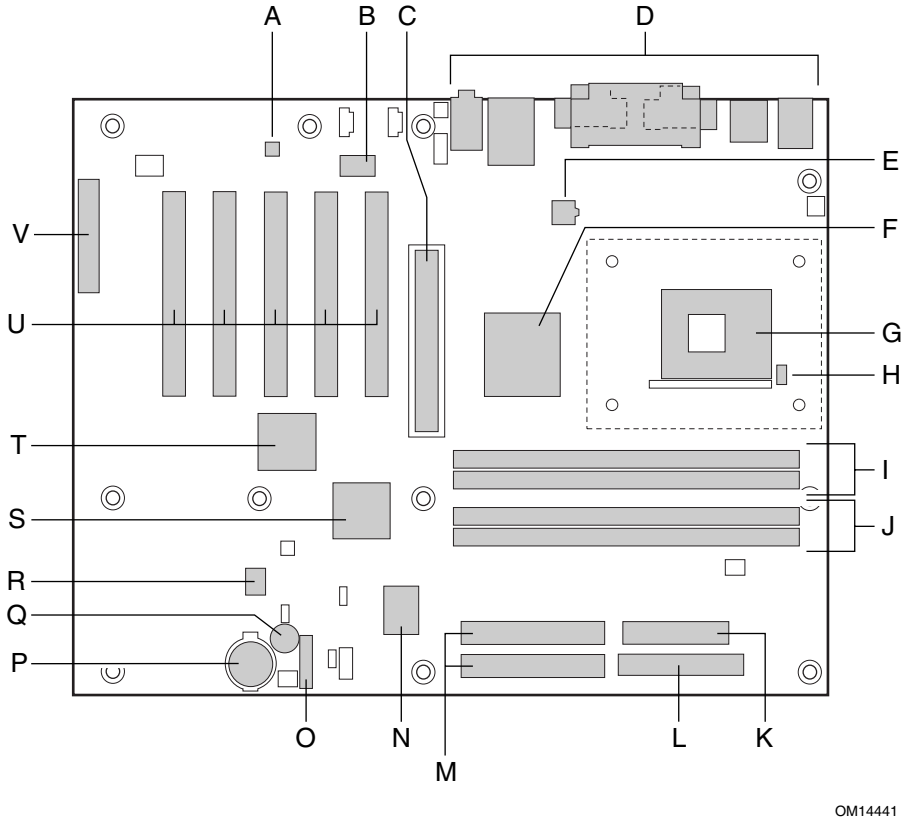
Figure 1 shows the location of the major components on the desktop board D850EMD2.



A	AD1885 audio codec	L	Diskette drive connector
B	Intel 82562ET PLC device (optional)	M	IDE connectors
C	AGP connector	N	LPC bus I/O controller
D	Back panel connectors	O	Front panel connector
E	+12 V power connector (ATX12V)	P	Battery
F	Intel 82850E MCH	Q	Speaker
G	µPGA478 processor socket	R	4 Mbit FWH
H	Hardware monitor	S	Intel 82801BA ICH2
I	RAMBUS† Bank 0 (RIMM1 and RIMM2)	T	NEC µPD720100 USB 2.0 host controller (optional)
J	RAMBUS Bank 1 (RIMM3 and RIMM4)	U	PCI bus add-in card connectors
K	Power connector	V	CNR connector (optional)

Figure 1. Desktop Board D850EMD2 Components

Figure 2 shows the location of the major components on the desktop board D850EMV2.



A	AD1885 audio codec	L	Diskette drive connector
B	Intel 82562ET PLC device (optional)	M	IDE connectors
C	AGP connector	N	LPC bus I/O controller
D	Back panel connectors	O	Front panel connector
E	+12 V power connector (ATX12V)	P	Battery
F	Intel 82850E MCH	Q	Speaker
G	µPGA478 processor socket	R	4 Mbit FWH
H	Hardware monitor	S	Intel 82801BA ICH2
I	RAMBUS Bank 0 (RIMM1 and RIMM2)	T	NEC µPD720100 USB 2.0 host controller (optional)
J	RAMBUS Bank 1 (RIMM3 and RIMM4)	U	PCI bus add-in card connectors
K	Power connector	V	CNR connector (optional)

Figure 2. Desktop Board D850EMV2 Components

1.2.4 Block Diagram

Figure 3 is a block diagram of the major functional areas of the standard desktop boards D850EMD2/D850EMV2. See Figure 6 on page 27 for USB port routing.

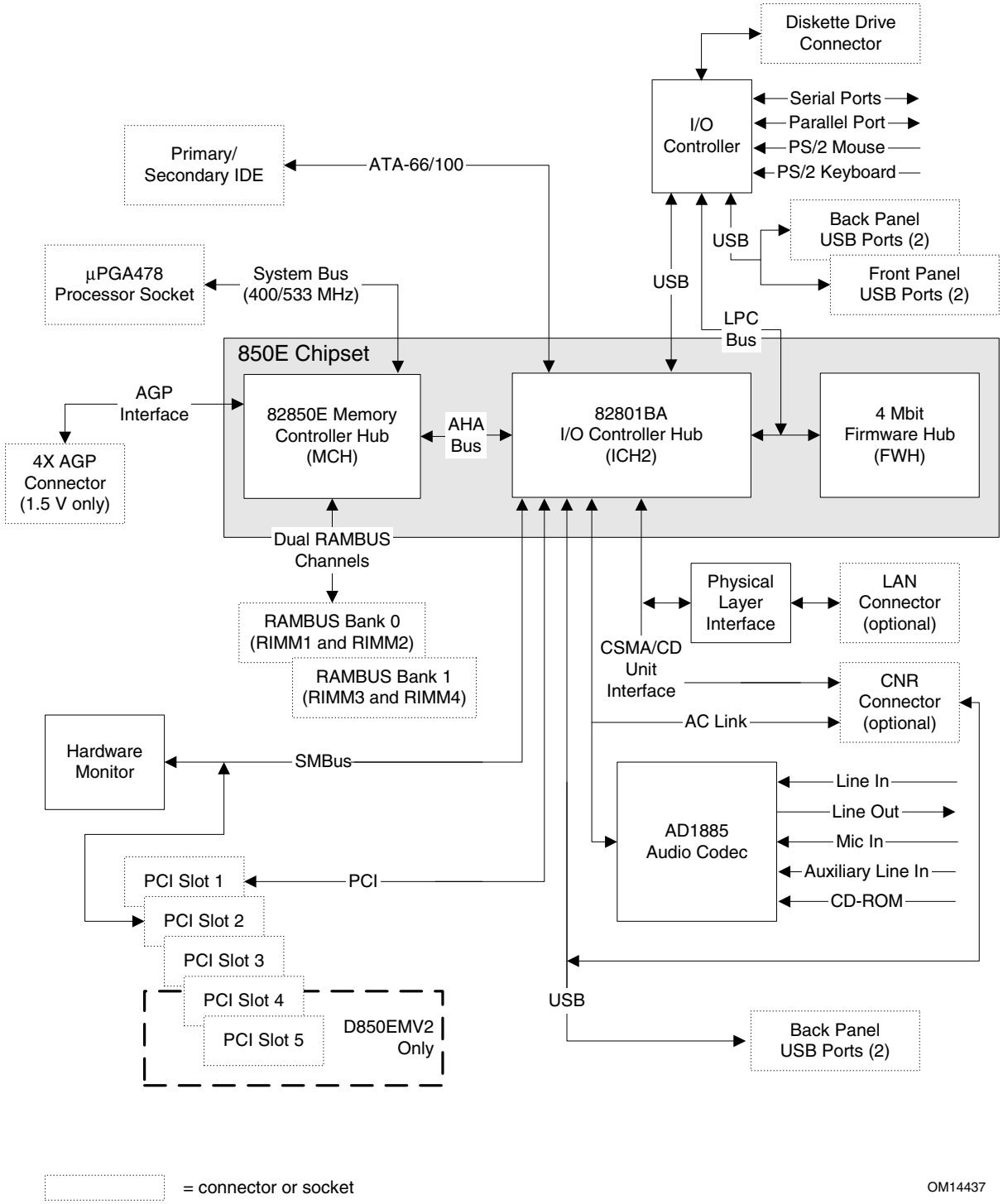


Figure 3. Standard Block Diagram

Figure 4 is a block diagram of the major functional areas of desktop boards D850EMD2 and D850EMV2 with the USB 2.0 manufacturing option. See Figure 7 on page 28 for USB port routing.

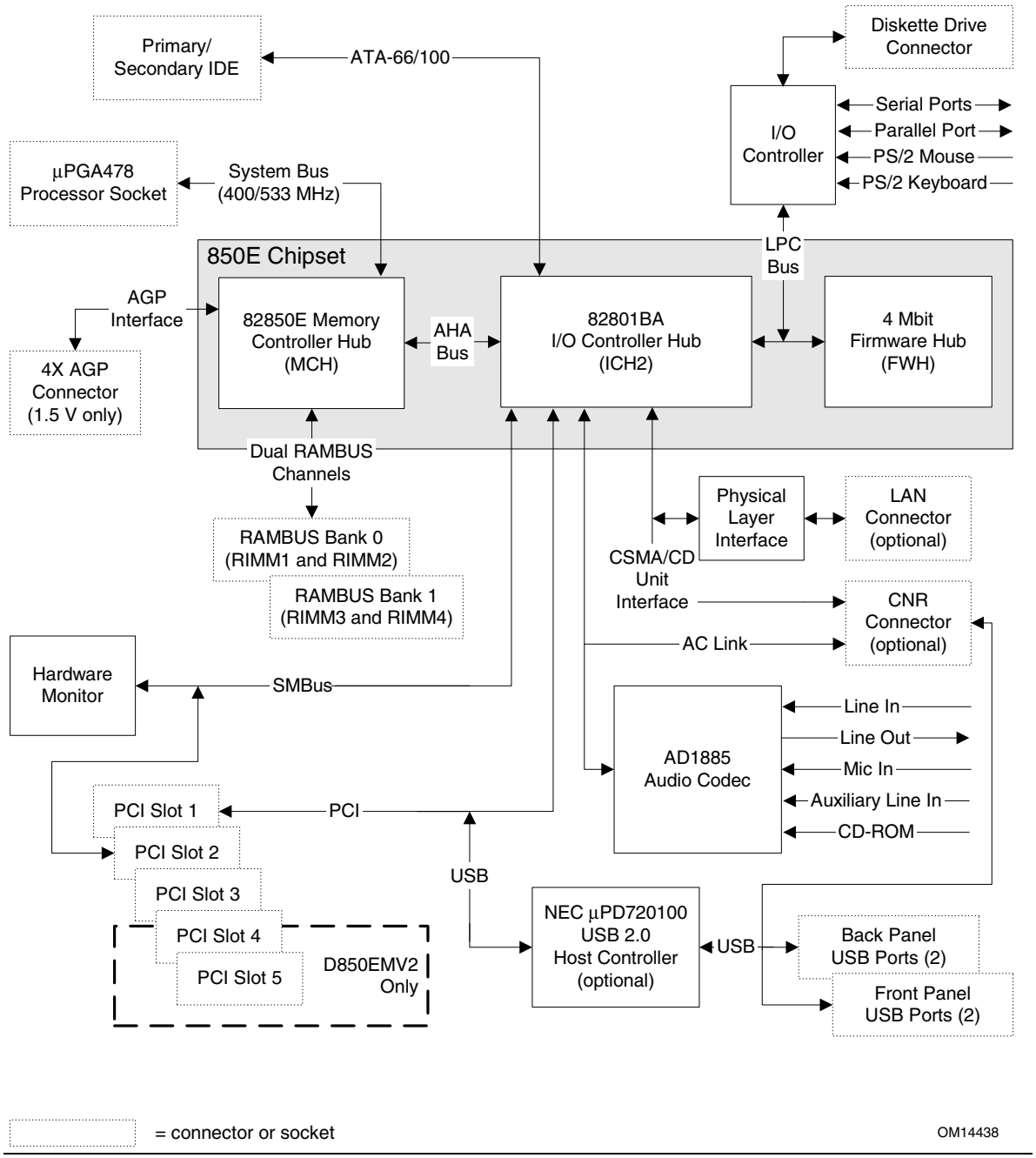


Figure 4. Block Diagram with Optional USB 2.0 Support

1.3 Online Support

To find information about…	Visit this World Wide Web site:
Intel's desktop boards 850EMD2/D850EMV2	http://www.intel.com/design/motherbd http://support.intel.com/support/motherboards/desktop
Processor data sheets	http://www.intel.com/design/litcentr
ICH2 addressing	http://developer.intel.com/design/chipsets/datashts
Custom splash screens	http://intel.com/design/motherbd/gen_indx.htm
Audio software and utilities	http://www.intel.com/design/motherbd
LAN software and drivers	http://www.intel.com/design/motherbd

1.4 Operating System Support

The desktop boards D850EMD2/D850EMV2 support drivers for all of the onboard hardware and subsystems under the following operating systems:

- Windows† 98 SE
- Windows Me
- Windows NT† 4.0
- Windows 2000
- Windows XP

For information about	Refer to
Supported drivers	Section 1.3, page 18

NOTE

Other drivers may be offered by other third-party vendors.

NOTE

USB 2.0 support has been tested with Windows 2000 and Windows XP drivers and is not currently supported by any other operating system.

1.5 Design Specifications

Table 4 lists the specifications applicable to the desktop boards D850EMD2/D850EMV2.

Table 4. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
AC '97	*Audio Codec '97*	Revision 2.2, September 2000, Intel Corporation.	ftp://download.intel.com/ial/scalableplatforms/ac97r22.pdf
ACPI	*Advanced Configuration and Power Interface Specification*	Version 2.0, July 27, 2000, Compaq Computer Corp., Intel Corporation, Microsoft Corporation, and Toshiba Corporation.	http://www.teleport.com/~acpi/
AGP	*Accelerated Graphics Port Interface Specification*	Version 2.0, May 4, 1998, Intel Corporation.	http://www.agpforum.org/
AMI BIOS	*AMIBIOS Desktop Core 8.0*	AMIBIOS 8.0, 2001, American Megatrends, Inc.	http://www.ami.com/support/doc/amibios8.pdf
ATA/ ATAPI-5	*Information Technology - AT Attachment with Packet Interface - 5, (ATA/ATAPI-5)*	Revision 3, February 29, 2000, Contact: T13 Chair, Seagate Technology.	http://www.t13.org
ATX	*ATX Specification*	Version 2.03, December 1998, Intel Corporation.	http://www.formfactors.org/developer/specs/atx/atxspecs.htm
ATX12V	*ATX / ATX12V Power Supply Design Guide*	Version 1.2, August 2000, Intel Corporation.	http://www.formfactors.org/developer/specs/atx/atxspecs.htm
BIS	*Boot Integrity Services (BIS) Application Programming Interface (API)*	Version 1.0, August 4, 1999, Intel Corporation.	http://www.intel.com/labs/manage/wfm/wfmspecs.htm
CNR	*Communication and Network Riser (CNR) Specification*	Revision 1.2, November 8, 2001, Intel Corporation.	http://developer.intel.com/technology/cnr/index.htm
EHCI	*Enhanced Host Controller Interface Specification for Universal Serial Bus*	Revision 1.0, March 12, 2002, Intel Corporation.	http://developer.intel.com/technology/usb/download/ehci-r10.pdf

continued

Table 4. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
EPP	*IEEE std 1284.1-1997* Enhanced Parallel Port	Version 1.7, 1997, Institute of Electrical and Electronic Engineers.	http://standards.ieee.org/reading/ieee/std_public/description/busarch/1284.1-1997_desc.html
El Torito	*Bootable CD-ROM format specification*	Version 1.0, January 25, 1995, Phoenix Technologies Ltd. and IBM Corporation.	http://www.ptltd.com/techs/specs.html
LPC	*Low Pin Count Interface Specification*	Version 1.0, September 29, 1997, Intel Corporation.	http://www.intel.com/design/chipsets/industry/lpc.htm
OHCI	*OpenHCI – Open Host Controller Interface Specification for USB*	Release 1.0a, September 14, 1999, Compaq Computer Corp., Microsoft Corporation, and National Semiconductor Corp.	http://www.usb.org/developers/docs.html
PCI	*PCI Local Bus Specification*	Version 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
	PCI Bus Power Management Interface Specification	Version 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
Plug and Play	*Plug and Play BIOS Specification*	Version 1.0a, May 5, 1994, Compaq Computer Corp., Phoenix Technologies Ltd., and Intel Corporation.	http://www.microsoft.com/hwdev/respec/pnpspecs.htm
PXE	*Preboot Execution Environment*	Version 2.1, September 1999, Intel Corporation.	http://developer.intel.com/ial/wfm/wfmspecs.htm
RIMM	*Rambus Serial Presence Detect (SPD) Specification*	Version 1.0, March 1999, Rambus Corporation.	http://www.rambus.com/developer/support_rimm.html
	Rambus RIMM Specification	Version 1.0, February 1999, Rambus Corporation.	http://www.rambus.com/developer/development_support.html

continued

Table 4. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
SMBIOS	*System Management BIOS*	Version 2.3.1, March 16, 1999, American Megatrends Inc., Award Software International Inc., Compaq Computer Corporation, Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, and SystemSoft Corporation.	http://www.dmtf.org/standards/bios.php
UHCI	*Universal Host Controller Interface Design Guide*	Version 1.1, March 1996, Intel Corporation.	http://www.usb.org/developers/docs.html
USB	*Universal Serial Bus Specification*	Version 1.1, September 23, 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC Corporation.	http://www.usb.org/developers/docs.html
		Version 2.0, April 27, 2000, Compaq Computer Corporation, Hewlett-Packard Company, Lucent Technologies Inc., Intel Corporation, Microsoft Corporation, NEC Corporation, and Koninklijke Philips Electronics N.V.	
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation.	http://www.intel.com/labs/manage/wfm/wfmspecs.htm

1.6 Processor

CAUTION

Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Desktop Board D850EMD2/D850EMV2 Specification Update *for the most up-to-date list of supported processors for these boards.*

The desktop boards D850EMD2/D850EMV2 support a single Pentium 4 processor (in a µPGA478 socket) with a system bus of 400/533 MHz. Table 5 lists the supported processors.

Table 5. Supported Processors

Type	Designation	System Bus	L2 Cache Size
Pentium 4 processor	Up to 2.4 GHz	400 MHz	256 KB
Pentium 4 processor	Up to 2.4A GHz	400 MHz	512 KB
Pentium 4 processor	Up to 2.53 GHz	533 MHz	512 KB

The list of supported processors for the desktop boards D850EMD2/D850EMV2 is available from Intel's World Wide Web site. All supported onboard memory can be cached. See the processor's data sheet for cachability limits.

CAUTION

Use only an ATX12V-compliant power supply with these desktop boards. ATX12V power supplies have two power leads that provide required supplemental power for the Intel Pentium 4 processor and the Intel 850E chipset. Always connect the 20-pin and 4-pin leads of the ATX12V power supply to the corresponding connectors on the board. Otherwise, the board and the processor could be damaged.

Do not use a standard ATX power supply. Doing so could damage the board and the processor.

For information about	Refer to
Processor support	Section 1.3, page 18
Processor usage	Section 1.3, page 18
Power supply connectors	Section 2.8.2.3, page 60

1.7 System Memory

CAUTION

Turn off the power and unplug the power cord before installing or removing RIMM modules. Failure to do so could damage the memory and the board. (After AC power is removed, the standby power indicator LED should not be lit. See Figure 11 on page 45 for the location of the standby power indicator LED.)

NOTE

The desktop boards D850EMD2/D850EMV2 support combinations of no more than 32 RDRAM components per RDRAM bank. If the total number of RDRAM components installed in all RIMM sockets exceeds 64, the computer will not boot.

1.7.1 Memory Features

The 82850E MCH integrates two lock-stepped Direct Rambus banks, providing a processor-to-memory bandwidth up to 3.2 GB/sec. The desktop boards D850EMD2/D850EMV2 have four RIMM sockets (two sockets for each bank) and support the following memory features:

- Single- or double-sided RIMM configurations
- Maximum of 32 Direct Rambus devices per bank
- Memory configurations from 128 MB (minimum) to 2 GB (maximum), using 128 Mbit or 256 Mbit technology PC800-compliant RDRAM
- Serial Presence Detect (SPD)–based configuration for optimal memory operation
- Suspend to RAM support
- ECC and non-ECC support

1.7.2 Continuity RIMM Modules

All RIMM sockets must be populated to achieve continuity for termination at the Rambus interface. Continuity RIMMs (or “pass-through” modules) must be installed in the second RDRAM bank if memory is not installed. If any of the RIMM sockets are not populated, the computer will not complete the Power-On Self-Test (POST) and the BIOS beep codes will not be heard.

1.7.3 RDRAM Memory Configuration

When installing memory, note the following:

- The four RIMM sockets are grouped into two banks:
  - Bank 0 (labeled on the board as RIMM1 and RIMM2)
  - Bank 1 (labeled on the board as RIMM3 and RIMM4)
- Bank 0 must be populated first, ensuring that the RDRAM installed in RIMM1 and RIMM2 is identical in speed, size, and density. For example, the minimum system configuration would use two 64 MB RIMM modules of PC800 RDRAM.
- If the desired memory configuration has been achieved by populating Bank 0, then Bank 1 should be filled with two Continuity RIMMs.
- If memory is to be installed in Bank 1, the RIMM modules installed in RIMM3 and RIMM4 must be identical in size and density to each other and match the speed of the RIMM modules in Bank 0. The RIMM modules do not, however, need to match those in Bank 0 in size and density. For example, if Bank 0 has two 128 MB RIMMs of PC800 RDRAM, Bank 1 would require PC800 RDRAM also; however, any other supported RIMM modules such as 64 MB or 192 MB could be used.
- If ECC functionality is required, all installed RIMM modules must be ECC compliant.

Table 6 gives examples of RDRAM component density for various RIMM modules. Component density (counts) can be identified on the RIMM label.

Table 6. Supported Memory Configurations

Rambus Technology	Capacity with 4 DRAM Components per RIMM	Capacity with 6 DRAM Components per RIMM	Capacity with 8 DRAM Components per RIMM	Capacity with 12 DRAM Components per RIMM	Capacity with 16 DRAM Components per RIMM
128/144 Mbit, -40	64 MB	96 MB	128 MB	192 MB	256 MB
256/288 Mbit, -40	128 MB	192 MB	256 MB	384 MB	512 MB

CAUTION

If the installed processor operates with a 533 MHz system bus, use only PC800-40 memory; do not use PC800-45 memory. Failure to follow this guideline may result in unreliable operation. If the installed processor operates with a 400 MHz system bus, you can use either PC800-40 or PC800-45 memory. Table 7 lists the supported combinations of memory types with processor system bus values.

Table 7. Memory Support Matrix

Processor System Bus	Support for PC800-40 memory?	Support for PC800-45 memory?	Support for PC700 memory?	Support for PC600 memory?
533 MHz	Yes	No	No	No
400 MHz	Yes	Yes	(Note)	Yes

Note: Will default to PC600-level performance.

1.8 Intel® 850E Chipset

The Intel 850E chipset consists of the following devices:

- Intel 82850E MCH with Accelerated Hub Architecture (AHA) bus
- Intel 82801BA ICH2 with AHA bus
- 4 Mbit FWH

The MCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the AHA interface. The ICH2 is a centralized controller for the board's I/O paths. The 4 Mbit FWH provides the nonvolatile storage of the BIOS. The component combination provides the chipset interfaces as shown in Figure 5.

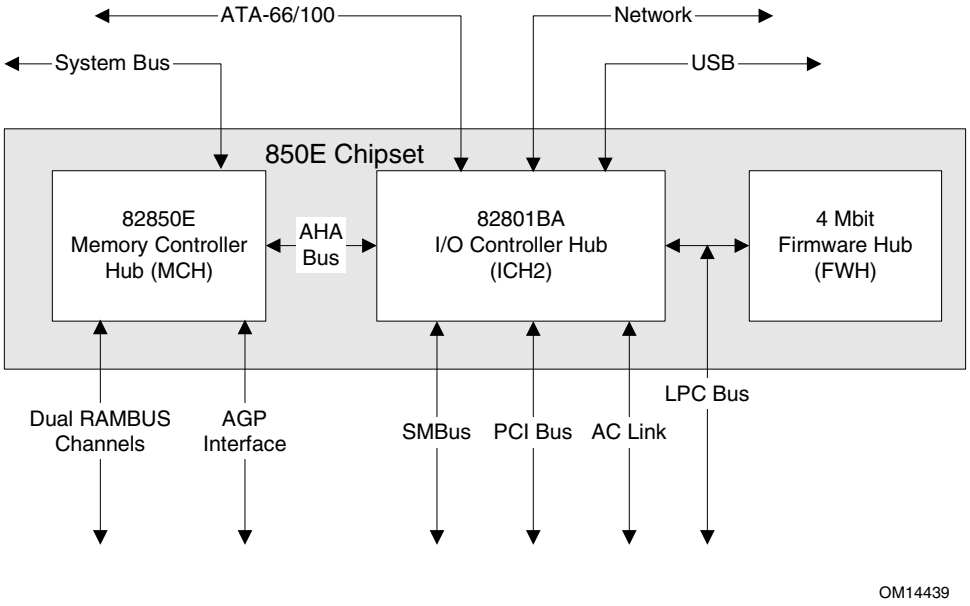


Figure 5. Intel 850E Chipset Block Diagram

NOTE

The USB bus is routed from the NEC USB 2.0 controller if the USB 2.0 option is supported.

For information about	Refer to
The Intel 850E chipset	http://developer.intel.com
Chipset resources	Section 1.3, page 19

1.8.1 AGP

NOTE

The AGP connector is keyed for 1.5 V AGP cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.

The AGP connector supports AGP add-in cards with 1.5 V Switching Voltage Level (SVL). Legacy 3.3 V AGP cards are not supported and will prevent the system from booting if installed.

For information about	Refer to
The location of the AGP connector	Figure 1, page 14
The signal names of the AGP connector	Table 40, page 67

AGP is a high-performance interface for graphics-intensive applications, such as 3-D applications. While based on the *PCI Local Bus Specification, Rev. 2.1,* AGP is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amounts of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent efficiency

For information about	Refer to
The *Accelerated Graphics Port Interface Specification*	Section 1.5, page 19

1.8.2 USB

The following sections describe the USB port configurations.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 12, page 54
The signal names of the back panel USB connectors	Table 22, page 55
The location of the front panel USB connector	Figure 17, page 70
The signal names of the front panel USB connector	Table 45, page 71
The USB specifications, OHCI, EHCI, and UHCI	Section 1.5, page 19

1.8.2.1 USB 1.1 Support

The desktop boards D850EMD2/D850EMV2 support up to seven USB ports, as shown in Figure 6. The ICH2 provides four ports:

- Two ports implemented with stacked back panel connectors, adjacent to the PS/2 connectors
- One port accessible through a CNR add-in card
- One port routed to the SMSC USB hub

The onboard SMSC USB hub provides four ports:

- Two ports implemented with stacked back panel connectors, adjacent to the audio connectors
- Two ports routed to the front panel USB connector

For more than seven USB devices, an external hub can be connected to any of the ports.

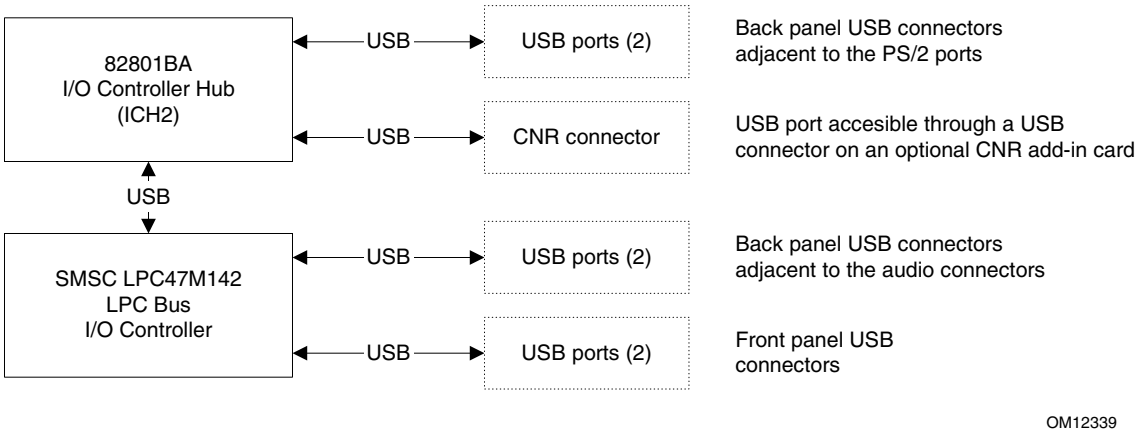


Figure 6. USB 1.1 Port Configuration (Optional)

1.8.2.2 USB 2.0 Support (Optional)

The desktop boards D850EMD2/D850EMV2 support USB 2.0 using the NEC µPD720100 USB 2.0 host controller, which is a manufacturing option. The port routing is implemented as shown in Figure 7. The NEC µPD720100 controller is connected through the PCI bus and provides support for up to five USB ports:

- Two ports implemented with stacked back panel connectors, adjacent to the audio connectors
- Two ports routed to the front panel USB connector
- One port accessible through a CNR add-in card

For more than five USB devices, an external hub can be connected to any of the ports. Boards with the USB 2.0 option fully support OHCI and EHCI and use OHCI- and EHCI-compatible drivers.

NOTE

USB 2.0 support has been tested with Windows 2000 and Windows XP drivers and is not currently supported by any other operating system.

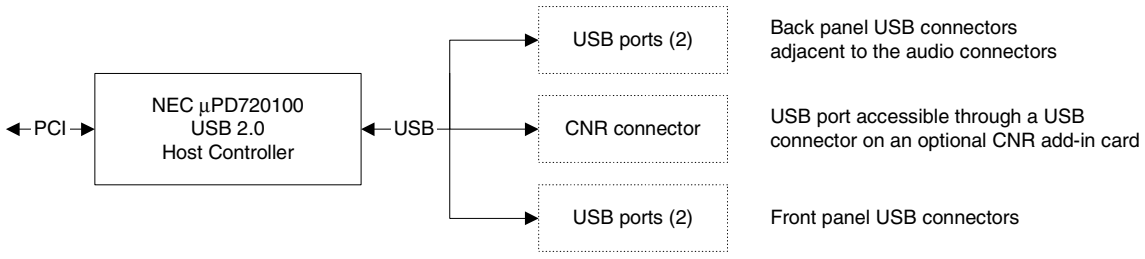


Figure 7. USB 2.0 Port Configuration (Optional)

1.8.3 IDE Support

1.8.3.1 IDE Interfaces

The ICH2's IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the modes listed in Table 8.

Table 8. Supported IDE Modes

Mode	Description	Supported Transfer Rates
Programmed I/O (PIO)	Processor controls data transfer	
8237-style DMA	DMA offloads the processor	Up to 16 MB/sec
Ultra DMA	• DMA protocol on the IDE bus • Supports host and target throttling	Up to 33 MB/sec
ATA-66	• DMA protocol on the IDE bus • Allows host and target throttling • Similar to Ultra DMA • Device driver compatible	Up to 66 MB/sec
ATA-100	• DMA protocol on the IDE bus • Allows host and target throttling	• Read transfer rates up to 100 MB/sec • Write transfer rates up to 88 MB/sec

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes listed in Section 4.4.4.1 on page 105.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The desktop boards D850EMD2/D850EMV2 support Laser Servo (LS-120) diskette technology through the IDE interfaces. The BIOS supports booting from an LS-120 drive.

NOTE

The BIOS will always recognize an LS-120 drive as an ATAPI floppy drive. To ensure correct operation, do not configure the drive as a hard disk drive.

For information about	Refer to
The location of the IDE connectors	Figure 15, page 63
The signal names of the IDE connectors	Table 42, page 69
The Boot menu in the BIOS Setup program	Section 4.7, page 113

1.8.3.2 SCSI Hard Drive Activity LED Connector

The SCSI hard drive activity LED connector is a 1 x 2–pin connector that allows an add-in SCSI controller to use the same LED as the onboard IDE controller. For proper operation, this connector should be wired to the LED output of the add-in SCSI controller. The LED indicates when data is being read from, or written to, both the add-in SCSI controller and the IDE controller.

For information about	Refer to
The location of the SCSI hard drive activity LED connector	Figure 17, page 70
The signal names of the SCSI hard drive activity LED connector	Table 43, page 69

1.8.4 Real-Time Clock, CMOS SRAM, and Battery

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ±13 minutes/year at 25 ºC with 3.3 VSB applied.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

1.8.5 4 Mbit FWH

The FWH provides the following:

- System BIOS program
- System security and manageability logic that enable protection for storing and updating of platform information

1.9 I/O Controller

The SMSC LPC47M142 I/O controller provides the following features:

- 3.3 V operation
- Two serial ports
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.2 MB or 1.44 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support
- Two fan tachometer inputs (not used on desktop boards D850EMD2/D850EMV2 equipped with the hardware monitoring and fan control ASIC)
- USB hub

The BIOS Setup program provides configuration options for the I/O controller.

NOTE

The SMSC LPC47M132 I/O controller is used if the USB 2.0 option is supported. The SMSC LPC47M132 I/O controller supports all the features of the LPC47M142 controller, except the LPC47M132 does not have a USB hub.

For information about	Refer to
SMSC LPC47M142 and LPC47M132 I/O controllers	http://www.smsc.com

1.9.1 Serial Port

The desktop boards D850EMD2/D850EMV2 have two serial port connectors on the back panel. The serial ports support data transfers at speeds up to 115.2 kbits/sec with BIOS support.

For information about	Refer to
The location of the serial port connectors	Figure 12, page 54
The signal names of the serial port connectors	Table 24, page 56

1.9.2 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. Use the BIOS Setup program to set the parallel port mode.

For information about	Refer to
The location of the parallel port connector	Figure 12, page 54
The signal names of the parallel port connector	Table 23, page 55
Setting the parallel port's mode	Section 4.4.3, page 102

1.9.3 Diskette Drive Controller

The I/O controller supports one diskette drive. Use the BIOS Setup program to configure the diskette drive interface.

For information about	Refer to
The location of the diskette drive connector	Section 2.8.2.4, page 63
The signal names of the diskette drive connector	Table 41, page 68
The supported diskette drive capacities and sizes	Table 73, page 107

1.9.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 12, page 54
The signal names of the keyboard and mouse connectors	Table 21, page 55

1.10 Audio Subsystem

The audio subsystem consists of the following devices:

- Intel 82801BA ICH2
- Analog Devices AD1885 analog codec

The audio subsystem includes these features:

- Split digital/analog architecture for improved signal-to-noise (S/N) ratio: ≥ 85 dB
- Power management support for ACPI 1.0 (driver dependant)
- 3-D stereo enhancement

The audio subsystem supports the following audio interfaces:

- ATAPI-style connectors:
  - CD-ROM
  - Auxiliary line in
- Front panel audio connector, including pins for:
  - Line out
  - Mic in
- Back panel audio connectors:
  - Line out
  - Line in
  - Mic in

Figure 8 is a block diagram of the audio subsystem.

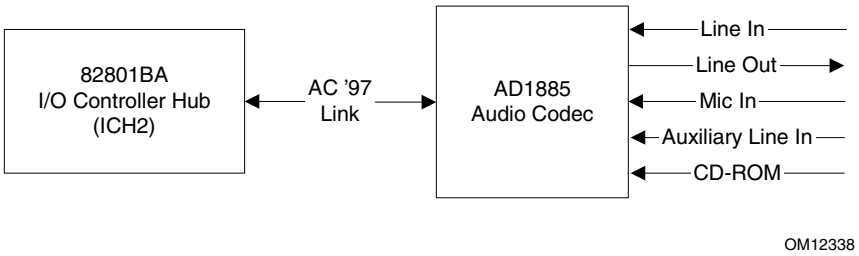


Figure 8. Audio Subsystem Block Diagram

For information about	Refer to
The location and signal names of the back panel audio connectors	Section 2.8.1, page 54

1.10.1 Audio Connectors

1.10.1.1 Front Panel Audio Connector

A 2 x 5-pin connector provides mic in and line out signals for front panel audio connectors.

For information about	Refer to
The location of the connector	Section 2.8.3, page 70
The signal names of the front panel audio connector	Table 44, page 71

NOTE

The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.9.1 on page 74 for more information.

1.10.1.2 Auxiliary Line In Connector

A 1 x 4–pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

For information about	Refer to
The location of the auxiliary line in connector	Figure 13, page 58
The signal names of the auxiliary line in connector	Table 29, page 59

1.10.1.3 ATAPI CD-ROM Audio Connector

A 1 x 4–pin ATAPI-style connector connects an internal ATAPI CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the ATAPI CD-ROM connector	Figure 13, page 58
The signal names of the ATAPI CD-ROM connector	Table 30, page 59

1.10.2 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.3, page 18

1.11 LAN Subsystem (Optional)

The Network Interface Controller subsystem consists of the ICH2 (with integrated LAN Media Access Controller) and a physical layer interface device. The LAN subsystem includes the following features:

- PCI Bus Master interface
- CSMA/CD Protocol Engine
- Serial CSMA/CD unit interface that supports the following physical layer interface devices:
  - 82562ET onboard LAN
  - 82562ET/EM (10/100 Mbit/sec Ethernet) on CNR bus
  - 82562EH (1 Mbit/sec HomePNA†) on CNR bus
- PCI Power Management
  - Supports ACPI technology
  - Supports wake-up from a suspend state using the PME# signal

1.11.1 Intel® 82562ET PLC Device

The Intel 82562ET component provides an interface to the back panel RJ-45 connector with integrated LEDs. This physical interface may alternately be provided through the CNR connector.

The Intel 82562ET provides the following functions:

- Basic 10/100 Ethernet LAN connectivity
- RJ-45 connector support with status indicator LEDs on the back panel
- Full device driver compatibility
- ACPI support
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

1.11.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 9 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 9. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbit/sec data rate is selected.
	On	100 Mbit/sec data rate is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

1.11.3 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.3, page 18

1.12 CNR (Optional)

The CNR connector provides an interface that supports the audio, modem, USB, and LAN interfaces of the Intel 850E chipset. Figure 9 shows the signal interface between the riser and the ICH2.

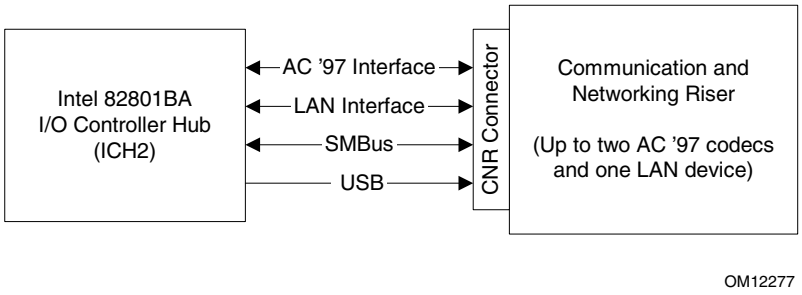


Figure 9. ICH2 and CNR Signal Interface

NOTE

The USB bus is routed from the NEC USB 2.0 controller if the USB 2.0 option is supported.

The CNR supports the following interfaces:

- AC '97 interface: supports audio and/or modem functions on the CNR board. The desktop boards D850EMD2/D850EMV2 support six-channel audio using a CNR board.
- LAN interface: eight-pin interface for use with PLC-based devices.
- SMBus interface: provides Plug and Play functionality for the CNR board.
- USB interface: provides a USB interface for the CNR board.

The CNR connector includes power signals required for power management and for CNR board operation. To learn more about the CNR, refer to the CNR specification.

NOTE

If you install a CNR card with an audio codec that cannot support a multichannel audio upgrade, the desktop boards D850EMD2/D850EMV2's integrated audio codec will be disabled. This only applies to desktop boards D850EMD2/D850EMV2 that have both the onboard audio subsystem and a CNR.

For information about	Refer to
CNR audio upgrade cards	http://developer.intel.com/technology/cnr/

1.13 Hardware Management Subsystem

The hardware management features enable the boards to be compatible with the Wired for Management (WfM) specification. The desktop boards D850EMD2/D850EMV2 have several hardware management features, including the following:

- Fan control and monitoring
- Thermal and voltage monitoring

For information about	Refer to
The WfM specification	Section 1.5, page 19

1.13.1 Hardware Monitoring ASICs

The desktop boards D850EMD2/D850EMV2 provide one of the following:

- A hardware monitoring ASIC
- A hardware monitoring and fan control ASIC

The features of these components are described in this section. Contact your Intel sales representative to determine which type of hardware monitoring ASIC is present on your Intel desktop board.

1.13.1.1 Hardware Monitoring ASIC

The features of the hardware monitoring ASIC (Analog Devices ADM1025, Philips Semiconductor NE1619, or equivalent) include:

- Internal ambient temperature sensor
- Remote thermal diode sensor for direct monitoring of processor temperature
- Power supply monitoring of four voltages (+5 V, +3.3 V, +1.5 V, and +VCCP1) to detect levels above or below acceptable values
- SMBus interface

For information about	Refer to
The location of the fan connectors and sensors for thermal monitoring	Figure 10, page 38
The Analog Devices ADM1025	http://www.analogdevices.com
The Philips Semiconductor NE1619	http://www.philipssemiconductor.com

1.13.1.2 Hardware Monitoring and Fan Control ASIC

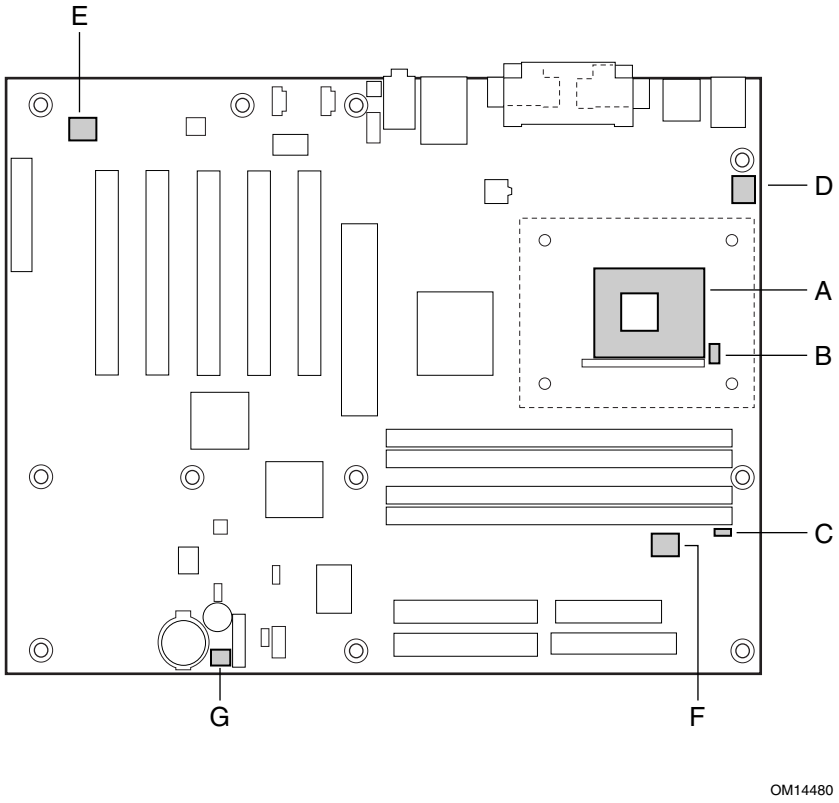
The features of the hardware monitoring and fan control ASIC (Analog Devices ADM1027, National Semiconductor LM85, Standard Microsystems SMSC EMC6D101, or equivalent) include:

- Internal ambient temperature sensor
- Two remote thermal diode sensors for direct monitoring of processor temperature and ambient temperature sensing
- Power supply monitoring of five voltages (+5 V, +12 V, +3.3 V, +1.5 V, and +VCCP1) to detect levels above or below acceptable values
- Fan monitoring for all fans (three fans on the Desktop Board D850EMD2; four fans on the Desktop Board D50EMV2)
- Thermally monitored closed-loop fan control, for all three fans, that can adjust the fan speed or switch the fans on or off as needed
- SMBus interface

For information about	Refer to
The location of the fan connectors and sensors for thermal monitoring	Figure 10, page 38
The Analog Devices ADM1027	http://www.analogdevices.com
The National Semiconductor LM85	http://www.national.com
The Standard Microsystems SMSC EMC6D101	http://www.smsc.com

1.13.1.3 Thermal Monitoring

Figure 10 shows the location of the sensors and fan connectors.



Item	Description
A	Thermal diode, located on processor die
B	Ambient temperature sensor, internal to both hardware monitoring ASIC options
C	Remote ambient temperature sensor (Note)
D	Processor fan
E	Rear chassis fan (Fan 3; present on the Desktop Board D850EMV2 only)
F	Front chassis fan (Fan 1)
G	Front chassis fan (Fan 2)

Note: This sensor is present only on Desktop Boards with the hardware monitoring and fan control ASIC.

Figure 10. Thermal Monitoring

1.13.2 Fan Control and Monitoring

The I/O controller provides two fan tachometer inputs. Monitoring and control can be implemented using third-party software.

For information about	Refer to
The functions of the fan connectors	Section 1.14.2.2, page 42
The location of the fan connectors	Figure 14, page 60
The signal names of the fan connectors	Section 2.8.2.3, page 60

1.14 Power Management

Power management is implemented at several levels, including:

- Software support using ACPI
- Hardware support:
  - Power connector
  - Fan connectors
  - LAN wake capabilities
  - Instantly Available technology
  - Wake from USB
  - Wake from PS/2 keyboard
  - PME# wake-up support

1.14.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the desktop boards D850EMD2/D850EMV2 requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration).
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives.
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state.
- A soft-off feature that enables the operating system to power off the computer.
- Support for multiple wake-up events (see Table 12 on page 41).
- Support for a front panel power and sleep mode switch. Table 10 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 10. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI S5 – soft-off)	Less than four seconds	Power-on (ACPI S0 – working state)
On (ACPI S0 – working state)	Less than four seconds	Soft-off/Standby (ACPI S1 – sleeping state)
On (ACPI S0 – working state)	More than four seconds	Fail-safe power-off (ACPI S5 – soft-off)
Sleep (ACPI S1 – sleeping state)	Less than four seconds	Wake-up (ACPI S0 – working state)
Sleep (ACPI S1 – sleeping state)	More than four seconds	Power-off (ACPI S5 – soft-off)

For information about	Refer to
The desktop boards D850EMD2/D850EMV2's compliance level with ACPI	Section 1.5, page 19

1.14.1.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 11 lists the power states supported by the desktop boards D850EMD2/D850EMV2 along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 11. Power States and Targeted System Power

Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
S0 – working	C0 – working	D0 – working state	Full power > 30 W
S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific	5 W < power < 52.5 W
S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic	Power < 5 W (Note 2)
S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic	Power < 5 W (Note 2)
S5 – Soft-off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic	Power < 5 W (Note 2)
No power to the system	No power	D3 – no power for wake-up logic, except when provided by battery or external source	No power to the system so that service can be performed

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.14.1.1.2 Wake-up Devices and Events

Table 12 lists the devices or specific events that can wake the computer from specific states.

Table 12. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S3, S4, S5
RTC alarm	S1, S3, S4, S5
LAN	S1, S3, S4, S5 (Note)
CNR	S1, S3, S4, S5 (Note)
PME#	S1, S3, S4, S5 (Note)
Modem (back panel serial port A)	S1, S3
USB	S1, S3
PS/2 keyboard	S1, S3

Note: For LAN, CNR, and PME#, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.14.1.1.3 Plug and Play

In addition to power management, ACPI provides control information so that operating systems can facilitate Plug and Play. ACPI is used only to configure devices that do not use other hardware configuration standards. PCI devices, for example, are not configured by ACPI.

1.14.2 Hardware Support

CAUTION

Ensure that the power supply provides adequate +5 V standby current if the LAN wake capabilities and Instantly Available technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 80 for additional information.

The desktop boards D850EMD2/D850EMV2 provide several power management hardware features, including:

- Power connector
- Fan connectors
- LAN wake capabilities
- Instantly Available technology
- Wake from USB
- Wake from PS/2 keyboard
- PME# wake-up support

LAN wake capabilities and Instantly Available technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

NOTE

The use of Wake from USB devices from an ACPI state requires an operating system that provides full ACPI support.

1.14.2.1 Power Connector

When used with an ATX12V-compliant power supply that supports remote power-on/off, the desktop boards D850EMD2/D850EMV2 can turn off the system power through software control. When the system BIOS receives the correct command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, the computer returns to either an on or off state, based on the BIOS configuration, when power resumes. The computer's response can be set using the After Power Failure feature in the BIOS Setup program's Power menu.

For information about	Refer to
The location of the power connector	Figure 14, page 60
The signal names of the power connector	Table 36, page 62
The Power menu in the BIOS Setup program	Section 4.6, page 113
The ATX specification	Section 1.5, page 19

1.14.2.2 Fan Connectors

The desktop boards D850EMD2/D850EMV2 have two fan connectors with thermal control signals (fan 1 and fan 2) that are used to switch the fans on and off as determined by the thermal sensors.

The ambient temperature of a desktop board D850EMD2/D850EMV2-based system is thermally monitored by separate temperature sensors that control voltage to the fan 1 and fan 2 connectors. If the fans attached to these connectors provide a tachometer signal, the sensor reports the fan speed to the hardware monitor component.

Table 13 summarizes the functions of the fan connectors for desktop boards D850EMD2/D850EMV2 that use the Hardware Monitoring ASIC.

Table 13. Fan Connector Descriptions for Boards that use the Hardware Monitoring ASIC

Feature	Processor Fan	Fan 1	Fan 2	Fan 3 (Note)
+12 V DC connection	Yes	Yes	Yes	Yes
Tachometer output	Yes	No	Yes	No
Controllable	No	No	No	No
Fan is on in the ACPI S0 or S1 states	Yes	Yes	Yes	Yes
Fan is off in the ACPI S3, S4, and S5 states	Yes	Yes	Yes	Yes

Note: This fan is present on the desktop board 850EMV2 only.

Table 14 summarizes the functions of the fan connectors for desktop boards D850EMD2/D850EMV2 that use the Hardware Monitoring and Fan Control ASIC.

Table 14. Fan Connector Descriptions for Boards that use the Hardware Monitoring and Fan Control ASIC

Feature	Processor Fan	Fan 1	Fan 2	Fan 3 (Note 1)
+12 V DC connection	Yes	Yes	Yes	Yes
Tachometer output	Yes	Yes	Yes	Yes
Controllable	Yes	Yes	Yes	Yes (Note 2)
Fan is on in the ACPI S0 or S1 states	Yes	Yes	Yes	Yes
Fan is off in the ACPI S3, S4, and S5 states	Yes	Yes	Yes	Yes

Notes: 1. This fan is present on the desktop board D850EMV2 only.

2. Fan 3 uses the same controls as fan 2. If fan 2 is switched off, fan 3 is also off.

For information about	Refer to
The location of the fan connectors	Figure 14, page 60
The signal names of the fan connectors	Section 2.8.2.3, page 58

1.14.2.3 LAN Wake Capabilities

CAUTION

For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply. Refer to Section 2.11.3 on page 80 for additional information.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the MII. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the desktop boards D850EMD2/D850EMV2 support LAN wake capabilities in the following ways, which are with ACPI only:

- Through the PCI bus PME# signal for PCI 2.2–compliant LAN designs
- Through the onboard LAN subsystem
- Through a CNR-based LAN subsystem

1.14.2.4 Instantly Available Technology

CAUTION

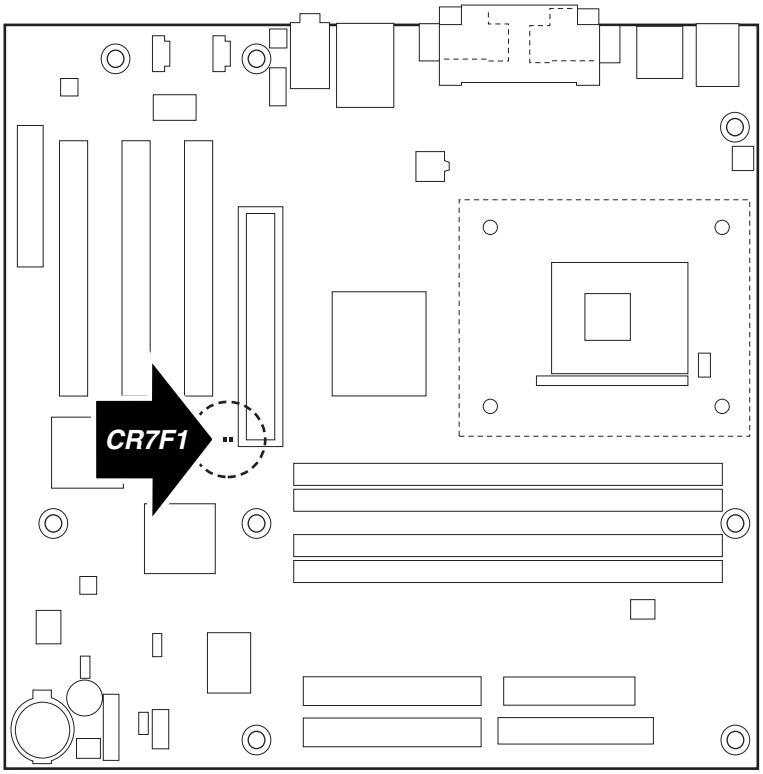
For Instantly Available technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available technology can damage the power supply. Refer to Section 2.11.3 on page 80 for additional information.

Instantly Available technology enables the desktop boards D850EMD2/D850EMV2 to enter the ACPI S3 (Suspend to RAM) sleep state. While in the S3 sleep state, the computer will appear to be off; the power supply fan is off, and the front panel LED is amber if dual colored or off if single colored. When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 12 on page 41 lists the devices and events that can wake the computer from the S3 state.

The desktop boards D850EMD2/D850EMV2 support the *PCI Bus Power Management Interface Specification*. For information on the versions of this specification, see Section 1.5. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available technology requires operating system support and PCI 2.2–compliant add-in cards and drivers.

The standby power indicator LED shows that power is still present at the RIMM, PCI bus, AGP, and CNR connectors, even when the computer appears to be off. Figure 11 shows the location of the standby power indicator LED.



OM14442

Figure 11. Location of the Standby Power Indicator LED

1.14.2.5 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.14.2.6 Wake from PS/2 Keyboard

PS/2 keyboard activity wakes the computer from an ACPI S1 or S3 state.

1.14.2.7 PME# Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with BIOS support).

2 Technical Reference

What This Chapter Contains

2.1 Introduction....47
2.2 Memory Map....47
2.3 Fixed I/O Map....48
2.4 DMA Channels....49
2.5 PCI Configuration Space Map....49
2.6 Interrupts....50
2.7 PCI Interrupt Routing Map....51
2.8 Connectors....53
2.9 Jumper Blocks....74
2.10 Mechanical Considerations....76
2.11 Electrical Considerations....79
2.12 Thermal Considerations....82
2.13 Reliability....83
2.14 Environmental....84
2.15 Regulatory Compliance....85

2.1 Introduction

Sections 2.2–2.6 contain several stand-alone tables. Table 15 describes the system memory map, Table 16 shows the I/O map, Table 17 lists the DMA channels, Table 18 defines the PCI configuration space map, and Table 19 describes the interrupts.

2.2 Memory Map

Table 15. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 2097152 K	100000 - 7FFFFFFF	2047 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Run-time BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to the PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 Fixed I/O Map

Table 16. Fixed I/O Map

Address (hex)	Size	Description
0000 - 00FF	256 bytes	Used by the desktop boards D850EMD2/D850EMV2. Refer to the ICH2 data sheet for dynamic addressing information.
One of these ranges: 0220 - 022F 0240 - 024F	16 bytes	Audio
0228 - 022F (Note 1)	8 bytes	LPT3
0278 - 027F (Note 1)	8 bytes	LPT2
02E8 - 02EF (Note 1)	8 bytes	COM4 / video (8514A)
02F8 - 02FF (Note 1)	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT1
03B0 - 03BB	12 bytes	Intel 82850E MCH
03C0 - 03DF	32 bytes	Intel 82850E MCH
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge / level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB (Note 2)	4 bytes	PCI configuration address register
0CF9 (Note 3)	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH2 address aliassing.

For information about	Refer to
ICH2 addressing	Section 1.3, page 18

2.4 DMA Channels

Table 17. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16 bits	Parallel port (for ECP or EPP)
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.5 PCI Configuration Space Map

Table 18. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82850E component
00	01	00	PCI to AGP bridge
00	1E	00	Hub link to PCI bridge
00	1F	00	Intel 82801BA ICH2 PCI to LPC bridge
00	1F	01	IDE controller
00	1F	02	USB
00	1F	03	SMBus controller
00	1F	04	USB
00	1F	05	AC ’97 audio controller (optional)
00	1F	06	AC ’97 modem controller (optional)
01	00	00	Add-in AGP adapter card
02	00	01	OHCI controller 1 (Note 1)
02	00	02	OHCI controller 2 (Note 1)
02	00	03	EHCI controller (Note 1)
02	08	00	LAN controller (optional)
02	09	00	PCI bus connector 1
02	0A	00	PCI bus connector 2
02	0B	00	PCI bus connector 3
02	0C	00	PCI bus connector 4 (Note 2)
02	0D	00	PCI bus connector 5 (Note 2)

Notes:

1. USB 2.0 option only
2. Desktop Board D850EMV2 only

2.6 Interrupts

The interrupts can be routed through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the ICH4 component. The PIC is supported in Windows 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and supports a total of 24 interrupts.

Table 19. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option)/User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for ICH2 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)
16 (Note 2)	AGP video (through PIRQA)
17 (Note 2)	AC ’97 audio/user available (through PIRQB)
18 (Note 2)	User available (through PIRQC)
19 (Note 2)	ICH2 USB controller #1 (through PIRQD)
20 (Note 2)	ICH2 LAN (optional) (through PIRQE)
21 (Note 2)	OHCI controller #2/user available (through PIRQF)
22 (Note 2)	EHCI controller #1/user available (through PIRQG)
23 (Note 2)	ICH2 USB controller #2/user available (through PIRQH)

Notes:

1. Default, but can be changed to another IRQ.
2. Available in APIC mode only.

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by sharing interrupts does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the desktop boards D850EMD2/D850EMV2 and therefore share the same interrupt. Table 20 shows an example of how the PIRQ signals are routed.

For example, using Table 20 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 4. In PCI bus connector 4, INTA is connected to PIRQB, which is already connected to the SMBus. The add-in card in PCI bus connector 4 now shares interrupts with these onboard interrupt sources.

Table 20. PCI Interrupt Routing Map

PCI Interrupt Source	ICH2 PIRQ Signal Name				
	PIRQF	PIRQG	PIRQH	PIRQB	Other
AGP connector				INTB	INTA to PIRQA
ICH2 USB controller #1					INTD to PIRQD
SMBus controller				INTB	
ICH2 USB controller #2			INTC		
ICH2 Audio / Modem				INTB	
ICH2 LAN					INTA to PIRQE
OHCI controller 1 (Note 1)					INTD to PIRQA
OHCI controller 2 (Note 1)					INTC to PIRQB
EHCI controller (Note 1)					INTH to PIRQC
PCI Bus Connector 1	INTA	INTB	INTC	INTD	
PCI Bus Connector 2	INTD	INTA	INTB	INTC	
PCI Bus Connector 3	INTC	INTD	INTA	INTB	
PCI Bus Connector 4 (Note 2)	INTB	INTC	INTD	INTA	
PCI Bus Connector 5 (Note 2)	INTA	INTB	INTC	INTD	

Notes:

1. USB 2.0 option only
2. Desktop Board D850EMV2 only

NOTE

In PIC mode, the ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. Refer to Table 19 for the allocation of PIRQ lines to IRQ signals in APIC mode.

2.8 Connectors

CAUTION

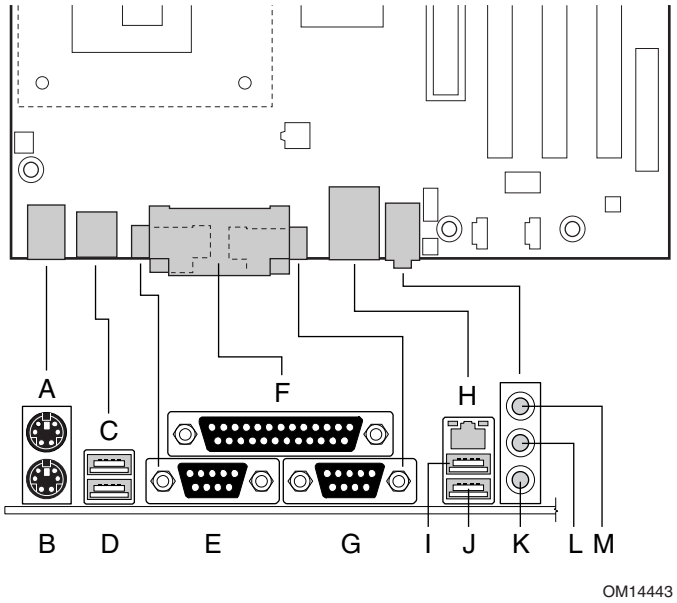
Only the back panel connectors and the front panel USB connector of the desktop boards D850EMD2/D850EMV2 have overcurrent protection. All of the remaining internal connectors on the desktop boards D850EMD2/D850EMV2 are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

This section describes the connectors. The connectors can be divided into the following groups:

- Back panel I/O connectors (see page 54)
  - PS/2 keyboard and mouse
  - USB (four with USB 1.1 option, two with USB 2.0)
  - Parallel port
  - Serial ports (two)
  - LAN (optional)
  - Audio (Line out, Line in, and Mic in)
- Internal I/O connectors (see page 57)
  - Audio (auxiliary line input and ATAPI CD-ROM)
  - Fans (three on the desktop board D850EMD2; four on the desktop board D850EMV2)
  - Power (three: two standard, one optional)
  - Add-in boards (CNR, PCI, and AGP)
  - IDE (two)
  - Diskette drive
  - SCSI hard drive activity LED
- External I/O connectors (see page 70)
  - Front panel audio
  - Front panel USB
  - Auxiliary front panel power/sleep/message-waiting LED
  - Front panel (power/sleep/message-waiting LED, power switch, hard drive activity LED, reset switch, and auxiliary front panel power LED)

2.8.1 Back Panel Connectors

Figure 12 shows the location of the back panel connectors. The back panel connectors are color coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.



Item	Description	Color	For more information see:
A	PS/2 mouse port	Green	Table 21, page 55
B	PS/2 keyboard port	Purple	Table 21, page 55
C	USB port (optional)	Black	Table 22, page 55
D	USB port (optional)	Black	Table 22, page 55
E	Serial port A	Teal	Table 24, page 56
F	Parallel port	Burgundy	Table 23, page 55
G	Serial port B	Teal	Table 24, page 56
H	LAN (optional)	Black	Table 25, page 56
I	USB port	Black	Table 22, page 55
J	USB port	Black	Table 22, page 55
K	Mic in	Pink	Table 28, page 56
L	Audio line out	Lime green	Table 27, page 56
M	Audio line in	Light blue	Table 26, page 56

Figure 12. Back Panel Connectors

NOTE

The USB ports adjacent to the PS/2 ports are not populated if the USB 2.0 option is supported.

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (nonamplified) speakers are connected to this output.

Table 21. PS/2 Mouse/Keyboard Connectors

Pin	Signal Name
1	Data
2	Not connected
3	Ground
4	+5 V
5	Clock
6	Not connected

Table 22. USB Connectors

Pin	Signal Name
1	+5 V
2	USB#
3	USB
4	Ground

Table 23. Parallel Port Connector

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	PD0	PD0	PD0
3	PD1	PD1	PD1
4	PD2	PD2	PD2
5	PD3	PD3	PD3
6	PD4	PD4	PD4
7	PD5	PD5	PD5
8	PD6	PD6	PD6
9	PD7	PD7	PD7
10	ACK#	ACK#	INTR
11	BUSY	BUSY#, PERIPHACK	WAIT#
12	PERROR	PE, ACKREVERSE#	PE
13	SELECT	SELECT	SELECT
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#
16	INIT#	INIT#, REVERSERQST#	RESET#
17	SLCTIN#	SLCTIN#	ADDRSTB#
18 - 25	Ground	Ground	Ground

Table 24. Serial Port Connectors

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	RXD# (Receive Data)
3	TXD# (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Table 25. LAN Connector (Optional)

Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	Ground
5	Ground
6	RX-
7	Ground
8	Ground

Table 26. Audio Line In Connector

Pin	Signal Name
Tip	Audio left in
Ring	Audio right in
Sleeve	Ground

Table 27. Audio Line Out Connector

Pin	Signal Name
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

Table 28. Mic In Connector

Pin	Signal Name
Tip	Mono in
Ring	Mic bias voltage
Sleeve	Ground

2.8.2 Internal I/O Connectors

The internal I/O connectors are divided into the following functional groups:

- Audio (see page 58)
  - Auxiliary line in
  - ATAPI CD-ROM
- Power and hardware control (see page 60)
  - Fans (three on the desktop board D850EMD2; four on the desktop board D850EMV2)
  - ATX12V
  - Main power
  - Auxiliary power (optional)
- Add-in boards and peripheral interfaces (see page 63)
  - CNR (optional)
  - PCI bus (three on the desktop board D850EMD2; five on the desktop board D850EMV2)
  - AGP
  - IDE (two)
  - Diskette drive
  - SCSI hard drive activity LED

2.8.2.1 Expansion Slots

The board has the following expansion slots:

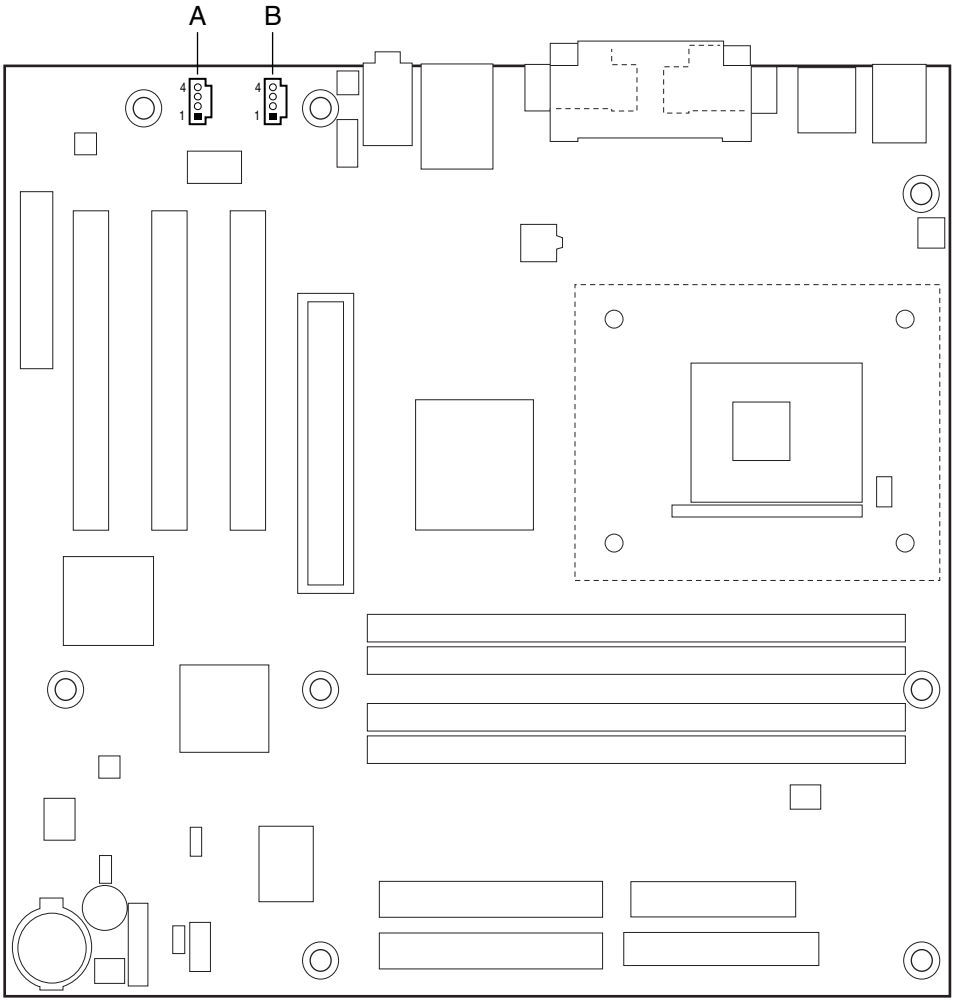
- One AGP connector. The AGP connector is keyed for 1.5 V AGP cards only. Do not install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.
- PCI 2.2–compliant local bus slots (three on the desktop board D850EMD2; five on the desktop board D850EMV2). The SMBus is routed to PCI bus connector 2 only (ATX expansion slot 4). PCI add-in cards with SMBus support can access sensor data and other information residing on the board.
- One CNR connector (optional), shared with PCI bus connector 3 (ATX expansion slot 1) on the desktop board D850EMD2 or with PCI bus connector 6 (ATX expansion slot 1) on the desktop board D850EMV2.

NOTE

This document references back panel slot numbering with respect to processor location on the board. The AGP slot is not numbered. PCI slots are identified as PCI slot #x, starting with the slot closest to the processor. The CNR slot shares PCI slot 6. The ATX/microATX specifications identify expansion slot locations with respect to the far edge of a full-sized ATX chassis. The ATX specification and the board's silkscreen are opposite and could cause confusion. The ATX numbering convention is made without respect to slot type (PCI vs. AGP) but refers to an actual slot location on a chassis. Figure 15 on page 63 illustrates the desktop board D850EMD2's PCI slot numbering. Figure 16 on page 64 illustrates the desktop board D850EMV2's PCI slot numbering.

2.8.2.2 Audio Connectors

Figure 13 shows the location of the audio connectors.



Item	Description	Color	For more information see:
A	Auxiliary line in, ATAPI style	White	Table 29, page 59
B	ATAPI CD-ROM	Black	Table 30, page 59

Figure 13. Audio Connectors

NOTE

The front panel audio connector is described in Section 2.8.3, beginning on page 70.

Table 29. Auxiliary Line In Connector

Pin	Signal Name
1	Left auxiliary line in
2	Ground
3	Ground
4	Right auxiliary line in

Table 30. ATAPI CD-ROM Connector

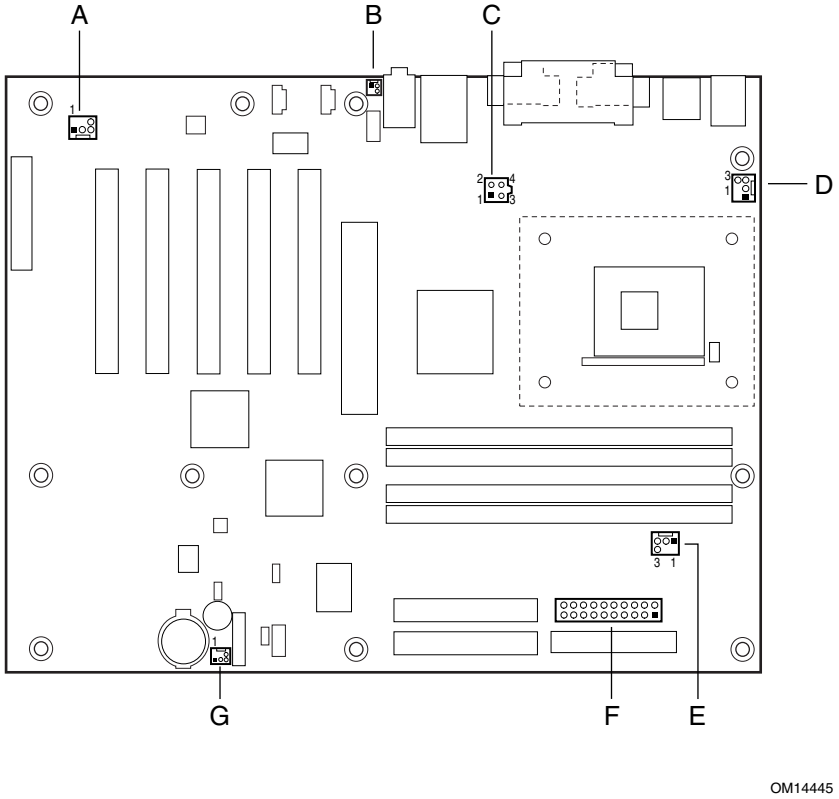
Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

2.8.2.3 Power and Hardware Control Connectors

Figure 14 shows the location of the power and hardware control connectors.

NOTE

Figure 14 shows the desktop board D850EMV2. Fan 3 is not present on the desktop board D850EMD2.



Item	Description	For more information see:
A	Fan 3 (Desktop Board D850EMV2 only)	Table 31, page 61
B	Chassis intrusion	Table 32, page 61
C	ATX12V power	Table 33, page 61
D	Processor fan	Table 34, page 61
E	Fan 1	Table 35, page 62
F	Main power	Table 36, page 62
G	Fan 2	Table 37, page 62

Figure 14. Power and Hardware Control Connectors

For information about	Refer to
The power connector	Section 1.14.2.1, page 42
The functions of the fan connectors	Section 1.14.2.2, page 42

CAUTION

Use only an ATX12V-compliant power supply with these desktop boards. ATX12V power supplies have two power leads that provide required supplemental power for the Intel Pentium 4 processor and the Intel 850E chipset. Always connect the 20-pin and 4-pin leads of the ATX12V power supply to the corresponding connectors on the board. Otherwise, the board and the processor could be damaged.

Do not use a standard ATX power supply. Doing so could damage the board and the processor.

Table 31. Fan 3 Connector (Desktop Board D850EMV2 Only)

Pin	Signal Name
1	(Note 1)
2	+12 V
3	(Note 2)

Notes: 1. Pin 1 is *Ground* if the Desktop Board uses the hardware monitoring ASIC.
Pin 1 is *Fan_Control* if the Desktop Board uses the hardware monitoring and fan control ASIC.

2. Pin 3 is *Reserved* if the Desktop Board uses the hardware monitoring ASIC.
Pin 3 is *Tachometer (FAN_3)* if the Desktop Board uses the hardware monitoring and fan control ASIC.

Table 32. Chassis Intrusion Connector

Pin	Signal Name
1	Intruder
2	Ground

Table 33. ATX12V Power Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	3	+12 V
2	Ground	4	+12 V

Table 34. Processor Fan Connector

Pin	Signal Name
1	(Note)
2	+12 V
3	Tachometer (CPU_FAN)

Note: Pin 1 is *Ground* if the Desktop Board uses the hardware monitoring ASIC.
Pin 1 is *Fan_Control* if the Desktop Board uses the hardware monitoring and fan control ASIC.

Table 35. Fan 1 Connector

Pin	Signal Name
1	(Note 1)
2	+12 V
3	(Note 2)

Notes: 1. Pin 1 is *Ground* if the Desktop Board uses the hardware monitoring ASIC.
Pin 1 is *Fan_Control* if the Desktop Board uses the hardware monitoring and fan control ASIC.

2. Pin 3 is *Ground* if the Desktop Board uses the hardware monitoring ASIC.
Pin 3 is *Tachometer (FAN_1)* if the Desktop Board uses the hardware monitoring and fan control ASIC.

Table 36. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS_ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	TP_PWRCONN_18
9	+5 V (Standby)	19	+5 V
10	+12 V	20	+5 V

Table 37. Fan 2 Connector

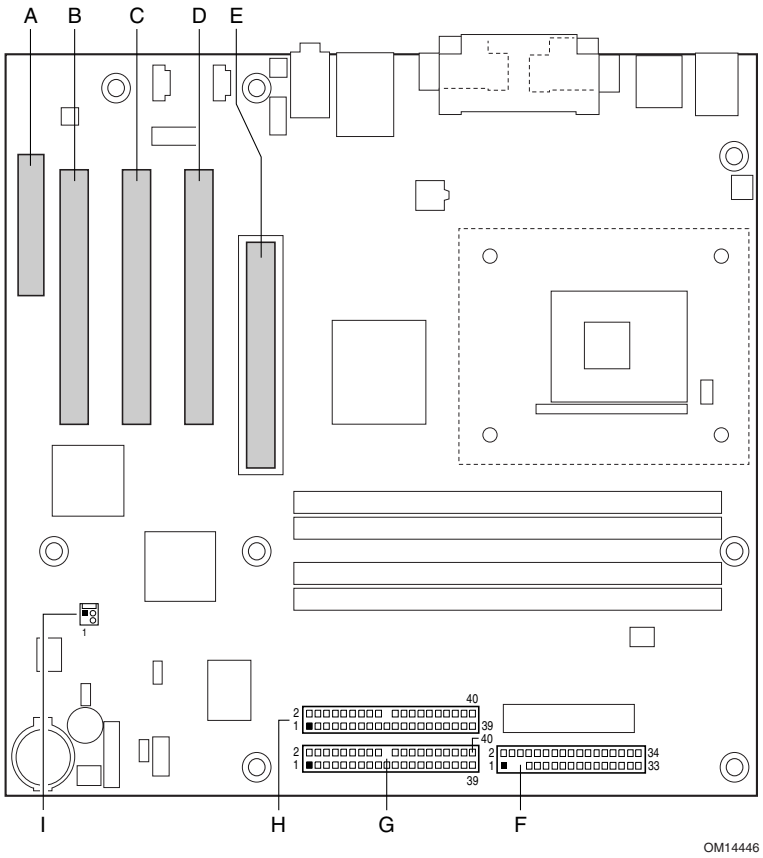
Pin	Signal Name
1	(Note)
2	+12 V
3	Tachometer (FAN_2)

Note: 1. Pin 1 is Ground if the Desktop Board uses the hardware monitoring ASIC.
Pin 1 is *Fan_Control* if the Desktop Board uses the hardware monitoring and fan control ASIC.

2.8.2.4 Add-in Board and Peripheral Interface Connectors

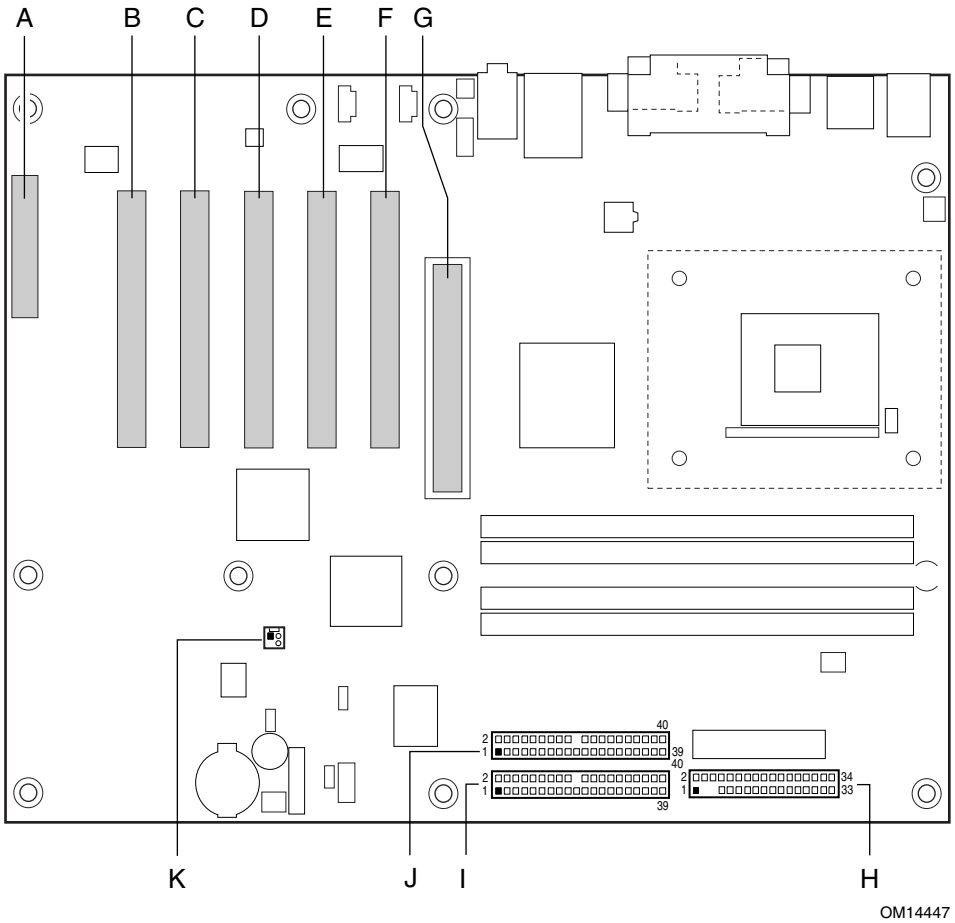
Figure 15 and Figure 16 show the locations of the add-in board connectors and peripheral connectors for the desktop boards D850EMD2 and D850EMV2, respectively. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus-master capable.
- PCI bus connector 2 has SMBus signals routed to it, which enables PCI bus add-in boards with SMBus support to access sensor data on the board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40
  - The SMBus data line is connected to pin A41



Item	Description	For more information see:
A	CNR (optional)	Table 38, page 65
B	PCI bus connector 3	Table 39, page 66
C	PCI bus connector 2	Table 39, page 66
D	PCI bus connector 1	Table 39, page 66
E	AGP connector	Table 40, page 67
F	Diskette drive	Table 41, page 68
G	Primary IDE	Table 42, page 69
H	Secondary IDE	Table 42, page 69
I	SCSI hard drive activity LED	Table 43, page 69

Figure 15. Add-in Board and Peripheral Interface Connectors (Desktop Board D850EMD2)



Item	Description	For more information see:
A	CNR (optional)	Table 38, page 65
B	PCI bus connector 5	Table 39, page 66
C	PCI bus connector 4	Table 39, page 66
D	PCI bus connector 3	Table 39, page 66
E	PCI bus connector 2	Table 39, page 66
F	PCI bus connector 1	Table 39, page 66
G	AGP connector	Table 40, page 67
H	Diskette drive	Table 41, page 68
I	Primary IDE	Table 42, page 69
J	Secondary IDE	Table 42, page 69
K	SCSI hard drive activity LED	Table 43, page 69

Figure 16. Add-in Board and Peripheral Interface Connectors (Desktop Board D850EMV2)

Table 38. CNR Connector (Optional)

Pin	Signal Name	Pin	Signal Name
A1	Reserved	B1	Reserved
A2	Reserved	B2	Reserved
A3	Ground	B3	Reserved
A4	Reserved	B4	Ground
A5	Reserved	B5	Reserved
A6	Ground	B6	Reserved
A7	LAN_TXD2	B7	Ground
A8	LAN_TXD0	B8	LAN_TXD1
A9	Ground	B9	LAN_RSTSYNC
A10	LAN_CLK	B10	Ground
A11	LAN_RXD1	B11	LAN_RXD2
A12	Reserved	B12	LAN_RXD0
A13	USB+	B13	Ground
A14	Ground	B14	Reserved
A15	USB-	B15	+5 V (dual)
A16	+12 V	B16	USB_OC
A17	Ground	B17	Ground
A18	+3.3 V (dual)	B18	-12 V
A19	+5 V	B19	+3.3 V
A20	Ground	B20	Ground
A21	EEDI	B21	EED0
A22	EECS	B22	EECK
A23	SMB_A1	B23	Ground
A24	SMB_A2	B24	SMB_A0
A25	SMB_SDA	B25	SMB_SCL
A26	AC97_RESET	B26	CDC_DWN_ENAB
A27	Reserved	B27	Ground
A28	AC97_SDATA_IN1	B28	AC97_SYNC
A29	AC97_SDATA_IN0	B29	AC97_SDATA_OUT
A30	Ground	B30	AC97_BITCLK

For information about	Refer to
The CNR	Section 1.12, page 35

Table 39. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	Not connected (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	Not connected (PRSNT1#)*	A40	Reserved **	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	Reserved ***	B41	+3.3 V
A11	Reserved	B11	Not connected (PRSNT2#)*	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

** On PCI bus connector 2, this pin is connected to the SMBus clock line.

*** On PCI bus connector 2, this pin is connected to the SMBus data line.

Table 40. AGP Connector

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12 V	B1	Not connected	A34	Vddq	B34	Vddq
A2	TYPEDET#	B2	+5 V	A35	AD22	B35	AD21
A3	Reserved	B3	+5 V	A36	AD20	B36	AD19
A4	Not connected	B4	Not connected	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	Vddq	B40	Vddq
A8	GNT1#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	+3.3 V (aux)
A10	ST1	B10	ST0	A43	Ground	B43	Ground
A11	Reserved	B11	ST2	A44	Reserved	B44	Reserved
A12	PIPE#	B12	RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	TRDY#	B46	DEVSEL#
A14	WBF#	B14	Not connected	A47	STOP#	B47	Vddq
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	SBSTB#	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	Ground	B19	Ground	A52	Vddq	B52	Vddq
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	Reserved	B22	Reserved	A55	Ground	B55	Ground
A23	Ground	B23	Ground	A56	AD9	B56	AD10
A24	Reserved	B24	+3.3 V (aux)	A57	C/BE0#	B57	AD8
A25	Vcc3.3	B25	Vcc3.3	A58	Vddq	B58	Vddq
A26	AD30	B26	AD31	A59	AD_STB0#	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	Ground	B31	Ground	A64	Vddq	B64	Vddq
A32	AD_STB1#	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	VRREFG_C	B66	VREFC_G

NOTE

The AGP connector is keyed for 1.5 V AGP cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.

Table 41. Diskette Drive Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	Not connected
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	Not connected
17	Not connected	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	Not connected	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 42. IDE Connectors

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select pull-up)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	DAG1 (Address 1)	34	GPIO_DMA66_Detect_Pri (GPIO_DMA66_Detect_Sec)
35	DAG0 (Address 0)	36	DAG2 (Address 2)
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

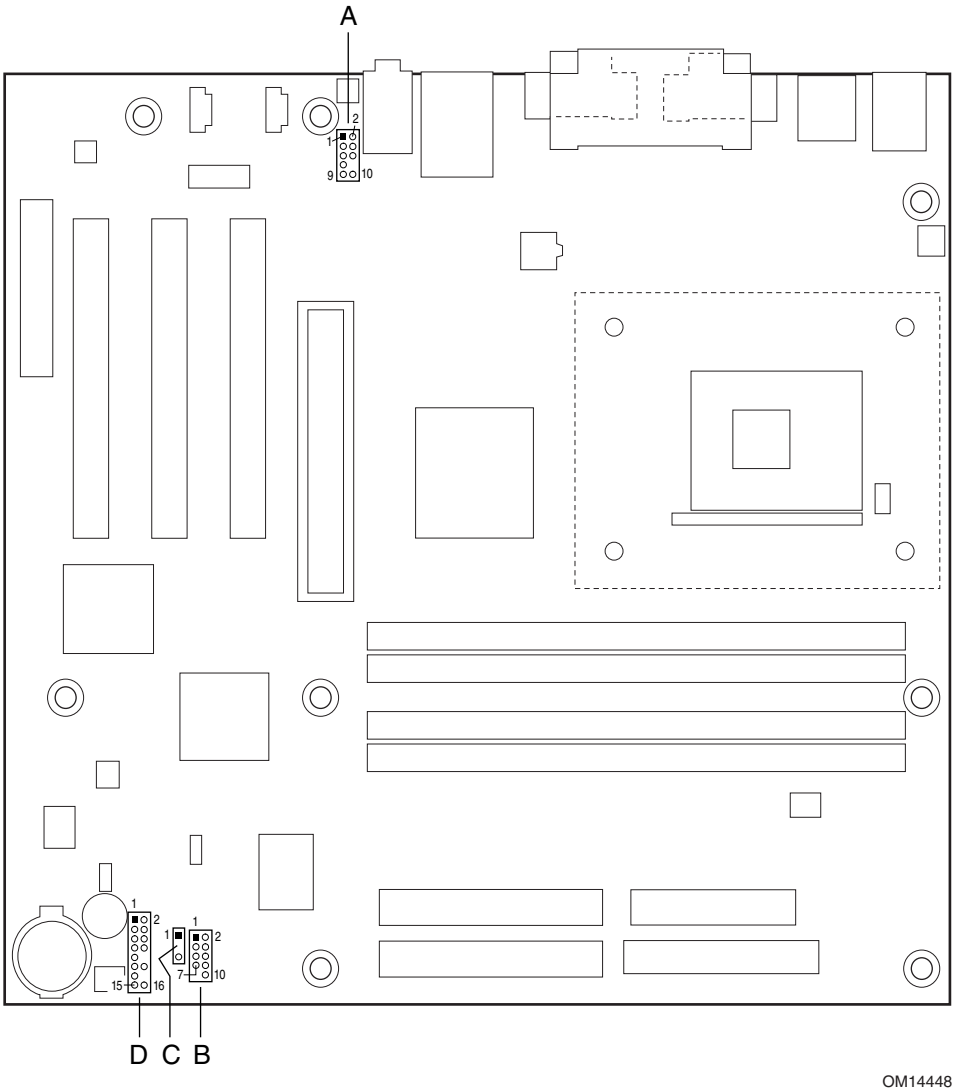
Signal names in brackets ([ ]) are for the secondary IDE connector.

Table 43. SCSI Hard Drive Activity LED Connector

Pin	Signal Name
1	SCSI_ACT#
2	No connect

2.8.3 External I/O Connectors

Figure 17 shows the locations of the external I/O connectors.



Item	Description	For more information see:
A	Front panel audio	Table 44, page 71
B	Front panel USB	Table 45, page 71
C	Auxiliary front panel power/sleep/message-waiting LED	Table 46, page 71
D	Front panel	Table 47, page 72

Figure 17. External I/O Connectors

Table 44. Front Panel Audio Connector

Pin	Signal Name	Pin	Signal Name
1	MIC_IN_FP	2	AUD_JACK_GND
3	MIC_BIAS	4	V_5P0_AUD_ANALOG
5	R_FNTOUT	6	R_RETIN
7	Not connected	8	Not connected
9	L_FNT_OUT	10	L_RETIN

Table 45. Front Panel USB Connector

Pin	Signal Name	Pin	Signal Name
1	USB_FNT_PWR	2	USB_FNT_PWR
3	USB_FNTA#	4	USB_FNTB#
5	USB_FNTA	6	USB_FNTB
7	Ground	8	Ground
9	Not connected	10	Not connected

2.8.3.1 Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector

Pins 1 and 3 on this connector duplicate the signals on pins 2 and 4 of the front panel connector.

Table 46. Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.8.3.2 Front Panel Connector

This section describes the functions of the front panel connector. Table 47 lists the signal names of the front panel connector.

Table 47. Front Panel Connector

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
1	HD_PWR	Out	Hard disk LED pull-up (330 Ω) to +5 V	2	HDR_BLNK_GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_YEL	Out	Front panel yellow LED
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
9	+5 V	Out	Reserved	10	N/C		
11	Reserved	In	Reserved	12	Ground		Ground
13	Ground		Ground	14	(pin removed)		Not connected
15	Reserved	Out	Reserved	16	+5 V	Out	Power

2.8.3.2.1 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary (SPST type) switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.8.3.2.2 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface. The LED will also show activity for devices connected to the SCSI hard drive activity LED connector.

For information about	Refer to
The SCSI hard drive activity LED connector	Section 1.8.3.2, page 29

2.8.3.2.3 Power/Sleep/Message-Waiting LED Connector

Pins 2 and 4 can be connected to a one- or two-color LED. Table 48 shows the possible states for a one-color LED. Table 49 shows the possible states for a two-color LED.

Table 48. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running
Blinking Green	Running/message waiting

Table 49. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE

To use the message-waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.3.2.4 Power Switch Connector

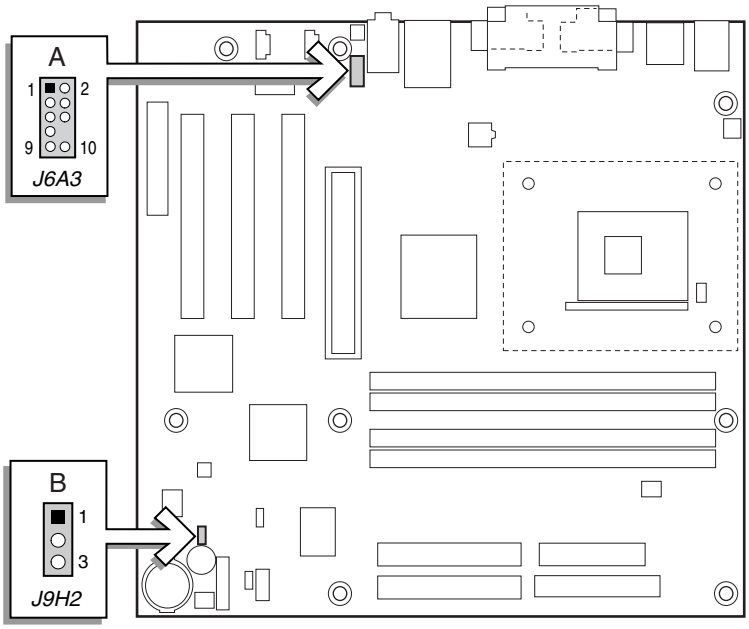
Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the desktop boards D850EMD2/D850EMV2.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.9 Jumper Blocks

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 18 shows the location of the jumper blocks.



Item	Description	Reference Designator
A	Front panel audio connector/jumper block	J6A3
B	BIOS Setup configuration jumper block	J9H2

Figure 18. Location of the Jumper Blocks

2.9.1 Front Panel Audio Connector/Jumper Block

This connector has two functions:

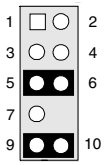
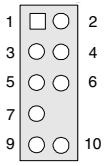
- With jumpers installed, the audio line out signals are routed to the back panel audio line out connector.
- With jumpers removed, the connector provides audio line out and mic in signals for front panel audio connectors.

Table 50 describes the two configurations of this connector/jumper block.

CAUTION

Do not place jumpers on this block in any configuration other than the one described in Table 50. Other jumper configurations are not supported and could damage the board.

Table 50. Front Panel Audio Connector/Jumper Block

Jumper Setting		Configuration
	5 and 6 9 and 10	Audio line out signals are routed to the back panel audio line out connector. The back panel audio line out connector is shown in Figure 12 on page 54.
	No jumpers installed	Audio line out and mic in signals are available for front panel audio connectors. Table 44 on page 71 lists the names of the signals available on this connector when no jumpers are installed.

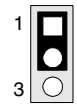
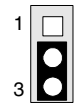
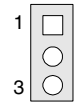
NOTE

When the jumpers are removed and this connector is used for front panel audio, the back panel audio line out and mic in connectors are disabled.

2.9.2 BIOS Setup Configuration Jumper Block

The 3-pin jumper block determines the BIOS Setup program's mode. Table 51 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configuration mode and the computer is powered up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

Table 51. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The Maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

2.10 Mechanical Considerations

2.10.1 Desktop Board D850EMD2 Form Factor

The Desktop Board D850EMD2 is designed to fit into a microATX form factor chassis. Figure 19 illustrates the mechanical form factor for the Desktop Board D850EMD2. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 9.60 inches [243.84 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification (see Section 1.5).

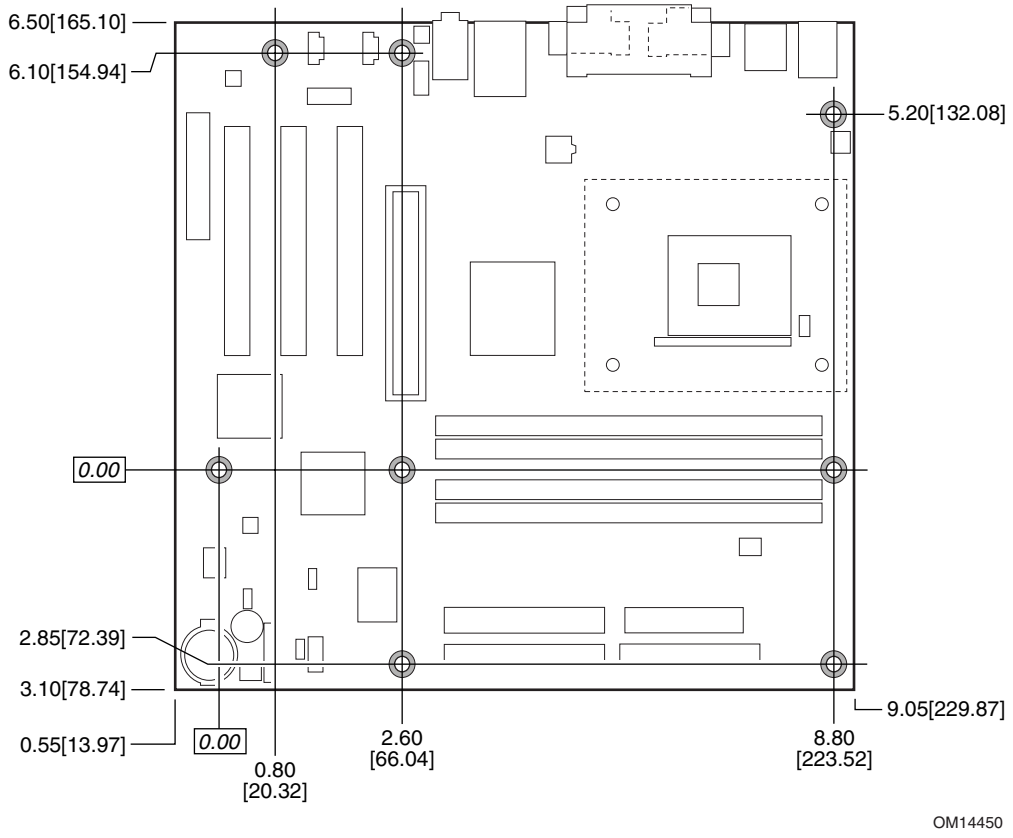


Figure 19. Desktop Board D850EMD2 Dimensions

NOTE

There may be mechanical interference with installed RDRAM modules in some combinations of ATX chassis and peripherals, such as CD-ROM drives.

2.10.2 Desktop Board D850EMV2 Form Factor

The Desktop Board D850EMV2 is designed to fit into an ATX form factor chassis. Figure 20 illustrates the mechanical form factor for the Desktop Board D850EMV2. Dimensions are given in inches [millimeters]. The outer dimensions are 12.00 inches by 9.60 inches [304.48 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification (see Section 1.5).

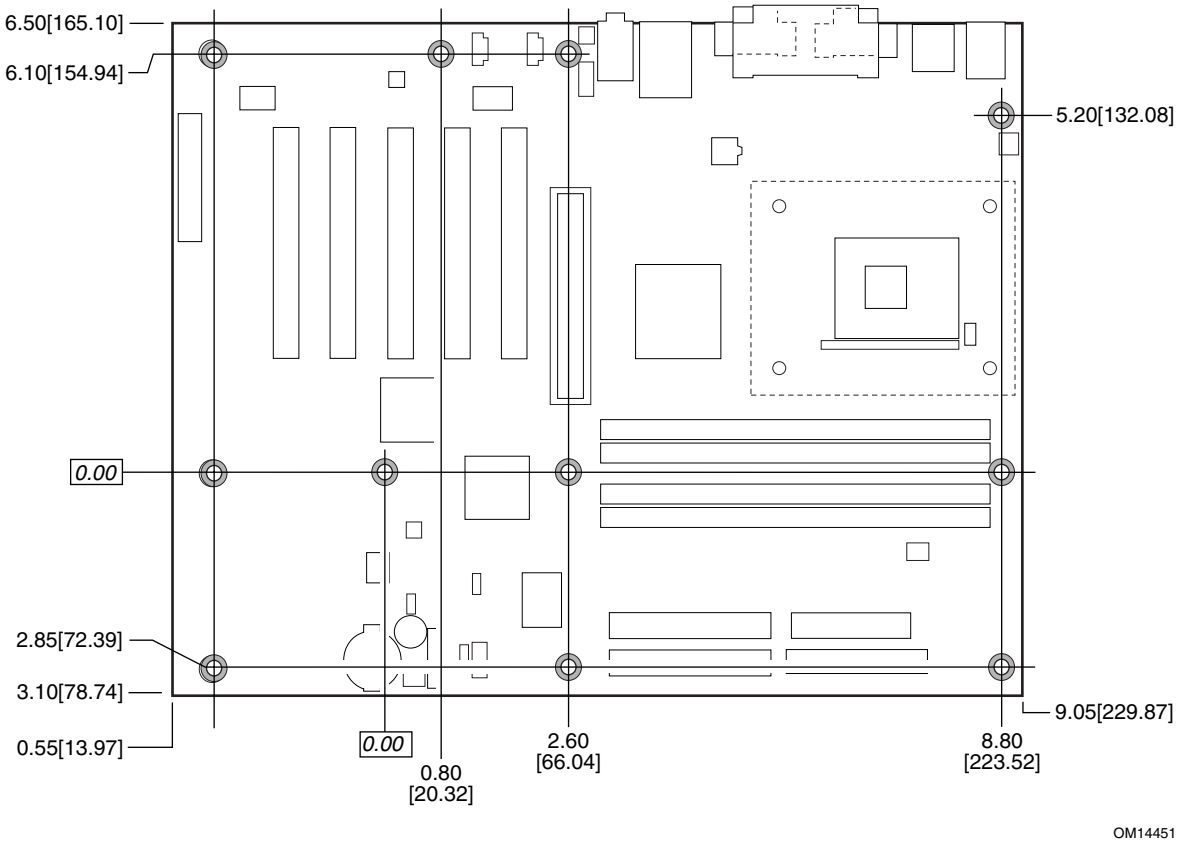


Figure 20. Desktop Board D850EMV2 Dimensions

NOTE

There may be mechanical interference with installed RDRAM modules in some combinations of ATX chassis and peripherals, such as CD-ROM drives.

2.10.3 I/O Shield

The back panel I/O shield for desktop boards D850EMD2/D850EMV2 must meet specific dimension and material requirements. Systems based on these boards need the back panel I/O shield to pass certification testing. Figure 21 shows the critical dimensions of the chassis-dependent I/O shield. Dimensions are given in inches to a tolerance of ±0.02 inches [±0.508 millimeters].

The figure also indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 1.5 for information about the ATX specification.

NOTE

The illustration below is for reference only. An I/O shield compliant with the ATX chassis specification 2.01 is available from Intel.

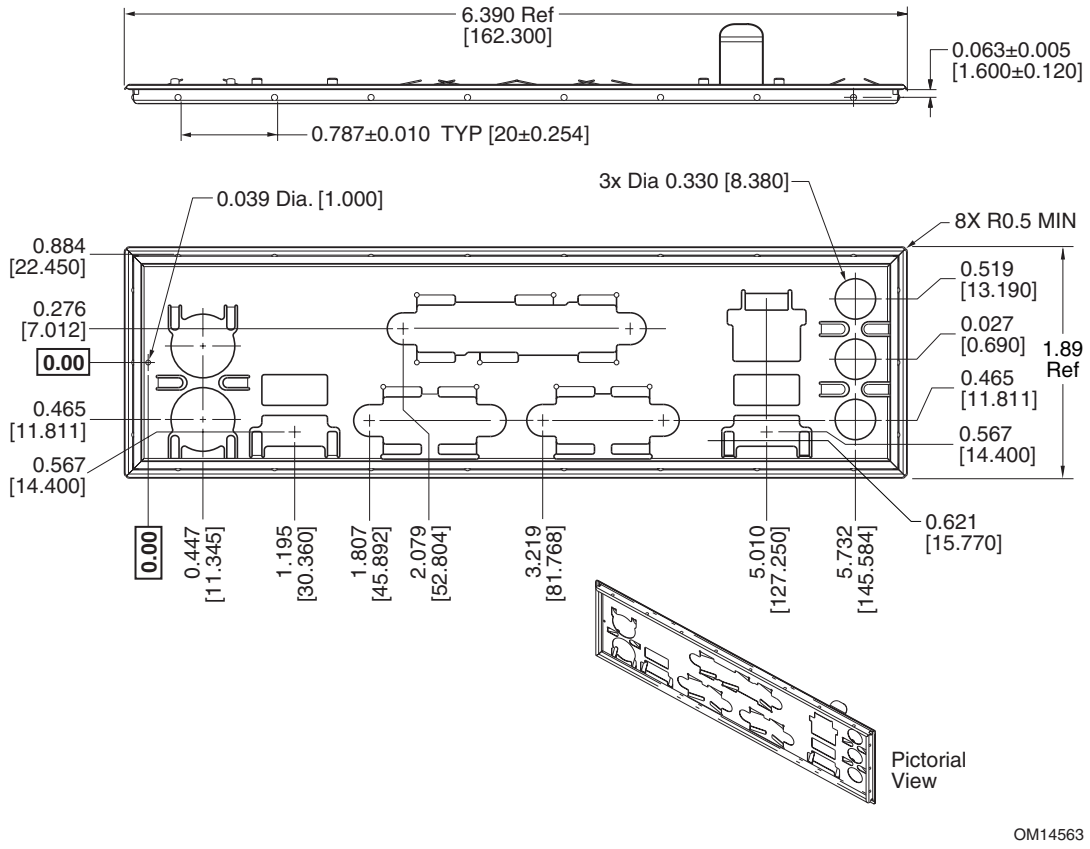


Figure 21. I/O Shield Dimensions

NOTE

The USB ports between the PS/2 and serial ports are not populated if USB 2.0 is supported.

2.11 Electrical Considerations

2.11.1 Power Consumption

Table 52 lists voltage and current measurements for a computer that contains the desktop board D850EMD2/D850EMV2 and the following:

- 1.7 GHz Intel Pentium 4 processor with a 256 KB cache
- 128 MB PC800 ECC RDRAM
- AGP 4X/2X video card
- 3.5-inch diskette drive
- 11.5 GB IDE hard disk drive
- 36X IDE CD-ROM drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 98 SE desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with the computer connected to a typical 250 W power supply, at nominal input voltage and frequency, with a true RMS wattmeter at the line input.

NOTE

Actual system power consumption depends upon system configuration. The power supply should comply with the recommendations found in the ATX / ATX12V Power Supply Design Guide, Version 1.1 *(see Section 1.5 for specification information).*

Table 52. Power Usage

Mode	AC Power	DC Current at:				
		+3.3 V	+5 V	+12 V	-12 V	+5 VSB
Windows 98 SE ACPI S0	69 W	2.6 A	2.3 A	1.5 A	0 A	0.3 A
Windows 98 SE ACPI S1	63 W	2.5 A	2.3 A	1.4 A	0 A	0.3 A
Windows 98 SE ACPI S3	3 W	0 A	0 A	0 A	0 A	0.4 A

2.11.2 Add-in Board Considerations

The desktop boards D850EMD2/D850EMV2 are designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards is as follows:

- For a fully loaded desktop board D850EMD2 (all four expansion slots filled), the total +5 V current draw must not exceed 8 A.
- For a fully loaded desktop board D850EMV2 (all seven expansion slots filled), the total +5 V current draw must not exceed 14 A.

2.11.3 Standby Current Requirements

CAUTION

If the standby current necessary to support multiple wake events from the PCI and/or USB buses exceeds power supply capacity, the desktop boards D850EMD2/D850EMV2 may lose register settings stored in memory, etc. Calculate the standby current requirements using the steps described below.

Power supplies used with the desktop boards D850EMD2/D850EMV2 must be able to provide enough standby current to support the Instantly Available (ACPI S3 sleep state) configuration as outlined in Table 53 below.

Values are determined by specifications such as PCI 2.2. Actual measured values may vary.

To estimate the amount of standby current required for a particular system configuration, standby current requirements of all installed components must be added to determine the total standby current requirement. Refer to the descriptions in Table 53 and review the following steps.

1. Note the total standby current required for the desktop boards D850EMD2/D850EMV2.
2. Add to that the total PS/2 port standby current requirement if a wake-enabled device is connected.
3. Add, from the PCI 2.2 slots (wake enabled) row, the total number of wake-enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
4. Add, from the PCI 2.2 slots (non–wake enabled) row, the total number of wake-enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
5. Add the standby current requirements for all additional wake-enabled and non-wake-enabled devices as applicable.
6. Add all the required current totals from steps 1 through 5 to determine the total estimated standby current power supply requirement.

Table 53. Standby Current Requirements

Instantly Available Current Support (Estimated for Integrated Board Components)	**Description**	**Standby Current Requirements (mA)**
	Total for desktop board D850EMD2	375
Instantly Available Standby Current Support • **Estimated for add-on components** • **Add to Instantly Available total current requirement** **(See instructions above)**	PS/2 ports (Note)	345
	PCI 2.2 slots (wake enabled)	375
	PCI 2.2 slots (non–wake enabled)	20
	CNR (Note)	375
	USB ports (Note)	500

Note: Dependent upon system configuration

NOTE

IBM PS/2 Port Specification (September 1991) states:

- *275 mA for keyboard*
- *70 mA for the mouse (non-wake-enabled device)*

PCI/AGP requirements are calculated by totaling the following:

- *One wake-enabled device @ 375 mA, plus*
- *Five non-wake-enabled devices @ 20 mA each, plus*

USB requirements are calculated as:

- *One wake-enabled device @ 500 mA*
- *USB hub @ 100 mA*
- *Three USB non-wake-enabled devices connected @ 2.5 mA each*

NOTE

Both USB ports are capable of providing up to 500 mA during normal S0 operation. Only one USB port will support up to 500 mA of standby current (wake-enabled device) during S3 suspended operation. The other ports may provide up to 7.5 mA (three non-wake-enabled devices) during S3 suspended operation.

2.11.4 Fan Connector Current Capability

The desktop boards D850EMD2/D850EMV2 are designed to supply a maximum of 1 A per fan connector.

2.11.5 Power Supply Considerations

CAUTION

The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 80 for additional information.

System integrators should refer to the power usage values listed in Table 52 on page 79 when selecting a power supply to use with the desktop boards D850EMD2/D850EMV2.

Measurements account only for current sourced by the desktop boards D850EMD2/D850EMV2 while running in idle modes of the started operating systems.

Additional required power will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

For information about	Refer to
The ATX form factor specification	Section 1.5, page 19

2.12 Thermal Considerations

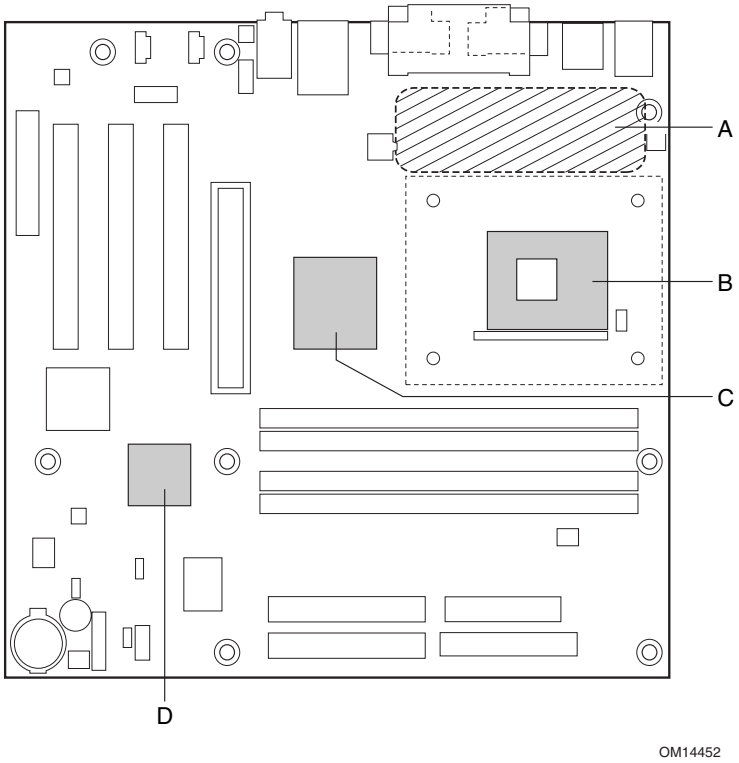
CAUTION

Ensure that the ambient temperature does not exceed the board's maximum operating temperature by more than 10 °C. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (item A in Figure 22) can reach a temperature of up to 85 °C in an open chassis.

Figure 22 shows the locations of the localized high temperature zones.



A Processor voltage regulator area
B Processor
C Intel 82850E MCH
D Intel 82801BA ICH2

Figure 22. Localized High-Temperature Zones

Table 54 provides maximum case temperatures for board components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the desktop boards D850EMD2/D850EMV2.

Table 54. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium 4 processor	For processor case temperature, see processor datasheets and processor specification updates
Intel 82850E MCH	105 °C (under bias)
Intel 82801BA ICH2	109 °C (under bias)

For information about	Refer to
Intel Pentium 4 processor datasheets and specification updates	Section 1.3, page 18

2.13 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 55 ºC.

Desktop boards D850EMD2/D850EMV2 MTBF: 110595.61 hours

2.14 Environmental

Table 55 lists the environmental specifications for the desktop boards D850EMD2/D850EMV2.

Table 55. Desktop Boards D850EMD2/D850EMV2 Environmental Specifications

Parameter	Specification		
Temperature			
Nonoperating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21 – 40	30	152
	41 – 80	24	136
	81 – 100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the desktop boards D850EMD2/D850EMV2's compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

2.15.1 Safety Regulations

Table 56 lists the safety regulations that the desktop boards D850EMD2/D850EMV2 comply with when correctly installed in a compatible host system.

Table 56. Safety Regulations

Regulation	Title
UL 1950/CSA C22.2 No. 950, 3rd edition	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 60950, 2nd Edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

2.15.2 EMC Regulations

Table 57 lists the EMC regulations that the desktop boards D850EMD2/D850EMV2 comply with when correctly installed in a compatible host system.

Table 57. EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radiofrequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022: 1994 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS 3548 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 2nd Edition (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International)

2.15.3 Product Certification Markings (Board Level)

The following tables describe the product certification markings on the desktop boards D850EMD2/D850EMV2. Table 58 lists the markings on the component side of the boards and Table 59 lists the solder side markings.

Table 58. Component Side Markings

Certification Mark	Description
UL joint US/Canada Recognized Component mark	• Consists of lower case *c* followed by a stylized backward *UR* and followed by a small *US* • Includes the adjacent UL file number for Intel desktop boards — For the Desktop Board D850EMD2, the number is E210882. — For the Desktop Board D850EMV2, the number is E210882.
CE mark	• Declares compliance to the European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) • Should also be on the shipping container
Australian Communications Authority (ACA) C-tick mark	• Consists of a stylized *C* overlaid with a check (tick) mark, followed by an Intel supplier code number, N-232 • Should also be on the shipping container
Korean EMC certification logo mark	Consists of MIC lettering within a stylized elliptical outline
Battery “+ Side Up” marking	Located in close proximity to the battery holder

Table 59. Solder Side Markings

Certification Mark	Description
FCC Declaration of Conformity logo mark for Class B equipment	Includes the Intel name and the desktop boards D850EMD2/D850EMV2 model designation
Printed wiring board manufacturer’s recognition mark	Consists of a unique UL-recognized manufacturer’s logo, along with a flammability rating (94V-0)
PB part number	• Intel bare circuit board part number • Also includes the SKU number, which starts with *AA* and is followed by additional alphanumeric characters — For the Desktop Board D850EMD2, the PB number is A49682-004. — For the Desktop Board D850EMV2, the PB number is A56437-004.

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction....87
3.2 BIOS Flash Memory Organization....87
3.3 Resource Configuration....87
3.4 SMBIOS....88
3.5 Legacy USB Support....89
3.6 BIOS Updates....89
3.7 Recovering BIOS Data....91
3.8 Boot Options....91
3.9 Fast Booting Systems with Intel® Rapid BIOS Boot....92
3.10 BIOS Security Features....93

3.1 Introduction

The desktop boards D850EMD2/D850EMV2 use an Intel/AMI BIOS that is stored in the FWH and can be updated using a software utility. The FWH contains the BIOS Setup program, POST, the PCI autoconfiguration utility, and Plug and Play support.

The desktop boards D850EMD2/D850EMV2 support system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected system memory.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as MV85010A.86A.

For information about	Refer to
The Desktop Boards D850EMD2/D850EMV2's compliance level with Plug and Play	Section 1.5, page 19

3.2 BIOS Flash Memory Organization

The FWH includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64 KB blocks that are individually erasable, lockable, and unlockable.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are

considered to be available for use by the add-in card. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.5.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI-compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.5 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for LBA and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the autoconfiguration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features, the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

ATA-66/100 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an ATA-66/100 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is reduced to that of the slowest device.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 SMBIOS

SMBIOS is a Desktop Management Interface (DMI)–compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags

- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non–Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non–Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The desktop boards D850EMD2/D850EMV2's compliance level with SMBIOS	Section 1.5, page 19

3.5 Legacy USB Support

Legacy USB support enables USB devices such as keyboards and mice to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program and to install an operating system that supports USB. By default, legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS, allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the Maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and nonlegacy USB devices are recognized by the operating system, and legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

NOTE

Legacy USB support is for keyboards and mice only. Other USB devices are not supported in legacy mode.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, a CD-ROM, or from the file location on the Web.

- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities support the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Updating the BIOS boot block separately.
- Changing the language section of the BIOS.
- Updating replaceable BIOS modules, such as the video BIOS module.
- Inserting a custom splash screen.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.3, page 18

3.6.1 Language Support

The BIOS Setup program and help messages are supported in five languages: US English, Spanish, German, Italian, and French. The default language is US English, which is present unless another language is selected in the BIOS Setup program.

3.6.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site.

For information about	Refer to
The Intel World Wide Web site	Section 1.3, page 18

3.7 Recovering BIOS Data

Some types of failure can corrupt the content of the FWH. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the nonerasable boot block area, there is no video support. You can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes. Larger BIOS flash memory devices require more time.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Update Utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

Even if the computer is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette and not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode jumper settings	Section 2.9, page 74
The Boot menu in the BIOS Setup program	Section 4.7, page 113
Contacting Intel customer support	Section 1.3, page 18

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, the ATAPI CD-ROM third, and the network fourth.

3.8.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

For information about	Refer to
The El Torito specification	Section 1.5, page 19

3.8.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces boot from the LAN.

3.8.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.8.4 Changing the Default Boot Device During POST

Pressing the <F8> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program's Boot Device Priority Submenu). Table 60 lists the boot device menu options.

Table 60. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, saves changes, and boots from the selected device
<Esc>	Exits the menu without saving changes

3.9 Fast Booting Systems with Intel® Rapid BIOS Boot

Three factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel® Rapid BIOS
- Selecting a compatible operating system

3.9.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as "power-up to data ready" less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.

3.9.2 Intel Rapid BIOS Boot

Use the following BIOS Setup program settings to reduce the POST execution time:

- In the Boot menu:
  - Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
  - Enable Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive.
  - Disable unused features.
- In the Peripheral Configuration submenu, disable the LAN device if it will not be used, which can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from 3 to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced menu in the IDE Configuration submenu of the BIOS Setup program).

For information about	Refer to
The IDE Configuration submenu in the BIOS Setup program	Section 4.4.4, page 104

3.9.3 Operating System

The Microsoft Windows Millennium Edition (Windows Me) operating system has built-in capabilities for making PCs boot more quickly. To speed operating system availability at boot time, limit the number of applications that load into the system tray or the task bar.

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives access to view and change Setup options in the BIOS Setup program based on the setting of the User Access Level option in the BIOS Setup Program's Security Menu. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user access to Setup based on the setting of the User Access Level option in the BIOS Setup Program's Security Menu.

- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 61 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 61. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 4.5, page 110

NOTE

For enhanced security, use different passwords for the supervisor and user passwords.

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction....95
4.2 Maintenance Menu....96
4.3 Main Menu....98
4.4 Advanced Menu....99
4.5 Security Menu....110
4.6 Power Menu....111
4.7 Boot Menu....113
4.8 Exit Menu....116

4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the POST memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

Table 62 lists the BIOS Setup program's menu features.

Table 62. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and BIS credentials and enables extended configuration mode	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

For information about	Refer to
BIS	Section 1.5, page 19

NOTE

In this chapter, all examples of the BIOS Setup program menu bar include the Maintenance menu; however, the Maintenance menu is displayed only when the board is in configuration mode. Section 2.9 on page 74 tells how to put the board in configuration mode.

Table 63 lists the function keys available for menu screens.

Table 63. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Loads the default configuration values for the current menu
<F10>	Saves the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

To access this menu, select Maintenance on the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The menu shown in Table 64 is for clearing Setup passwords and enabling extended configuration mode. Setup displays this menu only in configuration mode. See Section 2.9 on page 74 for information on setting configuration mode.

Table 64. Maintenance Menu

Feature	Options	Description
Clear All Passwords	• **Yes (default)** • No	Clears the user and supervisor passwords.
Clear BIS Credentials	• **Yes (default)** • No	Clears the WfM BIS credentials.
Extended Configuration	Select to display submenu	Invokes the Extended Configuration submenu.
CPU Information	No options	Displays CPU information.
CPU Stepping Signature	No options	Displays the CPU's stepping signature.
CPU Microcode Update Revision	No options	Displays the CPU's microcode update revision.

4.2.1 Extended Configuration Submenu

To access this submenu, select Maintenance on the menu bar and then Extended Configuration.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The submenu represented by Table 65 is for setting video memory cache mode. This submenu becomes available when User Defined is selected under Extended Configuration.

Table 65. Extended Configuration Submenu

Feature	Options	Description
Extended Configuration	• **Default (default)** • User Defined	*User Defined* allows you to set memory control and video memory cache mode. If selected here, it will also display in the Advanced menu as "Extended Menu: Used."
Video Memory Cache Mode	• USWC	Selects Uncacheable Speculative Write-Combining (USWC) video memory cache mode. Full 32-byte contents of the Write Combining buffer are written to memory as required. Cache lookups are not performed. Both the video driver and the application must support Write Combining.
	• **UC (default)**	Selects UnCacheable (UC) video memory cache mode. This setting identifies the video memory range as uncacheable by the processor. Memory writes are performed in program order. Cache lookups are not performed. This setting is well suited for applications that do not support Write Combining.

4.3 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 66 describes the Main menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 66. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
System Bus Speed	No options	Displays the system bus speed.
Cache RAM	No options	Displays the size of second-level cache and whether it is ECC capable.
Total Memory	No options	Displays the total amount of RAM.
RIMM 1 RIMM 2 RIMM 3 RIMM 4	No options	Displays the amount and type of RAM in the memory banks.
Language	• **English (default)** • Español • Deutsch • Italiano • Français	Selects the current default language used by the BIOS.
Memory Configuration	• Non-ECC • **ECC (default)**	If ECC memory is installed, allows the user to enable error reporting. If Non-ECC memory is installed, this option will not appear.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Day of week Month/day/year	Specifies the current date.

4.4 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

Table 67 describes the Advanced menu. This menu is used for setting advanced features that are available through the chipset.

Table 67. Advanced Menu

Feature	Options	Description
Extended Configuration	No options	If *Used* is displayed, *User Defined* has been selected in Extended Configuration under the Maintenance menu.
PCI Configuration	Select to display submenu	Configures individual PCI slot's IRQ priority.
Boot Configuration	Select to display submenu	Configures Plug and Play and the Numlock key, and resets configuration data.
Peripheral Configuration	Select to display submenu	Configures peripheral ports and devices.
IDE Configuration	Select to display submenu	Specifies the types of connected IDE devices.
Diskette Configuration	Select to display submenu	Configures the diskette drive.
Event Log Configuration	Select to display submenu	Configures event logging.
Video Configuration	Select to display submenu	Configures video features.

4.4.1 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar and then PCI Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu shown in Table 68 is used to configure the IRQ priority of PCI slots individually.

Table 68. PCI Configuration Submenu

Feature	Options	Description
PCI Slot1 IRQ Priority	• **Auto (default)** • 5 • 9 • 10 • 11	Allows selection of IRQ priority.
PCI Slot2 IRQ Priority	• **Auto (default)** • 5 • 9 • 10 • 11	Allows selection of IRQ priority.
PCI Slot3 IRQ Priority	• **Auto (default)** • 5 • 9 • 10 • 11	Allows selection of IRQ priority.
PCI Slot4 IRQ Priority	• **Auto (default)** • 5 • 9 • 10 • 11	Allows selection of IRQ priority. This option is available on the desktop board D850EMV2 only.
PCI Slot5 IRQ Priority	• **Auto (default)** • 5 • 9 • 10 • 11	Allows selection of IRQ priority. This option is available on the desktop board D850EMV2 only.

4.4.2 Boot Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Boot Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 69 is for setting Plug and Play options, resetting configuration data, and setting the power-on state of the Numlock key.

Table 69. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if manual configuration is desired. *No* lets the BIOS configure all devices. This setting is appropriate when using a Plug and Play operating system. *Yes* lets the operating system configure Plug and Play devices that are not required to boot the system. This option is available for use during lab testing.
Reset Config Data	• **No (default)** • Yes	*No* does not clear the PCI/Plug and Play configuration data stored in flash memory on the next boot. *Yes* clears the PCI/Plug and Play configuration data stored in flash memory on the next boot.
Numlock	• Off • **On (default)**	Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard.
ISA Enable Bit	• **Enabled (default)** • Disabled	When set to *Enable*, a PCI-to-PCI bridge will only recognize I/O addresses that do not alias to an ISA range (within the bridge's assigned I/O range).

4.4.3 Peripheral Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Peripheral Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 70 is used for configuring computer peripherals.

Table 70. Peripheral Configuration Submenu

Feature	Options	Description
Serial Port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address (This feature is present only when Serial Port A is set to *Enabled*)	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A, if serial port A is set to *Enabled.*
Interrupt (This feature is present only when Serial Port A is set to *Enabled*)	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A, if serial port A is set to *Enabled.*
Serial Port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. *Auto* assigns the first free COM port, normally COM 2, the address 3F8h and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address (This feature is displayed only if Serial Port B is set to *Enabled*.)	• 3F8 • **2F8 (default)** • 3E8 • 2E8	Specifies the base I/O address for serial port B, if serial port B is set to *Enabled*.
Interrupt (This feature is displayed only if Serial Port B is set to *Enabled*.)	• **IRQ 3 (default)** • IRQ 4	Specifies the interrupt for serial port B, if serial port B is set to *Enabled*.

continued

Table 70. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Parallel Port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT†-compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bidirectional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bidirectional mode.
Base I/O address (This feature is present only when Parallel Port is set to *Enabled*)	• **378 (default)** • 278	Specifies the base I/O address for the parallel port.
Interrupt (This feature is present only when Parallel Port is set to *Enabled*)	• IRQ 5 • **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
DMA (This feature is present only when Parallel Port Mode is set to *ECP*)	• 1 • **3 (default)**	Specifies the DMA channel.
Audio Device	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem. For boards with no onboard audio subsystem, this option does not appear; however, this option does appear if a CNR card with an audio subsystem is installed.
LAN Device	• Disabled • **Enabled (default)**	Enables or disables the onboard LAN device. For boards with no onboard LAN subsystem, this option will not appear; however, this option does appear if a CNR card with a LAN subsystem is installed.
Modem Device	• Disabled • **Enabled (default)**	Enables or disables a modem device on a CNR card. This option appears only when a CNR card with a modem is installed.
Legacy USB Support	• Disabled • **Enabled (default)**	Enables or disables legacy USB support.

4.4.4 IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar and then IDE Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The menu represented in Table 71 is used to configure IDE device options.

Table 71. IDE Configuration Submenu

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the primary IDE controller. *Secondary* enables only the secondary IDE controller. *Both* enables both IDE controllers.
PCI IDE Bus Master	• Disabled • **Enabled (default)**	Enables/disables the use of DMA for hard drive BIOS INT13 reads and writes.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive predelay.
Primary IDE Master	Select to display submenu	Reports type of connected IDE device.
Primary IDE Slave	Select to display submenu	Reports type of connected IDE device.
Secondary IDE Master	Select to display submenu	Reports type of connected IDE device.
Secondary IDE Slave	Select to display submenu	Reports type of connected IDE device.

4.4.4.1 Primary/Secondary IDE Master/Slave Submenus

To access these submenus, select Advanced on the menu bar, then IDE Configuration, and then the master or slave to be configured.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration **Primary IDE Master** **Primary IDE Slave** **Secondary IDE Master** **Secondary IDE Slave**
Diskette Configuration
Event Log Configuration
Video Configuration

There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 72 shows the format of the IDE submenus. For brevity, only one example is shown.

Table 72. Primary/Secondary IDE Master/Slave Submenus

Feature	Options	Description
Drive Installed	No options	Displays the type of drive installed.
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User* allows capabilities to be changed. *Auto* fills in capabilities from ATA/ATAPI devices.
Maximum Capacity	No options	Displays the capacity of the drive.
LBA Mode Control	• **Disabled (default)** • Enabled	Enables or disables LBA mode control.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies the number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.

continued

Table 72. Primary/Secondary IDE Master/Slave Submenus (continued)

Feature	Options	Description
PIO Mode	• **Auto (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the PIO mode.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4 • Mode 5	Specifies the Ultra DMA mode for the drive.
Cable Detected	No options	Displays the type of cable connected to the IDE interface: 40-conductor or 80-conductor (for ATA-100 peripherals).

Note: If an LS-120 drive is attached to the system, a row entitled ARMD Emulation Type will be displayed in the above table. The BIOS will always recognize the drive as an ATAPI floppy drive. The ARMD Emulation Type should always be set to Floppy.

4.4.5 Diskette Configuration Submenu

To access this menu, select Advanced on the menu bar and then Diskette Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 73 is used to configure the diskette drive.

Table 73. Diskette Configuration Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A	• Not Installed • 360 KB 5¼" • 1.2 MB 5¼" • 720 KB 3½" • **1.44/1.25 MB 3½" (default)** • 2.88 MB 3½"	Specifies the capacity and physical size of diskette drive A.
Diskette Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protection for the diskette drive.

4.4.6 Event Log Configuration Submenu

To access this menu, select Advanced on the menu bar and then Event Log Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 74 is used to configure the event logging features.

Table 74. Event Log Configuration Submenu

Feature	Options	Description
Event Log	No options	Indicates if there is space available in the event log.
Event Log Validity	No options	Indicates if the contents of the event log are valid.
View Event Log	[Enter]	Displays the event log.
Clear All Event Logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of events.
ECC Event Logging	• Disabled • **Enabled (default)**	Enables logging of ECC events.
Mark Events As Read	• **Yes (default)** • No	Marks all events as read.

4.4.7 Video Configuration Submenu

To access this menu, select Advanced on the menu bar and then Video Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 75 is used to configure the video features.

Table 75. Video Configuration Submenu

Feature	Options	Description
AGP Aperture Size	• **64 MB (default)** • 128 MB • 256 MB	Sets the aperture size for the AGP video controller.
Primary Video Adapter	• **AGP (default)** • PCI	Selects the primary video adapter to be used during boot.

4.5 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 76 is used to set passwords and security features.

Table 76. Security Menu

If no password entered previously:		
Feature	**Options**	**Description**
Supervisor Password Is	No options	Reports if a supervisor password is set.
User Password Is	No options	Reports if a user password is set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password (Note 1)	• **Yes (default)** • No	Clears the user password.
User Access Level (Note 2)	• Limited • No Access • View Only • **Full (default)**	Sets BIOS Setup Utility access rights for user level.
Unattended Start (Note 1)	• **Disabled (default)** • Enabled	*Enabled* allows the system to complete the boot process without a password. The keyboard remains locked until a password is entered. A password is required to boot from a diskette.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if a supervisor password has been set.

4.6 Power Menu

To access this menu, select Power from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				APM		
				ACPI		

The menu represented in Table 77 is for setting the power management features.

Table 77. Power Menu

Feature	Options	Description
APM	Select to display submenu	Sets the APM power management options.
ACPI	Select to display submenu	Sets the ACPI power management options.
After Power Failure	• Stay Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC power loss occurs. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before the power loss occurred. *Power On* restores power to the computer.
Wake on LAN	• **Stay Off (default)** • Power On	For onboard LAN and CNR only, determines how the system responds to a LAN wake-up event.
Wake On PME	• **Stay Off (default)** • Power On	Specifies how the system responds to a PCI power management event.
Wake On Modem Ring	• **Stay Off (default)** • Power On	Specifies how the computer responds to an incoming call on an installed modem when the power is off.

4.6.1 APM Submenu

To access this menu, select Power from the menu bar at the top of the screen and then APM.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				APM		
				ACPI		

The submenu represented in Table 78 is for setting the APM power options.

Table 78. APM Submenu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the APM power management feature.
Inactivity Timer	• Off • 1 Minute • 5 Minutes • 10 Minutes • **20 Minutes (default)** • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters APM standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby modes.

4.6.2 ACPI Submenu

To access this menu, select Power from the menu bar at the top of the screen and then ACPI.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				APM		
				ACPI		

The submenu represented in Table 79 is for setting the ACPI power options.

Table 79. ACPI Submenu

Feature	Options	Description
ACPI Suspend State	• **S1 State (default)** • S3 State	Specifies the ACPI sleep state.
Wake on LAN† from S5	• **Stay Off (default)** • Power On	In ACPI soft-off mode only, determines how the system responds to a LAN wake-up event.

4.7 Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit

Boot Device Priority
Hard Disk Drives
Removable Devices
ATAPI CD-ROM Drives

The menu represented in Table 80 is used to set the boot features and the boot sequence.

Table 80. Boot Menu

Feature	Options	Description
Quiet Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays an OEM graphic instead of POST messages.
Intel Rapid BIOS Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
USB Boot	• Disabled • **Enabled (default)**	Disables/enables booting to USB boot devices.
PXE Remote Boot	• **Disabled (default)** • Enabled	Disables/enables PXE remote boot. Note: When set to *Enabled*, you must reboot for the Intel Boot Agent device to be available in the Boot Device menu.
Boot Device Priority	Select to display submenu	Specifies the boot sequence from the available types of boot devices.
Hard Disk Drives	Select to display submenu	Specifies the boot sequence from the available hard disk drives.
Removable Devices	Select to display submenu	Specifies the boot sequence from the available removable devices.
ATAPI CD-ROM Drives	Select to display submenu	Specifies the boot sequence from the available ATAPI CD-ROM drives.

4.7.1 Boot Device Priority Submenu

To access this menu, select Boot on the menu bar and then Boot Device Priority.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 81 is for setting boot device priorities.

Table 81. Boot Device Priority Submenu

Feature	Options	Description
1st Boot Device 2nd Boot Device 3rd Boot Device 4th Boot Device	• Removable Dev. • Hard Drive • ATAPI CD-ROM • Intel® Boot Agent (Note) • Disabled	Specifies the boot sequence according to the device type. The computer will attempt to boot from up to five devices as specified here. Only one of the devices can be an IDE hard disk drive. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The default settings for the first through fourth boot devices are, respectively: • Removable Device • Hard Drive • ATAPI CD-ROM • Intel Boot Agent • Disabled

Note: The boot device identifier for Intel Boot Agent (IBA) may vary depending on the BIOS release.

4.7.2 Hard Disk Drives Submenu

To access this menu, select Boot on the menu bar and then Hard Disk Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 82 is for setting hard disk drive priority.

Table 82. Hard Disk Drives Submenu

Feature	Options	Description
1st Hard Disk Drive (Note)	Dependent on installed hard drives	Specifies the boot sequence from the available hard disk drives. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to twelve hard disk drives, the maximum number of hard disk drives supported by the BIOS.

4.7.3 Removable Devices Submenu

To access this menu, select Boot on the menu bar and then Removable Devices.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 83 is for setting removable device priority.

Table 83. Removable Devices Submenu

Feature	Options	Description
1st Removable Device (Note)	Dependent on installed removable devices	Specifies the boot sequence from the available removable devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four removable devices, the maximum number of removable devices supported by the BIOS.

4.7.4 ATAPI CD-ROM Drives Submenu

To access this menu, select Boot on the menu bar and then ATAPI CD-ROM Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 84 is for setting ATAPI CD-ROM drive priority.

Table 84. ATAPI CD-ROM Drives Submenu

Feature	Options	Description
1st ATAPI CDROM (Note)	Dependent on installed ATAPI CD-ROM drives	Specifies the boot sequence from the available ATAPI CD-ROM drives. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four ATAPI CD-ROM drives, the maximum number of ATAPI CD-ROM drives supported by the BIOS.

4.8 Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 85 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 85. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages....117
5.2 Port 80h POST Codes....119
5.3 Bus Initialization Checkpoints....123
5.4 Speaker....124
5.5 BIOS Beep Codes....124

5.1 BIOS Error Messages

Table 86 lists the error messages and provides a brief description of each.

Table 86. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive is not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No response from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.

continued

Table 86. BIOS Error Messages (continued)

Error Message	Explanation
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but could not be updated.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed, then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added, there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed, then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM / CMOS / PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card, often called a POST card (PCI, not ISA). The POST card can decode the port and display the contents on a medium such as a seven-segment display.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 87 defines the uncompressed INIT code checkpoints, Table 88 describes the boot block recovery code checkpoints, and Table 89 lists the run-time code uncompressed in F000 shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 87. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to checkpoint E0 for recovery. Otherwise go to checkpoint D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 88. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, and initialize DMA controller and interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed. Look for ATAPI (LS-120, Zip) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to checkpoint E9).

Table 89. Run-Time Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> keys during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found, then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 89. Run-Time Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wraparound at 0:0 and find the total system memory size.
46	Memory wraparound test done. Memory size calculation over. About to write patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to checkpoint 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to checkpoint 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started and will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful. CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 89. Run-Time Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID, and numlock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module run-time image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 89. Run-Time Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the run-time SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 90 describes the bus initialization checkpoints.

Table 90. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 91 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 91. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 92 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 92. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	Onboard system devices
2	ISA devices
3	EISA devices
4	ISA Plug and Play devices
5	PCI devices

5.4 Speaker

A 47 Ω inductive speaker is mounted on the desktop boards 850EMDV2/D850EMV2. The speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker on the desktop board D850EMD2	Figure 1, page 14
The location of the onboard speaker on the desktop board D850EMV2	Figure 2, page 15

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem as shown in Table 93. The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 93. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)