# Intel® Desktop Board D845GEBV2/D845GERG2

## Technical Product Specification

*October 2002*

*Order Number: C14584-001*

The Intel® Desktop Board D845GEBV2/D845GERG2 may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D845GEBV2/D845GERG2 Specification Update.

# Revision History

| Revision | Revision History | Date |
|---|---|---|
| -001 | First release of the Intel® Desktop Board D845GEBV2/D845GERG2 Technical Product Specification. | October 2002 |

This product specification applies to only standard Intel® Desktop Boards D845GEBV2 and D845GERG2 with BIOS identifier RG84510A.86A.

Changes to this specification will be published in the Intel Desktop Board D845GEBV2/D845GERG2 Specification Update before being incorporated into a revision of this document.

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# Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for these Intel® Desktop Boards: D845GEBV2 and D845GERG2. It describes the standard product and available manufacturing options.

## Intended Audience

The TPS is intended to provide detailed, technical information about the Desktop Boards D845GEBV2 and D845GERG2 and their components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

## What This Document Contains

| Chapter | Description |
|---|---|
| 1 | A description of the hardware used on the Desktop Boards D845GEBV2 and D845GERG2 |
| 2 | A map of the resources of the Desktop Boards |
| 3 | The features supported by the BIOS Setup program |
| 4 | The contents of the BIOS Setup program's menus and submenus |
| 5 | A description of the BIOS error messages, beep codes, and POST codes |

## Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

### Notes, Cautions, and Warnings

**NOTE**

*Notes call attention to important information.*

**INTEGRATOR'S NOTES**

*Integrator's notes are used to call attention to information that may be useful to system integrators.*

**CAUTION**

*Cautions are included to help you avoid damaging hardware or losing data.*

**WARNING**

*Warnings indicate conditions, which if not observed, can cause personal injury.*

## Other Common Notation

| | |
|---|---|
| # | Used after a signal name to identify an active-low signal (such as USBP0#) |
| (NxnX) | When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the Desktop Boards D845GEBV2 and D845GERG2, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area. |
| GB | Gigabyte (1,073,741,824 bytes) |
| GB/sec | Gigabytes per second |
| KB | Kilobyte (1024 bytes) |
| Kbit | Kilobit (1024 bits) |
| kbits/sec | 1000 bits per second |
| MB | Megabyte (1,048,576 bytes) |
| MB/sec | Megabytes per second |
| Mbit | Megabit (1,048,576 bits) |
| Mbit/sec | Megabits per second |
| xxh | An address or data value ending with a lowercase h indicates a hexadecimal value. |
| x.x V | Volts. Voltages are DC unless otherwise specified. |
| † | This symbol is used to indicate third-party brands and names that are the property of their respective owners. |

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# 1 Product Description

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## 1.1 Board Differences

This TPS describes these Intel® Desktop Boards: D845GEBV2 and D845GERG2. The Desktop Boards are identical with the exception of the items listed in Table 1.

**Table 1. Summary of Board Differences**

| | |
|---|---|
| **D845GEBV2** | • ATX Form Factor (12.00 inches by 8.20 inches)<br>• Six PCI bus connectors |
| **D845GERG2** | • microATX Form Factor (9.60 inches by 8.20 inches)<br>• Three PCI bus connectors |

**NOTE**

*Most of the illustrations in this document show only the Desktop Board D845GEBV2. When there are significant differences between the two Desktop Boards, illustrations of both boards are provided.*

# 1.2 Overview

## 1.2.1 Feature Summary

Table 2 summarizes the major features of the Desktop Boards D845GEBV2 and D845GERG2.

**Table 2. Feature Summary**

| | |
|---|---|
| **Form Factor** | D845GEBV2: ATX (12.00 inches by 8.20 inches)<br>D845GERG2: microATX (9.60 inches by 8.20 inches) |
| **Processor** | • Support for an Intel® Pentium® 4 processor in an mPGA478 socket with a 400/533 MHz system bus<br>• Support for an Intel® Celeron® processor in an mPGA478 socket with a 400 MHz system bus |
| **Memory** | • Two 184-pin DDR SDRAM Dual Inline Memory Module (DIMM) sockets<br>• Support for single-sided or double-sided DIMMs (DDR333/266)<br>• Support for up to 2 GB system memory<br>**NOTE:** *The Desktop Boards D845GEBV2/D845GERG2 have been designed to support DIMMs based on 512 Mbit technology for a maximum onboard capacity of up to 2 GB, but this technology has not been validated (currently validated up to 1.0 GB) on this board. Please refer to the following Intel web sites.*<br>*For the Desktop Board D845GEBV2:*<br>http://developer.intel.com/design/motherbd/bv2/bv2_mem.htm<br>*For the Desktop Board D845GERG2:*<br>*http://developer.intel.com/design/motherbd/rg2/rg2_mem.htm* |
| **Chipset** | Intel® 845GE Chipset, consisting of:<br>• Intel® 82845GE Graphics and Memory Controller Hub (GMCH)<br>• Intel® 82801DB I/O Controller Hub (ICH4)<br>• 4 Mbit Firmware Hub (FWH) |
| **Video** | • Intel® Extreme Graphics controller<br>• AGP connector supporting 1x, 2x, and 4x AGP cards (1.5 V only) or an AGP Digital Display (ADD) card<br>• Integrated retention mechanism |
| **Audio** | Audio subsystem for AC ‘97 processing using the Analog Devices AD1981B codec |
| **I/O Control** | SMSC LPC47M172 LPC Bus I/O controller |
| **USB** | Support for USB 2.0 devices |
| **Peripheral Interfaces** | • Up to six USB ports<br>• One serial port<br>• One parallel port<br>• Two IDE interfaces with UDMA 33, ATA-66/100 support<br>• One diskette drive interface<br>• PS/2† keyboard and mouse ports<br>• Three fan connectors |

continued

**Table 2. Feature Summary** (continued)

| | |
|---|---|
| **BIOS** | • Intel/AMI BIOS (resident in the 4 Mbit FWH)<br>• Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS |
| **Instantly Available PC Technology** | • Support for PCI Local Bus Specification Revision 2.2<br>• Suspend to RAM support<br>• Wake on PCI, CNR, RS-232, front panel, PS/2 devices, and USB ports |
| **Expansion Capabilities** | • D845GEBV2: Six PCI bus add-in card connectors (SMBus routed to PCI bus connector 2)<br>• D845GERG2: Three PCI bus add-in card connectors (SMBus routed to PCI bus connector 2) |

| For information about | Refer to |
|---|---|
| The board's compliance level with ACPI, Plug and Play, and SMBIOS | Section 1.5, page 20 |

## 1.2.2 Manufacturing Options

Table 3 describes the manufacturing options on the Desktop Boards D845GEBV2 and D845GERG2. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

**Table 3. Manufacturing Options**

| | |
|---|---|
| **CNR** | One Communication and Networking Riser (CNR) connector (slot shared with PCI bus connector 6 on the Desktop Board D845GEBV2 and with PCI bus connector 3 on the Desktop Board D845GERG2) |
| **Hardware Monitor Subsystem** | • Voltage sense to detect out of range power supply voltages<br>• Thermal sense to detect out of range thermal values<br>• Three fan sense inputs used to monitor fan activity<br>• Fan speed control<br>• Hardware monitoring and fan control ASIC |
| **10/100 LAN** | Intel® 82562ET 10/100 Mbit/sec Platform LAN Connect (PLC) device |
| **10/100/1000 LAN** | Intel® 82540EM 10/100/1000 Gigabit Ethernet Controller (Desktop Board D845GERG2 only) |

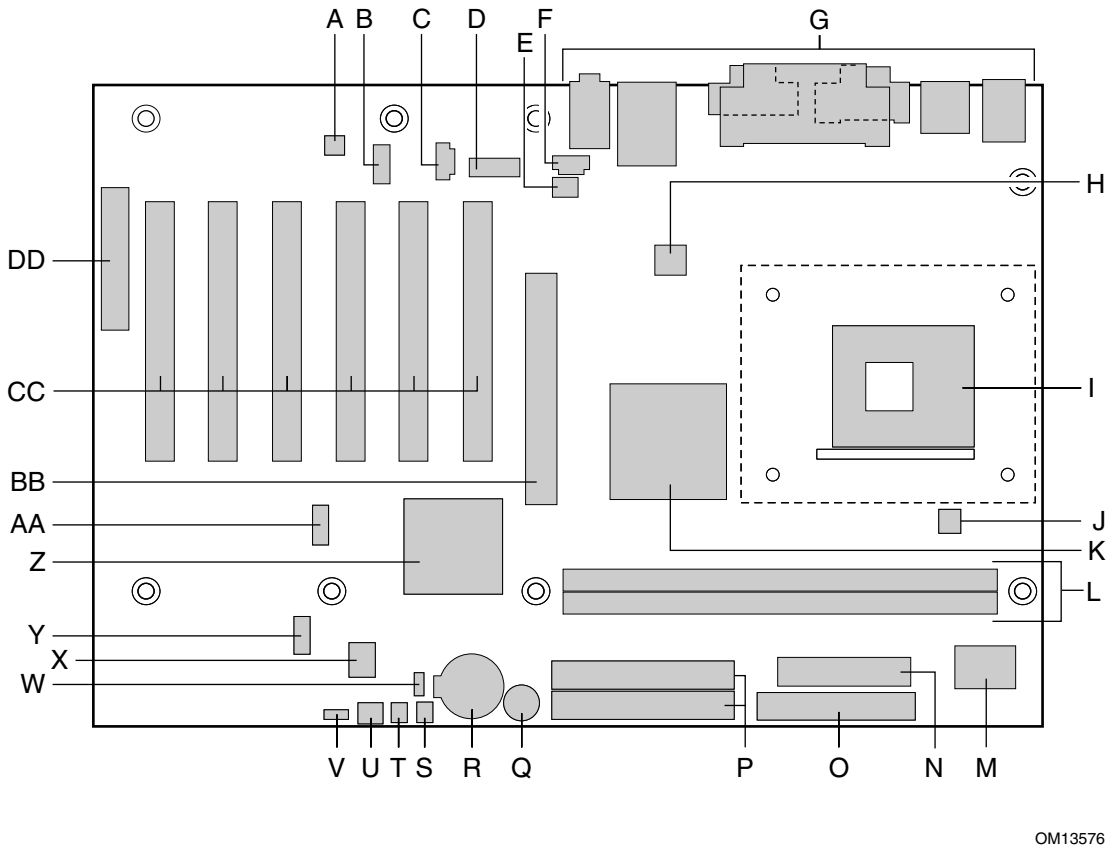
| For information about | Refer to |
|---|---|
| Available configurations for the Desktop Boards D845GEBV2 and D845GERG2 | Section 1.3, page 19 |

### INTEGRATOR'S NOTE

*The LAN and the CNR manufacturing options are mutually exclusive.*

## 1.2.3 Board Layouts

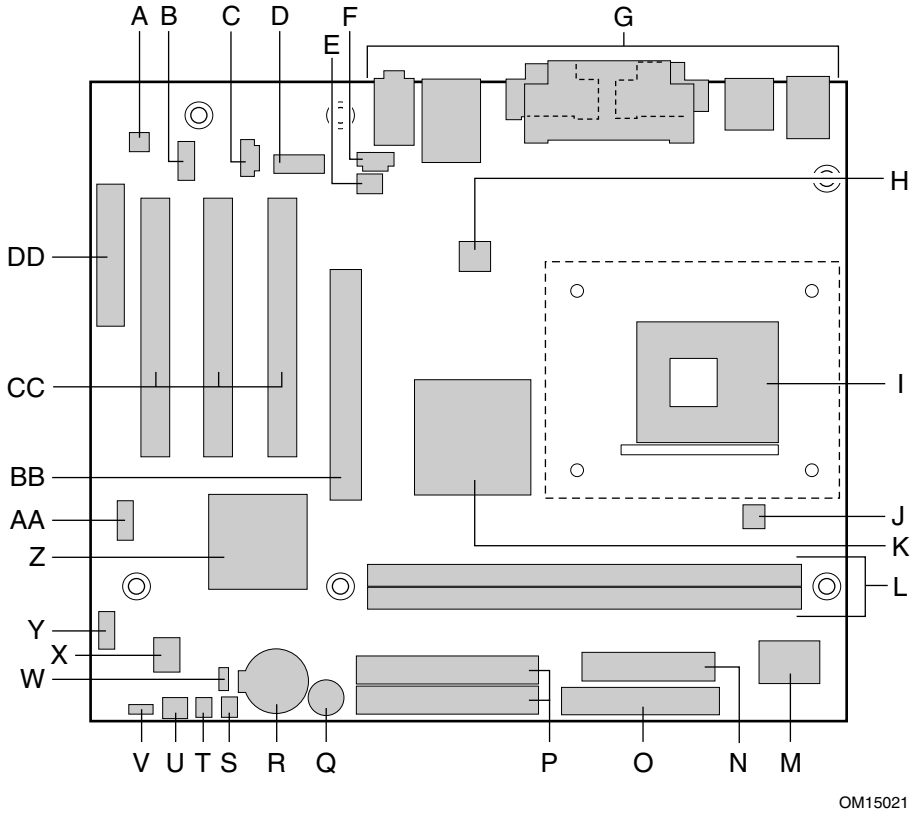
Figure 1 shows the location of the major components on the Desktop Board D845GEBV2.




| | | | |
|---|---|---|---|
| A | Audio codec | P | IDE connectors |
| B | Front panel audio connector | Q | Speaker |
| C | Auxiliary line-in connector | R | Battery |
| D | Intel 82562ET 10/100 Mbit/sec (PLC) device (Optional) | S | SCSI LED connector |
| E | Rear chassis fan connector | T | Chassis intrusion connector |
| F | ATAPI CD-ROM connector | U | Front chassis fan connector |
| G | Back panel connectors | V | BIOS Setup configuration jumper block |
| H | +12V power connector (ATX12V) | W | Auxiliary front panel power LED connector |
| I | mPGA478 processor socket | X | 4 Mbit Firmware Hub (FWH) |
| J | Processor fan connector | Y | Front panel connector |
| K | Intel 82845GE Graphics and Memory Controller Hub (GMCH) | Z | Intel 82801DB I/O Controller Hub (ICH4) |
| L | DIMM sockets | AA | Front panel USB connector |
| M | I/O Controller | BB | AGP connector |
| N | Power connector | CC | PCI bus add-in card connectors |
| O | Diskette drive connector | DD | CNR connector (optional) |

**Figure 1. Desktop Board D845GEBV2 Components**

Figure 2 shows the location of the major components on the Desktop Board D845GERG2.

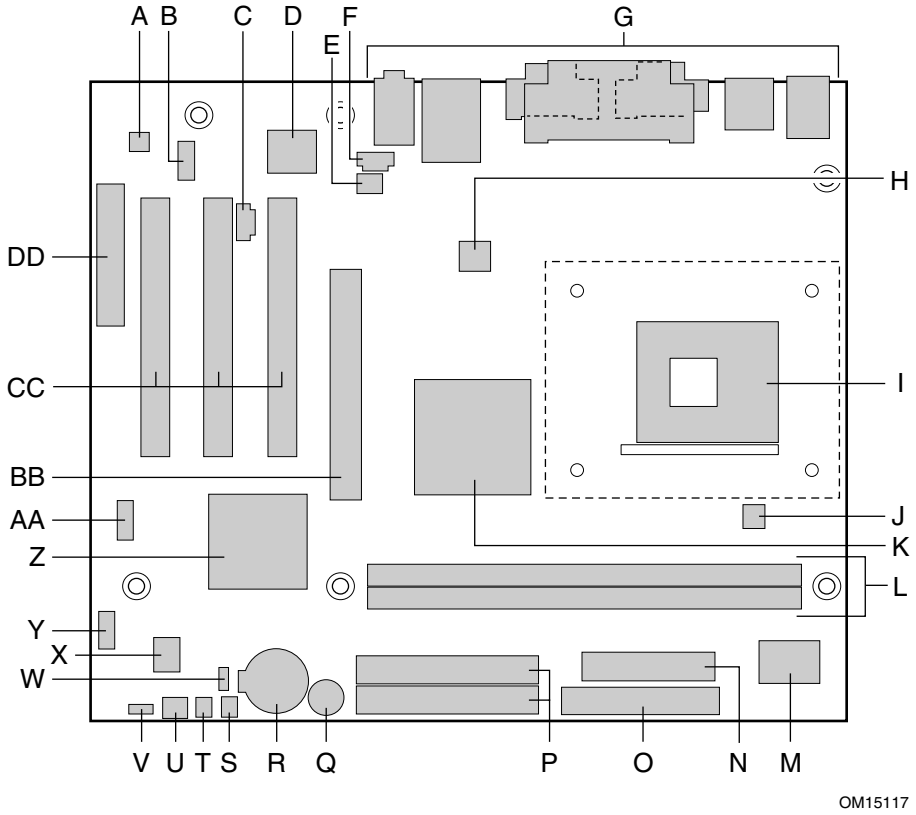



| | | | |
|---|---|---|---|
| A | Audio codec | P | IDE connectors |
| B | Front panel audio connector | Q | Speaker |
| C | Auxiliary line-in connector | R | Battery |
| D | Intel 82562ET 10/100 Mbit/sec (PLC) device (Optional) | S | SCSI LED connector |
| E | Rear chassis fan connector | T | Chassis intrusion connector |
| F | ATAPI CD-ROM connector | U | Front chassis fan connector |
| G | Back panel connectors | V | BIOS Setup configuration jumper block |
| H | +12V power connector (ATX12V) | W | Auxiliary front panel power LED connector |
| I | mPGA478 processor socket | X | 4 Mbit Firmware Hub (FWH) |
| J | Processor fan connector | Y | Front panel connector |
| K | Intel 82845GE Graphics and Memory Controller Hub (GMCH) | Z | Intel 82801DB I/O Controller Hub (ICH4) |
| L | DIMM sockets | AA | Front panel USB connector |
| M | I/O Controller | BB | AGP connector |
| N | Power connector | CC | PCI bus add-in card connectors |
| O | Diskette drive connector | DD | CNR connector (optional) |

**Figure 2. Desktop Board D845GERG2 Components**

Figure 3 shows the location of the major components on the Desktop Board D845GERG2 that includes the Gigabit Ethernet LAN option. The callouts in Figure 2 and Figure 3 are identical, except as follows:

- In Figure 3, the auxiliary line in connector (callout "C") has been moved
- In Figure 3, callout "D" highlights the Intel 82540EM Gigabit Ethernet LAN Controller




| | | | |
|---|---|---|---|
| A | Audio codec | P | IDE connectors |
| B | Front panel audio connector | Q | Speaker |
| C | Auxiliary line-in connector | R | Battery |
| D | Intel 82540EM Gigabit Ethernet LAN Controller | S | SCSI LED connector |
| E | Rear chassis fan connector | T | Chassis intrusion connector |
| F | ATAPI CD-ROM connector | U | Front chassis fan connector |
| G | Back panel connectors | V | BIOS Setup configuration jumper block |
| H | +12V power connector (ATX12V) | W | Auxiliary front panel power LED connector |
| I | mPGA478 processor socket | X | 4 Mbit Firmware Hub (FWH) |
| J | Processor fan connector | Y | Front panel connector |
| K | Intel 82845GE GMCH | Z | Intel 82801DB I/O Controller Hub (ICH4) |
| L | DIMM sockets | AA | Front panel USB connector |
| M | I/O Controller | BB | AGP connector |
| N | Power connector | CC | PCI bus add-in card connectors |
| O | Diskette drive connector | DD | CNR connector (optional) |

**Figure 3. Desktop Board D845GERG2 Components (with Gigabit Ethernet LAN option)**

## 1.2.4 Block Diagrams

Figure 4 is a block diagram of the major functional areas of the Desktop Boards D845GEBV2 and D845GERG2. See Figure 7 on page 33 for USB port routing.

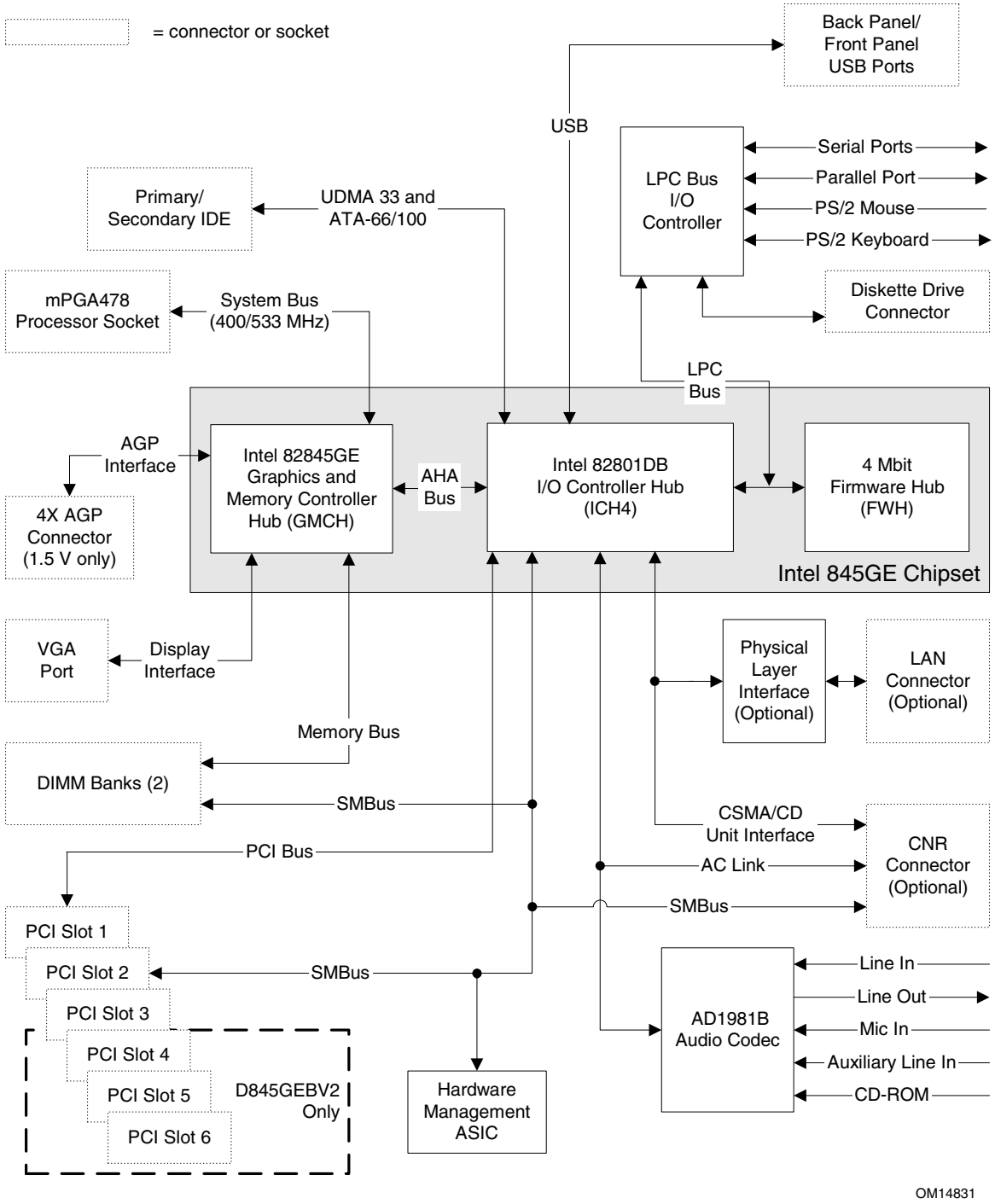



**Figure 4. Block Diagram**

Figure 5 is a block diagram of the major functional areas of the Desktop Board D845GEBV2 with the Gigabit Ethernet LAN option. See Figure 7 on page 33 for USB port routing.

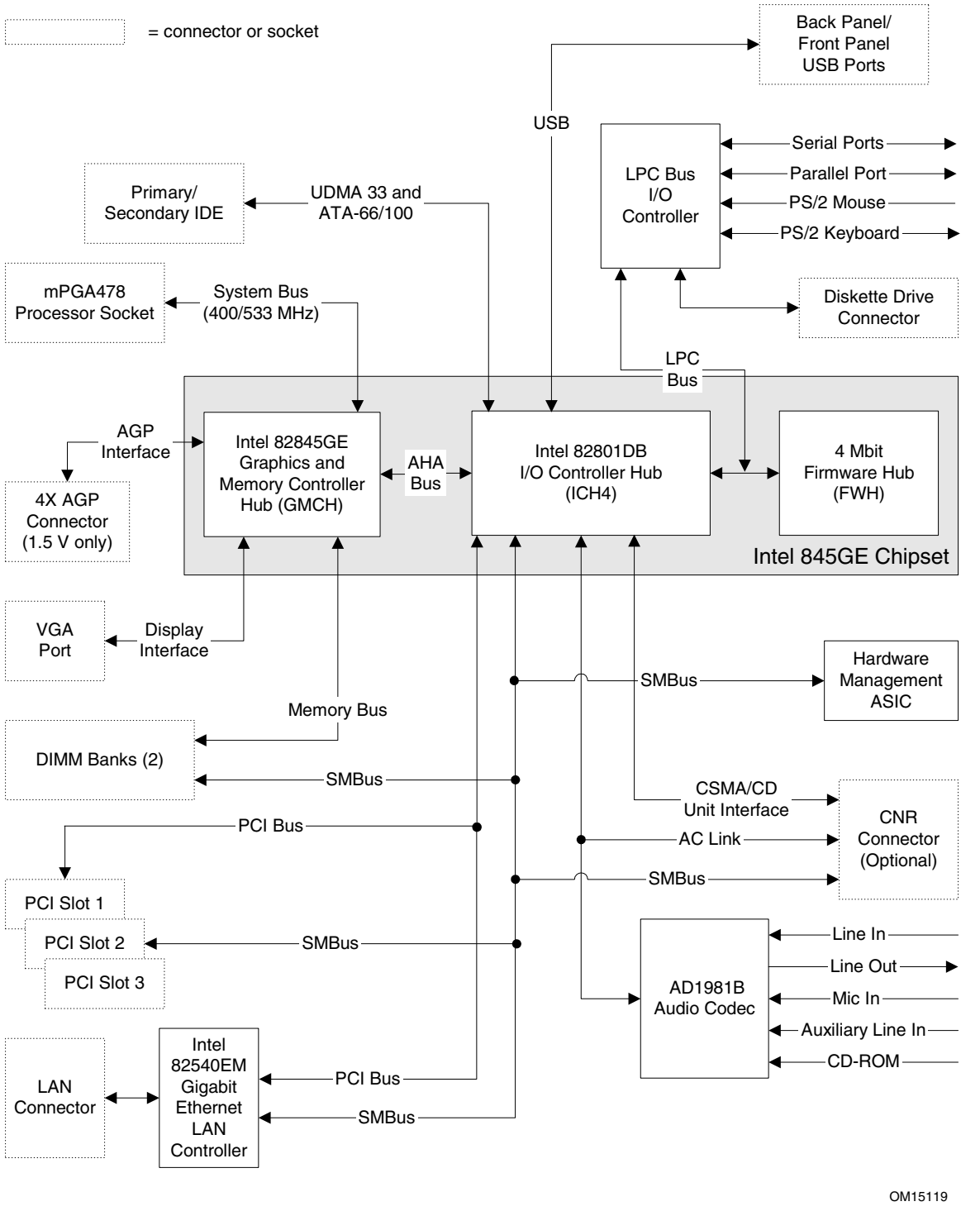



**Figure 5. Block Diagram of the Desktop Board D845GEBV2 with the Gigabit Ethernet LAN option**

## 1.3 Online Support

| To find information about… | Visit this World Wide Web site: |
|---|---|
| Intel Desktop Boards D845GEBV2 and D845GERG2 under “Desktop Board Products” or “Desktop Board Support” | http://www.intel.com/design/motherbd<br>http://support.intel.com/support/motherboards/desktop |
| Available configurations for the Desktop Board D845GEBV2 | http://developer.intel.com/design/motherbd/bv2/bv2_available.htm |
| Available configurations for the Desktop Board D845GERG2 | http://developer.intel.com/design/motherbd/rg2/rg2_available.htm |
| Processor data sheets | http://www.intel.com/design/litcentr |
| ICH4 addressing | http://developer.intel.com/design/chipsets/datashts |
| Custom splash screens | http://intel.com/design/motherbd/gen_indx.htm |
| Audio software and utilities | http://www.intel.com/design/motherbd |
| LAN software and drivers | http://www.intel.com/design/motherbd |

## 1.4 Operating System Support

The Desktop Boards D845GEBV2 and D845GERG2 support drivers for all of the onboard hardware and subsystems under the following operating systems:

- Windows† XP
- Windows ME
- Windows 2000
- Windows NT† 4.0
- Microsoft Windows 98 SE

| For information about | Refer to |
|---|---|
| Supported drivers | Section 1.3 |

### NOTE

*Third party vendors may offer other drivers.*

### NOTE

*USB 2.0 support has been tested with Windows 2000 and Windows XP drivers and is not currently supported by any other operating system.*

## 1.5 Design Specifications

Table 4 lists the specifications applicable to the Desktop Boards D845GEBV2 and D845GERG2.

**Table 4. Specifications**

| Reference Name | Specification Title | Version, Revision Date, and Ownership | The information is available from… |
|---|---|---|---|
| AC '97 | *Audio Codec '97* | Revision 2.2, September 2000, Intel Corporation. | ftp://download.intel.com/ial/scalableplatforms/ac97r22.pdf |
| ACPI | *Advanced Configuration and Power Interface Specification* | Version 2.0, July 27, 2000, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Limited, and Toshiba Corporation. | http://www.acpi.info/spec.htm |
| AGP | *Accelerated Graphics Port Interface Specification* | Revision 2.0, May 4, 1998, Intel Corporation. | http://www.agpforum.org/specs_specs.htm |
| AMI BIOS | *AMIBIOS Desktop Core 8.0* | AMIBIOS 8.0, 2001, American Megatrends, Inc. | http://www.ami.com/support/doc/amibios8.pdf |
| ATA/ ATAPI-5 | *Information Technology-AT Attachment with Packet Interface - 5* (ATA/ATAPI-5) | Revision 3, February 29, 2000, Contact: T13 Chair, Seagate Technology. | http://www.t13.org |
| ATX | *ATX Specification* | Version 2.03, December 1998, Intel Corporation. | http://www.formfactors.org/developer/specs/atx/atxspecs.htm |
| ATX12V | *ATX/ATX12V Power Supply Design Guide* | Version 1.2, August 2000, Intel Corporation. | http://www.formfactors.org/developer/specs/atx/atxspecs.htm |
| BIS | *Boot Integrity Services (BIS) Application Programming Interface (API)* | Version 1.0, August 4, 1999, Intel Corporation. | http://www.intel.com/labs/manage/wfm/wfmspecs.htm |
| CNR | *Communication and Network Riser (CNR) Specification* | Revision 1.2, November 8, 2001, Intel Corporation. | http://developer.intel.com/technology/cnr/index.htm |

continued

**Table 4. Specifications** (continued)

| Reference Name | Specification Title | Version, Revision Date and Ownership | The information is available from… |
|---|---|---|---|
| DDR SDRAM | *Double Data Rate (DDR) SDRAM Specification* | Version 1.0, June 2000, JEDEC Solid State Technology Association. | http://www.jedec.org/ |
| | *Design Specification for a 184 Pin DDR Unbuffered DIMM* | Revision 1.0, October 2001, JEDEC Solid State Technology Association. | http://www.jedec.org/ |
| | *Intel® JEDEC DDR 200/266 Unbuffered DIMM Specification Addendum* | Revision 0.9, September 27, 2001, Intel Corporation. | http://developer.intel.com/technology/memory/index.htm |
| EHCI | *Enhanced Host Controller Interface Specification for Universal Serial Bus* | Revision 1.0, March 12, 2002, Intel Corporation. | http://developer.intel.com/technology/usb/download/ehci-r10.pdf |
| EPP | *IEEE Std 1284.1-1997* (Enhanced Parallel Port) | Version 1.7, 1997, Institute of Electrical and Electronic Engineers. | http://standards.ieee.org/reading/ieee/std_public/description/busarch/1284.1-1997_desc.html |
| El Torito | *Bootable CD-ROM Format Specification* | Version 1.0, January 25, 1995, Phoenix Technologies Limited and International Business Machines Corporation. | http://www.phoenix.com/PlatSS/products/specs.html |
| Front Panel | *Front Panel I/O Connectivity Design Guide* | Version 1.0, October 2000, Intel Corporation. | http://www.formfactors.org/formfactors/front_panel_io.htm |
| LPC | *Low Pin Count Interface Specification* | Revision 1.0, September 29, 1997, Intel Corporation. | http://www.intel.com/design/chipsets/industry/lpc.htm |
| MicroATX | *microATX Motherboard Interface Specification* | Version 1.0, December 1997, Intel Corporation. | http://www.formfactors.org/developer/specs/microatx/microatxspecs.htm |
| PCI | *PCI Local Bus Specification* | Revision 2.2, December 18, 1998, PCI Special Interest Group. | http://www.pcisig.com/specifications |
| | *PCI Bus Power Management Interface Specification* | Revision 1.1, December 18, 1998, PCI Special Interest Group. | http://www.pcisig.com/specifications |
| Plug and Play | *Plug and Play BIOS Specification* | Version 1.0a, May 5, 1994, Compaq Computer Corporation, Phoenix Technologies Limited, and Intel Corporation. | http://www.microsoft.com/hwdev/tech/PnP/default.asp |

continued

**Table 4. Specifications** (continued)

| Reference Name | Specification Title | Version, Revision Date and Ownership | The information is available from… |
|---|---|---|---|
| PXE | *Preboot Execution Environment* | Version 2.1,<br>September 20, 1999,<br>Intel Corporation. | ftp://download.intel.com/ial/wfm/pxespec.pdf |
| SFX | *SFX/SFX12V Power Supply Design Guide* | Version 2.0,<br>May 2001,<br>Intel Corporation. | http://www.formfactors.org/developer/specs/sfx/sfx12v.pdf |
| SMBIOS | *System Management BIOS* | Version 2.3.1,<br>March 16, 1999,<br>American Megatrends Incorporated,<br>Award Software International Incorporated,<br>Compaq Computer Corporation,<br>Dell Computer Corporation,<br>Hewlett-Packard Company,<br>Intel Corporation,<br>International Business Machines Corporation,<br>Phoenix Technologies Limited,<br>and SystemSoft Corporation. | http://www.dmtf.org/download/standards/DSP0119.pdf |
| UHCI | *Universal Host Controller Interface Design Guide* | Revision 1.1,<br>March 1996,<br>Intel Corporation. | http://www.usb.org/developers/docs.html |
| USB | *Universal Serial Bus Specification* | Revision 2.0,<br>April 27, 2000,<br>Compaq Computer Corporation,<br>Hewlett-Packard Company,<br>Lucent Technologies Inc.,<br>Intel Corporation,<br>Microsoft Corporation,<br>NEC Corporation, and<br>Koninklijke Philips Electronics N.V. | http://www.usb.org/developers/docs.html |
| WfM | *Wired for Management Baseline* | Version 2.0,<br>December 18, 1998,<br>Intel Corporation. | http://www.intel.com/labs/manage/wfm/wfmspecs.htm |

# 1.6 Processor

## NOTE

*Refer to Thermal Considerations (Section 2.12, page 81) for important information when using an Intel Pentium 4 processor operating above 2.80 GHz with this Intel desktop board.*

## CAUTION

*Use only the processors listed below. Use of unsupported processors can damage the board, the processor, and the power supply. See Intel's World Wide Web site for the most up-to-date list of supported processors for these boards.*

The board provides an mPGA478 processor socket. Table 5 lists the supported processors. All supported onboard memory can be cached. See the processor's data sheet for cachability limits.

**Table 5. Supported Processors**

| Processor Family | Designation | System Bus Frequency | L2 Cache Size |
|---|---|---|---|
| Pentium® 4 processor | 2.80, 2.66, 2.53, 2.40B, and 2.26 GHz | 533 MHz | 512 KB |
| Pentium 4 processor | 2.60, 2.50, 2.40, 2.20, 2A, 1.80A, and 1.60A GHz | 400 MHz | 512 KB |
| Pentium 4 processor | 2, 1.90, 1.80, 1.70, 1.60, 1.50, and 1.40 GHz | 400 MHz | 256 KB |
| Celeron® processor | 1.80, and 1.70 GHz | 400 MHz | 128 KB |

## INTEGRATOR'S NOTES

- *Use only ATX12V-compliant power supplies with the Desktop Board D845GEBV2 and only ATX12V- or SFX12V-compliant power supplies with the Desktop Board D845GERG2. ATX12V and SFX12V power supplies have an additional power lead that provides required supplemental power for the processor. Always connect the 20-pin and 4-pin leads of ATX12V and SFX12V power supplies to the corresponding connectors on the desktop board, otherwise the board will not boot. Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.*
- *Refer to Table 7 on page 25 for a list of supported system bus frequency and memory speed combinations.*

| For information about | Refer to |
|---|---|
| Processor support | Section 1.3, page 19 |
| Power supply connectors | Section 2.8.2.2, page 62 |

## 1.7 System Memory

The Desktop Boards D845GEBV2 and D845GERG2 both have two DIMM sockets and support the following memory features:

- 2.5 V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts
- Unbuffered, unregistered single-sided or double-sided DIMMs
- Maximum total system memory: 2 GB; minimum total system memory: 64 MB
- DDR333/266 MHz SDRAM DIMMs only
- Serial Presence Detect (SPD)
- Suspend to RAM

### CAUTION

*Do not use ECC DIMMs with these Desktop Boards. Using ECC DIMMs could damage the Desktop Board.*

### INTEGRATOR'S NOTES

- *Registered DIMMs are not supported.*
- *Double-sided x16 DIMMs are not supported.*
- *Remove the AGP video card before installing or upgrading memory to avoid interference with the memory retention mechanism.*
- *These Desktop Boards have been designed to support DIMMs based on 512 Mbit technology for a maximum onboard capacity of up to 2 GB, but this technology has not been validated (currently validated up to 1.0 GB) on this board. Please refer to the following Intel web sites for the latest lists of tested memory:*
  *For the Desktop Board D845GEBV2:*
  http://developer.intel.com/design/motherbd/bv2/bv2_mem.htm
  *For the Desktop Board D845GERG2:*
  http://developer.intel.com/design/motherbd/rg2/rg2_mem.htm

### NOTE

*To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance.*

| For information about | Refer to |
|---|---|
| Obtaining DDR SDRAM specifications | Section 1.5, page 20 |
| Obtaining the PC Serial Presence Detect (SPD) Specification | Section 1.5, page 20 |

Table 6 lists the supported DDR DIMM configurations.

**Table 6. Supported DDR DIMM Configurations**

| DIMM Capacity | Configuration (Note 1) | DDR SDRAM Density | DDR SDRAM Organization Front-side/Back-side | Number of DDR SDRAM Devices |
|---|---|---|---|---|
| 64 MB | SS | 64 Mbit | 8 M x 8/empty | 8 |
| 64 MB | SS | 128 Mbit | 8 M x 16/empty | 4 |
| 128 MB | DS | 64 Mbit | 8 M x 8/8 M x 8 | 16 |
| 128 MB | SS | 128 Mbit | 16 M x 8/empty | 8 |
| 128 MB | SS | 256 Mbit | 16 M x 16/empty | 4 |
| 256 MB | DS | 128 Mbit | 16 M x 8/16 M x 8 | 16 |
| 256 MB | SS | 256 Mbit | 32 M x 8/empty | 8 |
| 256 MB | SS | 512 Mbit | 32 M x 16/empty | 4 |
| 512 MB | DS | 256 Mbit | 32 M x 8/32 M x 8 | 16 |
| 512 MB | SS | 512 Mbit | 64 M x 8 | 8 |
| 1024 MB (Note 2) | DS | 512 Mbit | 64 M x 8/64 M x 8 | 16 |

Notes:
1. In this column, “DS” refers to double-sided memory modules (containing DDR SDRAM devices on both sides) and “SS” refers to single-sided memory modules (containing DDR SDRAM devices on only one side).
2. DDR333 1 GB (1024 MB) DIMMs have not been validated with these desktop boards.

Table 7 lists the supported system bus frequency / memory speed configurations.

**Table 7. Supported System Bus Frequency / Memory Speed Combinations**

| To use this type of DIMM… | The processor’s system bus frequency must be… |
|---|---|
| DDR333 | 533 MHz |
| DDR266 | 533 MHz or 400 MHz |

## 1.8 Intel® 845GE Chipset

The Intel 845GE chipset consists of the following devices:

- Intel 82845GE Graphics and Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- Intel 82801DB I/O Controller Hub (ICH4) with AHA bus
- Firmware Hub (FWH)

The GMCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture interface. The ICH4 is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS. The component combination provides the chipset interfaces as shown in Figure 6.

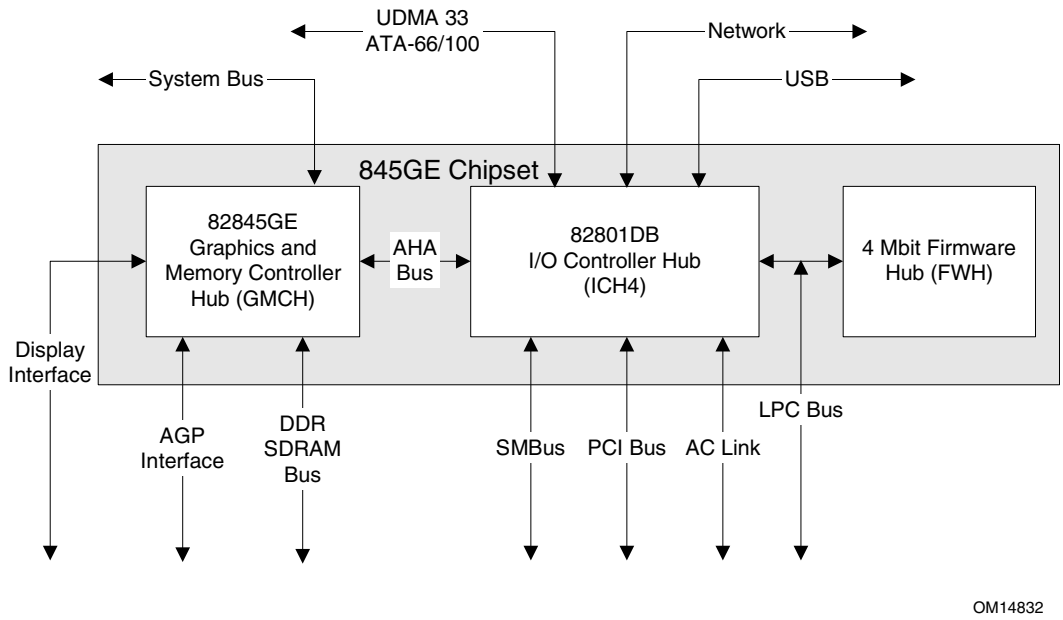



**Figure 6. Intel 845GE Chipset Block Diagram**

| For information about | Refer to |
|---|---|
| The Intel 845GE chipset | http://developer.intel.com |
| Resources used by the chipset | Chapter 2 |

## 1.8.1 Intel 845GE Graphics Subsystem

The Intel 845GE chipset contains two separate, mutually exclusive graphics options. Either the Intel Extreme Graphics controller (contained within the 82845GE GMCH) is used, or an AGP add-in card can be used. When an AGP add-in card is installed, the Intel Extreme Graphics controller is disabled.

### 1.8.1.1 Intel® Extreme Graphics Controller

The Intel Extreme Graphics controller features the following:

- Integrated graphics controller
  - 32 bpp (Bits Per Pixel) graphics engine
  - 266 MHz core frequency
  - 256-bit internal data path for 2-D and 3-D graphics
  - Motion video acceleration
- 3-D graphics visual and texturing enhancement
- Display
  - Integrated 24-bit 350 MHz RAMDAC
  - DDC2B compliant interface
- Video
  - Dual monitor synchronous display
  - Hardware motion compensation for software MPEG2 decode
  - Two multiplexed DVO port interfaces with 165 MHz pixel clocks using an AGP Digital Display (ADD) card
- Dynamic Video Memory Technology (DVMT) support up to 64 MB

| For information about | Refer to |
|---|---|
| DVMT | Section 1.8.1.2, page 31 |

**INTEGRATOR'S NOTE**

*EMC emission testing of high-speed video was performed on this Desktop Board using scrolling H's displayed on the video monitor in accordance with ANSI C63.4-2000 documentation. The scrolling H's are displayed using the following font sizes:*

- *For video resolutions greater than 1600 x 1200 (including 2048 x 1536 and 1920 x 1440), a font size of 200% is used.*
- *For a 1600 x 1200 video resolution, a 150% font size is used.*
- *For resolutions less than 1600 x 1200, a normal or large font size is used.*

*All available resolutions are tested using the highest available color depth and monitor refresh rate.*

Table 8 lists the Direct Draw supported modes.

**Table 8. Direct Draw Supported Modes**

| Resolution | Color Palette | Refresh Frequency (Hz) | Notes |
|---|---|---|---|
| 320 x 200 | 256 colors | 70 | Y |
| | 64 K colors | 70 | 3 |
| | 16 M colors | 70 | 3 |
| 320 x 240 | 256 colors | 70 | Y |
| | 64 K colors | 70 | 3 |
| | 16 M colors | 70 | 3 |
| 352 x 480 | 256 colors | 70 | Y |
| | 64 K colors | 70 | 3 |
| | 16 M colors | 70 | 3 |
| 352 x 576 | 256 colors | 70 | Y |
| | 64 K colors | 70 | 3 |
| | 16 M colors | 70 | 3 |
| 400 x 300 | 256 colors | 70 | Y |
| | 64 K colors | 70 | 3 |
| | 16 M colors | 70 | 3 |
| 512 x 384 | 256 colors | 70 | Y |
| | 64 K colors | 70 | 3 |
| | 16 M colors | 70 | 3 |
| 640 x 400 | 256 colors | 70 | Y |
| | 64 K colors | 70 | 3 |
| | 16 M colors | 70 | 3 |

Notes: Y = Supported in driver without Direct3D† and OpenGL†
3 = Direct3D and OpenGL

Table 9 lists the video BIOS video modes supported by the graphics subsystem.

**Table 9. Video BIOS Video Modes Supported for Analog CRTs**

| Resolution | Color Palette | Available Refresh Frequencies (Hz) | Notes |
|---|---|---|---|
| 320 x 200 | 16 colors | 70 | T, G, B |
| | 256 colors | 70 | G, B |
| 320 x 350 | 16 colors | 70 | T, B |
| 360 x 400 | 16 colors | 70 | T, B |
| 640 x 200 | 16 colors | 70 | T, G, B |
| 640 x 350 | 16 colors | 70 | T, G, B |
| 640 x 480 | 16 colors | 60 | G, B |
| | 256 colors | 60, 75, 85 | G, B, L |
| | 64 K colors | 60, 75, 85 | G, B, L |
| | 16 M colors | 60, 75, 85 | G, B, L |
| 720 x 400 | 16 colors | 70 | T, B |
| 800 x 600 | 256 colors | 60, 75, 85 | G, B, L |
| | 64 K colors | 60, 75, 85 | G, B, L |
| | 16 M colors | 60, 75, 85 | G, B, L |
| 1024 x 768 | 256 colors | 60, 75, 85 | G, B, L |
| | 64 K colors | 60, 75, 85 | G, B, L |
| | 16 M colors | 60, 75, 85 | G, B, L |
| 1056 x 350 | 16 colors | 70 | T, B |
| 1056 x 400 | 16 colors | 70 | T, B |
| 1056 x 480 | 16 colors | 70 | T, B |
| 1280 x 1024 | 256 colors | 60, 75, 85 | G, B, L |
| | 64 K colors | 60, 75, 85 | G, B, L |
| | 16 M colors | 60, 75, 85 | G, B, L |
| 1600 x 1200 | 256 colors | 60, 75, 85 | G, B, L |
| | 64 K colors | 60, 75, 85 | G, B, L |
| | 16 M colors | 60, 75, 85 | G, B, L |
| 1920 x 1440 | 256 colors | 60, 75 | G, B, L |
| | 64 K colors | 60, 75 | G, B, L |

Notes: T = Text mode
G = Graphics mode
B = Banked addressing mode
L = Linear addressing mode

Table 10 lists the supported configuration modes of the graphics subsystem.

**Table 10. Supported Configuration Modes**

| Resolution | Available Refresh Frequencies (Hz) | Supported bpp Configuration Mode (see Table 11 for more information) |
|---|---|---|
| 640 x 480 | 60, 72, 75, 85, 100, 120 | 6 |
| 800 x 600 | 60, 72, 75, 85, 100, 120 | 6 |
| 1024 x 768 | 60, 70, 75, 85, 100 | 6 |
| 1024 x 768 | 120 | 5 |
| 1152 x 864 | 60, 75, 85 | 6 |
| 1152 x 864 | 100 | 5 |
| 1280 x 720 | 60, 75, 85 | 6 |
| 1280 x 720 | 100 | 5 |
| 1280 x 768 | Reduced blanking | 6 |
| 1280 x 960 | 60, 75 | 6 |
| 1280 x 960 | 85 | 5 |
| 1280 x 1024 | 60 | 6 |
| 1280 x 1024 | 75 | 5 |
| 1280 x 1024 | 85, 100 | 4 |
| 1280 x 1024 | 120 | 3 |
| 1400 x 1050 | 60 | 6 |
| 1600 x 900 | 60 | 6 |
| 1600 x 900 | 75, 85 | 4 |
| 1600 x 900 | 100 | 3 |
| 1600 x 1200 | 60 | 4 |
| 1600 x 1200 | 75, 85, 100 | 3 |
| 1856 x 1392 | 60, 75 | 3 |
| 1920 x 1080 | 60 | 4 |
| 1920 x 1080 | 75, 85 | 3 |
| 1920 x 1200 | 60 | 3 |
| 1920 x 1440 | 60, 75 | 3 |
| 2048 x 1536 | 60 | 3 |

Table 11 describes the bpp configuration mode values referenced in Table 10. In Table 11, assume that for each configuration mode number, the features of all lower numbers are also supported. For example, if the supported configuration mode is 4, then modes 1 through 3 are also supported. DVD consists of both the overlay engine as well as the MPEG decoding; both are necessary for DVD playback.

**Table 11. Details of bpp Configuration Modes**

| Configuration Mode Number | Description |
|---|---|
| 6 | 32 bpp (16 M colors) with DVD (Overlay + MPEG decode) On |
| 5 | 16 bpp (64 K colors) with DVD On |
| 4 | 32 bpp (16 M colors) with DVD Off |
| 3 | 16 bpp (64 K colors) with DVD Off |
| 2 | 8 bpp (256 colors) with DVD On |
| 1 | 8 bpp (256 colors) with DVD off |

| For information about | Refer to |
|---|---|
| Obtaining graphics software and utilities | Section 1.3, page 19 |

### 1.8.1.2 Dynamic Video Memory Technology (DVMT)

DVMT enables enhanced graphics and memory performance through Direct AGP, and highly efficient memory utilization. DVMT ensures the most efficient use of available system memory (up to 64 MB) for maximum 2-D/3-D graphics performance.

DVMT uses a portion of system physical memory (as set in the BIOS Setup program) for compatibility with legacy applications. An example of this would be when using VGA graphics under DOS. Once loaded, the operating system and graphics drivers allocate the buffers needed for performing graphics functions.

**NOTE**

*The use of DVMT requires operating system driver support.*

| For information about | Refer to |
|---|---|
| Obtaining the DVMT white paper | http://developer.intel.com/design/chipsets/845g/ |

### 1.8.1.3 Zone Rendering Technology (ZRT)

The Intel Extreme Graphics Controller supports Zone Rendering Technology (ZRT). ZRT is a process by which the screen is divided into several zones. Each zone is completely cached and rendered on chip before being written to the frame buffer. The benefits of ZRT include the following:

- Increased memory efficiency via better localization of data
- Increased on-chip processing speed due to decreased wait time for data
- Increased effective pixel fill rates

- Increased headroom for larger resolution and color depth
- Reduced power as a result of decreased memory bandwidth
- Reduction in depth and color bandwidth associated with conventional rendering

| For information about | Refer to |
|---|---|
| Obtaining the Zone Rendering white paper | http://developer.intel.com/design/chipsets/845g/ |

### 1.8.1.4 AGP Connector

The AGP connector supports either:

- 1x, 2x, or 4x AGP add-in cards with 1.5 V I/O
- AGP Digital Display (ADD) cards

| For information about | Refer to |
|---|---|
| Obtaining the *Accelerated Graphics Port Interface Specification* | Section 1.5, page 20 |

### INTEGRATOR'S NOTES

- *Install memory in the DIMM sockets prior to installing the AGP video card to avoid interference with the memory retention mechanism.*
- *The AGP connector is keyed for 1.5 V AGP cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.*

### 1.8.1.5 AGP Digital Display (ADD) Card Support

The GMCH routes two 12-bit multiplexed DVO ports that are each capable of driving a 165 MHz pixel clock to the AGP connector. The DVO ports can be paired for dual channel mode. In dual channel mode, the GMCH is capable of driving a 24-bit 330 MHz pixel clock. When an AGP add-in card is used, the Intel Extreme Graphics controller is disabled and the AGP connector operates in AGP mode. When an ADD card is detected, the Intel Extreme Graphics controller is enabled and the AGP connector is configured for DVO mode. DVO mode enables the DVO ports to be accessed by an ADD card. ADD cards can support up to two display devices with the following configurations:

- TV-Out
- Transition Minimized Differential Signaling (TMDS)
- Low Voltage Differential Signaling (LVDS)
- Single device operating in dual channel mode

### INTEGRATOR'S NOTES

- *Synchronous display is not supported when one of the display devices is a TV.*
- *Digital Visual Interface (DVI) support is present only when an ADD card is installed.*

## 1.8.2 USB

The Desktop Boards support up to six USB 2.0 ports and fully support UHCI and EHCI and use UHCI- and EHCI-compatible drivers. For more than six USB devices, an external hub can be connected to any of the ports.

The ICH4 provides the USB controller for all ports, as shown in Figure 7. The port arrangement is as follows:

- Two ports are implemented with stacked back panel connectors, adjacent to the PS/2 connectors
- Two ports are implemented with stacked back panel connectors, adjacent to the audio connectors
- Two ports are routed to the front panel USB connector

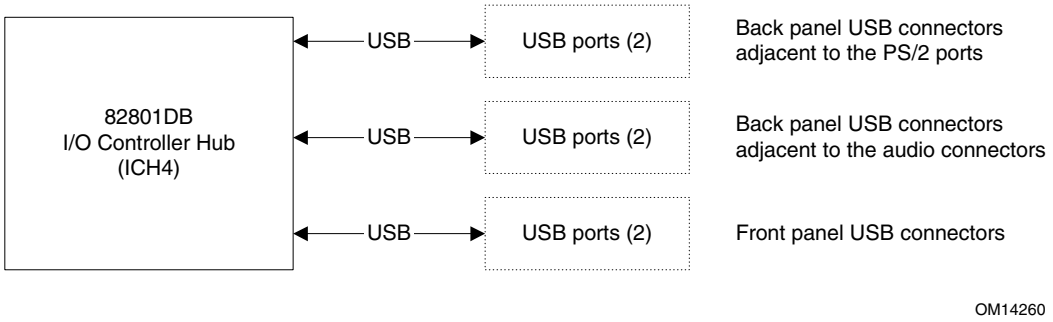



**Figure 7. USB Port Configuration**

### NOTE

*Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.*

### NOTE

*USB 2.0 support has been tested with Windows 2000 and Windows XP drivers and is not currently supported by any other operating system.*

| For information about | Refer to |
|---|---|
| The location of the USB connectors on the back panel | Figure 12, page 60 |
| The location of the front panel USB connector | Figure 17, page 69 |
| The EHCI, front panel, UHCI, and USB specifications | Section 1.5, page 20 |

## 1.8.3 IDE Support

### 1.8.3.1 IDE Interfaces

The ICH4's IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH4's ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

**NOTE**

*ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.*

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes listed in Section 4.4.4.1 on page 104.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The Desktop Boards support Laser Servo (LS-120) diskette technology through the IDE interfaces. An LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

| For information about | Refer to |
|---|---|
| The location of the IDE connectors on the D845GERG2 board | Figure 15, page 67 |
| The location of the IDE connectors on the D845GEBV2 board | Figure 16, page 68 |

### 1.8.3.2 SCSI LED Connector

The SCSI LED connector is a 1 x 2-pin connector that allows an add-in SCSI controller (or other add-in card hard drive controller) to use the same LED as the onboard IDE controller. For proper operation, this connector should be wired to the LED output of the add-in SCSI controller. The LED indicates when data is being read from, or written to, both the add-in SCSI controller and the IDE controller.

| For information about | Refer to |
|---|---|
| The location of the SCSI LED connector on the D845GERG2 board | Figure 15, page 67 |
| The location of the SCSI LED connector on the D845GEBV2 board | Figure 16, page 68 |
| The signal names of the SCSI LED connector | Table 34, page 68 |

### 1.8.4 Real-Time Clock, CMOS SRAM, and Battery

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

**NOTE**

*If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.*

## 1.9 I/O Controller

The SMSC LPC47M172 I/O controller provides the following features:

- One serial port
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.44 MB or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

| For information about | Refer to |
|---|---|
| SMSC LPC47M172 I/O controller | http://www.smsc.com |

### 1.9.1 Serial Port

The boards have one serial port connector located on the back panel. The serial port supports data transfers at speeds up to 115.2 kbits/sec with BIOS support.

| For information about | Refer to |
|---|---|
| The location of the serial port A connector | Figure 12, page 60 |

### 1.9.2 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. Use the BIOS Setup program to set the parallel port mode.

| For information about | Refer to |
|---|---|
| The location of the parallel port connector | Figure 12, page 60 |
| Setting the parallel port's mode | Table 58, page 101 |

### 1.9.3 Diskette Drive Controller

The I/O controller supports one diskette drive. Use the BIOS Setup program to configure the diskette drive interface.

| For information about | Refer to |
|---|---|
| The location of the diskette drive connector on the D845GERG2 board | Figure 15, page 67 |
| The location of the diskette drive connector on the D845GEBV2 board | Figure 16, page 68 |
| The supported diskette drive capacities and sizes | Table 61, page 106 |

### 1.9.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel.

**NOTE**

*The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.*

| For information about | Refer to |
|---|---|
| The location of the keyboard and mouse connectors | Figure 12, page 60 |

## 1.10 Audio Subsystem

The audio subsystem consists of the following devices:

- Intel 82801DB I/O Controller Hub (ICH4)
- Analog Devices AD1981B audio codec

The audio subsystem includes these features:

- Split digital/analog architecture for improved S/N (signal-to-noise) ratio: ≥ 85 dB
- Power management support for ACPI 2.0 (driver dependant)
- Mono/Stereo mic in pre-amp that supports dynamic, condenser, and electret microphones

The audio subsystem supports the following audio interfaces:

- ATAPI-style connectors:
  - Auxiliary line in
  - CD-ROM
- Front panel audio connector, including pins for:
  - Line out
  - Mic in (mono or stereo)
- Back panel audio connectors:
  - Line out
  - Line in
  - Mic in (mono or stereo)

Figure 8 is a block diagram of the audio subsystem.

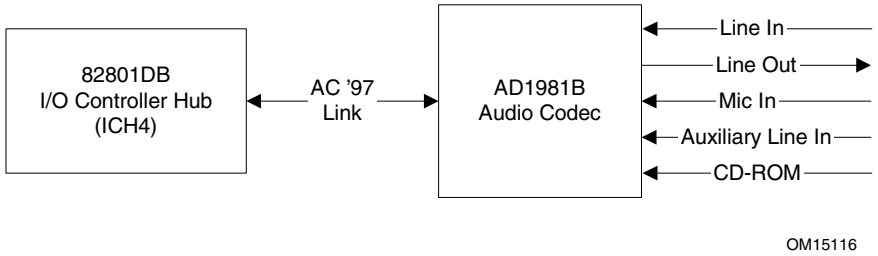



**Figure 8. Audio Subsystem Block Diagram**

| For information about | Refer to |
|---|---|
| Upgrading the onboard audio subsystem using a CNR audio card | Section 1.12, page 40 |
| The front panel audio connector | Section 2.8.2.2, page 62 |
| The back panel audio connectors | Section 2.8.1, page 60 |

## 1.10.1 Audio Connectors

### 1.10.1.1 Front Panel Audio Connector

A 2 x 5-pin connector provides mic in and line out signals for front panel audio connectors.

| For information about | Refer to |
|---|---|
| The location of the connector | Figure 13, page 62 |
| The signal names of the front panel audio connector | Table 25, page 64 |
| Obtaining the *Front Panel I/O Connectivity Design Guide* | Section 1.5, page 20 |

**NOTE**

*The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.9.1 on page 72 for more information.*

### 1.10.1.2 Auxiliary Line In Connector

A 1 x 4-pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

| For information about | Refer to |
|---|---|
| The location of the auxiliary line in connector | Figure 13, page 62 |
| The signal names of the auxiliary line in connector | Table 26, page 64 |

### 1.10.1.3 ATAPI CD-ROM Audio Connector

A 1 x 4-pin ATAPI-style connector connects an internal ATAPI CD-ROM drive to the audio mixer.

| For information about | Refer to |
|---|---|
| The location of the ATAPI CD-ROM connector | Figure 13, page 62 |
| The signal names of the ATAPI CD-ROM connector | Table 28, page 64 |

## 1.10.2 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

| For information about | Refer to |
|---|---|
| Obtaining audio software and drivers | Section 1.3, page 19 |

# 1.11 LAN Subsystem (Optional)

The Network Interface Controller subsystem consists of the ICH4 (with integrated LAN Media Access Controller) and a physical layer interface device. Features of the LAN subsystem include:

- PCI Bus Master interface
- CSMA/CD Protocol Engine
- Serial CSMA/CD unit interface that supports the 82562ET (10/100 Mbit/sec Ethernet) on the CNR bus
- PCI Power Management
  - Supports ACPI technology
  - Supports LAN wake capabilities

The Desktop Board D845GERG2 supports a Gigabit Ethernet Controller option, described below.

## 1.11.1 Intel® 82562ET Platform LAN Connect Device

The Intel 82562ET component provides an interface to the back panel RJ-45 connector with integrated LEDs. This physical interface may alternately be provided through the CNR connector.

The Intel 82562ET provides the following functions:

- Basic 10/100 Ethernet LAN connectivity
- Supports RJ-45 connector with status indicator LEDs on the back panel
- Full device driver compatibility
- ACPI support
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

## 1.11.2 Intel® 82540EM Gigabit Ethernet Controller

The Intel 82540EM Gigabit Ethernet Controller (available only on the Desktop Board D845GERG2) provides the following functions:

- Gigabit Ethernet MAC and PHY layer functions in a single component
- Basic 10/100/1000 Ethernet LAN connectivity
- Integrated PHY for 10/100/1000 Mbit/sec full and half duplex operation
- Supports RJ-45 connector with status indicator LEDs on the back panel
- ACPI support
- Configuration EEPROM that contains the MAC address

## 1.11.3 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 12 describes the LED states when the Desktop Board is powered up and the 10/100 LAN subsystem is operating.

**Table 12. 10/100 Ethernet LAN Connector LED States**

| LED Color | LED State | Condition |
|---|---|---|
| Green | Off | 10 Mbit/sec data rate is selected. |
| | On | 100 Mbit/sec data rate is selected. |
| Yellow | Off | LAN link is not established. |
| | On (steady state) | LAN link is established. |
| | On (brighter and pulsing) | The computer is communicating with another computer on the LAN. |

Table 13 describes the LED states when the Desktop Board is powered up and the 10/100/1000 LAN subsystem is operating.

**Table 13. 10/100/1000 Ethernet LAN Connector LED States**

| LED Color | LED State | Condition |
|---|---|---|
| Green/Yellow | Off | 10 Mbit/sec data rate is selected. |
| | Green | 100 Mbit/sec data rate is selected. |
| | Yellow | 1 Gbit/sec data rate is selected. |
| Yellow | Off | LAN link is not established. |
| | On (steady state) | LAN link is established. |
| | On (brighter and pulsing) | The computer is communicating with another computer on the LAN. |

### 1.11.4 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

| For information about | Refer to |
|---|---|
| Obtaining LAN software and drivers | Section 1.3, page 19 |

## 1.12 CNR (Optional)

The Communication and Networking Riser (CNR) connector provides an interface that supports the audio, modem, and LAN interfaces of the Intel 845GE chipset. Figure 9 shows the signal interface between the riser and the ICH4.

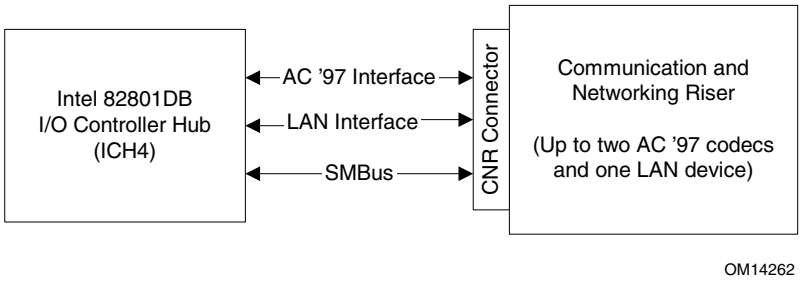



**Figure 9. ICH4 and CNR Signal Interface**

The interfaces supported by the CNR include the following:

- AC ’97 interface: supports audio and/or modem functions on the CNR card.
- LAN interfaces: an eight-pin interface for use with Platform LAN Connection (PLC) based devices.
- SMBus interface: provides Plug-and-Play functionality for the CNR card.

The CNR connector includes power signals required for power management and for CNR card operation. To learn more about the CNR, refer to the CNR specification.

The onboard two-channel audio subsystem can be upgraded to four- or six-channel audio using a CNR audio upgrade card in a slave configuration. CNR audio upgrade cards are available in multiple configurations from several vendors supporting analog or S/P-DIF digital connections.

| For information about | Refer to |
|---|---|
| CNR audio upgrade cards | http://developer.intel.com/technology/cnr/ |

## INTEGRATOR’S NOTES

- *If you install a CNR card that cannot support a multichannel audio upgrade, the Desktop Boards’ integrated audio codec will be disabled. This only applies to D845GEBV2 and D845GERG2 boards that have both the onboard audio subsystem and a CNR.*
- *The brand and type of audio codec used on the CNR card must match that of the Desktop Boards’ codec (Analog Devices AD1981B).*
- *Check with your CNR vendor to ensure that the CNR card has been tested with ICH4-based systems.*
- *There is no USB interface routed to the CNR connector.*

| For information about | Refer to |
|---|---|
| Obtaining the CNR specification | Section 1.5, page 20 |

# 1.13 Hardware Management Subsystem

The hardware management features enable the Desktop Boards to be compatible with the Wired for Management (WfM) specification. The Desktop Board has several hardware management features, including the following:

- Fan monitoring and control (through the I/O controller or the hardware monitoring and fan control ASIC)
- Thermal and voltage monitoring
- Chassis intrusion detection

| For information about | Refer to |
|---|---|
| The WfM specification | Section 1.5, page 20 |

## 1.13.1 Hardware Monitoring ASICs

The Desktop Boards provide one of the following:

- A hardware monitoring ASIC
- A hardware monitoring and fan control ASIC

The features of these components are described in this section. Contact your Intel sales representative to determine which type of hardware monitoring ASIC is present on your Intel Desktop Board.

### 1.13.1.1 Hardware Monitoring ASIC

The features of the hardware monitoring ASIC include:

- Internal ambient temperature sensor
- Remote thermal diode sensor for direct monitoring of processor temperature
- Power supply monitoring of four voltages (+5 V, +3.3 VSB, +1.5 V, and +VCCP) to detect levels above or below acceptable values
- SMBus interface

| For information about | Refer to |
|---|---|
| The location of the fan connectors and sensors for thermal monitoring | Figure 10, page 43 |

### 1.13.1.2 Hardware Monitoring and Fan Control ASIC

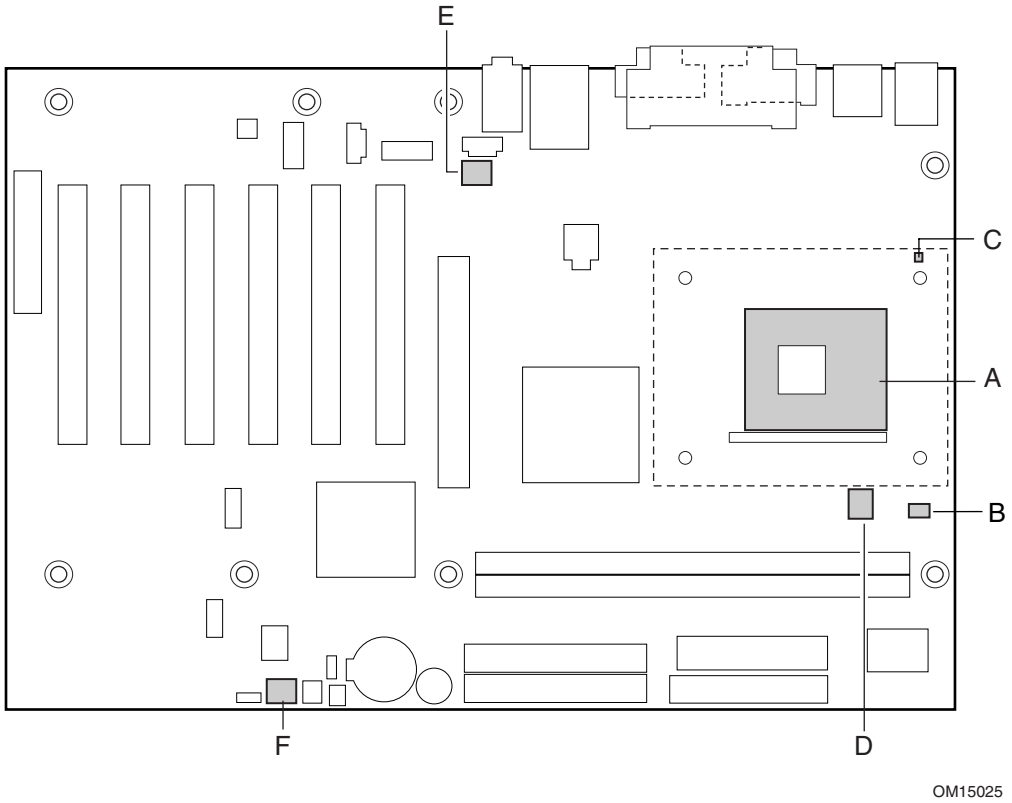
The features of the hardware monitoring and fan control ASIC include:

- Internal ambient temperature sensor
- Two remote thermal diode sensors for direct monitoring of processor temperature and ambient temperature sensing
- Power supply monitoring of five voltages (+5 V, +12 V, +3.3 VSB, +1.5 V, and +VCCP) to detect levels above or below acceptable values
- Thermally monitored closed-loop fan control, for all three fans, that can adjust the fan speed or switch the fans on or off as needed
- SMBus interface

| For information about | Refer to |
|---|---|
| The location of the fan connectors and sensors for thermal monitoring | Figure 10, page 43 |

### 1.13.1.3 Thermal Monitoring

Figure 10 shows the location of the sensors and fan connectors.




| Item | Description |
|---|---|
| A | Thermal diode, located on processor die |
| B | Ambient temperature sensor, internal to both hardware monitoring ASIC options |
| C | Remote ambient temperature sensor (Note) |
| D | Processor fan |
| E | Rear chassis fan |
| F | Front chassis fan |

Note: This sensor is present only on Desktop Boards with the hardware monitoring and fan control ASIC.

**Figure 10. Thermal Monitoring**

### 1.13.2 Fan Monitoring

Fan monitoring can be implemented using Intel® Active Monitor, Intel® LANDesk® Client Manager, or third-party software. The level of monitoring and control is dependent on the hardware monitoring ASIC used with the Desktop Board.

| For information about | Refer to |
|---|---|
| The functions of the fan connectors | Section 1.14.2.2, page 48 |

### 1.13.3 Chassis Intrusion and Detection

The Desktop Boards D845GEBV2 and D845GERG2 support a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. When the chassis cover is removed, the mechanical switch is in the closed position.

## 1.14 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - LAN wake capabilities
  - Instantly Available PC technology
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event signal (PME#) wake-up support

### 1.14.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the Desktop Boards D845GEBV2 and D845GERG2 requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 16 on page 47)
- Support for a front panel power and sleep mode switch

Table 14 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

**Table 14. Effects of Pressing the Power Switch**

| If the system is in this state… | …and the power switch is pressed for | …the system enters this state |
|---|---|---|
| Off<br>(ACPI G2/G5 – Soft off) | Less than four seconds | Power-on<br>(ACPI G0 – working state) |
| On<br>(ACPI G0 – working state) | Less than four seconds | Soft-off/Standby<br>(ACPI G1 – sleeping state) |
| On<br>(ACPI G0 – working state) | More than four seconds | Fail safe power-off<br>(ACPI G2/G5 – Soft off) |
| Sleep<br>(ACPI G1 – sleeping state) | Less than four seconds | Wake-up<br>(ACPI G0 – working state) |
| Sleep<br>(ACPI G1 – sleeping state) | More than four seconds | Power-off<br>(ACPI G2/G5 – Soft off) |

| For information about | Refer to |
|---|---|
| The Desktop Boards' compliance level with ACPI | Section 1.5, page 20 |

#### 1.14.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 15 lists the power states supported by the Desktop Boards D845GEBV2 and D845GERG2 along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

**Table 15. Power States and Targeted System Power**

| Global States | Sleeping States | Processor States | Device States | Targeted System Power (Note 1) |
|---|---|---|---|---|
| G0 – working state | S0 – working | C0 – working | D0 – working state. | Full power > 30 W |
| G1 – sleeping state | S1 – Processor stopped | C1 – stop grant | D1, D2, D3 – device specification specific. | 5 W < power < 52.5 W |
| G1 – sleeping state | S3 – Suspend to RAM. Context saved to RAM. | No power | D3 – no power except for wake-up logic. | Power < 5 W (Note 2) |
| G1 – sleeping state | S4 – Suspend to disk. Context saved to disk. | No power | D3 – no power except for wake-up logic. | Power < 5 W (Note 2) |
| G2/S5 | S5 – Soft off. Context not saved. Cold boot is required. | No power | D3 – no power except for wake-up logic. | Power < 5 W (Note 2) |
| G3 – mechanical off<br>AC power is disconnected from the computer. | No power to the system. | No power | D3 – no power for wake-up logic, except when provided by battery or external source. | No power to the system. Service can be performed safely. |

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

#### 1.14.1.2 Wake-up Devices and Events

Table 16 lists the devices or specific events that can wake the computer from specific states.

**Table 16. Wake-up Devices and Events**

| These devices/events can wake up the computer… | …from this state |
|---|---|
| CNR | S1, S3, S4, S5 |
| LAN | S1, S3, S4, S5 (Note) |
| Modem (back panel Serial Port A) | S1, S3 |
| PME# signal | S1, S3, S4, S5 (Note) |
| Power switch | S1, S3, S4, S5 |
| PS/2 devices | S1, S3 |
| RTC alarm | S1, S3, S4, S5 |
| USB | S1, S3 |

Note: For LAN and PME# signal, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.

**NOTE**

*The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.*

### 1.14.2 Hardware Support

**CAUTION**

*Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 79 for additional information.*

The Desktop Boards D845GEBV2 and D845GERG2 provide several power management hardware features, including:

- Power connector
- Fan connectors
- LAN wake capabilities
- Instantly Available PC technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# signal wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal).

**NOTE**

*The use of Resume on Ring and Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.*

#### 1.14.2.1 Power Connector

ATX12V- and SFX12V-compliant power supplies can turn off the system power through system control. When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

| For information about | Refer to |
|---|---|
| The location of the power connector | Figure 13, page 62 |
| The signal names of the power connector | Table 31, page 66 |
| The BIOS Setup program's Boot menu | Table 70, page 115 |
| The ATX and SFX specifications | Section 1.5, page 20 |

#### 1.14.2.2 Fan Connectors

Table 17 summarizes the function/operation of the fan connectors for Desktop Boards with the hardware monitoring ASIC. Table 18 summarizes the function/operation of the fan connectors for Desktop Boards with the hardware monitoring and fan control ASIC.

**Table 17. Fan Connector Function/Operation for Desktop Boards with a Hardware Monitoring ASIC**

| Connector | Description |
|---|---|
| Processor fan | • +12 V DC connection for a processor fan or active fan heatsink.<br>• Fan is on in the S0 or S1 state.<br>Fan is off when the system is off or in the S3, S4, or S5 state.<br>• Wired to a fan tachometer input of the I/O controller. |
| Front chassis fan | • +12 V DC connection for a system or chassis fan.<br>• Fan is on in the S0 or S1 state.<br>Fan is off when the system is off or in the S3, S4, or S5 state. |
| Rear chassis fan | • +12 V DC connection for a system or chassis fan.<br>• Fan is on in the S0 or S1 state.<br>Fan is off when the system is off or in the S3, S4, or S5 state.<br>• Wired to a fan tachometer input of the I/O controller. |

**Table 18. Fan Connector Function/Operation for Desktop Boards with a Hardware Monitoring and Fan Control ASIC**

| Connector | Description |
|---|---|
| Processor fan | • +12 V DC connection for a processor fan or active fan heatsink.<br>• Fan is on in the S0 or S1 state.<br>Fan is off when the system is off or in the S3, S4, or S5 state.<br>• Wired to a fan tachometer input of the hardware monitoring and fan control ASIC.<br>• Closed-loop fan control that can adjust the fan speed or switch the fans on or off as needed. |
| Front chassis fan | • +12 V DC connection for a system or chassis fan.<br>• Fan is on in the S0 or S1 state.<br>Fan is off when the system is off or in the S3, S4, or S5 state.<br>• Wired to a fan tachometer input of the hardware monitoring and fan control ASIC.<br>• Closed-loop fan control that can adjust the fan speed or switch the fans on or off as needed. |
| Rear chassis fan | • +12 V DC connection for a system or chassis fan.<br>• Fan is on in the S0 or S1 state.<br>Fan is off when the system is off or in the S3, S4, or S5 state.<br>• Wired to a fan tachometer input of the hardware monitoring and fan control ASIC.<br>• Closed-loop fan control that can adjust the fan speed or switch the fans on or off as needed. |

| For information about | Refer to |
|---|---|
| The location of the fan connectors | Figure 13, page 62 |
| The location of the fan connectors and sensors for thermal monitoring | Figure 10, on page 43 |
| The signal names of the fan connectors | Section 2.8.2.2, page 62 |

### 1.14.2.3 LAN Wake Capabilities

**CAUTION**

*For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply. Refer to Section 2.11.3 on page 79 for additional information.*

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the Desktop Boards D845GEBV2 and D845GERG2 support LAN wake capabilities with ACPI in the following ways:

- The PCI bus PME# signal for PCI 2.2 compliant LAN designs
- The onboard LAN subsystem
- A CNR-based LAN subsystem

#### 1.14.2.4 Instantly Available PC Technology

**CAUTION**

*For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply. Refer to Section 2.11.3 on page 79 for additional information.*

Instantly Available PC technology enables the Desktop Boards D845GEBV2 and D845GERG2 to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 16 on page 47 lists the devices and events that can wake the computer from the S3 state.

The Desktop Boards D845GEBV2 and D845GERG2 support the *PCI Bus Power Management Interface Specification*. For information on the version of this specification, see Section 1.5. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.2 compliant add-in cards and drivers.

### 1.14.2.5 +5 V Standby Power Indicator LED

The +5 V standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 11 shows the location of the standby power indicator LED on the D845GEBV2 board.

**CAUTION**

*If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.*

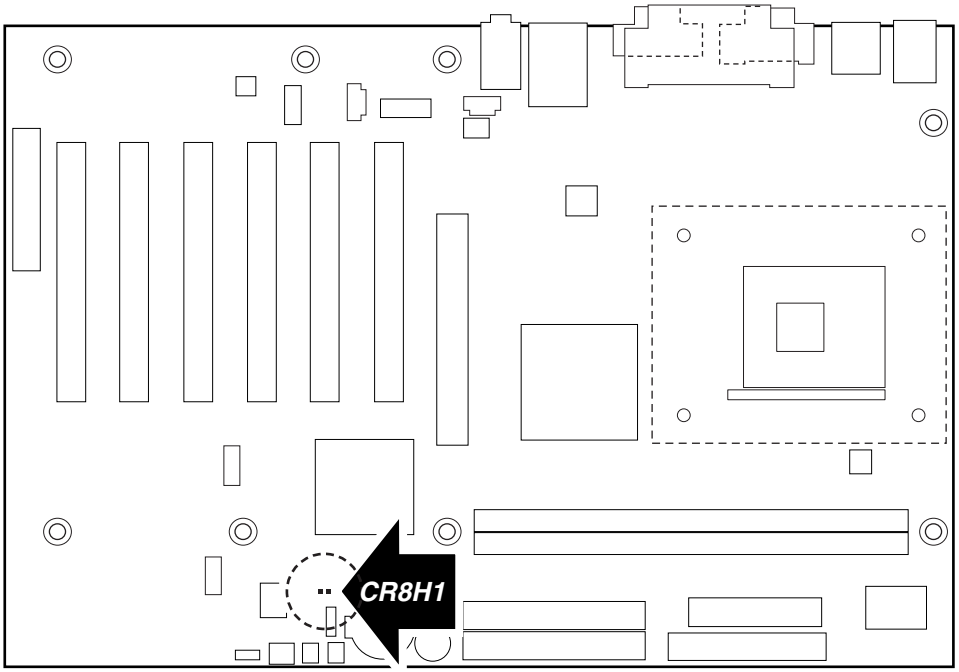



**Figure 11. Location of the Standby Power Indicator LED on the D845GEBV2 Board**

### 1.14.2.6 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from ACPI S1 or S3 states
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

#### 1.14.2.7 Wake from USB

USB bus activity wakes the computer from ACPI S1 or S3 states.

**NOTE**

*Wake from USB requires the use of a USB peripheral that supports Wake from USB.*

#### 1.14.2.8 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1 or S3 state.

#### 1.14.2.9 PME# Signal Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with Wake on PME enabled in BIOS).

# 2 Technical Reference

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## 2.1 Introduction

Sections 2.2 - 2.6 contain several standalone tables. Table 19 describes the system memory map, Table 20 shows the I/O map, Table 21 lists the DMA channels, Table 22 defines the PCI configuration space map, and Table 23 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

## 2.2 Memory Map

**Table 19. System Memory Map**

| Address Range (decimal) | Address Range (hex) | Size | Description |
|---|---|---|---|
| 1024 K - 2097152 K | 100000 - 7FFFFFFF | 2047 MB | Extended memory |
| 960 K - 1024 K | F0000 - FFFFF | 64 KB | Runtime BIOS |
| 896 K - 960 K | E0000 - EFFFF | 64 KB | Reserved |
| 800 K - 896 K | C8000 - DFFFF | 96 KB | Available high DOS memory (open to the PCI bus) |
| 640 K - 800 K | A0000 - C7FFF | 160 KB | Video memory and BIOS |
| 639 K - 640 K | 9FC00 - 9FFFF | 1 KB | Extended BIOS data (movable by memory manager software) |
| 512 K - 639 K | 80000 - 9FBFF | 127 KB | Extended conventional memory |
| 0 K - 512 K | 00000 - 7FFFF | 512 KB | Conventional memory |

## 2.3 Fixed I/O Map

**Table 20. I/O Map**

| Address (hex) | Size | Description |
|---|---|---|
| 0000 - 00FF | 256 bytes | Used by the Desktop Board D845GEBV2/D845GERG2. Refer to the ICH4 data sheet for dynamic addressing information. |
| 0170 - 0177 | 8 bytes | Secondary IDE channel |
| 01F0 - 01F7 | 8 bytes | Primary IDE channel |
| 0228 - 022F (Note 1) | 8 bytes | LPT3 |
| 0278 - 027F (Note 1) | 8 bytes | LPT2 |
| 02E8 - 02EF (Note 1) | 8 bytes | COM4 |
| 02F8 - 02FF (Note 1) | 8 bytes | COM2 |
| 0376 | 1 byte | Secondary IDE channel command port |
| 0377, bits 6:0 | 7 bits | Secondary IDE channel status port |
| 0378 - 037F | 8 bytes | LPT1 |
| 03B0 - 03BB | 12 bytes | Intel 82845GE GMCH |
| 03C0 - 03DF | 32 bytes | Intel 82845GE GMCH |
| 03E8 - 03EF | 8 bytes | COM3 |
| 03F0 - 03F5 | 6 bytes | Diskette channel 1 |
| 03F6 | 1 byte | Primary IDE channel command port |
| 03F8 - 03FF | 8 bytes | COM1 |
| 04D0 - 04D1 | 2 bytes | Edge/level triggered PIC |
| LPTn + 400 | 8 bytes | ECP port, LPTn base address + 400h |
| 0CF8 - 0CFB (Note 2) | 4 bytes | PCI configuration address register |
| 0CF9 (Note 3) | 1 byte | Turbo and reset control register |
| 0CFC - 0CFF | 4 bytes | PCI configuration data register |
| FFA0 - FFA7 | 8 bytes | Primary bus master IDE registers |
| FFA8 - FFAF | 8 bytes | Secondary bus master IDE registers |

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

### NOTE

*Some additional I/O addresses are not available due to ICH4 address aliassing. The ICH4 data sheet provides more information on address aliassing.*

| For information about | Refer to |
|---|---|
| Obtaining the ICH4 data sheet | Section 1.3 on page 19 |

## 2.4 DMA Channels

**Table 21. DMA Channels**

| DMA Channel Number | Data Width | System Resource |
|---|---|---|
| 0 | 8 or 16 bits | Open |
| 1 | 8 or 16 bits | Parallel port |
| 2 | 8 or 16 bits | Diskette drive |
| 3 | 8 or 16 bits | Parallel port (for ECP or EPP) |
| 4 | 8 or 16 bits | DMA controller |
| 5 | 16 bits | Open |
| 6 | 16 bits | Open |
| 7 | 16 bits | Open |

## 2.5 PCI Configuration Space Map

**Table 22. PCI Configuration Space Map**

| Bus Number (hex) | Device Number (hex) | Function Number (hex) | Description |
|---|---|---|---|
| 00 | 00 | 00 | Memory controller of Intel 82845GE component |
| 00 | 01 | 00 | Host to AGP bridge (virtual P2P) |
| 00 | 1E | 00 | Hub link to PCI bridge |
| 00 | 1F | 00 | Intel 82801DB ICH4 PCI to LPC bridge |
| 00 | 1F | 01 | IDE controller |
| 00 | 1F | 03 | SMBus controller |
| 00 | 1F | 05 | AC ’97 audio controller |
| 00 | 1F | 06 | AC ’97 modem controller |
| 00 | 1D | 00 | USB UHCI controller 1 |
| 00 | 1D | 01 | USB UHCI controller 2 |
| 00 | 1D | 02 | USB UHCI controller 3 |
| 00 | 1D | 07 | EHCI controller |
| 01 | 00 | 00 | AGP add-in card |
| (Note 1) | 08 | 00 | LAN controller (optional) |
| (Note 1) | 00 | 00 | PCI bus connector 1 |
| (Note 1) | 01 | 00 | PCI bus connector 2 |
| (Note 1) | 02 | 00 | PCI bus connector 3 |
| (Note 1) | 03 | 00 | PCI bus connector 4 (Note 2) |
| (Note 1) | 04 | 00 | PCI bus connector 5 (Note 2) |
| (Note 1) | 05 | 00 | PCI bus connector 6 (Note 2) |

Notes:
1. Bus number = 01 when the Intel Extreme Graphics controller is used. Bus number = 02 when an AGP add-in card is used.
2. Desktop Board D845GEBV2 only

## 2.6 Interrupts

The interrupts can be routed through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the ICH4 component. The PIC is supported in Windows 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and supports a total of 24 interrupts.

**Table 23. Interrupts**

| IRQ | System Resource |
|---|---|
| NMI | I/O channel check |
| 0 | Reserved, interval timer |
| 1 | Reserved, keyboard buffer full |
| 2 | Reserved, cascade interrupt from slave PIC |
| 3 | COM2 (Note 1) |
| 4 | COM1 (Note 1) |
| 5 | LPT2 (Plug and Play option)/User available |
| 6 | Diskette drive |
| 7 | LPT1 (Note 1) |
| 8 | Real-time clock |
| 9 | Reserved for ICH4 system management bus |
| 10 | User available |
| 11 | User available |
| 12 | Onboard mouse port (if present, else user available) |
| 13 | Reserved, math coprocessor |
| 14 | Primary IDE (if present, else user available) |
| 15 | Secondary IDE (if present, else user available) |
| 16 (Note 2) | USB UHCI controller 1 (through PIRQA) |
| 17 (Note 2) | AC ’97 audio/modem/User available (through PIRQB) |
| 18 (Note 2) | ICH4 USB controller 3 (through PIRQC) |
| 19 (Note 2) | ICH4 USB controller 2 (through PIRQD) |
| 20 (Note 2) | ICH4 LAN (optional) (through PIRQE) |
| 21 (Note 2) | User available (through PIRQF) |
| 22 (Note 2) | User available (through PIRQG) |
| 23 (Note 2) | ICH4 USB 2.0 EHCI controller/User available (through PIRQH) |

Notes:

1. Default, but can be changed to another IRQ.
2. Available in APIC mode only.

## 2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH4 has eight Programmable Interrupt Request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the Desktop Boards D845GEBV2 and D845GERG2 and therefore share the same interrupt. Table 24 shows an example of how the PIRQ signals are routed.

For example, using Table 24 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 3. In PCI bus connector 3, INTA is connected to PIRQC, which is already connected to the ICH4 USB. The add-in card in PCI bus connector 3 now shares an interrupt with the onboard interrupt source.

**Table 24. PCI Interrupt Routing Map**

| PCI Interrupt Source | ICH4 PIRQ Signal Name | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | PIRQA | PIRQB | PIRQC | PIRQD | PIRQE | PIRQF | PIRQG | PIRQH |
| AGP connector | INTA | INTB | | | | | | |
| ICH4 USB UHCI controller 1 | INTA | | | | | | | |
| SMBus controller | | INTB | | | | | | |
| ICH4 USB UHCI controller 2 | | | | INTB | | | | |
| AC '97 ICH4 Audio/Modem | | INTB | | | | | | |
| ICH4 LAN | | | | | INTA | | | |
| ICH4 USB UHCI controller 3 | | | INTC | | | | | |
| ICH4 USB 2.0 EHCI controller | | | | | | | | INTD |
| PCI bus connector 1 | | | | | INTD | INTA | INTB | INTC |
| PCI bus connector 2 | | | | | INTC | INTB | INTA | INTD |
| PCI bus connector 3 | INTD | INTC | INTA | INTB | | | | |
| PCI bus connector 4 (Note) | | | INTB | INTA | | INTC | INTD | |
| PCI bus connector 5 (Note) | INTC | INTA | | | INTD | | | INTB |
| PCI bus connector 6 (Note) | | | INTA | | INTB | INTD | INTC | |

Note: Desktop Board D845GEBV2 only

## NOTE

*In PIC mode, the ICH4 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. Refer to Table 23 for the allocation of PIRQ lines to IRQ signals in APIC mode.*

## 2.8 Connectors

### CAUTION

*Only the back panel USB, front panel USB, VGA, and PS/2 connectors of the Desktop Boards D845GEBV2 and D845GERG2 have overcurrent protection. The Desktop Boards' internal connectors are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.*

This section describes the Desktop Board's connectors. The connectors can be divided into these groups:

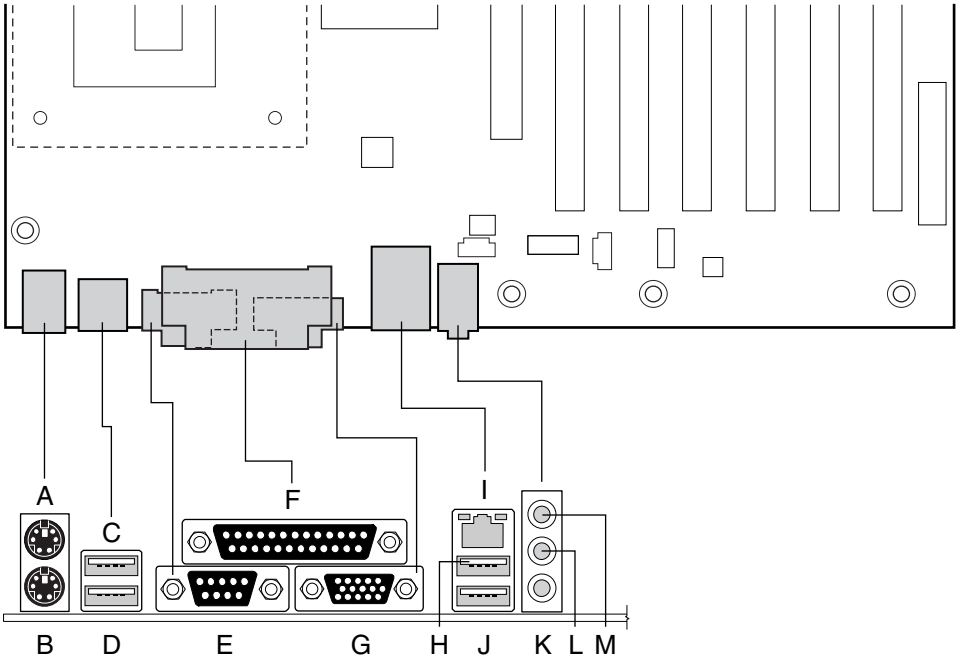
- Back panel I/O connectors (see page 60)
  - PS/2 keyboard and mouse
  - USB (four ports)
  - Parallel port
  - Serial port A
  - LAN (optional)
  - Audio (line out, line in, and mic in)
- Internal I/O connectors (see page 61)
  - Audio (auxiliary line input, ATAPI CD-ROM, and front panel audio)
  - Fans
  - Power
  - Add-in boards (PCI and AGP)
  - CNR (optional)
  - IDE
  - Diskette drive
  - SCSI LED
  - Chassis intrusion
- External I/O connectors (see page 69)
  - Front panel USB (one connector for two ports)
  - Auxiliary front panel power/sleep/message-waiting LED
  - Front panel (power/sleep/message-waiting LED, power switch, hard drive activity LED, reset switch, and auxiliary front panel power LED)

### NOTE

*When installing the D845GERG2 board in a microATX chassis, make sure that peripheral devices are installed at least 1.5 inches above the main power connector, the diskette drive connector, the IDE connector, and the DIMM sockets.*

## 2.8.1 Back Panel Connectors

Figure 12 shows the location of the back panel connectors. The back panel connectors are color-coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.




| Item | Description | Color |
|---|---|---|
| A | PS/2 mouse port | Green |
| B | PS/2 keyboard port | Purple |
| C | USB port | Black |
| D | USB port | Black |
| E | Serial port A | Teal |
| F | Parallel port | Burgundy |
| G | VGA port | Dark blue |
| H | USB port | Black |
| I | LAN (optional) | Black |
| J | USB port | Black |
| K | Mic in | Pink |
| L | Audio line out | Lime green |
| M | Audio line in | Light blue |

**Figure 12. Back Panel Connectors**

**NOTE**

*The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.*

## 2.8.2 Internal I/O Connectors

The internal I/O connectors are divided into the following functional groups:

- Audio, power, and hardware control (see page 62)
  - Auxiliary line in
  - ATAPI CD-ROM
  - Front panel audio
  - Fans
  - ATX12V power
  - Main power
- Add-in boards and peripheral interfaces (see page 67)
  - CNR (optional)
  - PCI bus
  - AGP
  - IDE
  - Diskette drive
  - SCSI LED

### 2.8.2.1 Expansion Slots

The board has the following expansion slots:

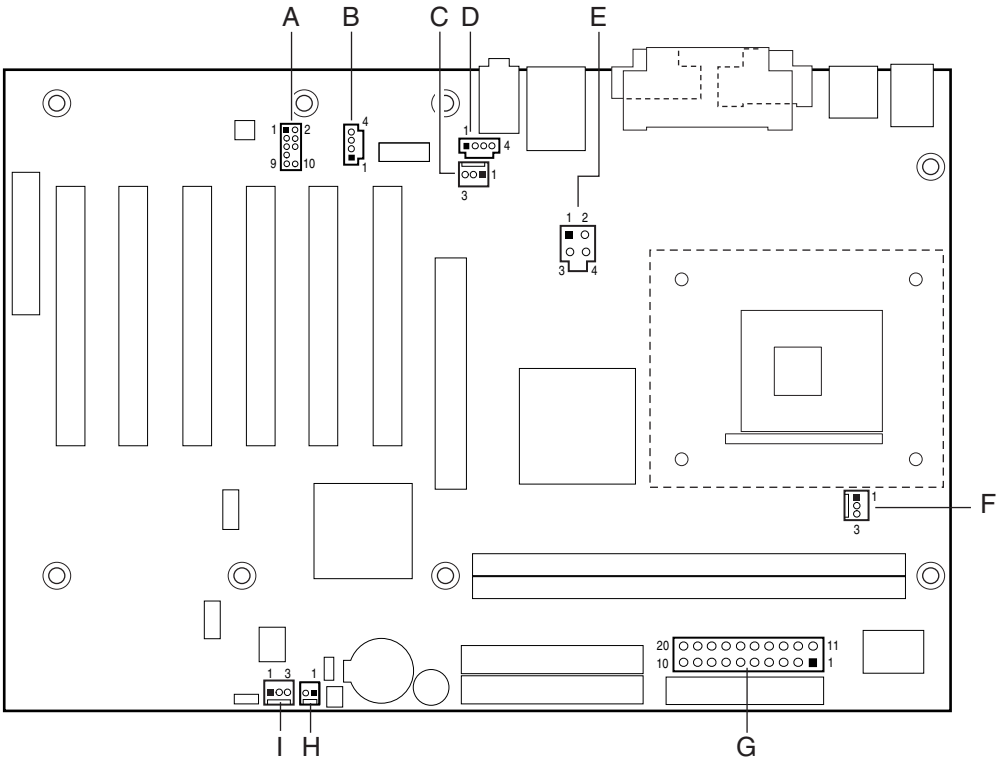
- One AGP connector. The AGP connector is keyed for 1.5 V AGP cards only. Do not install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.
- PCI rev 2.2 compliant local bus slots (six on the Desktop Board D845GEBV2, three on the Desktop Board D845GERG2). The SMBus is routed to PCI bus connector 2 only (ATX expansion slot 6). PCI add-in cards with SMBus support can access sensor data and other information residing on the Desktop Board.
- One CNR (optional), shared with PCI bus connector 6 (ATX expansion slot 1) on the Desktop Board D845GEBV2, or with PCI bus connector 3 (ATX expansion slot 1) on the Desktop Board D845GERG2.

**NOTE**

*This document references back-panel slot numbering with respect to processor location on the board. The AGP slot is not numbered. PCI slots are identified as PCI slot #x, starting with the slot closest to the processor. The CNR slot shares an ATX expansion; slot 6 on the D845GEBV2 board and slot 3 on the D845GERG2 board. The ATX/MicroATX specifications identify expansion slot locations with respect to the far edge of a full-sized ATX chassis. The ATX specification and the board's silkscreen are opposite and could cause confusion. The ATX numbering convention is made without respect to slot type (PCI vs. AGP), but refers to an actual slot location on a chassis. Figure 15 (page 67) and Figure 16 (page 68) illustrate the board's PCI slot numbering.*

### 2.8.2.2 Audio, Power, and Hardware Control Connectors

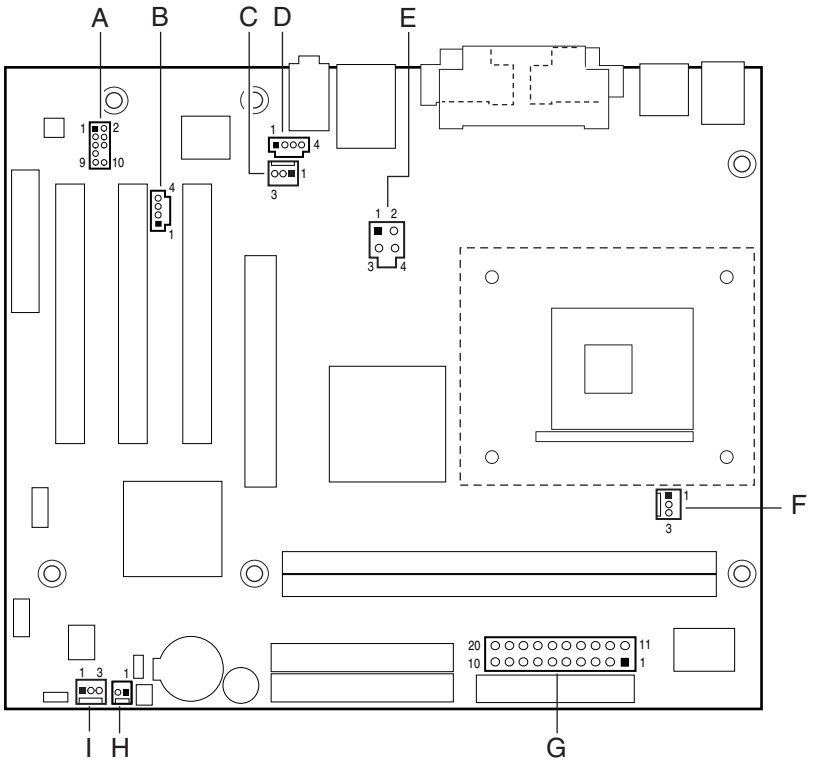
Figure 13 shows the location of the audio, power, and hardware control connectors.




| Item | Description | For more information see: |
|---|---|---|
| A | Front panel audio | Table 25 |
| B | Auxiliary line in, ATAPI style (white) | Table 26 |
| C | Rear chassis fan | Table 27 |
| D | ATAPI CD-ROM (black) | Table 28 |
| E | +12 V power connector (ATX12V) | Table 29 |
| F | Processor fan | Table 30 |
| G | Main power | Table 31 |
| H | Chassis intrusion | Table 32 |
| I | Front chassis fan | Table 33 |

**Figure 13. Audio, Power, and Hardware Control Connectors**

Figure 14 shows the location of the audio, power, and hardware control connectors on the Desktop Board D845GERG2 with the Gigabit Ethernet LAN option.




| Item | Description | For more information see: |
|---|---|---|
| A | Front panel audio | Table 25 |
| B | Auxiliary line in, ATAPI style (white) | Table 26 |
| C | Rear chassis fan | Table 27 |
| D | ATAPI CD-ROM (black) | Table 28 |
| E | +12 V power connector (ATX12V) | Table 29 |
| F | Processor fan | Table 30 |
| G | Main power | Table 31 |
| H | Chassis intrusion | Table 32 |
| I | Front chassis fan | Table 33 |

**Figure 14. Audio, Power, and Hardware Control Connectors on the Desktop Board D845GERG2 with the Gigabit Ethernet LAN option**

**Table 25. Front Panel Audio Connector**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | MIC_IN | 2 | Ground |
| 3 | MIC_BIAS | 4 | +5 V |
| 5 | RIGHT_OUT | 6 | RIGHT_IN |
| 7 | Ground | 8 | Key |
| 9 | LEFT_OUT | 10 | LEFT_IN |

## INTEGRATOR'S NOTE

*The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.9.1 on page 72 for more information.*

**Table 26. Auxiliary Line In Connector**

| Pin | Signal Name |
|---|---|
| 1 | Left auxiliary line in |
| 2 | Ground |
| 3 | Ground |
| 4 | Right auxiliary line in |

**Table 27. Rear Chassis Fan Connector**

| Pin | Signal Name |
|---|---|
| 1 | (Note) |
| 2 | +12 V |
| 3 | REAR_TACH_OUT |

Note: Pin 1 is *Control* if the Desktop Board uses the hardware monitoring and fan control ASIC.
Pin 1 is *Ground* if the Desktop Board uses the hardware monitoring ASIC.

**Table 28. ATAPI CD-ROM Connector**

| Pin | Signal Name |
|---|---|
| 1 | Left audio input from CD-ROM |
| 2 | CD audio differential ground |
| 3 | CD audio differential ground |
| 4 | Right audio input from CD-ROM |

## INTEGRATOR'S NOTES

- *Use only ATX12V-compliant power supplies with these boards. ATX12V power supplies have an additional power lead that provides required supplemental power for the processor. Always connect the 20-pin and 4-pin leads of ATX12V power supplies to the corresponding connectors on the board, otherwise the board will not boot.*
- *Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.*

**Table 29. ATX12V Power Connector**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | Ground | 2 | Ground |
| 3 | +12 V | 4 | +12 V |

**Table 30. Processor Fan Connector**

| Pin | Signal Name |
|---|---|
| 1 | (Note) |
| 2 | +12 V |
| 3 | CPU_FAN_TACH |

Note: Pin 1 is *Control* if the Desktop Board uses the hardware monitoring and fan control ASIC.
Pin 1 is *Ground* if the Desktop Board uses the hardware monitoring ASIC.

### Table 31. Main Power Connector

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | +3.3 V | 11 | +3.3 V |
| 2 | +3.3 V | 12 | -12 V |
| 3 | Ground | 13 | Ground |
| 4 | +5 V | 14 | PS-ON# (power supply remote on/off) |
| 5 | Ground | 15 | Ground |
| 6 | +5 V | 16 | Ground |
| 7 | Ground | 17 | Ground |
| 8 | PWRGD (Power Good) | 18 | No connect |
| 9 | +5 V (Standby) | 19 | +5 V |
| 10 | +12 V | 20 | +5 V |

### Table 32. Chassis Intrusion Connector

| Pin | Signal Name |
|---|---|
| 1 | Intruder |
| 2 | Ground |

### Table 33. Front Chassis Fan Connector

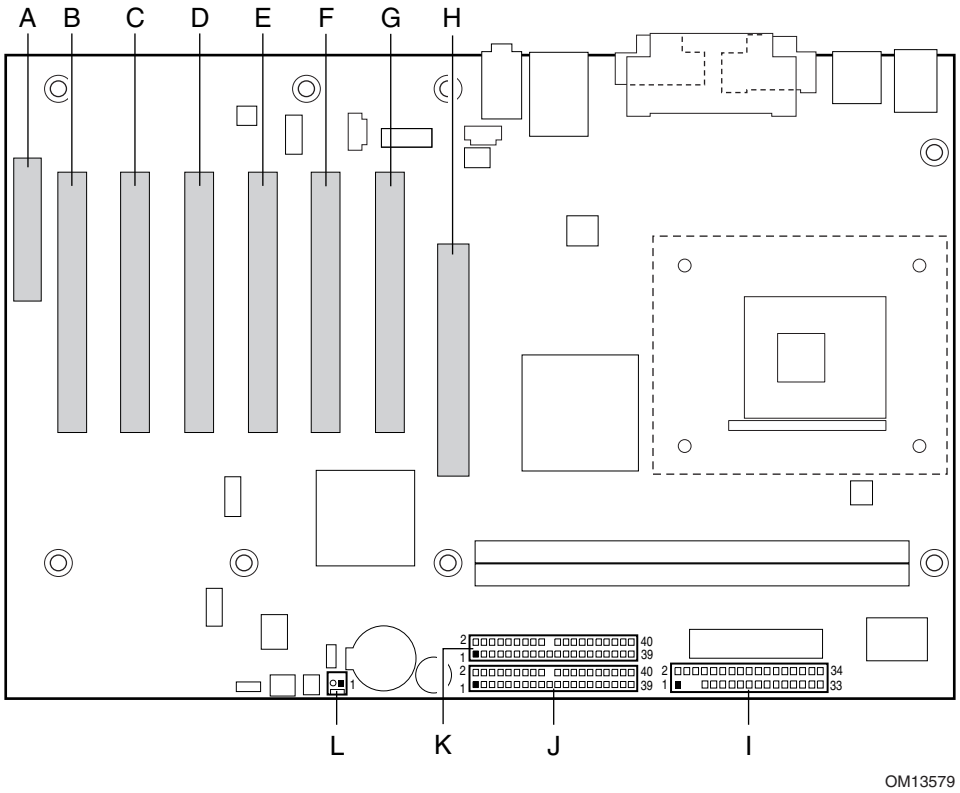
| Pin | Signal Name |
|---|---|
| 1 | (Note 1) |
| 2 | +12 V |
| 3 | (Note 2) |

Notes:
1. Pin 1 is *Control* if the Desktop Board uses the hardware monitoring and fan control ASIC.
   Pin 1 is *Ground* if the Desktop Board uses the hardware monitoring ASIC.
2. Pin 3 is *FRONT_TACH_OUT* if the Desktop Board uses the hardware monitoring and fan control ASIC.
   Pin 3 is *No connect* if the Desktop Board uses the hardware monitoring ASIC.

### 2.8.2.3 Add-in Board and Peripheral Interface Connectors

Figure 15 shows the location of the add-in board connector and peripheral connectors for the Desktop Board D845GEBV2. Note the following considerations for the PCI bus connectors (for both Desktop Boards):

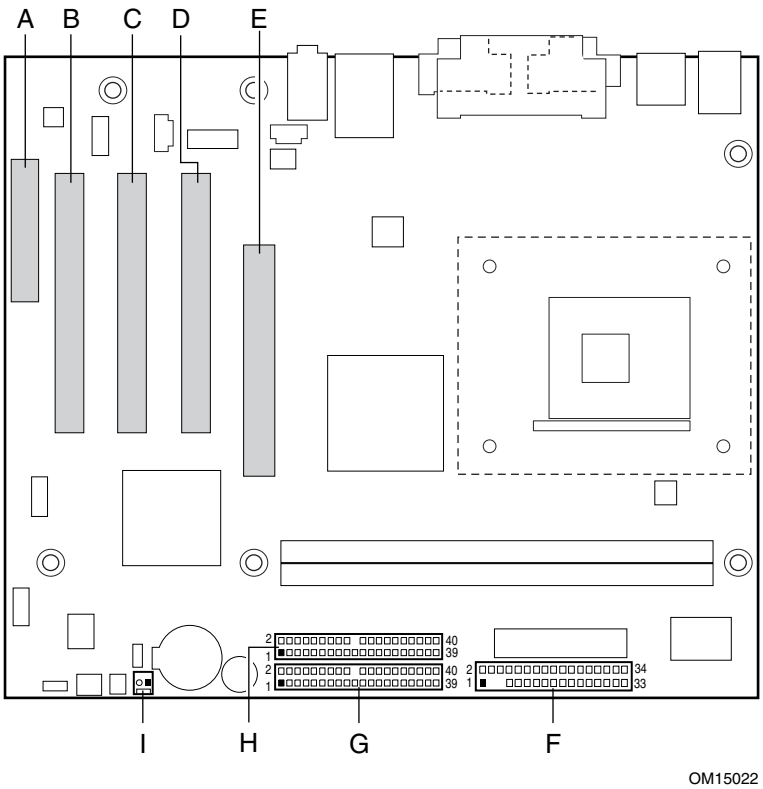
- All of the PCI bus connectors are bus master capable.
- SMBus signals are routed to PCI bus connector 2. This enables PCI bus add-in boards with SMBus support to access sensor data on the Desktop Board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40.
  - The SMBus data line is connected to pin A41.




| Item | Description | Item | Description |
|---|---|---|---|
| A | CNR (optional) | G | PCI bus connector 1 |
| B | PCI bus connector 6 | H | AGP connector |
| C | PCI bus connector 5 | I | Diskette drive |
| D | PCI bus connector 4 | J | Primary IDE |
| E | PCI bus connector 3 | K | Secondary IDE |
| F | PCI bus connector 2 | L | SCSI LED |

**Figure 15. D845GEBV2 Add-in Board and Peripheral Interface Connectors**

Figure 16 shows the location of the add-in board connector and peripheral connectors for the Desktop Board D845GERG2.




| Item | Description | Item | Description |
|---|---|---|---|
| A | CNR (optional) | F | Diskette drive |
| B | PCI bus connector 3 | G | Primary IDE |
| C | PCI bus connector 2 | H | Secondary IDE |
| D | PCI bus connector 1 | I | SCSI LED |
| E | AGP connector | | |

**Figure 16. D845GERG2 Add-in Board and Peripheral Interface Connectors**

## INTEGRATOR'S NOTES

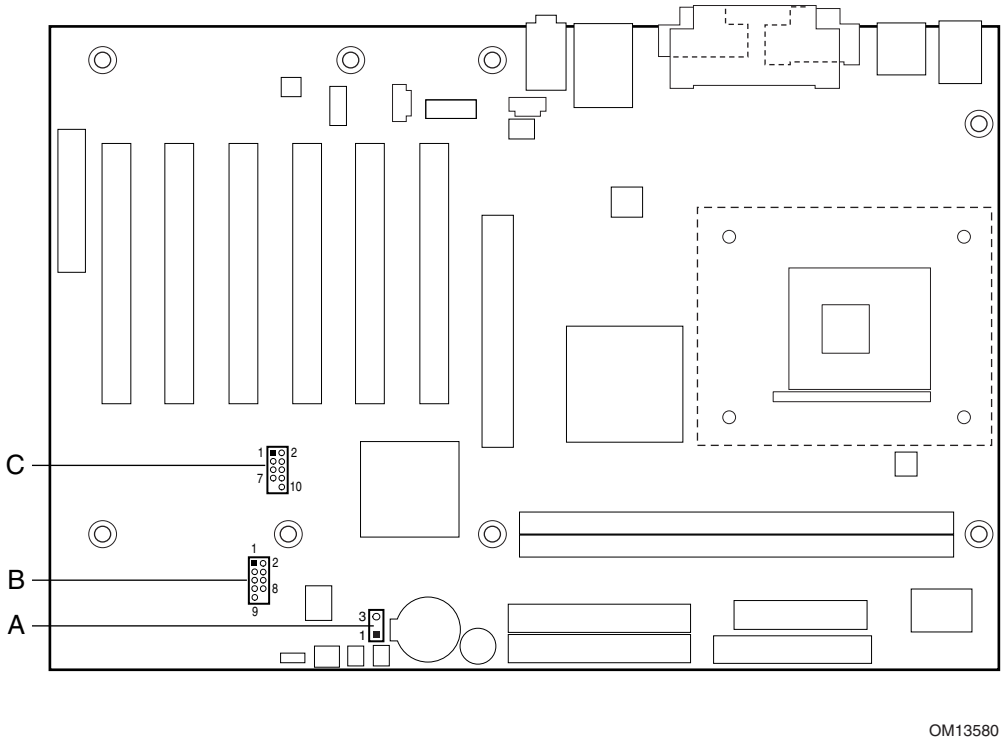
- *The AGP connector is keyed for 1.5 V AGP cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.*
- *Not all PCI video cards can be used in PCI bus connectors 1 and 2 (the PCI bus connectors closest to the processor). To avoid clearance problems, install PCI video cards in PCI bus connector 3.*

**Table 34. SCSI LED Connector**

| Pin | Signal Name |
|---|---|
| 1 | SCSI_ACT# |
| 2 | No connect |

## 2.8.3 External I/O Connectors

Figure 17 shows the locations of the external I/O connectors.




| Item | Description | For more information see: |
|---|---|---|
| A | Auxiliary front panel power/sleep/message-waiting LED | Table 39 |
| B | Front panel | Table 36 |
| C | Front panel USB | Table 35 |

**Figure 17. External I/O Connectors**

**Table 35. Front Panel USB Connector**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | USB_FNT_PWR | 2 | USB_FNT_PWR |
| 3 | USB_FNTA# | 4 | USB_FNTB# |
| 5 | USB_FNTA | 6 | USB_FNTB |
| 7 | Ground | 8 | Ground |
| 9 | Key | 10 | USB_FP_OC (USB front panel overcurrent signal) |

### INTEGRATOR'S NOTE

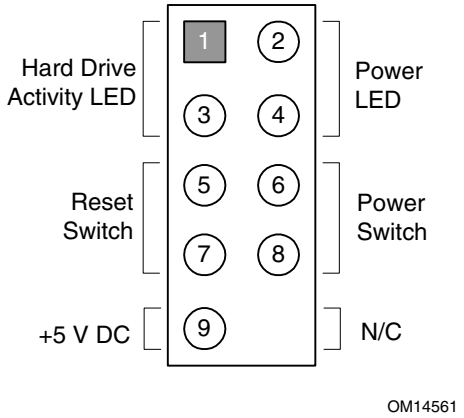
*Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*

### 2.8.3.1 Front Panel Connector

This section describes the functions of the front panel connector. Table 36 lists the signal names of the front panel connector.

**Table 36. Front Panel Connector**

| Pin | Signal | In/Out | Description | Pin | Signal | In/Out | Description |
|---|---|---|---|---|---|---|---|
| **Hard Drive Activity LED** | | | | **Power LED** | | | |
| 1 | HD_PWR | Out | Hard disk LED pull-up (330 Ω) to +5 V | 2 | HDR_BLNK_ GRN | Out | Front panel green LED |
| 3 | HAD# | Out | Hard disk active LED | 4 | HDR_BLNK_ YEL | Out | Front panel yellow LED |
| **Reset Switch** | | | | **On/Off Switch** | | | |
| 5 | Ground | | Ground | 6 | SWITCH_ON# | In | Power switch |
| 7 | FP_RESET# | In | Reset switch | 8 | Ground | | Ground |
| 9 | +5 V | Out | Power | 10 | N/C | | Not connected |




#### 2.8.3.1.1 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface. The LED will also show activity for devices connected to the SCSI hard drive activity LED connector.

| For information about | Refer to |
|---|---|
| The SCSI hard drive activity LED connector | Section 1.8.3.2, page 34 |

#### 2.8.3.1.2 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the Desktop Board resets and runs the POST.

#### 2.8.3.1.3 Power/Sleep/Message Waiting LED Connector

Pins 2 and 4 can be connected to a one- or two-color LED. Table 37 shows the possible states for a one-color LED. Table 38 shows the possible states for a two-color LED.

**Table 37. States for a One-Color Power LED**

| LED State | Description |
|---|---|
| Off | Power off/sleeping |
| Steady Green | Running |
| Blinking Green | Running/message waiting |

**Table 38. States for a Two-Color Power LED**

| LED State | Description |
|---|---|
| Off | Power off |
| Steady Green | Running |
| Blinking Green | Running/message waiting |
| Steady Yellow | Sleeping |
| Blinking Yellow | Sleeping/message waiting |

**INTEGRATOR'S NOTE**

*To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.*

#### 2.8.3.1.4 Power Switch Connector

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

### 2.8.3.2 Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector

Pins 1 and 3 of this connector duplicate the signals on pins 2 and 4 of the front panel connector. Table 39 lists the signal names of the Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector.

**Table 39. Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector**

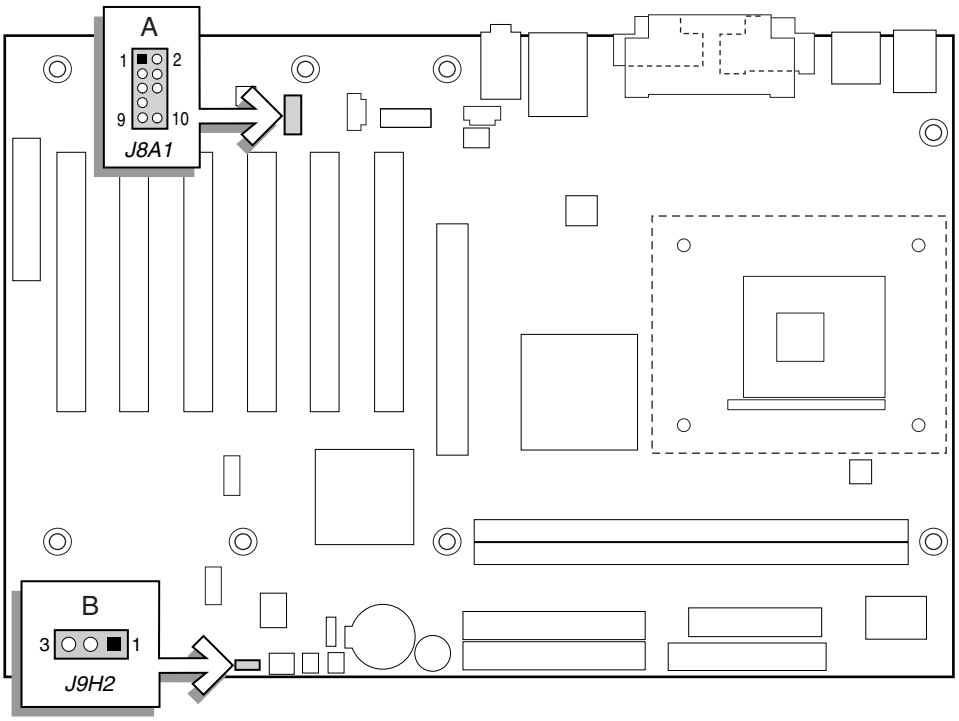
| Pin | Signal Name | In/Out | Description |
|---|---|---|---|
| 1 | HDR_BLNK_GRN | Out | Front panel green LED |
| 2 | Not connected | | |
| 3 | HDR_BLNK_YEL | Out | Front panel yellow LED |

## 2.9 Jumper Blocks

**CAUTION**

*Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the Desktop Board could be damaged.*

Figure 18 shows the location of the jumper blocks.




| Item | Description | Reference Designator |
|---|---|---|
| A | Front panel audio connector/jumper block | J8A1 |
| B | BIOS Setup configuration jumper block | J9H2 |

**Figure 18. Location of the Jumper Blocks**

### 2.9.1 Front Panel Audio Connector/Jumper Block

This connector has two functions:

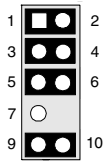
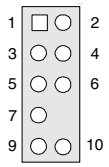
- With jumpers installed, the audio line out signals are routed to the back panel audio line out connector.
- With jumpers removed, the connector provides audio line out and mic in signals for front panel audio connectors.

Table 40 describes the two configurations of this connector/jumper block.

### CAUTION

*Do not place jumpers on this block in any configuration other than the one described in Table 40. Other jumper configurations are not supported and could damage the Desktop Board.*

**Table 40. Front Panel Audio Connector/Jumper Block**

| Jumper Setting | | Configuration |
|---|---|---|
|  | 1 and 2<br>3 and 4<br>5 and 6<br><br>9 and 10 | Audio line out signals are routed to the back panel audio line out connector. The back panel audio line out connector is shown in Figure 12 on page 60. |
|  | No jumpers installed | Audio line out and mic in signals are available for front panel audio connectors. Table 25 on page 64 lists the names of the signals available on this connector when no jumpers are installed. |

### INTEGRATOR'S NOTE

*When the jumpers are removed and this connector is used for front panel audio, the back panel audio line out and mic in connectors are disabled.*

## 2.9.2 BIOS Setup Configuration Jumper Block

The 3-pin jumper block determines the BIOS Setup program's mode. Table 41 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configuration mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

**Table 41. BIOS Setup Configuration Jumper Settings**

| Function/Mode | Jumper Setting | | Configuration |
|---|---|---|---|
| Normal | 1-2 | | The BIOS uses current configuration information and passwords for booting. |
| Configure | 2-3 | | After the POST runs, Setup runs automatically. The maintenance menu is displayed. |
| Recovery | None | | The BIOS attempts to recover the BIOS configuration. A recovery diskette is required. |

# 2.10 Mechanical Considerations

## 2.10.1 D845GEBV2 Form Factor

The Desktop Board D845GEBV2 is designed to fit into an ATX-form-factor chassis. Figure 19 illustrates the mechanical form factor for the Desktop Board D845GEBV2. Dimensions are given in inches [millimeters]. The outer dimensions are 12.00 inches by 8.20 inches [304.80 millimeters by 208.28 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification (see Section 1.5).

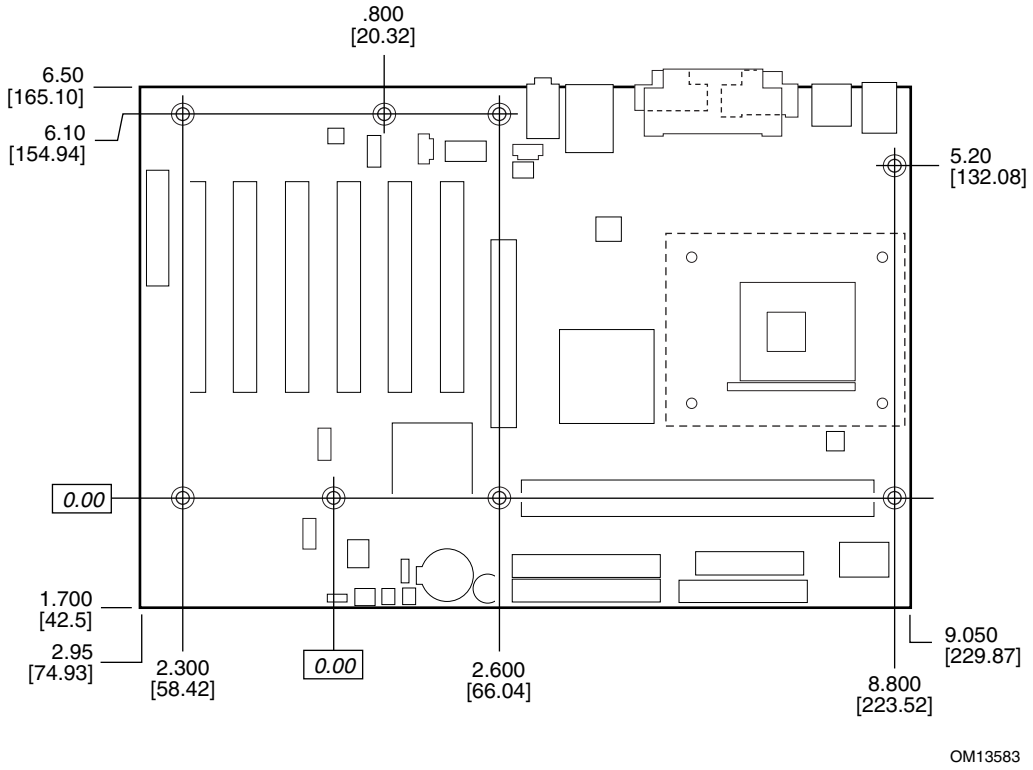



**Figure 19. Desktop Board D845GEBV2 Dimensions**

## 2.10.2 D845GERG2 Form Factor

The Desktop Board D845GERG2 is designed to fit into either a microATX or an ATX-form-factor chassis. Figure 20 illustrates the mechanical form factor for the Desktop Board D845GERG2. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 8.20 inches [243.84 millimeters by 208.28 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification (see Section 1.5).

### NOTE

*When installing the Desktop Board in a microATX chassis, make sure that peripheral devices are installed at least 1.5 inches above the main power connector, the diskette drive connector, and the IDE connector, and the DIMM sockets.*

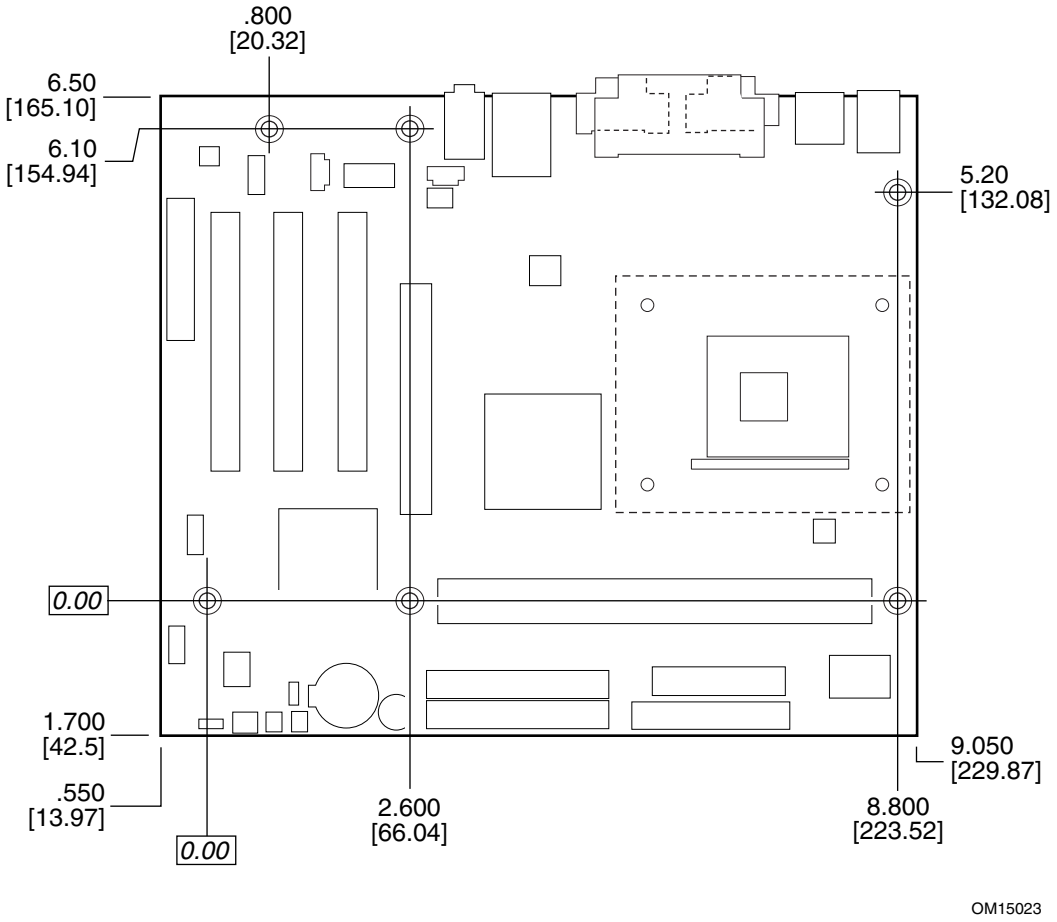



**Figure 20. Desktop Board D845GERG2 Dimensions**

## 2.10.3 I/O Shield

The back panel I/O shield for the Desktop Boards D845GEBV2 and D845GERG2 must meet specific dimension and material requirements. Systems based on these Desktop Boards need the back panel I/O shield to pass certification testing. Figure 21 shows the I/O shield for Desktop Boards with the onboard LAN subsystem. Figure 22 shows the I/O shield for Desktop Boards without the onboard LAN subsystem. Dimensions are given in inches to a tolerance of ±0.02 inches.

The figures also indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 1.5 for information about the ATX specification.

### NOTE

*The I/O shield drawings in this document are for reference only. An I/O shield compliant with the ATX chassis specification 2.03 is available from Intel.*

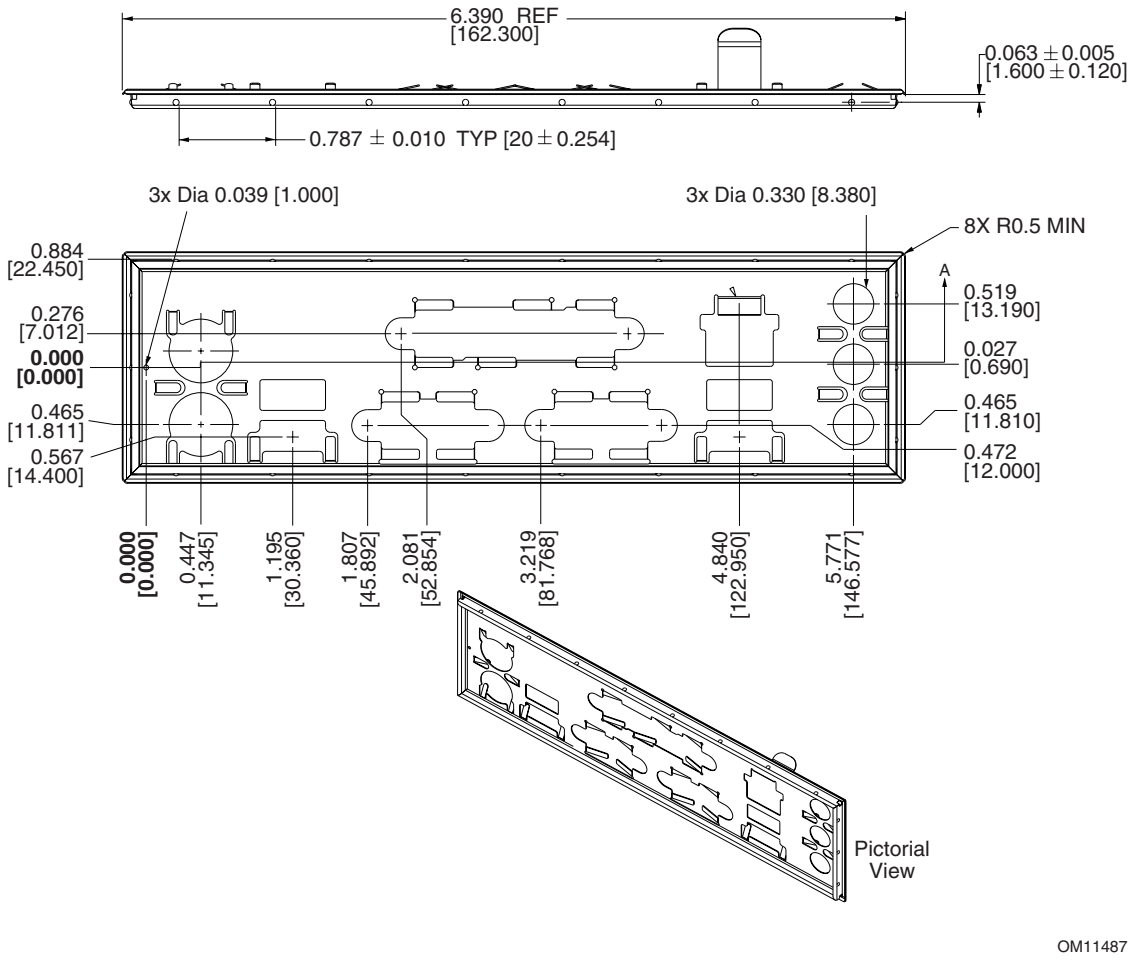



**Figure 21. I/O Shield Dimensions (for Desktop Boards with the LAN Subsystem)**

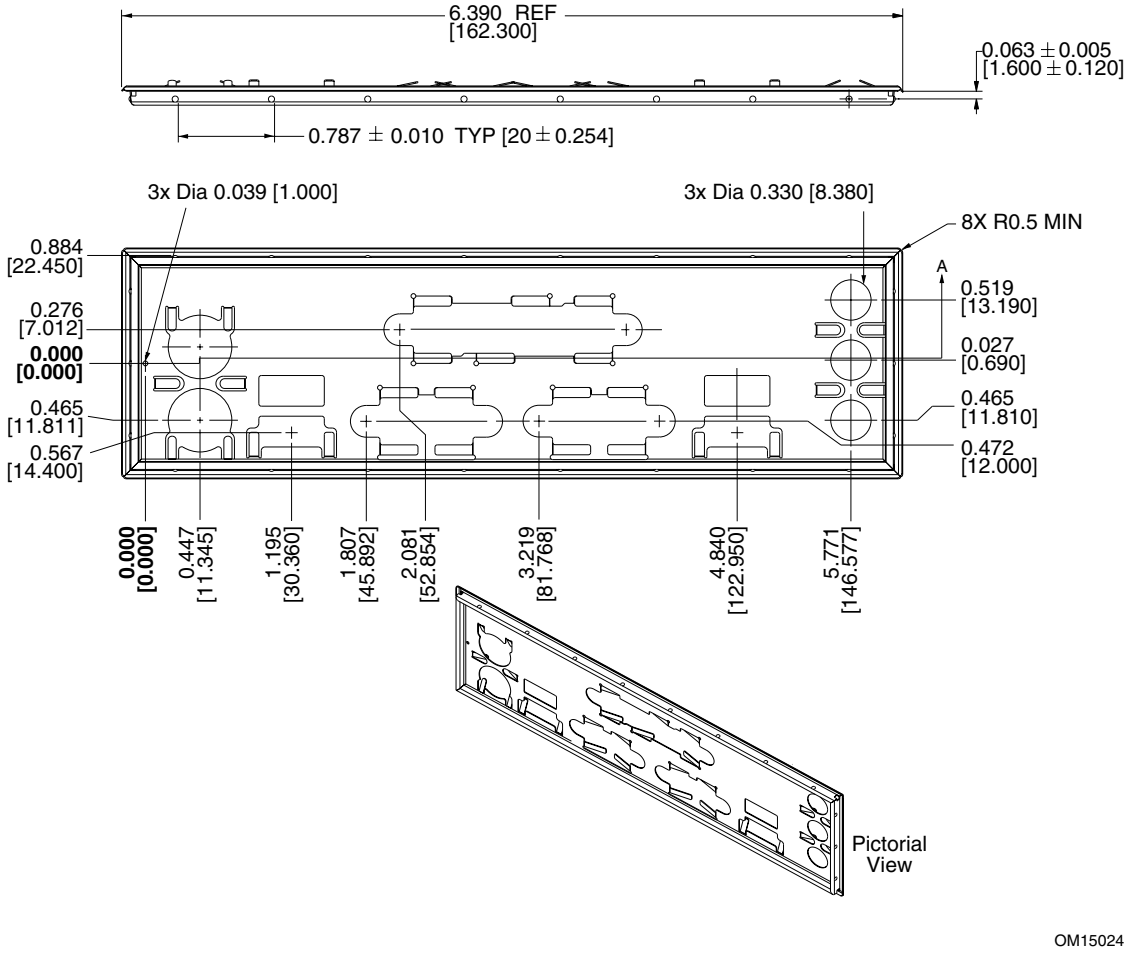



**Figure 22. I/O Shield Dimensions (for Desktop Boards with no LAN Subsystem)**

# 2.11 Electrical Considerations

## 2.11.1 Power Consumption

Table 42 lists voltage and current measurements for a computer that contains the Desktop Board D845GEBV2/D845GERG2 and the following:

- 2.80 GHz Intel Pentium 4 processor with a 512 KB cache
- 64 MB AGP add-in card
- 256 MB DDR 333 SDRAM
- 3.5-inch diskette drive
- 10 GB IDE hard disk drive
- 6.2 X IDE CD-ROM/32 X CD-ROM drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows XP desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with the computer is connected to a typical 300 W power supply, at nominal input voltage and frequency, with a true RMS wattmeter at the line input.

**NOTE**

*Actual system power consumption depends upon system configuration. The power supply should comply with the recommendations found in the ATX/ATX12V Power Supply Design Guide, Version 1.1 (see Section 1.5 on page 20 for specification information).*

**Table 42. Power Usage**

| | | DC Current at: | | | | |
|---|---|---|---|---|---|---|
| **Mode** | **AC Power** | **+3.3 V** | **+5 V** | **+12 V** | **-12 V** | **+5 VSB** |
| ACPI S0 | 163.0 W | 5.68 A | 1.52 A | 7.24 A | 67 mA | 396 mA |
| ACPI S1 | 93.0 W | 4.04 A | 0.51 A | 2.75 A | 38 mA | 152 mA |
| ACPI S3 | 3.6 W | 0 A | 0 mA | 0 A | 0 mA | 370 mA |
| ACPI S5 | 3.1 W | 0 A | 0 mA | 0 A | 0 mA | 290 mA |

## 2.11.2 Add-in Board Considerations

The Desktop Boards D845GEBV2 and D845GERG2 are designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards is as follows:

- For a fully loaded Desktop Board D845GEBV2 (all seven expansion slots filled), the total +5 V current draw must not exceed 14 A.
- For a fully loaded Desktop Board D845GERG2 (all four expansion slots filled), the total +5 V current draw must not exceed 8 A.

### 2.11.3 Standby Current Requirements

**CAUTION**

*If the standby current necessary to support multiple wake events from the PCI and/or USB buses exceeds power supply capacity, the Desktop Boards D845GEBV2 and D845GERG2 may lose register settings stored in memory, etc. Calculate the standby current requirements using the steps described below.*

Power supplies used with the Desktop Boards D845GEBV2 and D845GERG2 must be able to provide enough standby current to support the Instantly Available PC (ACPI S3 sleep state) configuration as outlined in Table 43 below.

Values are determined by specifications such as PCI 2.2. Actual measured values may vary.

To estimate the amount of standby current required for a particular system configuration, standby current requirements of all installed components must be added to determine the total standby current requirement. Refer to the descriptions in Table 43 and review the following steps.

1. Note the total Desktop Board D845GEBV2 or D845GERG2 standby current requirement.
2. Add to that the total PS/2 port standby current requirement if a wake-enabled device is connected.
3. Add, from the PCI 2.2 slots (wake enabled) row, the total number of wake-enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
4. Add, from the PCI 2.2 slots (nonwake enabled) row, the total number of wake-enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
5. Add all additional wake-enabled devices' and nonwake-enabled devices' standby current requirements as applicable.
6. Add all the required current totals from steps 1 through 5 to determine the total estimated standby current power supply requirement.

**Table 43. Standby Current Requirements**

| **Instantly Available PC Current Support (Estimated for Integrated Board Components)** | **Description** | **Standby Current Requirements (mA)** |
|---|---|---|
| | Total for Desktop Board D845GEBV2/D845GERG2 | 370 |
| **Instantly Available PC Stand-by Current Support**<br>• **Estimated for add-on components**<br>• **Add to Instantly Available PC total current requirement**<br>**(See instructions above)** | PS/2 ports (Note) | 345 |
| | PCI 2.2 slots (wake enabled) | 375 |
| | PCI 2.2 slots (nonwake enabled) | 20 |
| | CNR (Note) | 375 |
| | USB ports (Note) | 500 |

Note: Dependent upon system configuration

**NOTE**

*IBM PS/2 Port Specification (Sept 1991) states:*

- *275 mA for keyboard*
- *70 mA for the mouse (nonwake-enable device)*

*PCI/AGP requirements are calculated by totaling the following:*

- *One wake-enabled device @ 375 mA, plus*
- *Five nonwake-enabled devices @ 20 mA each, plus*

*USB requirements are calculated as:*

- *One wake-enabled device @ 500 mA*
- *USB hub @ 100 mA*
- *Three USB nonwake-enabled devices connected @ 2.5 mA each*

**NOTE**

*Both USB ports are capable of providing up to 500 mA during normal G0/S0 operation. Only one USB port will support up to 500 mA of stand-by-current (wake-enabled device) during G1/S3 suspended operation. The other port may provide up to 7.5 mA (three nonwake-enabled devices.) during G1/S3 suspended operation.*

### 2.11.4 Fan Connector Current Capability

Table 44 lists the current capability of the fan connectors on the Desktop Boards D845GEBV2 and D845GERG2.

**Table 44. Fan Connector Current Capability**

| | Maximum Available Current for Desktop Boards with the: | |
|---|---|---|
| **Fan Connector** | **Hardware Monitoring ASIC** | **Hardware Monitoring and Fan Control ASIC** |
| Processor fan | 1.00 A | 0.80 A |
| Front chassis fan | 0.50 A | 0.30 A |
| Rear chassis fan | 0.35 A | 0.30 A |

### 2.11.5 Power Supply Considerations

**CAUTION**

*The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 78 for additional information.*

System integrators should refer to the power usage values listed in Table 42 when selecting a power supply for use with the Desktop Board D845GEBV2 or D845GERG2.

Measurements account only for current sourced by the Desktop Board D845GEBV2 or D845GERG2 while running in idle modes of the started operating systems.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

| For information about | Refer to |
|---|---|
| The ATX form factor specification | Section 1.5, page 20 |

## 2.12 Thermal Considerations

**CAUTION**

*The use of an Intel Pentium 4 processor operating above 2.80 GHz with this Intel desktop board requires the following:*

- *A chassis with appropriate airflow to ensure proper cooling of the components on the board*
- *A processor fan heatsink that meets the thermal performance targets for Pentium 4 processors operating above 2.80 GHz*

*Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the desktop board. For a list of chassis that have been tested with Intel desktop boards please refer to the following website:*

http://developer.intel.com/design/motherbd/cooling.htm

*All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.*

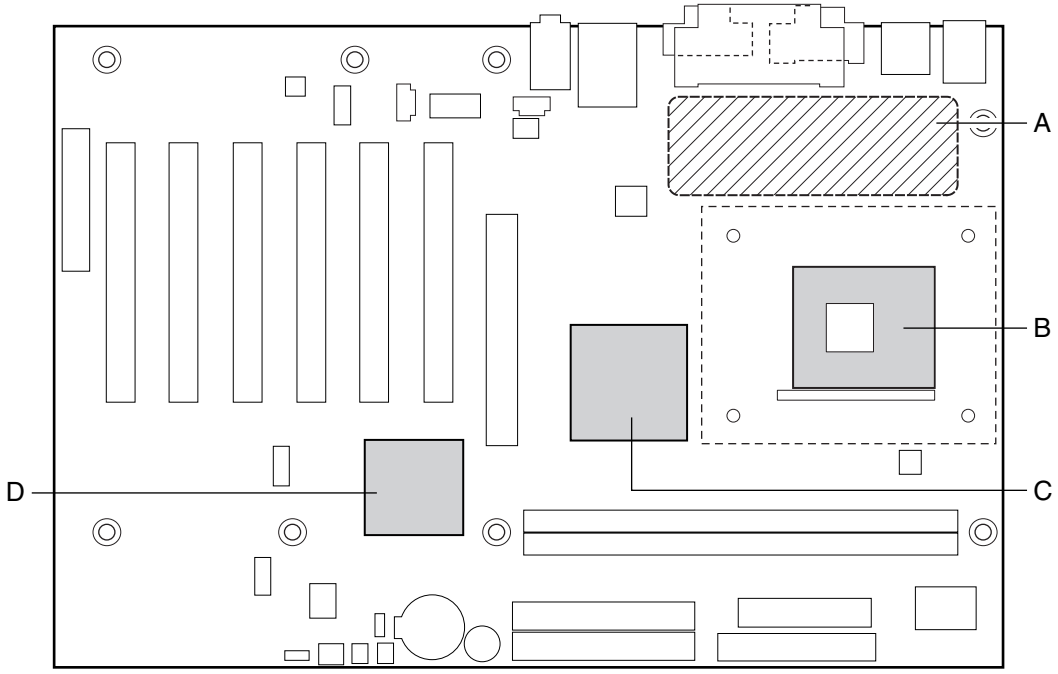
## CAUTION

*Ensure that the ambient temperature does not exceed the Desktop Board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.*

## CAUTION

*Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (item A in Figure 23) can reach a temperature of up to 85 °C in an open chassis.*

Figure 23 shows the locations of the localized high temperature zones.




| | |
|---|---|
| A | Processor voltage regulator area |
| B | Processor |
| C | Intel 82845GE GMCH |
| D | Intel 82801DB ICH4 |

**Figure 23. Localized High Temperature Zones**

Table 45 provides maximum case temperatures for the Desktop Board D845GEBV2/D845GERG2 components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the Desktop Board D845GEBV2/D845GERG2.

**Table 45. Thermal Considerations for Components**

| Component | Maximum Case Temperature |
|---|---|
| Intel Pentium 4 processor | For processor case temperature, see processor datasheets and processor specification updates |
| Intel 82845GE GMCH | 83 °C (under bias) |
| Intel 82801DB ICH4 | 110 °C (under bias) |

| For information about | Refer to |
|---|---|
| Intel Pentium 4 processor datasheets and specification updates | Section 1.3, page 19 |

## 2.13 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The MTBF data is calculated from predicted data at 55 ºC. The MTBF calculations for the Desktop Boards are as follows:

- Desktop Board D845GEBV2 MTBF: 108748 hours
- Desktop Board D845GERG2 MTBF: 111270 hours

## 2.14 Environmental

Table 46 lists the environmental specifications for the Desktop Boards D845GEBV2 and D845GERG2.

**Table 46. Desktop Board D845GEBV2/D845GERG2 Environmental Specifications**

| Parameter | Specification | | |
|---|---|---|---|
| **Temperature** | | | |
| Non-Operating | -40 °C to +70 °C | | |
| Operating | 0 °C to +55 °C | | |
| **Shock** | | | |
| Unpackaged | 50 g trapezoidal waveform | | |
| | Velocity change of 170 inches/second | | |
| Packaged | Half sine 2 millisecond | | |
| | Product Weight (pounds) | Free Fall (inches) | Velocity Change (inches/sec) |
| | <20 | 36 | 167 |
| | 21-40 | 30 | 152 |
| | 41-80 | 24 | 136 |
| | 81-100 | 18 | 118 |
| **Vibration** | | | |
| Unpackaged | 5 Hz to 20 Hz: 0.01 $g^2$ Hz sloping up to 0.02 $g^2$ Hz | | |
| | 20 Hz to 500 Hz: 0.02 $g^2$ Hz (flat) | | |
| Packaged | 10 Hz to 40 Hz: 0.015 $g^2$ Hz (flat) | | |
| | 40 Hz to 500 Hz: 0.015 $g^2$ Hz sloping down to 0.00015 $g^2$ Hz | | |

# 2.15 Regulatory Compliance

This section describes the Desktop Boards' compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

## 2.15.1 Safety Regulations

Table 47 lists the safety regulations the Desktop Boards D845GEBV2 and D845GERG2 comply with when correctly installed in a compatible host system.

**Table 47. Safety Regulations**

| Regulation | Title |
|---|---|
| CSA C22.2 No. 60950/ UL 60950, 3rd Edition, 2000 | Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada) |
| EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4) | The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union) |
| IEC 60950, 2nd Edition, 1991 (with Amendments 1, 2, 3, and 4) | The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International) |
| EMKO-TSE (74-SEC) 207/94 | Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland) |

## 2.15.2 EMC Regulations

Table 48 lists the EMC regulations the Desktop Boards D845GEBV2 and D845GERG2 comply with when correctly installed in a compatible host system.

**Table 48. EMC Regulations**

| Regulation | Title |
|---|---|
| FCC (Class B) | Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radio Frequency devices. (USA) |
| ICES-003 (Class B) | Interference-Causing Equipment Standard, Digital Apparatus. (Canada) |
| EN55022: 1998 (Class B) | Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union) |
| EN55024: 1998 | Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union) |
| AS/NZS 3548 (Class B) | Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand) |
| CISPR 22, 3rd Edition (Class B) | Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International) |
| CISPR 24: 1997 | Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International) |

### 2.15.3 Product Certification Markings (Board Level)

The Desktop Boards D845GEBV2 and D845GERG2 have the following product certification markings:

- UL joint US/Canada Recognized Component mark: Consists of lower case c followed by a stylized backward UR and followed by a small US. Includes adjacent UL file number for Intel Desktop Boards: E210882 (component side).
- FCC Declaration of Conformity logo mark for Class B equipment; to include Intel name and D845GEBV2 and D845GERG2 model designation (solder side).
- CE mark: Declaring compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) (component side). The CE mark should also be on the shipping container.
- Australian Communications Authority (ACA) C-Tick mark: consists of a stylized C overlaid with a check (tick) mark (component side), followed by Intel supplier code number, N-232. The C-tick mark should also be on the shipping container.
- Korean EMC certification logo mark: consists of MIC lettering within a stylized elliptical outline.
- Printed wiring board manufacturer's recognition mark: consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (solder side).
- PB part number: Intel bare circuit board part number (solder side). Also includes SKU number starting with AA followed by additional alphanumeric characters.
  - For the Desktop Board D845GEBV2, the PB number A97500-00x.
  - For the Desktop Board D845GERG2, the PB number is A97503-00x.
- Battery "+ Side Up" marking: located on the component side of the Desktop Board in close proximity to the battery holder.

# 3 Overview of BIOS Features

## What This Chapter Contains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## 3.1 Introduction

The Desktop Boards D845GEBV2 and D845GERG2 use an Intel/AMI BIOS that is stored in the Firmware Hub (FWH) and can be updated using a disk-based program. The FWH contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as RG84510A.86A.

When the Desktop Board's jumper is set to configuration mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

| For information about | Refer to |
|---|---|
| The Desktop Boards' compliance level with Plug and Play | Section 1.5, page 20 |

## 3.2 BIOS Flash Memory Organization

The Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable.

# 3.3 Resource Configuration

## 3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.5.

## 3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.5 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

**NOTE**

*ATA-66/100 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an ATA-66/100 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is reduced to that of the slowest device.*

**NOTE**

*Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.*

## 3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

| For information about | Refer to |
|---|---|
| The Desktop Boards' compliance level with SMBIOS | Section 1.5, page 20 |

## 3.5 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

**NOTE**

*Legacy USB support is for keyboards, mice, and hubs only. Other USB devices are not supported in legacy mode.*

## 3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities support the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Updating the BIOS boot block separately.
- Changing the language section of the BIOS.
- Updating replaceable BIOS modules, such as the video BIOS module.
- Inserting a custom splash screen.

**NOTE**

*Review the instructions distributed with the upgrade utility before attempting a BIOS update.*

| For information about | Refer to |
|---|---|
| The Intel World Wide Web site | Section 1.3, page 19 |

### 3.6.1 Language Support

The BIOS Setup program and help messages are supported in five languages: US English, German, Italian, French, and Spanish. The default language is US English, which is present unless another language is selected in the BIOS Setup program.

### 3.6.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site.

| For information about | Refer to |
|---|---|
| The Intel World Wide Web site | Section 1.3, page 19 |

## 3.7 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. You can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Update Utility are available from Intel Customer Support through the Intel World Wide Web site.

**NOTE**

*Even if the computer is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.*

| For information about | Refer to |
|---|---|
| The BIOS recovery mode jumper settings | Section 2.9.2, page 73 |
| The Boot menu in the BIOS Setup program | Section 4.7, page 115 |
| Contacting Intel customer support | Section 1.3, page 19 |

# 3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

## 3.8.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

| For information about | Refer to |
|---|---|
| The El Torito specification | Section 1.5, page 20 |

## 3.8.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces boot from the LAN.

## 3.8.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

## 3.8.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices (as set in the BIOS setup program's Boot Device Priority Submenu). Table 49 lists the boot device menu options.

**Table 49. Boot Device Menu Options**

| Boot Device Menu Function Keys | Description |
|---|---|
| <↑> or <↓> | Selects a default boot device |
| <Enter> | Exits the menu, saves changes, and boots from the selected device |
| <Esc> | Exits the menu without saving changes |

# 3.9 Fast Booting Systems with Intel® Rapid BIOS Boot

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel Rapid® BIOS

## 3.9.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as “power-up to data ready” less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

## 3.9.2 Intel Rapid BIOS Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot Menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enabled Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive.

In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

**NOTE**

*It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.*

*This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from three to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the IDE Configuration Submenu of the BIOS Setup program).*

| For information about | Refer to |
|---|---|
| IDE Configuration Submenu in the BIOS Setup program | Section 4.4.4, page 103 |

## 3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 50 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

**Table 50. Supervisor and User Password Functions**

| Password Set | Supervisor Mode | User Mode | Setup Options | Password to Enter Setup | Password During Boot |
|---|---|---|---|---|---|
| Neither | Can change all options (Note) | Can change all options (Note) | None | None | None |
| Supervisor only | Can change all options | Can change a limited number of options | Supervisor Password | Supervisor | None |
| User only | N/A | Can change all options | Enter Password<br>Clear User Password | User | User |
| Supervisor and user set | Can change all options | Can change a limited number of options | Supervisor Password<br>Enter Password | Supervisor or user | Supervisor or user |

Note: If no password is set, any user can change all Setup options.

| For information about | Refer to |
|---|---|
| Setting user and supervisor passwords | Section 4.4.10, page 112 |

# 4 BIOS Setup Program

## What This Chapter Contains


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## 4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

| | | | | | | |
|---|---|---|---|---|---|---|
| Maintenance | Main | Advanced | Security | Power | Boot | Exit |

Table 51 lists the BIOS Setup program menu features.

**Table 51. BIOS Setup Program Menu Bar**

| Maintenance | Main | Advanced | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|
| Clears passwords and BIS credentials and enables extended configuration mode | Allocates resources for hardware components | Configures advanced features available through the chipset | Sets passwords and security features | Configures power management features | Selects boot options and power supply controls | Saves or discards changes to Setup program options |

| For information about | Refer to |
|---|---|
| Boot Integrity Services (BIS) | Section 1.5, page 20 |

**NOTE**

*In this chapter, all examples of the BIOS Setup program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the Desktop Board is in configuration mode. Section 2.9.2 on page 73 tells how to put the Desktop Board in configuration mode.*

Table 52 lists the function keys available for menu screens.

**Table 52. BIOS Setup Program Function Keys**

| BIOS Setup Program Function Key | Description |
|---|---|
| <←> or <→> | Selects a different menu screen (Moves the cursor left or right) |
| <↑> or <↓> | Selects an item (Moves the cursor up or down) |
| <Tab> | Selects a field (Not implemented) |
| <Enter> | Executes command or selects the submenu |
| <F9> | Load the default configuration values for the current menu |
| <F10> | Save the current values and exits the BIOS Setup program |
| <Esc> | Exits the menu |

## 4.2 Maintenance Menu

To access this menu, select Maintenance on the menu bar at the top of the screen.

| **Maintenance** | Main | Advanced | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

The menu shown in Table 53 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 2.9.2 on page 73 for configuration mode setting information.

**Table 53. Maintenance Menu**

| Feature | Options | Description |
|---|---|---|
| Clear All Passwords | • **Ok (default)**<br>• Cancel | Clears the user and supervisor passwords. |
| Clear BIS Credentials | • **Ok (default)**<br>• Cancel | Clears the Wired for Management Boot Integrity Service (BIS) credentials. |
| CPU Stepping Signature | No options | Displays CPU's Stepping Signature. |
| CPU Microcode Update Revision | No options | Displays CPU's Microcode Update Revision. |

## 4.3 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

| Maintenance | **Main** | Advanced | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

Table 54 describes the Main menu. This menu reports processor and memory information and is for configuring the system date and system time.

**Table 54. Main Menu**

| Feature | Options | Description |
|---|---|---|
| BIOS Version | No options | Displays the version of the BIOS. |
| Processor Type | No options | Displays processor type. |
| Hyper-Threading Technology | • Disabled<br>• **Enabled (default)** | Disables/enables Hyper-Threading Technology. This option is present only when a processor that supports Hyper-Threading Technology is installed. |
| Processor Speed | No options | Displays processor speed. |
| System Bus Speed | No options | Displays the system bus speed. |
| System Memory Speed | No options | Displays the system memory speed. |
| Cache RAM | No options | Displays the size of second-level cache. |
| Total Memory | No options | Displays the total amount of RAM. |
| Memory Bank 0<br>Memory Bank 1 | No options | Displays the amount and type of RAM in the memory banks. |
| Language | • **English (default)**<br>• Francais | Selects the current default language used by the BIOS. |
| System Time | Hour, minute, and second | Specifies the current time. |
| System Date | Day of week<br>Month/day/year | Specifies the current date. |

## 4.4 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |
| USB Configuration |
| Chipset Configuration |
| Fan Control Configuration |

Table 55 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

**Table 55. Advanced Menu**

| Feature | Options | Description |
|---|---|---|
| PCI Configuration | Select to display submenu | Configures individual PCI slot's IRQ priority. |
| Boot Configuration | Select to display submenu | Configures Plug and Play and the Numlock key, and resets configuration data. |
| Peripheral Configuration | Select to display submenu | Configures peripheral ports and devices. |
| IDE Configuration | Select to display submenu | Specifies type of connected IDE devices. |
| Diskette Configuration | Select to display submenu | Configures the diskette drive. |
| Event Log Configuration | Select to display submenu | Configures Event Logging. |
| Video Configuration | Select to display submenu | Configures video features. |
| USB Configuration | Select to display submenu | Configures USB support. |
| Chipset Configuration | Select to display submenu | Configures advanced chipset features. |
| Fan Control Configuration | Select to display submenu | Configures fan control options. |

### 4.4.1 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar and then PCI Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| **PCI Configuration** |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |
| USB Configuration |
| Chipset Configuration |
| Fan Control Configuration |

The submenu shown in Table 56 is used to configure the IRQ priority of PCI slots individually.

**Table 56. PCI Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| PCI Slot1 IRQ Priority (Note 1) | • **Auto (default)**<br>• 5<br>• 9<br>• 10<br>• 11 | Allows selection of IRQ priority for PCI bus connector 1. |
| PCI Slot2 IRQ Priority (Note 1) | • **Auto (default)**<br>• 5<br>• 9<br>• 10<br>• 11 | Allows selection of IRQ priority for PCI bus connector 2. |
| PCI Slot3 IRQ Priority (Note 1) | • **Auto (default)**<br>• 5<br>• 9<br>• 10<br>• 11 | Allows selection of IRQ priority for PCI bus connector 3. |
| PCI Slot4 IRQ Priority (Note 1, Note 2) | • **Auto (default)**<br>• 5<br>• 9<br>• 10<br>• 11 | Allows selection of IRQ priority for PCI bus connector 4. |

continued

**Table 56. PCI Configuration Submenu** (continued)

| Feature | Options | Description |
|---|---|---|
| PCI Slot5 IRQ Priority<br>(Note 1, Note 2) | • **Auto (default)**<br>• 5<br>• 9<br>• 10<br>• 11 | Allows selection of IRQ priority for PCI bus connector 5. |
| PCI Slot6 IRQ Priority<br>(Note 1, Note 2) | • **Auto (default)**<br>• 5<br>• 9<br>• 10<br>• 11 | Allows selection of IRQ priority for PCI bus connector 6. |

Notes

1. Additional interrupts may be available if certain onboard devices (such as the serial and parallel ports) are disabled.
2. This option appears only on the Desktop Board D845GEBV2.

## 4.4.2 Boot Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Boot Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| **Boot Configuration** |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |
| USB Configuration |
| Chipset Configuration |
| Fan Control Configuration |

The submenu represented by Table 57 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

**Table 57. Boot Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Plug & Play O/S | • **No (default)**<br>• Yes | Specifies if manual configuration is desired.<br>*No* lets the BIOS configure all devices. This setting is appropriate when using a Plug and Play operating system.<br>*Yes* lets the operating system configure Plug and Play devices not required to boot the system. This option is available for use during lab testing. |
| Numlock | • Off<br>• **On (default)** | Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard. |

## 4.4.3 Peripheral Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Peripheral Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| **Peripheral Configuration** |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |
| USB Configuration |
| Chipset Configuration |
| Fan Control Configuration |

The submenu represented in Table 58 is used for configuring computer peripherals.

**Table 58. Peripheral Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Serial Port A | • Disabled<br>• Enabled<br>• **Auto (default)** | Configures serial port A.<br>*Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4.<br>An * (asterisk) displayed next to an address indicates a conflict with another device. |
| Base I/O address<br>(This feature is present only when Serial Port A is set to *Enabled*) | • **3F8 (default)**<br>• 2F8<br>• 3E8<br>• 2E8 | Specifies the base I/O address for serial port A, if serial port A is set to *Enabled*. |
| Interrupt<br>(This feature is present only when Serial Port A is set to *Enabled*) | • IRQ 3<br>• **IRQ 4 (default)** | Specifies the interrupt for serial port A, if serial port A is set to *Enabled*. |
| Parallel port | • Disabled<br>• Enabled<br>• **Auto (default)** | Configures the parallel port.<br>*Auto* assigns LPT1 the address 378h and the interrupt IRQ7.<br>An * (asterisk) displayed next to an address indicates a conflict with another device. |
| Mode | • Output Only<br>• **Bi-directional (default)**<br>• EPP<br>• ECP | Selects the mode for the parallel port. Not available if the parallel port is disabled.<br>*Output Only* operates in AT†-compatible mode.<br>*Bi-directional* operates in PS/2-compatible mode.<br>*EPP* is Extended Parallel Port mode, a high-speed bi-directional mode.<br>*ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode. |

continued

**Table 58. Peripheral Configuration Submenu** (continued)

| Feature | Options | Description |
|---|---|---|
| Base I/O address<br>(This feature is present only when Parallel Port is set to *Enabled*) | • **378 (default)**<br>• 278 | Specifies the base I/O address for the parallel port. |
| Interrupt<br>(This feature is present only when Parallel Port is set to *Enabled*) | • IRQ 5<br>• **IRQ 7 (default)** | Specifies the interrupt for the parallel port. |
| DMA<br>(This feature is present only when Parallel Port Mode is set to *ECP*) | • 1<br>• **3 (default)** | Specifies the DMA channel. |
| Audio | • **Enabled (default)**<br>• Disabled | Enables or disables the onboard audio subsystem.<br>For boards with no onboard audio subsystem, this option does not appear. |
| LAN Device | • Disabled<br>• **Enabled (default)** | Enables or disables the onboard LAN device.<br>For boards with no onboard LAN subsystem, this option will not appear. |

### 4.4.4 IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar and then IDE Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| **IDE Configuration** |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |
| USB Configuration |
| Chipset Configuration |
| Fan Control Configuration |

The menu represented in Table 59 is used to configure IDE device options.

**Table 59. IDE Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| IDE Controller | • Disabled<br>• Primary<br>• Secondary<br>• **Both (default)** | Specifies the integrated IDE controller.<br>*Primary* enables only the primary IDE controller.<br>*Secondary* enables only the secondary IDE controller.<br>*Both* enables both IDE controllers. |
| PCI IDE Bus Master | • Disabled<br>• **Enabled (default)** | Enables/disables the use of DMA for hard drive BIOS INT13 reads and writes. |
| Hard Disk Pre-Delay | • **Disabled (default)**<br>• 3 Seconds<br>• 6 Seconds<br>• 9 Seconds<br>• 12 Seconds<br>• 15 Seconds<br>• 21 Seconds<br>• 30 Seconds | Specifies the hard disk drive pre-delay. |
| Primary IDE Master | Select to display sub-menu | Reports type of connected IDE device. |
| Primary IDE Slave | Select to display sub-menu | Reports type of connected IDE device. |
| Secondary IDE Master | Select to display sub-menu | Reports type of connected IDE device. |
| Secondary IDE Slave | Select to display sub-menu | Reports type of connected IDE device. |

### 4.4.4.1 Primary/Secondary IDE Master/Slave Submenus

To access these submenus, select Advanced on the menu bar, then IDE Configuration, and then the master or slave to be configured.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|
| | | PCI Configuration | | | | |
| | | Boot Configuration | | | | |
| | | Peripheral Configuration | | | | |
| | | **IDE Configuration**<br>**Primary IDE Master**<br>**Primary IDE Slave**<br>**Secondary IDE Master**<br>**Secondary IDE Slave** | | | | |
| | | Diskette Configuration | | | | |
| | | Event Log Configuration | | | | |
| | | Video Configuration | | | | |
| | | USB Configuration | | | | |
| | | Chipset Configuration | | | | |
| | | Fan Control Configuration | | | | |

There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 60 shows the format of the IDE submenus. For brevity, only one example is shown.

**Table 60. Primary/Secondary IDE Master/Slave Submenus**

| Feature | Options | Description |
|---|---|---|
| Drive Installed | No options | Displays the type of drive installed. |
| Type | • **Auto (default)**<br>• User | Specifies the IDE configuration mode for IDE devices.<br>*User* allows capabilities to be changed.<br>*Auto* fills-in capabilities from ATA/ATAPI device. |
| Maximum Capacity | No options | Displays the capacity of the drive. |
| LBA/Large Mode | • Disabled<br>• **Auto (default)** | Selects the translation mode for the IDE hard disk.<br>(This item is read-only unless Type is set to *User*.) |
| Block Mode | • Disabled<br>• **Auto (default)** | *Disabled* = Data transfers to/from the device occur one sector at a time.<br>*Auto* = Data transfers to/from the device occur multiple sectors at a time if the device supports block mode transfers.<br>(This item is read-only unless Type is set to *User*.) |
| PIO Mode | • **Auto (default)**<br>• 0<br>• 1<br>• 2<br>• 3<br>• 4 | Specifies the PIO mode.<br>(This item is read-only unless Type is set to *User*.) |

continued

**Table 60. Primary/Secondary IDE Master/Slave Submenus** (continued)

| Feature | Options | Description |
|---|---|---|
| DMA Mode | • **Auto (default)**<br>• SWDMA0<br>• SWDMA1<br>• SWDMA2<br>• MWDMA0<br>• MWDMA1<br>• MWDMA2<br>• UDMA0<br>• UDMA1<br>• UDMA2<br>• UDMA3<br>• UDMA4<br>• UDMA5 | Specifies the DMA mode for the drive.<br>*Auto* = Auto-detected<br>*SWDMAn* = Single Word DMA*n*<br>*SWDMAn* = Multi Word DMA*n*<br>*UDMAn* = Ultra DMA*n*<br><br>(This item is read-only unless Type is set to *User*.) |
| S.M.A.R.T. | • **Auto (default)**<br>• Disabled<br>• Enabled | Enables/disables S.M.A.R.T. (Self-Monitoring, Analysis, and Reporting Technology).<br>(This item is read-only unless Type is set to *User*.) |
| Cable Detected | No options | Displays the type of cable connected to the IDE interface: 40-conductor or 80-conductor (for ATA-100 peripherals). |

## 4.4.5 Diskette Configuration Submenu

To access this menu, select Advanced on the menu bar and then Diskette Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| **Diskette Configuration** |
| Event Log Configuration |
| Video Configuration |
| USB Configuration |
| Chipset Configuration |
| Fan Control Configuration |

The submenu represented by Table 61 is used for configuring the diskette drive.

**Table 61. Diskette Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Diskette Controller | • Disabled<br>• **Enabled (default)** | Disables or enables the integrated diskette controller. |
| Floppy A | • Not Installed<br>• 360 KB 5¼"<br>• 1.2 MB 5¼"<br>• 720 KB 3½"<br>• **1.44 MB 3½" (default)**<br>• 2.88 MB 3½" | Specifies the capacity and physical size of diskette drive A. |
| Diskette Write Protect | • **Disabled (default)**<br>• Enabled | Disables or enables write protection for the diskette drive. |

## 4.4.6 Event Log Configuration Submenu

To access this menu, select Advanced on the menu bar and then Event Log Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| **Event Log Configuration** |
| Video Configuration |
| USB Configuration |
| Chipset Configuration |
| Fan Control Configuration |

The submenu represented by Table 62 is used to configure the event logging features.

**Table 62. Event Log Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Event Log | No options | Indicates if there is space available in the event log. |
| View Event Log | [Enter] | Displays the event log. |
| Clear All Event Logs | • **Ok (default)**<br>• Cancel | Clears the event log after rebooting. |
| Mark Events As Read | • **Ok (default)**<br>• Cancel | Marks all events as read. |

## 4.4.7 Video Configuration Submenu

To access this menu, select Advanced on the menu bar and then Video Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| **Video Configuration** |
| USB Configuration |
| Chipset Configuration |
| Fan Control Configuration |

The submenu represented in Table 63 is for configuring the video features.

**Table 63. Video Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Graphics Aperture Size | • 4 MB<br>• 8 MB<br>• 16 MB<br>• 32 MB<br>• **64 MB (default)**<br>• 128 MB<br>• 256 MB | Sets the aperture size for the video controller. |
| Primary Video Adapter | • **AGP (default)**<br>• PCI | Selects primary video adapter to be used during boot. |
| Frame Buffer Size | • **512 KB (default)**<br>• 1 MB<br>• 8 MB | Control how much system RAM is reserved for use by the internal graphics device. A larger frame buffer should provide higher performance. |

## 4.4.8 USB Configuration Submenu

To access this menu, select Advanced on the menu bar and then USB Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |
| **USB Configuration** |
| Chipset Configuration |
| Fan Control Configuration |

The submenu represented in Table 64 is for configuring the USB features.

**Table 64. USB Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| High-speed USB | • Disabled<br>• **Enabled (default)** | Set to *Disabled* when a USB 2.0 driver is not available. |
| Legacy USB Support | • Disabled<br>• **Enabled (default)** | Enables/disables legacy USB support. |

## 4.4.9 Chipset Configuration Submenu

To access this menu, select Advanced on the menu bar and then Chipset Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |
| USB Configuration |
| **Chipset Configuration** |
| Fan Control Configuration |

The submenu represented in Table 65 is for configuring the chipset options.

**Table 65. Chipset Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| ISA Enable Bit | • **Enabled (default)**<br>• Disabled | When set to *Enable*, a PCI-to-PCI bridge will only recognize I/O addresses that do not alias to an ISA range (within the bridge's assigned I/O range). |
| PCI Latency Timer | • **32 (default)**<br>• 64<br>• 96<br>• 128<br>• 160<br>• 192<br>• 224<br>• 248 | Allows you to control the time (in PCI bus clock cycles) that an agent on the PC bus can hold the bus when another agent has requested the bus. |
| Extended Configuration | • **Default (default)**<br>• User Defined | Allows the setting of extended configuration options. |
| SDRAM Frequency | • **Auto (default)**<br>• 266 MHz<br>• 333 MHz | Allows override of detected memory frequency value.<br>NOTE: If SDRAM Frequency is changed, you must reboot for the change to take effect. After changing this setting and rebooting, the System Memory Speed parameter in the Main menu will reflect the new value. |
| SDRAM Timing Control | • **Auto (default)**<br>• Manual – Aggressive<br>• Manual – User Defined | *Auto* = Timings will be programmed according to the memory detected.<br>*Manual – Aggressive* = Selects most aggressive user-defined timings.<br>*Manual – User Defined* = Allows manual override of detected SDRAM settings. |

continued

**Table 65. Primary/Secondary IDE Master/Slave Submenus** (continued)

| Feature | Options | Description |
|---|---|---|
| SDRAM RAS# Active to Precharge | • 8<br>• 7<br>• **6 (default)**<br>• 5 | Corresponds to tRAS. |
| SDRAM CAS# Latency | • **2.0 (default)**<br>• 2.5 | Selects the number of clock cycles required to address a column in memory. |
| SDRAM RAS# to CAS# Delay | • 4<br>• **3 (default)**<br>• 2 | Selects the number of clock cycles between addressing a row and addressing a column. |
| SDRAM RAS# Precharge | • 4<br>• **3 (default)**<br>• 2 | Selects the length of time required before accessing a new row. |

## 4.4.10 Fan Control Configuration Submenu

To access this menu, select Advanced on the menu bar and then Fan Control Configuration.

| Maintenance | Main | **Advanced** | Security | Power | Boot | Exit |
|---|---|---|---|---|---|---|

| |
|---|
| PCI Configuration |
| Boot Configuration |
| Peripheral Configuration |
| IDE Configuration |
| Diskette Configuration |
| Event Log Configuration |
| Video Configuration |
| USB Configuration |
| Chipset Configuration |
| **Fan Control Configuration** |

The submenu represented in Table 66 is for configuring the fan control options.

**Table 66. Fan Control Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Fan Control | • Disabled<br>• **Enabled (default)** | Disables/enables fan control. |
| Lowest Fan Speed | • **Slow (default)**<br>• Off | Defines the lower limit of chassis fan speed operation.<br>*Slow* = At low system temperatures, the fans will continue to run at a slow speed.<br>*Off* = At low system temperatures, the fans will turn off. |

### NOTE

*These options will not take effect until power has been completely removed from the system. After saving the BIOS settings and turning the system off, unplug the power cord and wait at least 30 seconds before re-applying power and turning the system back on.*

# 4.5 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

| Maintenance | Main | Advanced | **Security** | Power | Boot | Exit |
|---|---|---|---|---|---|---|

The menu represented by Table 67 is for setting passwords and security features.

**Table 67. Security Menu**

| **If no password entered previously:** | | |
|---|---|---|
| **Feature** | **Options** | **Description** |
| Supervisor Password | No options | Reports if there is a supervisor password set. |
| User Password | No options | Reports if there is a user password set. |
| Set Supervisor Password | Password can be up to seven alphanumeric characters. | Specifies the supervisor password. |
| User Access Level (Note 1) | • No Access<br>• View Only<br>• Limited<br>• **Full (default)** | Sets BIOS Setup Utility access rights for user level. |
| Set User Password | Password can be up to seven alphanumeric characters. | Specifies the user password. |
| Clear User Password (Note 2) | • **Ok (default)**<br>• Cancel | Clears the user password. |
| Chassis Intrusion | • **Disabled (default)**<br>• Log,<br>• Log, notify once<br>• Log, notify til cleared | *Disabled* = Disables Chassis Intrusion<br>*Log* = Logs the intrusion in the event log<br>*Log, notify once* = Halts system during POST. User must press <F4> to continue. Intrusion flag is cleared and the event log is updated.<br>Log, notify til cleared = Halts system during POST. User must enter BIOS setup Security Menu and select “Clear Chassis Intrusion Status” to clear the Chassis intrusion flag. |

Notes:

1. This feature appears only if a supervisor password has been set.
2. This feature appears only if a user password has been set.
3. This feature appears only if the Chassis Intrusion log, *notify til cleared* option has been set.

# 4.6 Power Menu

To access this menu, select Power from the menu bar at the top of the screen.

| Maintenance | Main | Advanced | Security | **Power** | Boot | Exit |
|---|---|---|---|---|---|---|
| | | | | ACPI | | |

The menu represented in Table 68 is for setting the power management features.

**Table 68. Power Menu**

| Feature | Options | Description |
|---|---|---|
| ACPI | Select to display submenu | Sets the ACPI power management options. |
| After Power Failure | • Stay Off<br>• **Last State (default)**<br>• Power On | Specifies the mode of operation if an AC power loss occurs.<br>*Stay Off* keeps the power off until the power button is pressed.<br>*Last State* restores the previous power state before power loss occurred.<br>*Power On* restores power to the computer. |
| Wake on PCI PME | • **Stay Off (default)**<br>• Power On | Specifies how the computer responds to a PCI power management event. |

## 4.6.1 ACPI Submenu

To access this menu, select Power from the menu bar at the top of the screen and then ACPI.

| Maintenance | Main | Advanced | Security | **Power** | Boot | Exit |
|---|---|---|---|---|---|---|
| | | | | **ACPI** | | |

The submenu represented in Table 69 is for setting the ACPI power options.

**Table 69. ACPI Submenu**

| Feature | Options | Description |
|---|---|---|
| ACPI Suspend State | • S1 State<br>• S3 State | S1 is the safest mode but consumes more power. S3 consumes less power, but some drivers may not support this state. |
| Wake on LAN from S5 | • **Stay Off (default)**<br>• Power On | In ACPI soft-off mode only, determines how the system responds to a LAN wake-up event. |

# 4.7 Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

| Maintenance | Main | Advanced | Security | Power | **Boot** | Exit |
|---|---|---|---|---|---|---|
| | | | | | Boot Device Priority | |
| | | | | | Hard Disk Drives | |
| | | | | | Removable Devices | |
| | | | | | ATAPI CD-ROM Drives | |

The menu represented in Table 70 is used to set the boot features and the boot sequence.

**Table 70. Boot Menu**

| Feature | Options | Description |
|---|---|---|
| Silent Boot | • Disabled<br>• **Enabled (default)** | *Disabled* displays normal POST messages.<br>*Enabled* displays OEM graphic instead of POST messages. |
| Intel(R) Rapid BIOS Boot | • Disabled<br>• **Enabled (default)** | Enables the computer to boot without running certain POST tests. |
| Scan User Flash Area | • Disabled<br>• **Enabled (default)** | Enables the BIOS to scan the flash memory for user binary files that are executed at boot time. |
| PXE Boot to LAN | • **Disabled (default)**<br>• Enabled | Disables/enables PXE boot to LAN.<br>Note: When set to *Enabled*, you must reboot for the Intel Boot Agent device to be available in the Boot Device menu. |
| USB Boot | • Disabled<br>• **Enabled (default)** | Disables/enables booting to USB boot devices. |
| Boot Device Priority | Select to display submenu | Specifies the boot sequence from the available types of boot devices. |
| Hard Disk Drives | Select to display submenu | Specifies the boot sequence from the available hard disk drives. |
| Removable Devices | Select to display submenu | Specifies the boot sequence from the available removable devices. |
| ATAPI CD-ROM Drives | Select to display submenu | Specifies the boot sequence from the available ATAPI CD-ROM drives. |

## 4.7.1 Boot Device Priority Submenu

To access this menu, select Boot on the menu bar and then Boot Devices Priority.

| Maintenance | Main | Advanced | Security | Power | **Boot** | Exit |
|---|---|---|---|---|---|---|
| | | | | | **Boot Device Priority** | |
| | | | | | Hard Disk Drives | |
| | | | | | Removable Devices | |
| | | | | | ATAPI CD-ROM Drives | |

The submenu represented in Table 71 is for setting boot devices priority.

**Table 71. Boot Device Priority Submenu**

| Feature | Options | Description |
|---|---|---|
| 1st Boot Device<br>2nd Boot Device<br>3rd Boot Device<br>4th Boot Device | • Removable Dev.<br>• Hard Drive<br>• ATAPI CD-ROM<br>• Intel® Boot Agent (Note)<br>• Disabled | Specifies the boot sequence according to the device type. The computer will attempt to boot from up to five devices as specified here. Only one of the devices can be an IDE hard disk drive. To specify boot sequence:<br>1. Select the boot device with <↑> or <↓>.<br>2. Press <Enter> to set the selection as the intended boot device.<br>The default settings for the first through fourth boot devices are, respectively:<br>• Removable Dev.<br>• Hard Drive<br>• ATAPI CD-ROM<br>• Intel Boot Agent |

Note: The boot device identifier for Intel Boot Agent (IBA) may vary depending on the BIOS release.

## 4.7.2 Hard Disk Drives Submenu

To access this menu, select Boot on the menu bar and then Hard Disk Drives.

| Maintenance | Main | Advanced | Security | Power | **Boot** | Exit |
|---|---|---|---|---|---|---|
| | | | | | Boot Device Priority | |
| | | | | | **Hard Disk Drives** | |
| | | | | | Removable Devices | |
| | | | | | ATAPI CD-ROM Drives | |

The submenu represented in Table 72 is for setting hard disk drive priority.

**Table 72. Hard Disk Drives Submenu**

| Feature | Options | Description |
|---|---|---|
| 1st Hard Disk Drive (Note) | Dependent on installed hard drives | Specifies the boot sequence from the available hard disk drives. To specify boot sequence:<br>1. Select the boot device with <↑> or <↓>.<br>2. Press <Enter> to set the selection as the intended boot device. |

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to twelve hard disk drives, the maximum number of hard disk drives supported by the BIOS.

## 4.7.3 Removable Devices Submenu

To access this menu, select Boot on the menu bar, then Removable Devices.

| Maintenance | Main | Advanced | Security | Power | **Boot** | Exit |
|---|---|---|---|---|---|---|
| | | | | | Boot Device Priority | |
| | | | | | Hard Disk Drives | |
| | | | | | **Removable Devices** | |
| | | | | | ATAPI CD-ROM Drives | |

The submenu represented in Table 73 is for setting removable device priority.

**Table 73. Removable Devices Submenu**

| Feature | Options | Description |
|---|---|---|
| 1st Removable Device (Note) | Dependent on installed removable devices | Specifies the boot sequence from the available removable devices. To specify boot sequence:<br>1. Select the boot device with <↑> or <↓>.<br>2. Press <Enter> to set the selection as the intended boot device. |

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four removable devices, the maximum number of removable devices supported by the BIOS.

### 4.7.4 ATAPI CD-ROM Drives Submenu

To access this menu, select Boot on the menu bar and then ATAPI CD-ROM Drives.

| Maintenance | Main | Advanced | Security | Power | **Boot** | Exit |
|---|---|---|---|---|---|---|
| | | | | | Boot Device Priority | |
| | | | | | Hard Disk Drives | |
| | | | | | Removable Devices | |
| | | | | | **ATAPI CD-ROM Drives** | |

The submenu represented in Table 74 is for setting ATAPI CD-ROM drive priority.

**Table 74. ATAPI CD-ROM Drives Submenu**

| Feature | Options | Description |
|---|---|---|
| 1st ATAPI CDROM (Note) | Dependent on installed ATAPI CD-ROM drives | Specifies the boot sequence from the available ATAPI CD-ROM drives. To specify boot sequence:<br>1. Select the boot device with <↑> or <↓>.<br>2. Press <Enter> to set the selection as the intended boot device. |

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four ATAPI CD-ROM drives, the maximum number of ATAPI CD-ROM drives supported by the BIOS.

## 4.8 Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

| Maintenance | Main | Advanced | Security | Power | Boot | **Exit** |
|---|---|---|---|---|---|---|

The menu represented in Table 75 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

**Table 75. Exit Menu**

| Feature | Description |
|---|---|
| Exit Saving Changes | Exits and saves the changes in CMOS SRAM. |
| Exit Discarding Changes | Exits without saving any changes made in the BIOS Setup program. |
| Load Optimal Defaults | Loads the optimal default values for all the Setup options. |
| Load Custom Defaults | Loads the custom defaults for Setup options. |
| Save Custom Defaults | Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults. |
| Discard Changes | Discards changes without exiting Setup. The option values present when the computer was turned on are used. |

# 5 Error Messages and Beep Codes

## What This Chapter Contains


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5.2 Port 80h POST Codes....121
5.3 Bus Initialization Checkpoints....125
5.4 Speaker....126
5.5 BIOS Beep Codes....126


## 5.1 BIOS Error Messages

Table 76 lists the error messages and provides a brief description of each.

**Table 76. BIOS Error Messages**

| Error Message | Explanation |
|---|---|
| GA20 Error | An error occurred with Gate A20 when switching to protected mode during the memory test. |
| Pri Master HDD Error<br>Pri Slave HDD Error<br>Sec Master HDD Error<br>Sec Slave HDD Error | Could not read sector from corresponding drive. |
| Pri Master Drive - ATAPI Incompatible<br>Pri Slave Drive - ATAPI Incompatible<br>Sec Master Drive - ATAPI Incompatible<br>Sec Slave Drive - ATAPI Incompatible | Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly. |
| A: Drive Error | No response from diskette drive. |
| Cache Memory Bad | An error occurred when testing L2 cache. Cache memory may be bad. |
| CMOS Battery Low | The battery may be losing power. Replace the battery soon. |
| CMOS Display Type Wrong | The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct. |
| CMOS Checksum Bad | The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values. |
| CMOS Settings Wrong | CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed. |
| CMOS Date/Time Not Set | The time and/or date values stored in CMOS are invalid. Run Setup to set correct values. |
| DMA Error | Error during read/write test of DMA controller. |
| FDC Failure | Error occurred trying to access diskette drive controller. |
| HDC Failure | Error occurred trying to access hard disk controller. |

continued

**Table 76. BIOS Error Messages** (continued)

| Error Message | Explanation |
|---|---|
| Checking NVRAM..... | NVRAM is being checked to see if it is valid. |
| Update OK! | NVRAM was invalid and has been updated. |
| Updated Failed | NVRAM was invalid but was unable to be updated. |
| Keyboard Error | Error in the keyboard connection. Make sure keyboard is connected properly. |
| KB/Interface Error | Keyboard interface test failed. |
| Memory Size Decreased | Memory size has decreased since the last boot. If no memory was removed then memory may be bad. |
| Memory Size Increased | Memory size has increased since the last boot. If no memory was added there may be a problem with the system. |
| Memory Size Changed | Memory size has changed since the last boot. If no memory was added or removed then memory may be bad. |
| No Boot Device Available | System did not find a device to boot. |
| Off Board Parity Error | A parity error occurred on an off-board card. This error is followed by an address. |
| On Board Parity Error | A parity error occurred in onboard memory. This error is followed by an address. |
| Parity Error | A parity error occurred in onboard memory at an unknown address. |
| NVRAM/CMOS/PASSWORD cleared by Jumper | NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed. |
| <CTRL_N> Pressed | CMOS is ignored and NVRAM is cleared. User must enter Setup. |

## 5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

### NOTE

*The POST card must be installed in PCI bus connector 1.*

The tables below offer descriptions of the POST codes generated by the BIOS. Table 77 defines the uncompressed INIT code checkpoints, Table 78 describes the boot block recovery code checkpoints, and Table 79 lists the runtime code uncompressed in F000 shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

**Table 77. Uncompressed INIT Code Checkpoints**

| Code | Description of POST Operation |
|---|---|
| D0 | NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting. |
| D1 | Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode. |
| D3 | Do necessary chipset initialization, start memory refresh, and do memory sizing. |
| D4 | Verify base memory. |
| D5 | Init code to be copied to segment 0 and control to be transferred to segment 0. |
| D6 | Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS. |
| D7 | Find Main BIOS module in ROM image. |
| D8 | Uncompress the main BIOS module. |
| D9 | Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM. |

**Table 78. Boot Block Recovery Code Checkpoints**

| Code | Description of POST Operation |
|---|---|
| E0 | Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller. |
| E8 | Initialize extra (Intel Recovery) Module. |
| E9 | Initialize floppy drive. |
| EA | Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code. |
| EB | Booting from floppy failed, look for ATAPI (LS-120, Zip) devices. |
| EC | Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code. |
| EF | Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9). |

**Table 79. Runtime Code Uncompressed in F000 Shadow RAM**

| Code | Description of POST Operation |
|---|---|
| 03 | NMI is Disabled. To check soft reset/power-on. |
| 05 | BIOS stack set. Going to disable cache if any. |
| 06 | POST code to be uncompressed. |
| 07 | CPU init and CPU data area init to be done. |
| 08 | CMOS checksum calculation to be done next. |
| 0B | Any initialization before keyboard BAT to be done next. |
| 0C | KB controller I/B free. To issue the BAT command to keyboard controller. |
| 0E | Any initialization after KB controller BAT to be done next. |
| 0F | Keyboard command byte to be written. |
| 10 | Going to issue Pin-23,24 blocking/unblocking command. |
| 11 | Going to check pressing of <INS>, <END> key during power-on. |
| 12 | To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers. |
| 13 | Video display is disabled and port-B is initialized. Chipset init about to begin. |
| 14 | 8254 timer test about to start. |
| 19 | About to start memory refresh test. |
| 1A | Memory Refresh line is toggling. Going to check 15 µs ON/OFF time. |
| 23 | To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable. |
| 24 | To do any setup before Int vector init. |
| 25 | Interrupt vector initialization to begin. To clear password if necessary. |
| 27 | Any initialization before setting video mode to be done. |
| 28 | Going for monochrome mode and color mode setting. |
| 2A | Different buses init (system, static, output devices) to start if present. (See Section 5.3 for details of different buses.) |
| 2B | To give control for any setup required before optional video ROM check. |
| 2C | To look for optional video ROM and give control. |
| 2D | To give control to do any processing after video ROM returns control. |
| 2E | If EGA/VGA not found then do display memory R/W test. |
| 2F | EGA/VGA not found. Display memory R/W test about to begin. |
| 30 | Display memory R/W test passed. About to look for the retrace checking. |
| 31 | Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test. |
| 32 | Alternate Display memory R/W test passed. To look for the alternate display retrace checking. |
| 34 | Video display checking over. Display mode to be set next. |
| 37 | Display mode set. Going to display the power-on message. |
| 38 | Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.) |
| 39 | Display different buses initialization error messages. (See Section 5.3 for details of different buses.) |
| 3A | New cursor position read and saved. To display the Hit <DEL> message. |

continued

**Table 79. Runtime Code Uncompressed in F000 Shadow RAM** (continued)

| Code | Description of POST Operation |
|---|---|
| 40 | To prepare the descriptor tables. |
| 42 | To enter in virtual mode for memory test. |
| 43 | To enable interrupts for diagnostics mode. |
| 44 | To initialize data to check memory wrap around at 0:0. |
| 45 | Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size. |
| 46 | Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory. |
| 47 | Pattern to be tested written in extended memory. Going to write patterns in base 640k memory. |
| 48 | Patterns written in base memory. Going to find out amount of memory below 1M memory. |
| 49 | Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory. |
| 4B | Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh). |
| 4C | Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M. |
| 4D | Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h). |
| 4E | Memory test started. (NOT SOFT RESET) About to display the first 64k memory size. |
| 4F | Memory size display started. This will be updated during memory test. Going for sequential and random memory test. |
| 50 | Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/shadow. |
| 51 | Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow. |
| 52 | Memory testing/initialization above 1M complete. Going to save memory size information. |
| 53 | Memory size information is saved. CPU registers are saved. Going to enter in real mode. |
| 54 | Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI. |
| 57 | A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow. |
| 58 | Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message. |
| 59 | Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test. |
| 60 | DMA page register test passed. To do DMA#1 base register test. |
| 62 | DMA#1 base register test passed. To do DMA#2 base register test. |
| 65 | DMA#2 base register test passed. To program DMA unit 1 and 2. |
| 66 | DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller. |
| 7F | Extended NMI sources enabling is in progress. |
| 80 | Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command. |
| 81 | Keyboard reset error/stuck key found. To issue keyboard controller interface test command. |
| 82 | Keyboard controller interface test over. To write command byte and init circular buffer. |
| 83 | Command byte written, global data init done. To check for lock-key. |

continued

**Table 79. Runtime Code Uncompressed in F000 Shadow RAM** (continued)

| Code | Description of POST Operation |
|---|---|
| 84 | Lock-key checking over. To check for memory size mismatch with CMOS. |
| 85 | Memory size check done. To display soft error and check for password or bypass setup. |
| 86 | Password checked. About to do programming before setup. |
| 87 | Programming before setup complete. To uncompress SETUP code and execute CMOS setup. |
| 88 | Returned from CMOS setup program and screen is cleared. About to do programming after setup. |
| 89 | Programming after setup complete. Going to display power-on screen message. |
| 8B | First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done. |
| 8C | Setup options programming after CMOS setup about to start. |
| 8D | Going for hard disk controller reset. |
| 8F | Hard disk controller reset done. Floppy setup to be done next. |
| 91 | Floppy setup complete. Hard disk setup to be done next. |
| 95 | Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.) |
| 96 | Going to do any init before C800 optional ROM control. |
| 97 | Any init before C800 optional ROM control is over. Optional ROM check and control will be done next. |
| 98 | Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache. |
| 99 | Any initialization required after optional ROM test over. Going to setup timer data area and printer base address. |
| 9A | Return after setting timer and printer base address. Going to set the RS-232 base address. |
| 9B | Returned after RS-232 base address. Going to do any initialization before Coprocessor test. |
| 9C | Required initialization before Coprocessor is over. Going to initialize the Coprocessor next. |
| 9D | Coprocessor initialized. Going to do any initialization after Coprocessor test. |
| 9E | Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock. |
| A2 | Going to display any soft errors. |
| A3 | Soft error display complete. Going to set keyboard typematic rate. |
| A4 | Keyboard typematic rate set. To program memory wait states. |
| A5 | Going to enable parity/NMI. |
| A7 | NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000. |
| A8 | Initialization before E000 ROM control over. E000 ROM to get control next. |
| A9 | Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control. |
| AA | Initialization after E000 optional ROM control is over. Going to display the system configuration. |
| AB | Put INT13 module runtime image to shadow. |
| AC | Generate MP for multiprocessor support (if present). |
| AD | Put CGA INT10 module (if present) in Shadow. |

continued

**Table 79. Runtime Code Uncompressed in F000 Shadow RAM** (continued)

| Code | Description of POST Operation |
|---|---|
| AE | Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow. |
| B1 | Going to copy any code to specific area. |
| 00 | Copying of code to specific area done. Going to give control to INT-19 boot loader. |

## 5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 80 describes the bus initialization checkpoints.

**Table 80. Bus Initialization Checkpoints**

| Checkpoint | Description |
|---|---|
| 2A | Different buses init (system, static, and output devices) to start if present. |
| 38 | Different buses init (input, IPL, and general devices) to start if present. |
| 39 | Display different buses initialization error messages. |
| 95 | Init of different buses optional ROMs from C800 to start. |

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 81 describes the upper nibble of the high byte and indicates the function that is being executed.

**Table 81. Upper Nibble High Byte Functions**

| Value | Description |
|---|---|
| 0 | func#0, disable all devices on the bus concerned. |
| 1 | func#1, static devices init on the bus concerned. |
| 2 | func#2, output device init on the bus concerned. |
| 3 | func#3, input device init on the bus concerned. |
| 4 | func#4, IPL device init on the bus concerned. |
| 5 | func#5, general device init on the bus concerned. |
| 6 | func#6, error reporting for the bus concerned. |
| 7 | func#7, add-on ROM init for all buses. |

Table 82 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

**Table 82. Lower Nibble High Byte Functions**

| Value | Description |
|---|---|
| 0 | Generic DIM (Device Initialization Manager) |
| 1 | On-board System devices |
| 2 | ISA devices |
| 3 | EISA devices |
| 4 | ISA PnP devices |
| 5 | PCI devices |

## 5.4 Speaker

A 47 Ω inductive speaker is mounted on the Desktop Board D845GEBV2 and the Desktop Board D845GERG2. The speaker provides audible error code (beep code) information during POST.

| For information about | Refer to |
|---|---|
| The location of the onboard speaker on the Desktop Board D845GEBV2 | Figure 1, on page 14 |
| The location of the onboard speaker on the Desktop Board D845GERG2 | Figure 2, on page 15 |

## 5.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 83). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

**Table 83. Beep Codes**

| Beep | Description |
|---|---|
| 1 | Refresh failure |
| 2 | Parity cannot be reset |
| 3 | First 64 KB memory failure |
| 4 | Timer not operational |
| 5 | Not used |
| 6 | 8042 GateA20 cannot be toggled |
| 7 | Exception interrupt error |
| 8 | Display memory R/W error |
| 9 | Not used |
| 10 | CMOS Shutdown register test error |
| 11 | Invalid BIOS (e.g. POST module not found, etc.) |