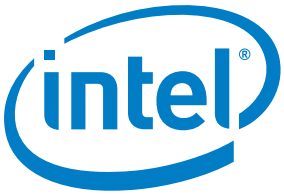


Intel® Curie™ Module

Application Note – Power Sequencing Considerations

Revision 1.0

November 2016

Contents

List of Figures

Revision History

Version	Description	Date
1.0	Initial release	November 2016

1.0 Application Note: Intel® Curie™ Power Sequencing

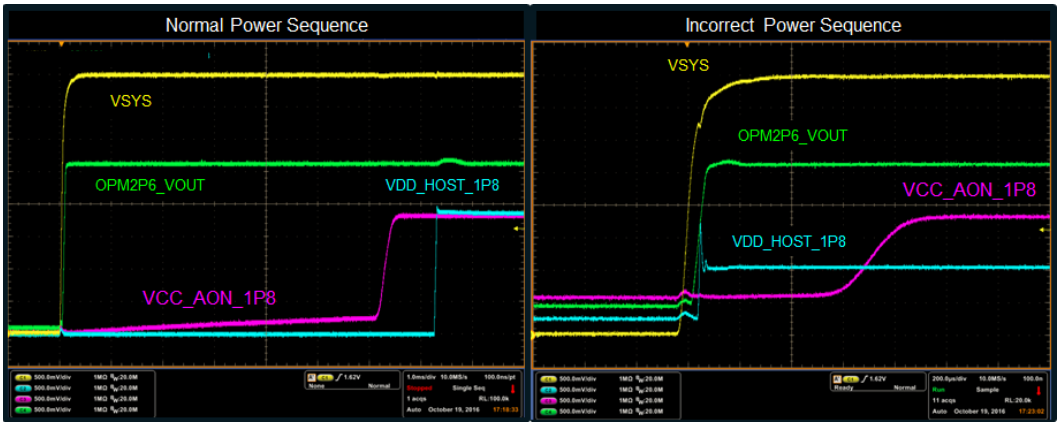
1.1 Introduction: Power sequencing failure

If the voltage transition on the power supply pin (VSYS)* of an Intel® Curie™ module causes it to power down and then commence a power up sequence before its internal reference voltage OPM2P6_VOUT has dropped below 100 mV, an incorrect power sequence may occur. If this happens, the device may become unresponsive or enter an indeterminate state in which the correct operation of the device is not guaranteed.

The reference voltage OPM2P6_VOUT of the Intel Curie module must remain below 100 mV at the start of a power up sequence. If this is not maintained, specific internal signals within the embedded Intel® Quark™ SE C1000 microcontroller might not be initialized correctly. Figure 1 below illustrates the sequence of events during a normal power up cycle as well as that during an incorrect power sequence. This diagram graphs the following signals:

- VSYS – main input power rail (Ball: L04)
- OPM2P6_VOUT – 2.6 V reference voltage output (Ball: J01)
- VDD_HOST_1P8 – 1.8 V power to host generated by regulator ESR3 (Ball: P03)

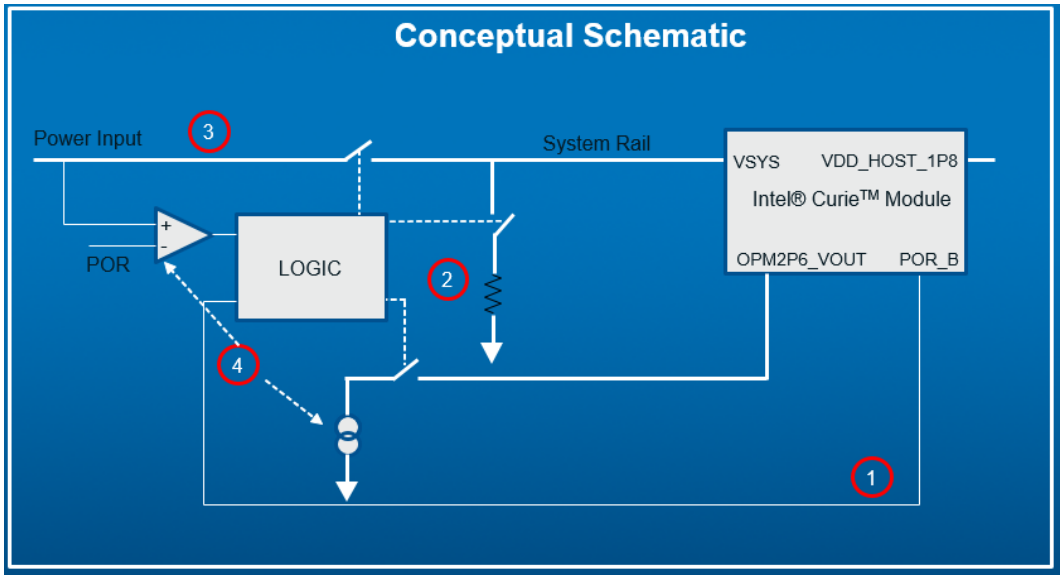
Figure 1 Intel® Curie™ module power sequencing



Intel recommends ensuring that the OPM2P6_VOUT node is discharged to ground (zero volts) before a power up cycle. The following sections in this document provide a generic description of an implementation that ensures a correct power sequence, and then present a detailed example.

1.2 Conceptual solution: OPM2P6_VOUT rail discharge

Figure 2 Intel® Curie™ module with OPM2P6_VOUT discharge



The block diagram in Figure 2 above illustrates a conceptual solution ensuring that the OPM2P6_VOUT is properly discharged. It uses a voltage monitor, a load switch, and active discharge circuitry. The circuit operates using two voltage thresholds:

a) POR_B – Generates a falling edge (high to low transition) from the Intel® Curie™ module, indicating that VSYS has dropped below 2.9 V

b) POR – Power up threshold for the system; its value needs to be selected to meet system requirements, based on desired hysteresis from 2.9 V

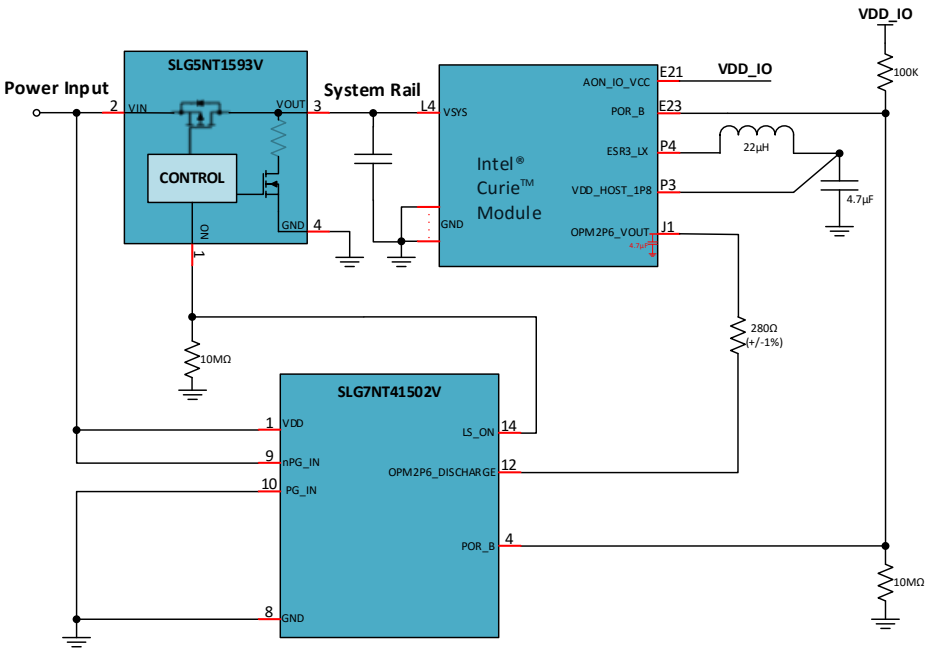
Sequence of events during power down/power up cycle

1. When the system rail falls below 2.9 V during power down, the POR_B signal generates a high to low transition.
2. When POR_B falls from high to low, the load switch should be disabled. The OPM2P6_VOUT and VSYS pins begin to be discharged.
3. Re-apply power input to the system.
4. Discharge OPM2P6_VOUT to Ground first. After ensuring that OPM2P6_VOUT is fully discharged to Ground, and once the input power voltage rises above the POR threshold, disable the active discharge circuitry connected to the system rail and OPM2P6_VOUT. (The POR threshold needs to be selected as discussed above.) After this, enable the load switch providing power to the Intel Curie module.

1.3 Application schematic of a proposed implementation

The schematic block diagram in Figure 3 below shows the circuitry for one possible implementation to guarantee proper power sequencing for the Intel Curie module.

Figure 3 Schematic connectivity for proposed implementation



The proposed implementation consists of using two devices from Silego*:

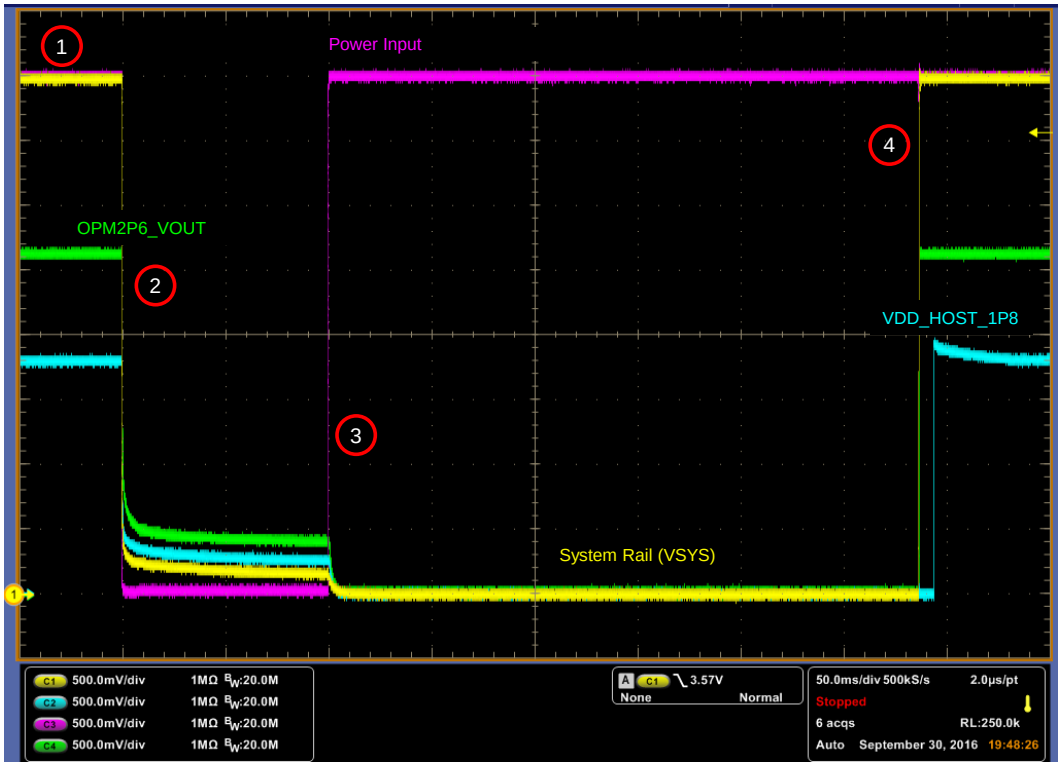
1. A programmable mixed signal device (SLG7NT41502V) used to control power sequencing and the discharging of the OPM2P6_VOUT rail.
2. A second device (SLG5NT1593V) used to gate the power supply input to the VSYS pin of the Intel Curie module and also to discharge the system rail. For systems with stringent inrush current needs, alternate devices can be used which incorporate a load switch with outputs that are actively discharged when turned off as well as output slew rate control when they are turned on.

The OPM2P6_VOUT voltage is generated by an embedded linear regulator that is supplied by the VSYS pin. There is an internal 4.7 µF capacitor inside the Intel Curie module connected to this pin. Since the power drain on this pin is very small, there could be situations where the input supply (VSYS) is fully discharged during a power cycle but the voltage on OPM2P6_VOUT has not been discharged to below 100mV to guarantee proper power sequencing. To facilitate this, the load switch used to control the delivery of power to the module must be able to actively discharge the connected voltage. The active discharge circuitry inside the load switch ensures that the voltage on VSYS is discharged to Ground. Disconnecting and discharging VSYS protects the

internal OPM2P6_VOUT regulator by preventing it from having a valid supply voltage on its input while its output is being discharged to Ground.

The operation of the schematic above can be better understood with the captured waveforms shown Figure 4 below. It captures an instance where the SLG7NT41502V and SLG5NT1593V devices mentioned above are being used to control the Intel Curie module.

Figure 4 Operation of circuitry controlling OPM2P6_VOUT discharge during a power cycle



The waveform shows the behavior of the OPM2P6_VOUT rail when the power input is powered down and subsequently powered up. (The numbers on the diagram refer to the **sequence of events during power down/power up cycle described above**.) When the voltage on VSYS decays to ~2.9 V, the POR_B signal from the Intel Curie module is asserted. Assertion of this signal causes the PFET ON signal (pin 14 - output from the SLG7NT41502V device) to be de-asserted, disabling the load switch and discharging VSYS to Ground. Simultaneously, the OPM2P6 discharge signal (pin 12 – open drain output on the SLG7NT41502V device) is driven low causing the OPM2P6_VOUT to be discharged to Ground through the 280 Ω resistor.

When power input is reapplied, the SLG7NT41502V device ensures that the load switch is enabled only after the minimum time necessary for forced discharging of OPM2P6_VOUT, to guarantee proper power sequencing. Once VSYS is applied, the

Intel Curie module proceeds with its normal power sequence of OPM2P6_VOUT rising to 2.6 V, followed by the powering up of AON_IO_VCC and the VDD_HOST_1P8 domain.

1.4 Alternate implementation using power good (PG) signal to control VSYS and OPM2P6_VOUT discharge

The circuit schematic in Figure 5 below shows an implementation of the OPM2P6_VOUT discharge circuitry in a pre-regulated system. In this implementation, the BUCK converter (TPS62172) generates a 3.3V supply (VDD_PLAT_3P3) that is used both as the main power rail and I/O supply to the Intel Curie module. When power is applied to the BUCK converter, the POWER GOOD (PG) output is asserted once the BUCK converter reaches regulation. The PG signal is used by the Silego* part SLG7NT41502V to enable the load switch after the minimum time necessary for forced discharging of VSYS and OPM2P6_VOUT to guarantee proper power sequencing. When the input power supply to the BUCK is disabled, the voltage on the system rail decays to ~2.9 V asserting the POR_B signal. This causes the PFET ON signal (pin 14 - output from the SLG7NT41502V device) to be de-asserted, disabling the load switch and discharging VSYS to GND. Simultaneously, the OPM2P6 discharge signal (pin 12 – open drain output on the SLG7NT41502V device) is driven low, causing the OPM2P6_VOUT to be discharged to Ground through the 280 Ω resistor.

Figure 6 below illustrates the signal waveforms for this operation.

Figure 5 Schematic connectivity in a 3.3 V pre-regulated system with power good (PG) signal

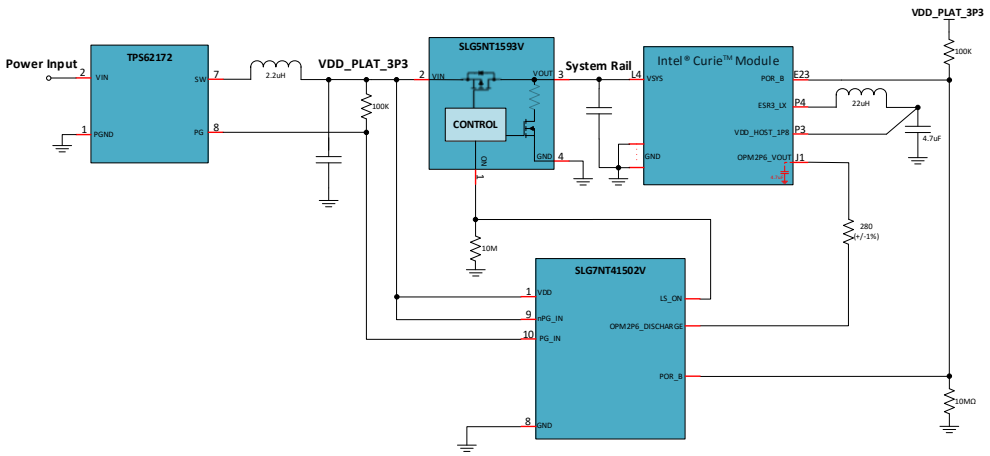


Figure 6 Operation of controlling OPM2P6_VOUT discharge using power good (PG) input