



# Intel® E7221 Chipset Memory Configuration Guide

White Paper

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*October 2004*



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## *Revision History*

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Revision Number	Description	Revision Date
-001	<ul style="list-style-type: none"> <li>Initial release</li> </ul>	October 2004

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# 1 Overview

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The Intel® E7221 chipset is Intel's dual-channel DDR/DDR2 Memory Controller Hub with Intel® Flex Memory Technology. Intel has enhanced its memory architecture design to allow for maximum configuration flexibility while providing optimal performance when combined with DDR2-533 and an Intel® Pentium 4® processor in the Land Grid Array 775 (LGA775) package with 800 MHz front side bus.

For great server application flexibility, the Intel® E7221 chipset is specifically designed to support Intel® Extended Memory 64 Technology\* (Intel® EM64T) enabling 64-bit memory addressability. Select versions of the Pentium 4 processor support Intel® Extended Memory 64 Technology\* (Intel® EM64T) as an enhancement to Intel's IA-32 architecture on server platforms. This enhancement enables the processor to execute operating systems and applications written to take advantage of Intel® EM64T. Further details on the 64-bit extension architecture and programming model can be found in the Intel® Extended Memory 64 Technology Software Developer Guide at <http://developer.intel.com/technology/64bitextensions/>.

\*Intel® Extended Memory 64 Technology (Intel® EM64T) requires a computer system with a processor, chipset, BIOS, OS, device drivers and applications enabled for Intel EM64T. Processor will not operate (including 32-bit operation) without an Intel EM64T-enabled BIOS. Performance will vary depending upon your hardware and software configurations. Intel EM64T-enabled OS, BIOS, device drivers and applications may not be available. Check with your vendor for more information.

This document details the E7221 chipset memory configurations and organization. It is intended for a technical audience interested in learning about the simplified population rules introduced by Intel Flex Memory Technology and the E7221 chipset platform. This white paper will provide a brief background regarding the supported memory technologies and configurations, and then discuss the styles of memory organization and modes of operation.

## 1.1 Memory Technology Supported

The E7221 chipset MCH supports DDR and DDR2 ECC and non-ECC DIMMs and memory technologies in the following configurations

- DDR-333 (PC2700), DDR-400 (PC3200)
- DDR2-400 (PC3200), DDR2-533 (PC4300)

**Table 1. Memory Technology Support**

DRAM Technology	Smallest Increments (One SS DIMM)	Largest Increments (One DS DIMM)	Maximum Capacity (Four DS DIMMs)
256 Mb	128 MB	512 MB	2048 MB
512 Mb	256 MB	1024 MB	4096 MB
1 Gb	512 MB	1024 MB	4 GB (Note 1)

**NOTES:** 1. This exceeds a 32-bit address limit of 4 GB. In a 32-bit system, only the first 4 GB of memory will be accessible.

## 1.2 Illegal Configurations

The following configurations are not valid with the E7221 chipset MCH:

- 64-Mb, 128-Mb, 2-Gb, and 4-Gb Memory Technologies for DDR and DDR2
- x4, x32 DIMMs
- Double-Sided x16 DIMMs
- Registered DIMMs

## 1.3 Valid Front Side Bus and Memory Speeds

Table 2. Valid Memory Configurations

DRAM Data Rate	DRAM Type	Single Channel Peak Bandwidth	Dual-Channel Peak Bandwidth
333 MT/s	DDR - DRAM	2.7 GB/s	5.4 GB/s
400 MT/s	DDR - DRAM	3.2 GB/s	6.4 GB/s
400 MT/s	DDR2 - DRAM	3.2 GB/s	6.4 GB/s
533 MT/s	DDR2 - DRAM	4.25 GB/s	8.5 GB/s

## 1.4 ECC Support

The E7221 chipset **supports** single-bit Error Correcting Code (or Error Checking and Correcting) on the main memory interface. The MCH generates an 8-bit code for each 64-bit quad word of memory.

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## 2 *Intel® E7221 Chipset Memory Organization and Operating Modes*

The E7221 chipset memory interface is designed with Flex Memory Technology where it can be configured to support single-channel or dual-channel DDR or DDR2 memory configurations.

Depending upon how the DIMMs are populated on each system memory channel, a number of different configurations can exist for DDR or DDR2:

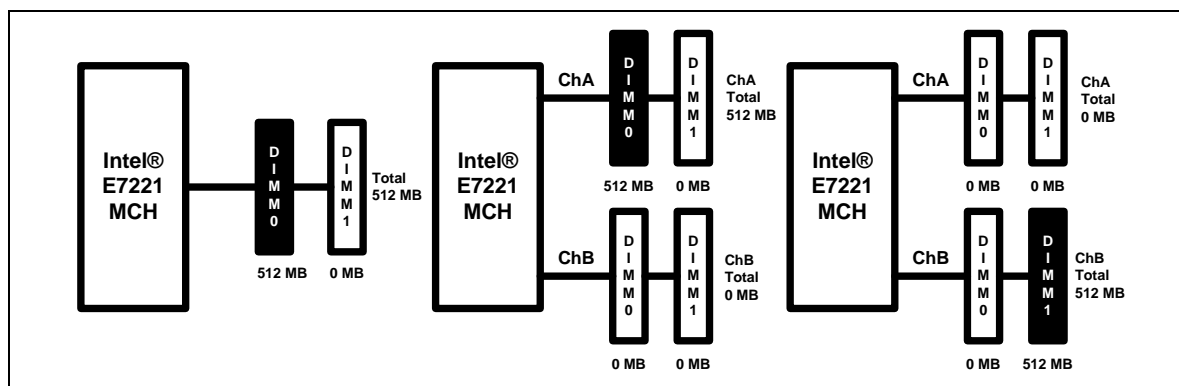
- Single Channel – only one channel of memory is routed and populated, or if two-channels of memory are routed, but only one channel is populated; can be either channel A or channel B.
- Dual-Channel Asymmetric – both channels are populated, but each channel has a different amount (MB) of total memory.
- Dual-Channel Symmetric – both channels are populated where each channel has the same amount (MB) of total memory.

The following sections explain and show the different memory configurations that are supported by the E7221 Chipset.

### 2.1 Single-Channel

The system will enter single-channel mode when only one channel of memory is routed on the motherboard, or if two-channels of memory are routed, but only one channel is populated. In this configuration, all memory cycles are directed to a single channel.

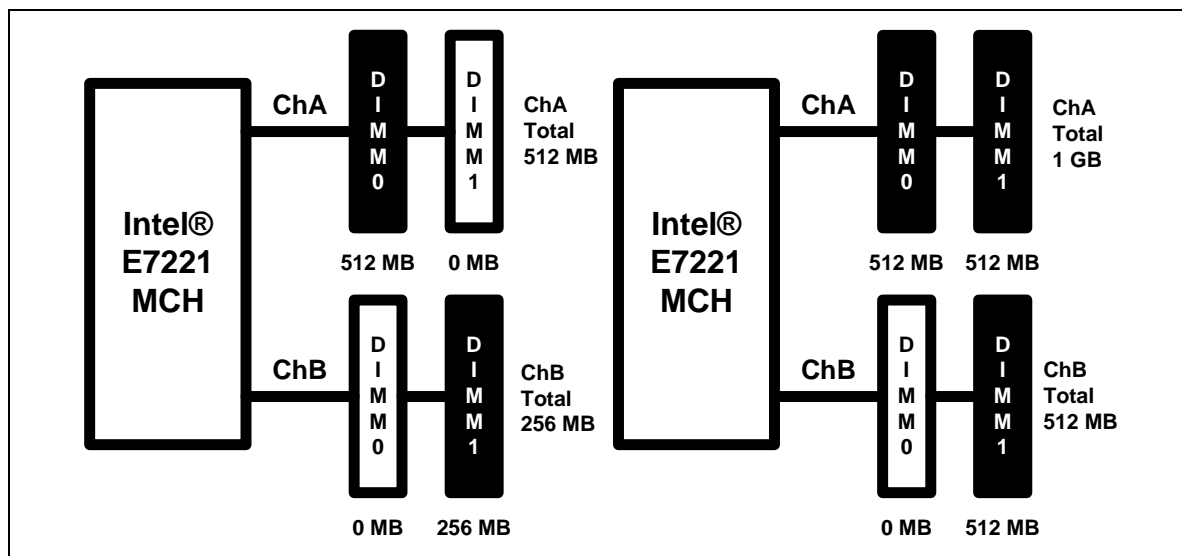
**Figure 1. Single-Channel Memory Mode**



## 2.2 Dual-Channel Asymmetric

This mode is entered when both memory channels are routed on the motherboard and populated with different amounts (MB) of total memory. This configuration allows addresses to be accessed in series across the channels starting in channel A until the end of its highest rank, then continue from the bottom of channel B to the top of the rank. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel.

**Figure 2. Dual-Channel Asymmetric Memory Mode**



## 2.3 Dual-Channel Symmetric

This mode allows the end user to achieve maximum performance on real applications by utilizing the full 64-bit dual-channel memory interface in parallel across the channels with the aid of Intel® Flex Memory Technology. The key advantage this technology brings is that the end user is only required to populate both channels with the same amount (MB) of total memory to achieve this mode. The DRAM component technology, device width, device ranks, and page size may vary from one channel to another.

Addresses are ping-ponged between the channels, and the switch happens after each cache line (64-byte boundary). If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels.





Figure 3. Dual-Channel Symmetric Memory Mode

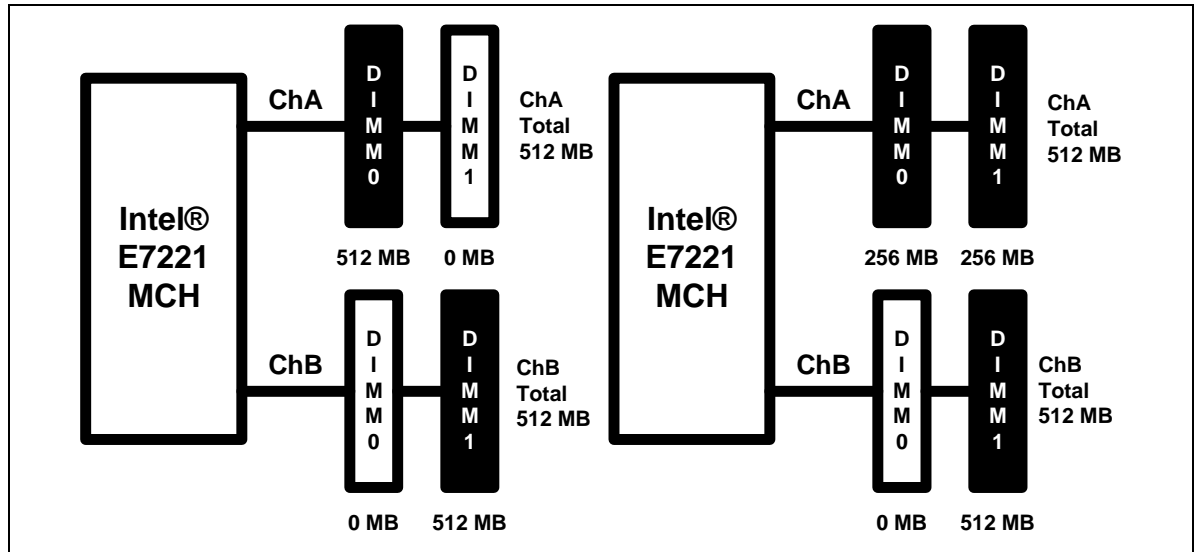
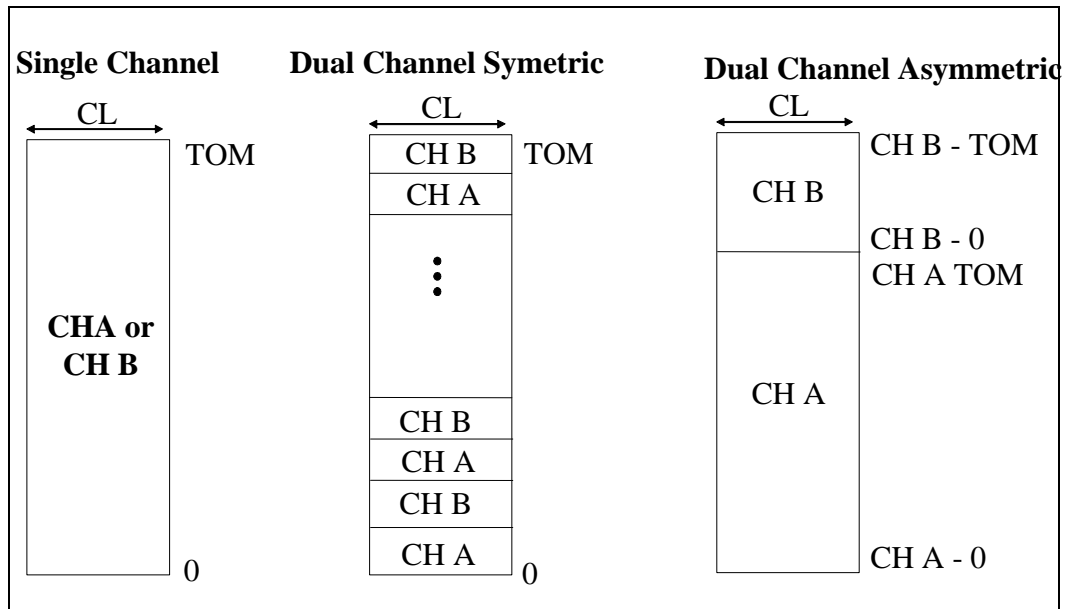


Figure 4. System Memory Mode Styles



## 2.4 Mixed DRAM Memory Speeds

The E7221 chipset will accept mixed DDR or DDR2 speed populations, assuming the SPDs on the DIMMs are programmed with the correct information and the BIOS is programmed as outlined in Intel's BIOS reference code.

In all operating modes (Single-Channel, Dual-Channel Asymmetric, and Dual-Channel Symmetric) the frequency of the System Memory will be set to the lowest frequency of all DIMMs populated in the system, as determined through the SPD registers on the DIMMs.

For example, a DDR2-533 DIMM installed with a DDR2-400 DIMM should run at 400 MHz. The DDR2-533 DIMM should downshift to DDR2-400 timings, thus allowing the system to run at 400 MHz speeds. The DDR2-533 DIMM will only downshift to DDR2-400, if the timings for DDR2-400 are programmed in the DDR2-533 DIMMs SPD.