RF CMOS Technology Scaling in High-k/Metal Gate Era for RF SoC (System-on-Chip) Applications

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Outline

- Introduction - RF SoC and RF CMOS
- CMOS Scaling Trend
- RF CMOS Scaling
- RF CMOS Designs – PA, LNA, Wireless Transceivers
- Conclusions
RF SoC → SoC derivatives with integrated RF and communication IPs
- Integration of RF subsystem into an advanced CMOS platform
- Is CMOS scaling capable of meeting RF system requirements?
32 nm RF CMOS Technology

- **TM1 Inductor**: high Q and density
- **Passives**:
  - Precision Resistor
  - High Q Inductor
  - High Density Decap
- **HV PA Transistor**
- **RF Transistor**: Templates/Modeling
  - Transistor:
    - Logic, low power, I/O
    - JFET, BJT
  - **Well**: Triple Well/Deep Nwell
  - **Substrate**: High Resistivity

Basic 32 nm CMOS technology is expanded with many more mixed signals/RF features to meet RF SoC requirements.
Introduction - RF SoC and RF CMOS

CMOS Scaling Trend

RF CMOS Scaling

RF CMOS Designs – PA, LNA, Wireless Transceivers

Conclusions
Intel CMOS Transistor Architecture 
Evolution in the Last Decade

.13 um and before  
90nm/65 nm  
45 nm/32 nm

Traditional  
Strained Silicon  
High k/Metal Gate + Strained Silicon

CMOS scaling has evolved from classical **dimensional scaling** to modern scaling **with innovations in structures and materials**
- Constant field oxide scaling not sustainable beyond 0.13 µm (high gate leakage)
- Strained silicon implementation at 90 nm compensated the lack of Tox scaling
- Hi-k/metal gate implementation at 45 nm recovered Tox scaling
Innovations of strained silicon and high k/metal gates enabled Moore’s law scaling with continuous ~ 30% /gen. performance/gm enhancement
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RF CMOS Technology Performance Metrics

- RF CMOS scaling focuses on a different set of performance metrics ($f_T$, noise, Q factor and so on) from basic CMOS technology.

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<td>PA, LNA, Mixer</td>
<td>L, Q</td>
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What are the impacts of CMOS scaling on these metrics?
32 nm RF CMOS Cut-off Frequency $f_T - 445$ GHz!

**De-embedding Structures**
- De-embedded to M1 (included)
- 7% faster than previous result from $g_m$ improvement

**A new 32 nm NMOS RF CMOS record 445 GHz $f_T$ achieved**

**Graph**
- NMOS
- $26 \text{nm} \times 0.6 \text{um} \times 50$
- $V_{GS} = 0.6 \text{V}, V_{DS} = 1 \text{V}$
- $f_{\text{MAX}} = 230 \text{ GHz}$
- $f_T = 445 \text{ GHz}$

**Graph Details**
- Mason's $U$, $H21$ (dB)
- Frequency (GHz)
- $-20$ dB/dec
RF Cut-off Frequency $f_T$ Scaling Trend

Cut-off frequency $f_T$ started from 200 GHz at 90 nm, to 360 GHz at 65 nm, to 395 GHz at 45 nm (HK/MG), to the new record of 445 GHz at 32 nm HK/MG.
CMOS Scaling on RF - Cut-off Frequency $f_T$

$$f_T = \frac{g_m}{2\pi C_{gg}}$$

- Record $f_T$ 445 GHz, closing gaps to SiGe HBT and III-V devices
- $f_T$ improvement ~ 20-30% per gen
- $g_m$ improvement dominating (thanks to CMOS technology scaling !)
- $C_{gg}$ effects somewhat mixed
- Parasitics and layout optimization critical for future scaling

CMOS Scaling on RF - 1/f Flicker Noise

- 10x 1/f flicker noise improvement over five nodes
- Enabled by Cox scaling from high-k
- Interface engineering to stabilize process factor K
RF 1/f Flicker Noise Scaling Trend

1/f flicker noise scaling, 10x reduction from 0.13 um to 32 nm, enabled by HK/MG Tox scaling and interface engineering
CMOS Scaling on RF - Noise Figures

\[ NF_{\text{min}} = 1 + K \frac{f}{f_t} \sqrt{g_m \cdot (R_g + R_s)} = 1 + K \frac{2 \pi f t C_{gg}}{\sqrt{g_m}} \sqrt{(R_g + R_s)} \]

- NF\text{min} improved to < 1 dB level after 45 nm node
- \( g_m \) improvement needs to balance gate cap and gate resistance increase
- Layout optimization becomes critical for future scaling

Noise figure $NF_{\text{min}}$ scaling to a low level after 45 nm node
CMOS Scaling on RF - Deep Nwell

P-well in CMOS twin-well architecture

Deep n-well in triple-well architecture with MeV implants at older technology

Deep n-well depth scaled by 2.5x from 0.13 um to 32 nm. Deep n-well integration is now more manufacturable with sub-MeV implants
Deep Nwell Applications for M/S RF

Substrate noise isolation (~ 50dB)

CMOS p-JFET

CMOS Parasitic NPN BJT

DNW B S G D

Isolation (dB)

No Deep Nwell

Deep Nwell

Collector Current, $I_C$ (mA)

Collector-Emitter Voltage, $V_{CE}$ (V)

$I_B$ = 50uA

40uA

30uA

20uA

10uA

$V_{BS}$ = -5 V

-4 V

-3 V

-2 V

-1 V

$V_{DS}$ (V)

$I_D$ (mA)

$V_{DS}$ = 0

0.05

0.1

0

1

2

3

4

5

Collector Current, $I_C$ (mA)

Collector-Emitter Voltage, $V_{CE}$ (V)
BJT immune to oxide interface charge trapping/de-trapping (source of 1/f flicker noise)

100x flicker noise reduction measured on BJT (via CMOS/Deep Nwell)

Applications in RF mixer circuits requiring very low flicker noise
CMOS voltage scaling not favored for high voltage needs of RF (PA)

New high voltage PA transistors are developed to support HV needs

CMOS Interconnect Scaling

Interconnect scaling adversely impacts quality factor of RF Passives. Thick metal (TM) solves the dilemma. Inductor Q of 25 achieved.
Metal spiral Inductor Q progressively degraded with the scaling of interconnect pitch and metal thickness ($Q = \omega L/R$)
Spiral Inductors by TM recover and improve the quality factor to achieve Q~25
Complex high Q monolithic silicon spiral inductors were developed using TM for 32 nm RF designs, including PA, LNA, and VCO.
Conclusions

- Moore’s Law alive and well for RF CMOS, enabled by the innovations in transistors architectures and interconnects
- Continuous improvement in CMOS $g_m$ and Cox keys to the RF CMOS cut-off frequency and noise performance scaling
- RF passives scaling needs creative solutions in interconnect architectures scaling
- 32 nm wireless transceiver demonstrated with state of the art 32 nm RF CMOS technology
For further information on Intel’s silicon technology, please visit our Technology & Research page at www.intel.com/technology