A 32nm SoC Platform Technology with 2nd Generation High-k/Metal Gate Transistors Optimized for Ultra Low Power


Logic Technology Development
Technology Manufacturing Group

Intel Corporation
Outline

- 32 nm High-k/Metal Gate SoC Technology
- 32 nm SoC Transistor Architecture
- 32 nm SoC Interconnects and Passives
- 32 nm SoC Embedded Memory
- Summary
32 nm High-k/Metal Gate Transistor

- 2nd gen high-k/metal gate
- Replacement Metal Gate (RMG) Flow
- 4th gen strained silicon
- 20% performance improvement over 45 nm high-k/metal gate
- In high volume manufacturing production of multi-core CPU products in multiple fabs
SoC process flow is derived from the 2nd generation CPU RMG (Replacement Metal Gate) flow
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A low cost implementation with three types of transistors “co-exist” on the same die:

- Logic (HP or SP): for burst CPU performance
- Low Power (LP): for always-on-always-connected application and long battery life
- HV I/O: for high voltage I/O

Take advantage of the low gate leakage of high-k/metal gate to avoid the traditional expensive “triple gate” approach.
## Transistors Summary

<table>
<thead>
<tr>
<th>Transistor Type</th>
<th>Logic (option for HP or SP)</th>
<th>Low Power</th>
<th>HV I/O (option for 1.8 or 3.3 V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HP</td>
<td>SP</td>
<td>LP</td>
</tr>
<tr>
<td>EOT (nm)</td>
<td>0.95</td>
<td>0.95</td>
<td>0.95</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>.75/1</td>
<td>.75/1</td>
<td>.75/1.2</td>
</tr>
<tr>
<td>Pitch (nm)</td>
<td>112.5</td>
<td>112.5</td>
<td>126</td>
</tr>
<tr>
<td>Lgate (nm)</td>
<td>30</td>
<td>34</td>
<td>46</td>
</tr>
<tr>
<td>NMOS I&lt;sub&gt;dsat&lt;/sub&gt; (mA/um)</td>
<td>1.53/1 @ 1 V</td>
<td>1.12/1 @ 1 V</td>
<td>0.71/1 @ 1 V</td>
</tr>
<tr>
<td>PMOS I&lt;sub&gt;dsat&lt;/sub&gt; (mA/um)</td>
<td>1.23/1 @ 1 V</td>
<td>0.87/1 @ 1 V</td>
<td>0.55/1 @ 1 V</td>
</tr>
<tr>
<td>I&lt;sub&gt;off&lt;/sub&gt; (nA/um)</td>
<td>100</td>
<td>1</td>
<td>0.03</td>
</tr>
</tbody>
</table>

Tightest minimum gate pitch for 32/28 nm processes
Logic and LP transistors cover 4 orders of magnitude (10,000 x) of leakage power to support a wide dynamic range SoC applications.
Logic Transistors Ion-Ioff (HP/SP)

- Highest reported drives for 32/28 nm SoC process at tightest gate pitch (112 nm) - 1.53 mA/um (N) / 1.12 mA/um (P) at 100nA/um
- 20-35% improvement over 45 nm high-k/MG logic transistors
Logic/LP Transistors Vt vs. L

- Short channel effect, DIBL, Vt roll-off are well controlled
- SP Vt < 400 mV, LP Vt ~ 500 mV
Well controlled transistor I-V characteristics – HP and SP
Sub-threshold slope ~ 100mV/decade (HP), < 90 mV/decade (SP)
DIBL – SP: 90 mV (N)/100 mV (P); HP: 130 mV (N)/140 mV (P)
Low Power Transistors Ion-Ioff (LP)

- Highest reported drive currents at lowest standby leakage (30pA/um, 1000x lower than HP) AND
- Low active power (0.75 V) with good performance
Low Power Transistor I-V Characteristics

- Well controlled transistor I-V characteristics - LP
- Sub-threshold slope ~ < 85 mV/decade
- DIBL - 70 mV (N)/100 mV (P)

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Low Power Transistors Total Leakage

$\mathbf{I_{LKG}} = \frac{1}{2} \text{ ("ON" State Leakage)} + \frac{1}{2} \text{ ("OFF" State Leakage)}$

$= \frac{1}{2} \left( I_{\text{gate (ON)}} \right) + \frac{1}{2} \left( S F \times I_{\text{off}} + I_{\text{junc}} + I_{\text{gate (OFF)}} \right)$

All leakage components - $I_{\text{off}}$, $I_{\text{gate(on)}}$, $I_{\text{gate(off)}}$ and $I_{\text{junction}}$ need to be mitigated for low power transistor
High Voltage Transistors (1.8/2.5 V or 3.3 V)

- 2nd gen high-k/metal gate I/O Transistors
- 1.8/2.5 V or 3.3 V options
- High-k/Oxide composite gate stack
- Min gate length = 140 nm (1.8 V)
  Min gate length = 300 nm (3.3 V)
Robust NMOS and PMOS high k + metal gate logic and I/O transistors TDDB
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32 nm SoC Interconnects

SOC interconnect system optimized for density and flexibility

Optimized for RC

Optimized for Density

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Dec. 9th, ’09
32 nm SoC Interconnects - Thick Top Metal

Thick top metal for power delivery and I/O routing
32 nm SoC High Q Inductors

Inductors

1 nH Inductor for VCO

6 nH inductor for 2.4 GHz Wi-Fi LNA

Quality Factor Comparison of M9 and M8 Inductors

Thick top metal ideal for high Q inductors (Q > 20)

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32 nm SoC Capacitors and Resistors

Capacitors

Metal Finger Capacitor

Q of Metal Finger Capacitor

Resistors

Linear Resistor

Precision Resistor

Rich high quality factor and high precision passives
Deep Nwell Architecture

Deep Nwell for Substrate Noise Isolation

50 dB substrate noise reduction measured on deep Nwell for noise sensitive analog circuits - ADC (Analog-Digital Converter), DAC (Digital-Analog Converter), PA (Power Amplifier) and VCO.
1/f Flicker Noise

NMOS 1/f Flicker Noise

- 65 nm Ox/Ply Vds=1.1V
- 45 nm Hi k/MG Vds=1.0V
- 32 nm Hi k/MG Vds=0.9V

PMOS 1/f Flicker Noise

- 65 nm Ox/Ply Vds=1.1V
- 45 nm Hi k/MG Vds=1.0V
- 32 nm Hi k/MG Vds=0.9V

65 (poly/ox) /45/32 nm (high k/metal gate) 1/f flicker noise trend shows healthy Si/dielectric interfaces and no degradation from high-k/metal gate processing, critical for analog circuits.
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Multiple SRAM bit cells offered for high speed, low voltage and high density SoC applications. Highest reported array density
All bit cells are capable of supporting high performance needs. 32 nm LP can operate up to 2 GHz, 2x faster than 65 nm LP.
Low bit cell leakages (< 20 pA/cells) at low retention Vccmin
SoC process has the same low defect density as CPU process.
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- 32 nm high-k/metal gate technology has been optimized for high performance/low power System-On-Chip (SOC) platform

- A new triple transistor architecture provides record drive currents and low leakages spanning 4 orders of magnitude of leakage

- Tightest reported gate pitch and highest reported SRAM array density of any 32nm or 28nm technology

- Other SOC device elements (resistors, inductors, capacitors, diodes, and varactors) all exhibit well controlled performance and reliability
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